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April 1st, 2010
Renesas Electronics Corporation

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MOS Integrated Circuit V850ES/FG2

32-bit single-chip micro controller

INTRODUCTION

The V850ES/FG2 are 32-bit single-chip microcontrollers that include the V850ES CPU core and integrate peripheral functions such as timers/counters, serial interfaces, and an A/D converter. These microcontrollers also incorporate a CAN (Controller Area Network) as an automotive LAN.

In addition to highly real-time responsive, 1-clock-pitch basic instructions, these microcontrollers have instructions ideal for digital servo applications, such as multiplication instructions using a hardware multiplier, sum-of-products operation instructions, and bit manipulation instructions. These microcontrollers can also realize a real-time control system that is highly cost effective and can be used in automotive instrumentation fields.

FEATURES

- Number of instructions: 83
- Minimum instruction execution time: 50 ns (main clock (fxx) = 20 MHz)
- General-purpose registers: 32 bits × 32
- Power-on clear function
- Low-voltage detection function
- Ring-OSC: 200 kHz (TYP.)
- Internal memory:
 - RAM: 6/12/16 KB
 - Flash memory: 256/384KB
 - Mask ROM: 128/256KB
- Interrupts/exceptions :
 - Non-maskable interrupts : 1 source
 - Maskable interrupts : 61 sources
 - Software exceptions: 2 sources
 - Exception trap: 1 source
- I/O lines I/O ports: 84
- Timer/counters:
 - 16-bit interval timer M (TMM): 1 ch
 - 16-bit timer/event counter P (TMP): 4 ch
 - 16-bit timer/event counter Q (TMQ): 2 ch
- Watch timer: 1 ch
- Watchdog timer 2: 1 ch
- Serial interface (SIO):
 - Asynchronous serial interface A (UART): 3 ch
 - 3-wire variable-length serial interface B (CSIB): 2 ch
- CAN controller: 2 ch
- A/D converter 10-bit resolution: 16 ch
- Clock generator Main clock/subclock operation:
 - CPU clock in seven steps (fxx, fxx/2, fxx/4, fxx/8, fxx/16, fxx/32, fxt)
 - Clock-through mode/PLL mode selectable
 - Internal oscillator: 200 kHz (TYP.)
- Power save function: HALT/IDLE1/IDLE2/software STOP/subclock/sub-IDLE modes
- Package: 100-pin plastic LQFP (fine pitch) (14 × 14)

| Part Number | Internal ROM | Internal RAM | CAN I/F |
|-------------|------------------|--------------|-----------|
| uPD703234 | 128KB (Mask ROM) | 6KB | 2 channel |
| uPD703235 | 256KB (Mask ROM) | 12KB | 2 channel |
| UPD70F3234 | 128KB (Flash) | 6KB | 2 channel |
| uPD70F3235 | 256KB (Flash) | 12KB | 2 channel |
| uPD70F3236 | 384KB (Flash) | 16KB | 2 channel |

Table of Contents

1. Electrical Specifications..... 4

 1.1 Electrical Specifications of (A)-Grade 4

 1.1.1 Absolute maximum ratings 4

 1.1.2 Capacitance 8

 1.1.3 Operating conditions 8

 1.1.4 Oscillator Characteristics 9

 1.1.5 PLL Characteristics 11

 1.1.6 Ring-OSC Characteristics 11

 1.1.7 Voltage Regulator Characteristics 11

 1.1.8 DC Characteristics 12

 1.1.9 Data Retention Characteristics 16

 1.1.10 AC Characteristics 17

 1.2 Electrical Specifications of (A1)-Grade 28

 1.2.1 Absolute maximum ratings 28

 1.2.2 Capacitance 32

 1.2.3 Operating conditions 32

 1.2.4 Oscillator Characteristics 33

 1.2.5 PLL Characteristics 35

 1.2.6 Ring-OSC Characteristics 35

 1.2.7 Voltage Regulator Characteristics 35

 1.2.8 DC Characteristics 36

 1.2.9 Data Retention Characteristics 40

 1.2.10 AC Characteristics 41

 1.3 Electrical Specifications of (A2)-Grade 52

 1.3.1 Absolute maximum ratings 52

 1.3.2 Capacitance 56

 1.3.3 Operating conditions 56

 1.3.4 Oscillator Characteristics 57

 1.3.5 PLL Characteristics 59

 1.3.6 Ring-OSC Characteristics 59

 1.3.7 Voltage Regulator Characteristics 59

 1.3.8 DC Characteristics 60

 1.3.9 Data Retention Characteristics 64

 1.3.10 AC Characteristics 65

2. Injected Current Specification..... 76

 2.1 Injected Current Specification of (A)-Grade 76

 2.1.1 Absolute Maximum Ratings 76

 2.1.2 DC Characteristics for overload current 76

 2.1.3 DC Characteristics for pins influenced by injected current on an adjacent pin 77

 2.1.4 A/D converter influenced by injected current on an adjacent pin 78

 2.2 Injected Current Specification of (A1)-Grade 79

 2.2.1 Absolute Maximum Ratings 79

 2.2.2 DC Characteristics for overload current 79

 2.2.3 DC Characteristics for pins influenced by injected current on an adjacent pin 80

 2.2.4 A/D converter influenced by injected current on an adjacent pin 81

 2.3 Injected Current Specification of (A2)-Grade 82

2.3.1 Absolute Maximum Ratings82

2.3.2 DC Characteristics for overload current82

2.3.3 DC Characteristics for pins influenced by injected current on an adjacent pin.....83

2.3.4 A/D converter influenced by injected current on an adjacent pin84

3. Package Drawings85

Figure 3-1: Package Drawing85

4. Recommended Soldering Conditions.....86

Table 4-1: Soldering Conditions.....86

1. Electrical Specifications

1.1 Electrical Specifications of (A)-Grade

1.1.1 Absolute maximum ratings

Absolute maximum ratings (T_A = 25°C): Flash memory products (1/2)

| Parameter | Symbol | Conditions | Ratings | Unit |
|----------------------|--------------------|---|--|------|
| Supply voltage | V _{DD} | V _{DD} = EV _{DD} = BV _{DD} | -0.5 to +6.5 | V |
| | BV _{DD} | V _{DD} = EV _{DD} = BV _{DD} | -0.5 to +6.5 | V |
| | EV _{DD} | V _{DD} = EV _{DD} = BV _{DD} | -0.5 to +6.5 | V |
| | AV _{REF0} | | -0.5 to +6.5 | V |
| | V _{SS} | V _{SS} = EV _{SS} = BV _{SS} = AV _{SS} | -0.5 to +0.5 | V |
| | AV _{SS} | V _{SS} = EV _{SS} = BV _{SS} = AV _{SS} | -0.5 to +0.5 | V |
| | BV _{SS} | V _{SS} = EV _{SS} = BV _{SS} = AV _{SS} | -0.5 to +0.5 | V |
| | EV _{SS} | V _{SS} = EV _{SS} = BV _{SS} = AV _{SS} | -0.5 to +0.5 | V |
| Input voltage | V _{I1} | P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P90 to P915, RESET, FLMD0 | -0.5 to EV _{DD} + 0.5 ^{Note} | V |
| | V _{I2} | PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL13 | -0.5 to BV _{DD} + 0.5 ^{Note} | V |
| | V _{I3} | X1, X2, XT1, XT2 | -0.5 to V _{RO} + 0.5 ^{Note} | V |
| Analog input voltage | V _{IAN} | P70 to P715 | -0.5 to AV _{REF0} + 0.5 ^{Note} | V |

Note Be sure not to exceed the absolute maximum ratings (MAX. value) of each supply voltage.

Cautions 1. Avoid direct connections among the IC device output (or I/O) pins and between V_{DD} or V_{CC} and GND.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Absolute maximum ratings (T_A = 25°C): Flash memory products (2/2)

| Parameter | Symbol | Conditions | Ratings | Unit | |
|-------------------------------|------------------|---|-------------------|------|----|
| Output current, low | I _{OL} | P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P90 to P915 | Per pin | 4 | mA |
| | | | Total of all pins | 50 | mA |
| | | P70 to P715 | Per pin | 4 | mA |
| | | | Total of all pins | 20 | mA |
| | | PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL13 | Per pin | 4 | mA |
| | | | Total of all pins | 50 | mA |
| Output current, high | I _{OH} | P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P90 to P915 | Per pin | -4 | mA |
| | | | Total of all pins | -50 | mA |
| | | P70 to P715 | Per pin | -4 | mA |
| | | | Total of all pins | -20 | mA |
| | | PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL13 | Per pin | -4 | mA |
| | | | Total of all pins | -50 | mA |
| Operating ambient temperature | T _A | Normal operating mode | -40 to +85 | °C | |
| | | Flash programming mode | -40 to +85 | °C | |
| Storage temperature | T _{stg} | | -40 to +125 | °C | |

- Cautions**
- 1. Avoid direct connections among the IC device output (or I/O) pins and between V_{DD} or V_{CC} and GND.**
 - 2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Absolute maximum ratings (T_A = 25°C): Mask ROM products (1/2)

| Parameter | Symbol | Conditions | Ratings | Unit |
|----------------------|--------------------|---|--|------|
| Supply voltage | V _{DD} | V _{DD} = EV _{DD} = BV _{DD} | -0.5 to +6.5 | V |
| | BV _{DD} | V _{DD} = EV _{DD} = BV _{DD} | -0.5 to +6.5 | V |
| | EV _{DD} | V _{DD} = EV _{DD} = BV _{DD} | -0.5 to +6.5 | V |
| | AV _{REF0} | | -0.5 to +6.5 | V |
| | V _{SS} | V _{SS} = EV _{SS} = BV _{SS} = AV _{SS} | -0.5 to +0.5 | V |
| | AV _{SS} | V _{SS} = EV _{SS} = BV _{SS} = AV _{SS} | -0.5 to +0.5 | V |
| | BV _{SS} | V _{SS} = EV _{SS} = BV _{SS} = AV _{SS} | -0.5 to +0.5 | V |
| | EV _{SS} | V _{SS} = EV _{SS} = BV _{SS} = AV _{SS} | -0.5 to +0.5 | V |
| Input voltage | V _{I1} | P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P90 to P915, $\overline{\text{RESET}}$, IC | -0.5 to EV _{DD} + 0.5 ^{Note} | V |
| | V _{I2} | PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL13 | -0.5 to BV _{DD} + 0.5 ^{Note} | V |
| | V _{I3} | X1, X2, XT1, XT2 | -0.5 to V _{RO} + 0.5 ^{Note} | V |
| Analog input voltage | V _{IAN} | P70 to P715 | -0.5 to AV _{REF0} + 0.5 ^{Note} | V |

Note Be sure not to exceed the absolute maximum ratings (MAX. value) of each supply voltage.

- Cautions**
1. Avoid direct connections among the IC device output (or I/O) pins and between V_{DD} or V_{CC} and GND.
 2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Absolute maximum ratings (T_A = 25°C): Mask ROM products (2/2)

| Parameter | Symbol | Conditions | Ratings | Unit | | | |
|---|-------------------|---|-------------------|---|-------------------|-----|----|
| Output current, low | I _{OL} | P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P90 to P915 | Per pin | 4 | mA | | |
| | | | Total of all pins | 50 | mA | | |
| | | P70 to P715 | Per pin | 4 | mA | | |
| | | | Total of all pins | 20 | mA | | |
| | | PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL13 | Per pin | 4 | mA | | |
| | | | Total of all pins | 50 | mA | | |
| | | Output current, high | I _{OH} | P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P90 to P915 | Per pin | -4 | mA |
| | | | | | Total of all pins | -50 | mA |
| P70 to P715 | Per pin | | | -4 | mA | | |
| | Total of all pins | | | -20 | mA | | |
| PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL13 | Per pin | | | -4 | mA | | |
| | Total of all pins | | | -50 | mA | | |
| Operating ambient temperature | T _A | | | Normal operating mode | -40 to +85 | °C | |
| Storage temperature | T _{stg} | | | | -65 to +150 | °C | |

- Cautions**
- 1. Avoid direct connections among the IC device output (or I/O) pins and between V_{DD} or V_{CC} and GND.**
 - 2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

1.1.2 Capacitance

($T_A = 25^\circ\text{C}$, $V_{DD} = EV_{DD} = AV_{REF0} = BV_{DD} = AV_{REF1} = V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0\text{ V}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-----------------|----------|--|------|------|------|------|
| I/O capacitance | C_{IO} | $f_x = 1\text{ MHz}$, Unmeasured pins returned to 0 V. | | | 10 | pF |

1.1.3 Operating conditions

($T_A = -40\text{ to }+85^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0\text{ V}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---------------------------------|-----------|---|----------------------|------|----------------------|------|
| Internal system clock frequency | f_{CLK} | REGC Capacity = $4.7\ \mu\text{F}$, at operation with main clock | 4 | | 20 | MHz |
| | | REGC Capacity = $4.7\ \mu\text{F}$, at operation with subclock (crystal resonator) | 32 | | 35 | kHz |
| | | REGC Capacity = $4.7\ \mu\text{F}$, at operation with subclock (RC resonator) | 12.5 ^{Note} | | 27.5 ^{Note} | kHz |

Note The internal system clock frequency is half the oscillation frequency.

1.1.4 Oscillator Characteristics

Main clock oscillator characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V)

| Resonator | Recommended Circuit | Parameter | Conditions | MIN. | TYP. | MAX. | Unit |
|--------------------------|---------------------|--|-------------------------|-----------------------|---------------|------|------|
| Ceramic resonator | | Oscillation frequency (fx) ^{Note 1} | | 4 | | 5 | MHz |
| | | Oscillation stabilization time ^{Note 2} | After reset release | | $2^{16}/f_x$ | | s |
| | | | After STOP mode release | 0.5 ^{Note 3} | Note 4 | | ms |
| After IDLE2 mode release | 0.35 | Note 4 | | ms | | | |
| Crystal resonator | | Oscillation frequency (fx) ^{Note 1} | | 4 | | 5 | MHz |
| | | Oscillation stabilization time ^{Note 2} | After reset release | | $2^{16}/f_x$ | | s |
| | | | After STOP mode release | 0.5 ^{Note 3} | Note 4 | | ms |
| After IDLE2 mode release | 350 | Note 4 | | μs | | | |

- Notes**
1. Indicates only oscillator characteristics.
 2. Time required to stabilize the crystal resonator after reset or STOP mode is released.
 3. Time required to stabilize access to the internal flash memory.
 4. The value differs depending on the OSTS register settings.

Cautions 1. When using the main clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
 - Do not cross the wiring with the other signal lines.
 - Do not route the wiring near a signal line through which a high fluctuating current flows.
 - Always make the ground point of the oscillator capacitor the same potential as V_{SS}.
 - Do not ground the capacitor to a ground pattern through which a high current flows.
 - Do not fetch signals from the oscillator.
2. When the main clock is stopped and the device is operating on the subclock, wait until the oscillation stabilization time has been secured by the program before switching back to the main clock.

Subclock oscillator characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V)

| Resonator | Recommended Circuit | Parameter | Conditions | MIN. | TYP. | MAX. | Unit |
|-----------------------------|---------------------|--|--|------|--------|------|---------|
| Crystal resonator Note 5 | | Oscillation frequency (f_{XT}) Note 1 | | 32 | 32.768 | 35 | kHz |
| | | Oscillation stabilization time Note 2 | | | | 10 | s |
| RC resonator | | Oscillation frequency (f_{XT}) Notes 1, 4 | R = 390 k Ω \pm 5% C = 47 pF \pm 10% Note 3 | 25 | 40 | 55 | kHz |
| | | Oscillation stabilization time Note 2 | | | | 100 | μ s |

- Notes**
1. Indicates only oscillator characteristics. Refer to **27. 1. 10 AC Characteristics** for CPU operating clock.
 2. Time required from when V_{DD} reaches oscillation voltage range (MIN.: 3.5 V) to when the crystal resonator stabilizes.
 3. In order to avoid the influence of wiring capacity, shorten wiring as much as possible.
 4. RC oscillation frequency is 40 kHz (Typ.). This clock is divided (1/2) internally. In case of RC oscillator, internal system clock frequency (f_{XT}) is 12.5 kHz (Min.), 20 kHz (Typ.), and 27.5 kHz (Max.).
 5. The values of capacitors $C1'$, $C2'$ and resistors $R1'$ depend on the resonator used and must be specified in cooperation with the manufacturer.

Cautions 1. When using the subclock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
 - Do not cross the wiring with the other signal lines.
 - Do not route the wiring near a signal line through which a high fluctuating current flows.
 - Always make the ground point of the oscillator capacitor the same potential as V_{SS} .
 - Do not ground the capacitor to a ground pattern through which a high current flows.
 - Do not fetch signals from the oscillator.
2. The subclock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main clock oscillator. Particular care is therefore required with the wiring method when the subclock is used.

1.1.5 PLL Characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|------------------|-----------|------------------------------------|------|------|------|---------------|
| Input frequency | f_x | | 4 | | 5 | MHz |
| Output frequency | f_{xx} | | 16 | | 20 | MHz |
| Clock time | t_{PLL} | After V_{DD} reaches MIN.: 3.5 V | | | 800 | μs |

1.1.6 Ring-OSC Characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD}$, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V)

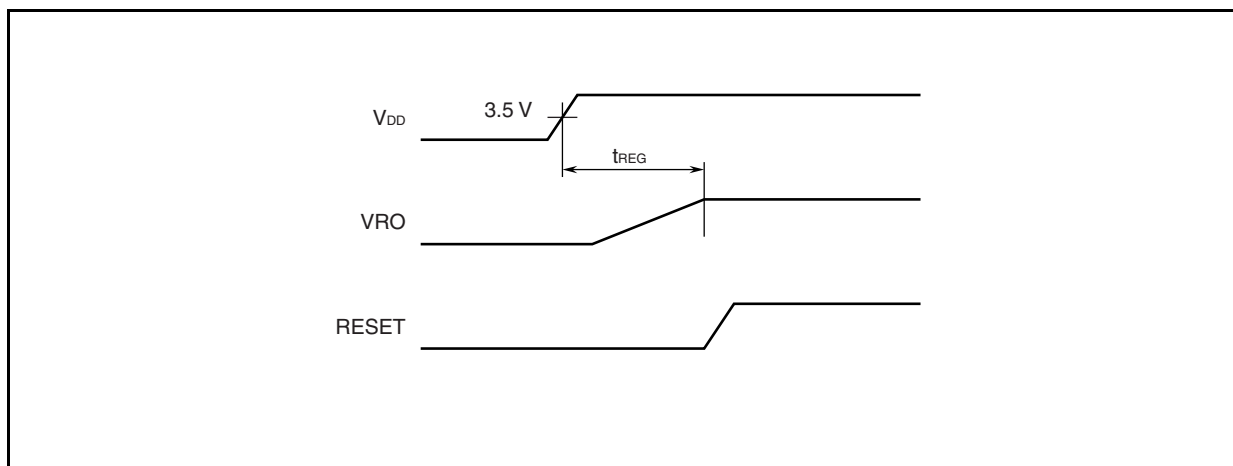
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|------------------|--------|------------|------|------|------|------|
| Output frequency | f_r | | 100 | 200 | 400 | kHz |

1.1.7 Voltage Regulator Characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD}$, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-----------------------------|-----------|--|------|------|------|------|
| Input voltage | V_{DD} | | 3.5 | | 5.5 | V |
| Output voltage | V_{RO} | | | 2.5 | | V |
| Lock time ^{Note 1} | t_{REG} | After V_{DD} reaches MIN.: 3.5 V Connect $C = 4.7 \mu\text{F} \pm 20\%$ to REGC pin | | | 1 | ms |

Note 1. The lock time does not have to be considered for devices that have POC.



1.1.8 DC Characteristics

(1) Input/Output level

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0\text{ V}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|---|-----------|---|---------------------------|-------------------|----------------|-------------|---|
| Input voltage, high | V_{IH1} | P30, P34, P38, P41, P98, P911 | $0.7EV_{DD}$ | | EV_{DD} | V | |
| | V_{IH2} | P00 to P06, P10, P11, P31 to P33, P35, P39, P40, P42, P50 to P55, P90 to P97, P99, P910, P912 to P915 | $0.8EV_{DD}$ | | EV_{DD} | V | |
| | V_{IH3} | PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL13 | $0.7BV_{DD}$ | | BV_{DD} | V | |
| | V_{IH4} | P70 to P715 | $0.7AV_{REF0}$ | | AV_{REF0} | V | |
| | V_{IH5} | RESET, FLMD0 | $0.8EV_{DD}$ | | EV_{DD} | V | |
| Input voltage, low | V_{IL1} | P30, P34, P38, P41, P98, P911 | EV_{SS} | | $0.3EV_{DD}$ | V | |
| | V_{IL2} | P00 to P06, P10, P11, P31 to P33, P35, P39, P40, P42, P50 to P55, P90 to P97, P99, P910, P912 to P915 | EV_{SS} | | $0.2EV_{DD}$ | V | |
| | V_{IL3} | PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL13 | BV_{SS} | | $0.3BV_{DD}$ | V | |
| | V_{IL4} | P70 to P715 | AV_{SS} | | $0.3AV_{REF0}$ | V | |
| | V_{IL5} | RESET, FLMD0 | EV_{SS} | | $0.2EV_{DD}$ | V | |
| Output voltage, high <small>Note 1</small> | V_{OH1} | P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P90 to P915 | $I_{OH} = -1.0\text{ mA}$ | $EV_{DD} - 1.0$ | | EV_{DD} | V |
| | | | $I_{OH} = -0.1\text{ mA}$ | $EV_{DD} - 0.5$ | | EV_{DD} | V |
| | V_{OH2} | PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL13 | $I_{OH} = -1.0\text{ mA}$ | $BV_{DD} - 1.0$ | | BV_{DD} | V |
| | | | $I_{OH} = -0.1\text{ mA}$ | $BV_{DD} - 0.5$ | | BV_{DD} | V |
| | V_{OH3} | P70 to P715 | $I_{OH} = -1.0\text{ mA}$ | $AV_{REF0} - 1.0$ | | AV_{REF0} | V |
| | | | $I_{OH} = -0.1\text{ mA}$ | $AV_{REF0} - 0.5$ | | AV_{REF0} | V |
| Output voltage, low <small>Note 1</small> | V_{OL1} | P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P90 to P915 | $I_{OL} = 1.0\text{ mA}$ | 0 | | 0.4 | V |
| | V_{OL2} | PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL13 | $I_{OL} = 1.0\text{ mA}$ | 0 | | 0.4 | V |
| | V_{OL3} | P70 to P715 | $I_{OL} = 1.0\text{ mA}$ | 0 | | 0.4 | V |
| Pull-up resistor | R_1 | $V_I = 0\text{ V}$ | 10 | 30 | 100 | $k\Omega$ | |
| Pull-down resistor <small>Note 2</small> | R_2 | $V_I = V_{DD}$ | 10 | 30 | 100 | $k\Omega$ | |

Notes 1. Total I_{OH}/I_{OL} (Max.) is 20 mA/-20 mA each power supply terminal (EV_{DD} , BV_{DD} and AV_{REF0}).

2. DRST pin only (OCDM0 is the control register).

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

(2) Pin leakage current

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|------------------------------|-------------------|-----------------------------------|------------------------------|------|------|------|---------------|
| Input leakage current, high | I _{LIH1} | V _{IN} = V _{DD} | Analog pins | | | +0.2 | μA |
| | | | Other pins ^{Note 1} | | | +0.5 | |
| Input leakage current, low | I _{LIL1} | V _{IN} = 0 V | Analog pins | | | -0.2 | μA |
| | | | Other pins ^{Note 1} | | | -0.5 | |
| Output leakage current, high | I _{LOH1} | V _O = V _{DD} | Analog pins | | | +0.2 | μA |
| | | | Other pins | | | +0.5 | |
| Output leakage current, low | I _{LOL1} | V _O = 0 V | Analog pins | | | -0.2 | μA |
| | | | Other pins | | | -0.5 | |

Note 1. For flash memory product, specification of FLMD0 is as follows:

- Input leakage current, high: 2 μA
- Input leakage current, low: -2 μA

(3) Supply current

Supply current (V850ES/FG2: μ PD70F3236, μ PD70F3235, μ PD70F3234)

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|--|------------------|---|---|------|------|------|---------|
| Flash memory products supply current ^{Note 1} | I _{DD1} | Normal operation | f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions operating | | 30 | 45 | mA |
| | | | f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions stopped | | 22 | | mA |
| | I _{DD2} | HALT mode | f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions operating | | 18 | 28 | mA |
| | | | f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions stopped | | 11 | | mA |
| | I _{DD3} | IDLE1 mode | f _{xx} = 5 MHz (OSC = 5 MHz), PLL off | | 0.6 | 0.9 | mA |
| | I _{DD4} | IDLE2 mode | f _{xx} = 5 MHz (OSC = 5 MHz), PLL off | | 0.25 | 0.7 | mA |
| | I _{DD5} | Subclock operation mode ^{Notes 2, 3} | Crystal resonator f _{XT} = 32.768 kHz | | 200 | 400 | μ A |
| | | | RC resonator f _{XT} = 40 kHz ^{Note 4} | | 200 | 400 | μ A |
| | I _{DD6} | Sub-IDLE mode ^{Notes 2, 3} | Crystal resonator f _{XT} = 32.768 kHz | | 20 | 120 | μ A |
| | | | RC resonator f _{XT} = 40 kHz ^{Note 4} | | 35 | 140 | μ A |
| | I _{DD7} | Stop mode ^{Notes 2, 5} | POC stopped, Ring-OSC stopped | | 7 | 50 | μ A |
| | | | POC operating, Ring-OSC stopped | | 10 | 55 | μ A |
| | | | POC stopped, Ring-OSC operating | | 15 | 65 | μ A |
| | | | POC operating, Ring-OSC operating | | 18 | 70 | μ A |

Notes 1. Total current of V_{DD}, EV_{DD}, and BV_{DD} (all ports stopped).

The current of AV_{REF0} and the port buffer current including the current flowing through the on-chip pull-up/pull-down resistors are not included.

2. When the main OSC is stopped.
3. POC operating, Ring-OSC operating.
4. The RC oscillation frequency is 40 kHz(TYP.). This clock is internally divided by 2.
5. When the sub-OSC is not used.

Supply current (V850ES/FG2: μ PD703235, μ PD703234)

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|---|------------------|---|---|------|------|------|---------|
| Mask ROM products supply current ^{Note 1} | I _{DD1} | Normal operation | f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions operating | | 25 | 40 | mA |
| | | | f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions stopped | | 20 | | mA |
| | I _{DD2} | HALT mode | f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions operating | | 14 | 24 | mA |
| | | | f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions stopped | | 9 | | mA |
| | I _{DD3} | IDLE1 mode | f _{xx} = 5 MHz (OSC = 5 MHz), PLL off | | 0.25 | 0.7 | mA |
| | I _{DD4} | IDLE2 mode | f _{xx} = 5 MHz (OSC = 5 MHz), PLL off | | 0.2 | 0.7 | mA |
| | I _{DD5} | Subclock operation mode ^{Notes 2, 3} | Crystal resonator f _{XT} = 32.768 kHz | | 50 | 350 | μ A |
| | I _{DD6} | Sub-IDLE mode ^{Notes 2, 3} | Crystal resonator f _{XT} = 32.768 kHz | | 20 | 120 | μ A |
| | | | RC resonator f _{XT} = 40 kHz ^{Note 4} | | 35 | 140 | μ A |
| | I _{DD7} | Stop mode ^{Notes 2, 5} | POC stopped, Ring-OSC stopped | | 7 | 50 | μ A |
| | | | POC operating, Ring-OSC stopped | | 10 | 55 | μ A |
| | | | POC stopped, Ring-OSC operating | | 15 | 65 | μ A |
| | | | POC operating, Ring-OSC operating | | 18 | 70 | μ A |

Notes 1. Total current of V_{DD}, EV_{DD}, and BV_{DD} (all ports stopped).

The current of AV_{REF0} and the port buffer current including the current flowing through the on-chip pull-up/pull-down resistors are not included.

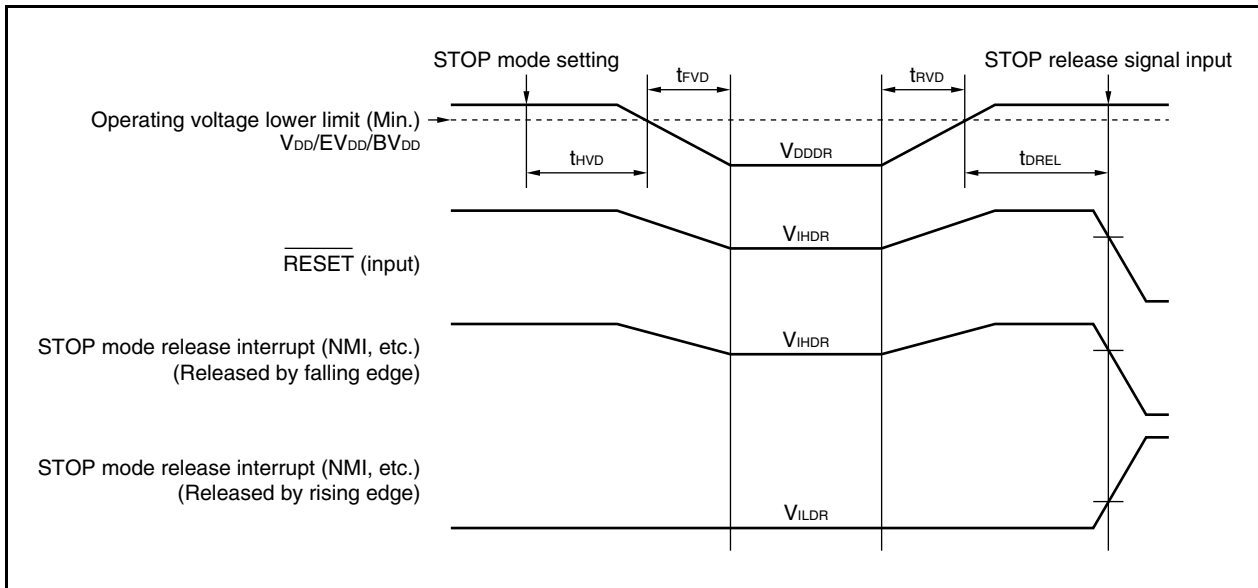
- 2. When the main OSC is stopped.
- 3. POC operating, Ring-OSC operating.
- 4. The RC oscillation frequency is 40 kHz(TYP.). This clock is internally divided by 2.
- 5. When the sub-OSC is not used.

1.1.9 Data Retention Characteristics

STOP Mode ($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 1.9$ V to 5.5 V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V)

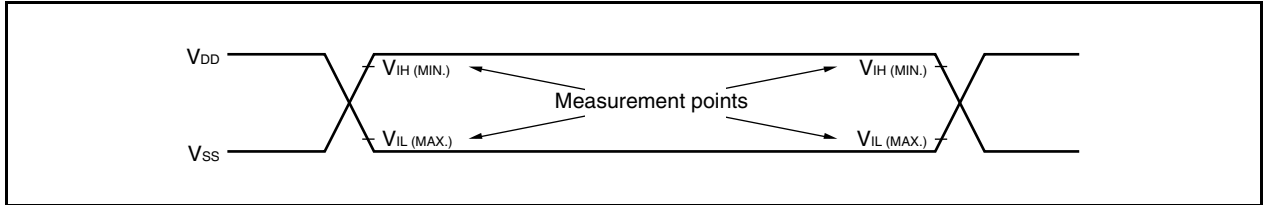
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|------------------------------------|------------|------------------------------------|---------------|------|---------------|---------------|
| Data retention voltage | V_{DDDR} | In STOP mode | 1.9 | | 5.5 | V |
| Data retention current | I_{DDDR} | $V_{DDDR} = 2.0$ V | | 6 | 450 | μA |
| Supply voltage rise time | t_{rVD} | | 1 | | | μs |
| Supply voltage fall time | t_{fVD} | | 1 | | | μs |
| Supply voltage retention time | t_{HVD} | After STOP mode release | 0 | | | ms |
| STOP release signal input time | t_{dREL} | After V_{DD} reaches MIN.: 3.5 V | 0 | | | μs |
| Data retention input voltage, high | V_{IHDR} | All input ports | $0.9V_{DDDR}$ | | V_{DDDR} | V |
| Data retention input voltage, low | V_{ILDR} | All input ports | 0 | | $0.1V_{DDDR}$ | V |

Caution Shifting to STOP mode and restoring from STOP mode must be performed within the rated operating range.

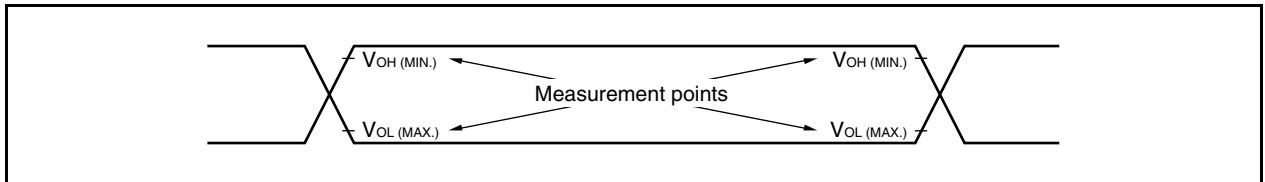


1.1.10 AC Characteristics

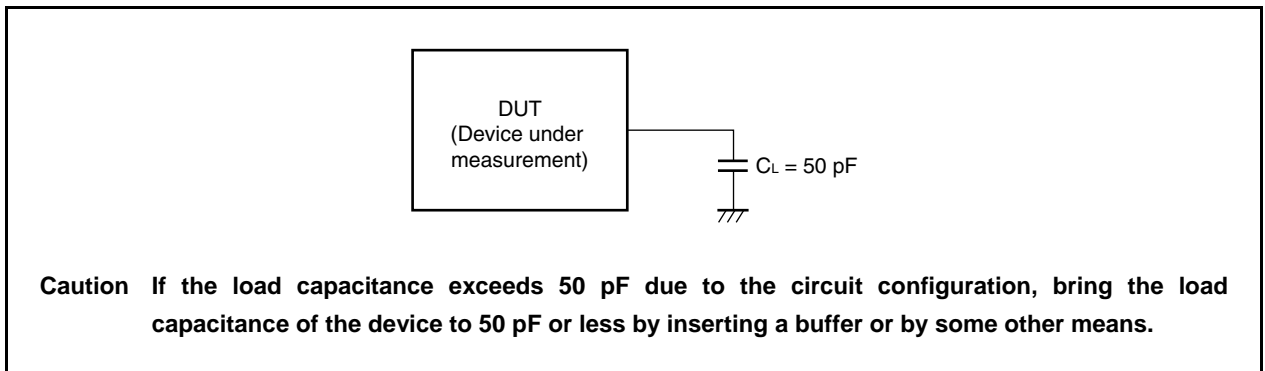
AC Test Input Measurement Points (V_{DD} , AV_{DD} , EV_{DD} , BV_{DD})



AC Test Output Measurement Points



Load Conditions

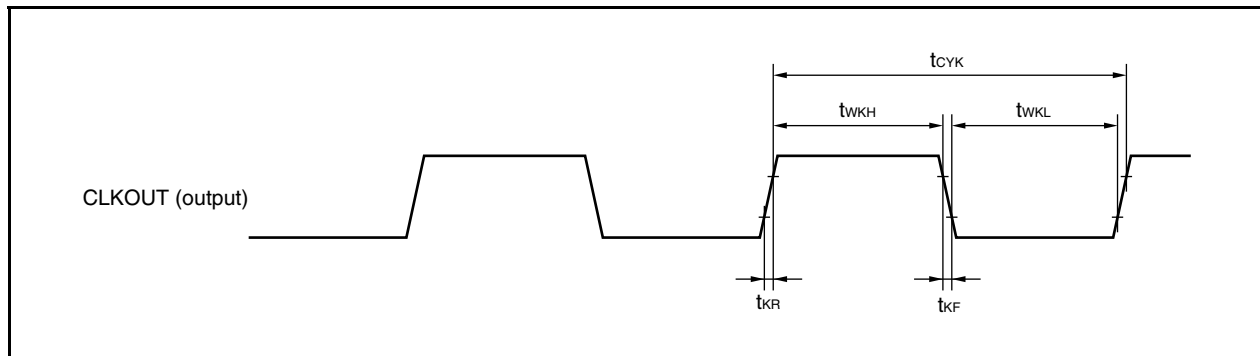


(1) CLKOUT output timing

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|------------------|-----------|------------|------------------|------------------|------|
| Output cycle | t_{CYK} | | 50 ns | 80 μs | |
| High-level width | t_{WKH} | | $t_{CYK}/2 - 15$ | | ns |
| Low-level width | t_{WKL} | | $t_{CYK}/2 - 15$ | | ns |
| Rise time | t_{KR} | | | 15 | ns |
| Fall time | t_{KF} | | | 15 | ns |

Clock Timing



(2) Basic Operation

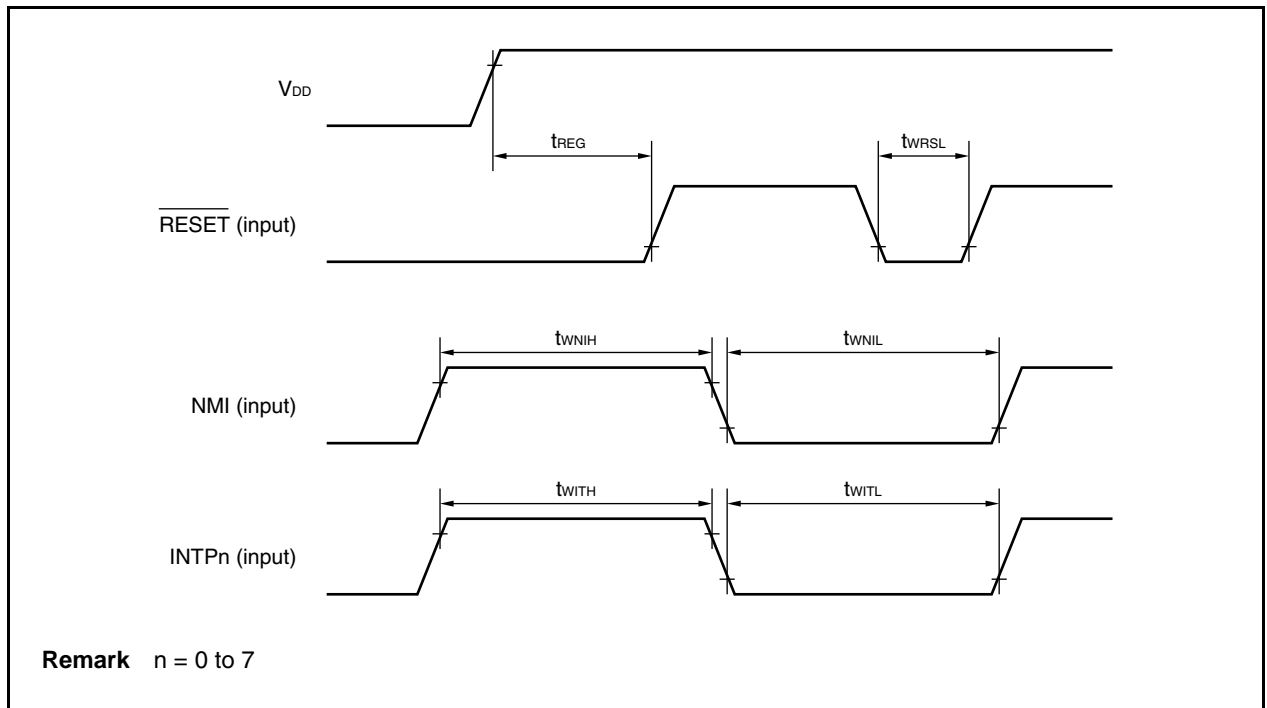
(a) Reset, Interrupt timing

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|--|------------|---------------------------------------|---------------|------|------|
| RESET low-level width | t_{WRSL} | | 500 | | ns |
| NMI high-level width | t_{WNIH} | Analog noise elimination | 500 | | ns |
| NMI low-level width | t_{WNIL} | Analog noise elimination | 500 | | ns |
| INTP _n ^{Note 1} high-level width | t_{WITH} | Analog noise elimination (n = 0 to 7) | 500 | | ns |
| | | Digital noise elimination (n = 3) | Note 2 | | ns |
| INTP _n ^{Note 1} low-level width | t_{WITL} | Analog noise elimination (n = 0 to 7) | 500 | | ns |
| | | Digital noise elimination (n = 3) | Note 2 | | ns |

- Notes**
- ADTRG is same spec (P03/INTP0/ADTRG). \overline{DRST} is same spec (P05/INTP2/ \overline{DRST}).
 - $2T_{\text{samp}} + 20$ or $3T_{\text{samp}} + 20$
 T_{samp} : Sampling clock for noise elimination

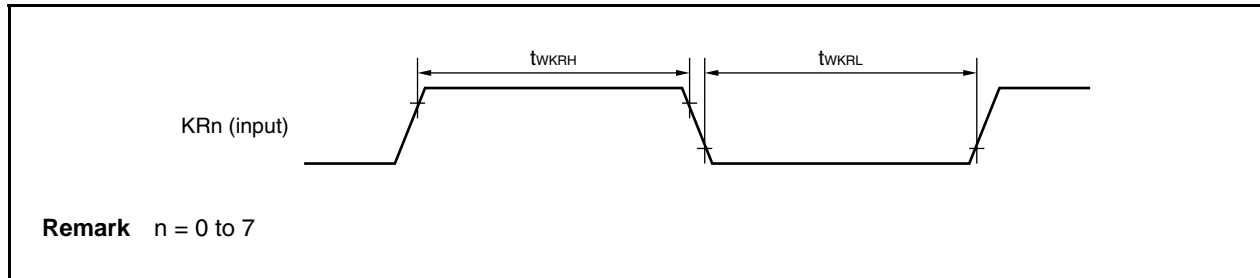
Reset/Interrupt



(b) Key return timing

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0\text{ V}$, $C_L = 50\text{ pF}$)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|----------------------------|------------|---|------|------|------|
| KRn input high-level width | t_{WKRH} | Analog noise elimination ($n = 0$ to 7) | 500 | | ns |
| KRn input low-level width | t_{WKRL} | | 500 | | ns |

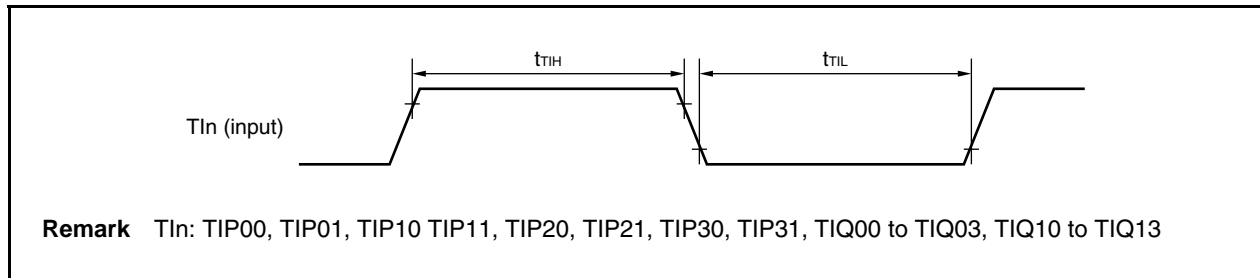


(c) Timer input timing

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0\text{ V}$, $C_L = 50\text{ pF}$)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|----------------------|-----------|---|-------------|------|------|
| TIn high-level width | t_{TIH} | TIP00, TIP01, TIP10, TIP11, TIP20, TIP21, TIP30, TIP31, | Note | | ns |
| TIn low-level width | t_{TIL} | TIQ00 to TIQ03, TIQ10 to TIQ13 | | | |

Note $2T_{\text{samp}} + 20$ or $3T_{\text{samp}} + 20$
 T_{samp} : Sampling clock for noise elimination



(d) CSIB timing

(i) Master mode

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|---|-------------|------------|-------------------|------|------|
| \overline{SCKBn} cycle time | t_{KCYn} | | 125 | | ns |
| \overline{SCKBn} high-level width | t_{KHn} | | $t_{KCYn}/2 - 15$ | | ns |
| \overline{SCKBn} low-level width | t_{KLn} | | $t_{KCYn}/2 - 15$ | | ns |
| SIBn setup time (to $\overline{SCKBn}\uparrow$) | t_{SIKn} | | 30 | | ns |
| SIBn hold time (from $\overline{SCKBn}\uparrow$) | t_{SIn} | | 25 | | ns |
| Output delay time from $\overline{SCKBn}\downarrow$ to SOBn | t_{KSOIn} | | | 25 | ns |

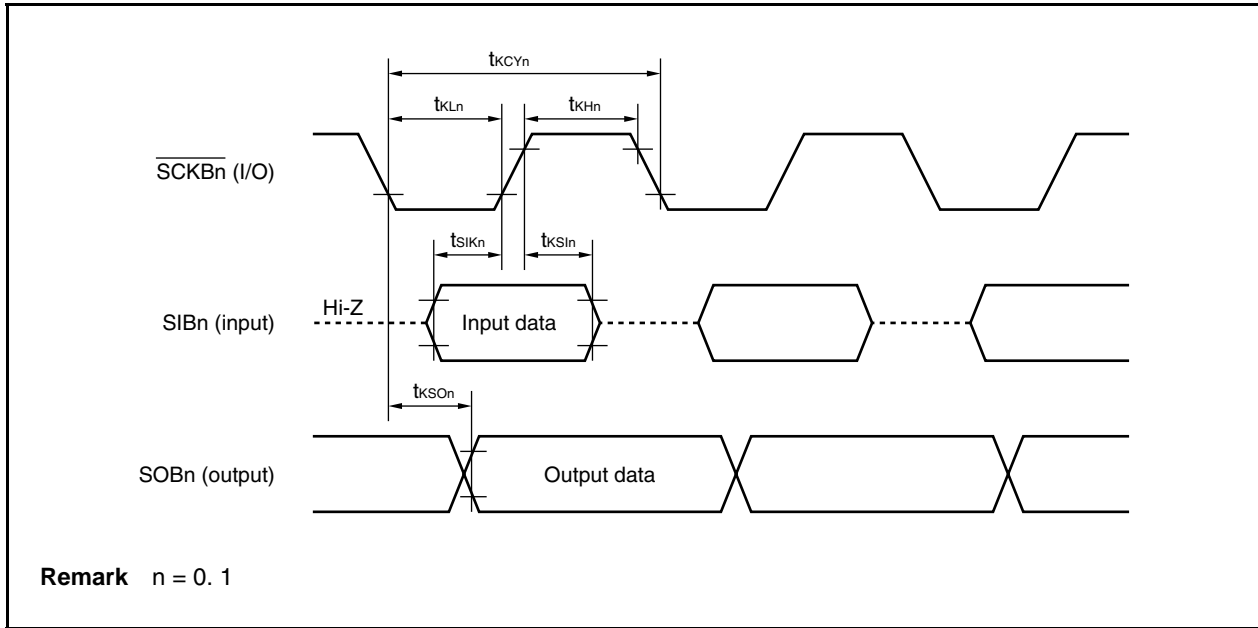
Remark n = 0, 1

(ii) Slave mode

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|---|-------------|------------|------|------|------|
| \overline{SCKBn} cycle time | t_{KCYn} | | 200 | | ns |
| \overline{SCKBn} high-level width | t_{KHn} | | 90 | | ns |
| \overline{SCKBn} low-level width | t_{KLn} | | 90 | | ns |
| SIBn setup time (to $\overline{SCKBn}\uparrow$) | t_{SIKn} | | 50 | | ns |
| SIBn hold time (from $\overline{SCKBn}\uparrow$) | t_{SIn} | | 50 | | ns |
| Output delay time from $\overline{SCKBn}\downarrow$ to SOBn | t_{KSOIn} | | | 50 | ns |

Remark n = 0, 1



(e) UART timing

$(T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

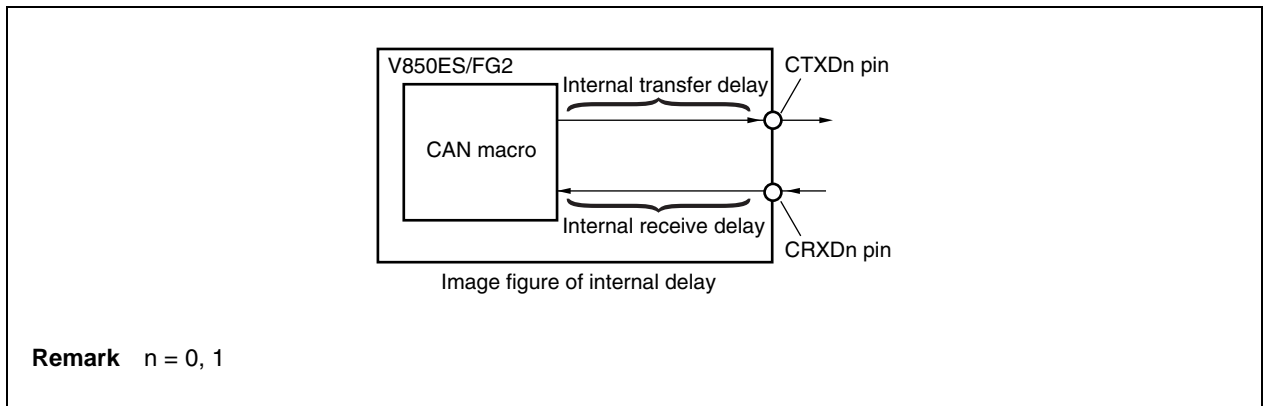
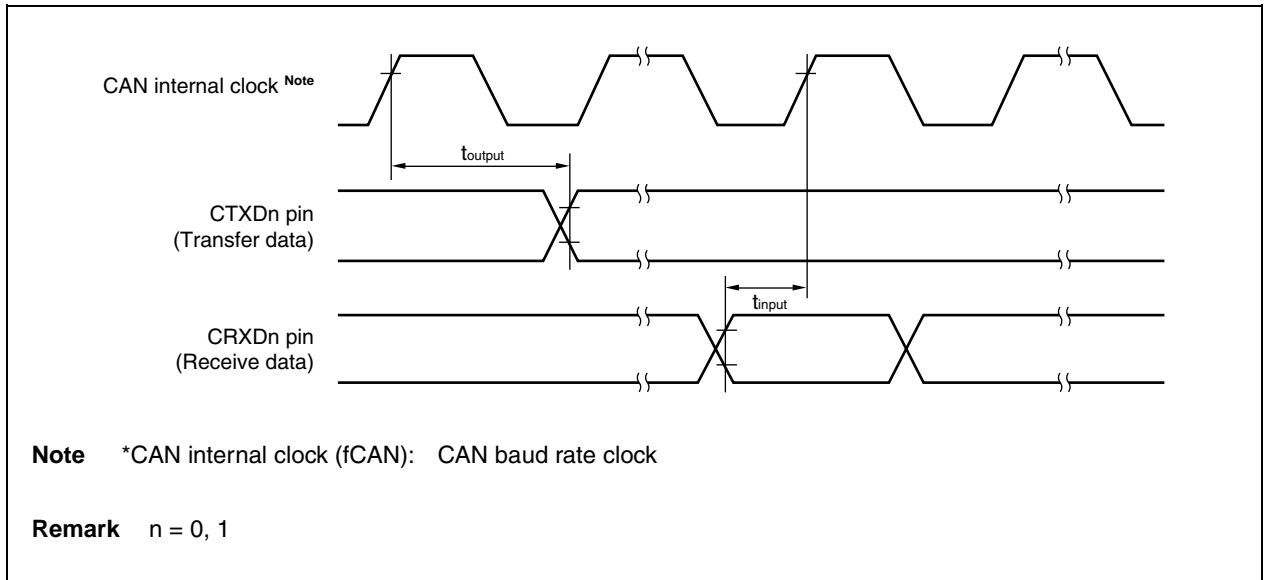
| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|--------------------|--------|------------|------|-------|------|
| Communication rate | | | | 312.5 | kbps |
| ASCK0 cycle time | | | | 10 | MHz |

(f) CAN timing

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V \leq $AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|-------------------------------------|--------|------------|------|------|------|
| Transfer rate | | | | 1 | Mbps |
| Internal delay time ^{Note} | | | | 100 | ns |

Note Internal delay time (t_{NODE}) = Internal transfer delay time (t_{OUTPUT}) + Internal receive delay time (t_{INPUT})



(g) A/D converter

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------------------|-------------|---------------------------------|-----------|------------|-------------|---------------|
| Resolution | | | | | 10 | bit |
| Overall error ^{Note} | | $4.0 \leq AV_{REF0} \leq 5.5$ V | | ± 0.15 | ± 0.3 | %FSR |
| Conversion time | t_{CONV} | | 3.1 | | 16 | μs |
| Analog input voltage | V_{IAN} | | AV_{SS} | | AV_{REF0} | V |
| AV_{REF0} current | I_{AREF0} | When using A/D converter | | 5 | 10 | mA |
| | | When not using A/D converter | | 1 | 10 | μA |

Note Excluding quantization error ($\pm 0.05\%$ FSR). Indicates the ratio to the full-scale value (%FSR).

Remark FSR: Full Scale Range

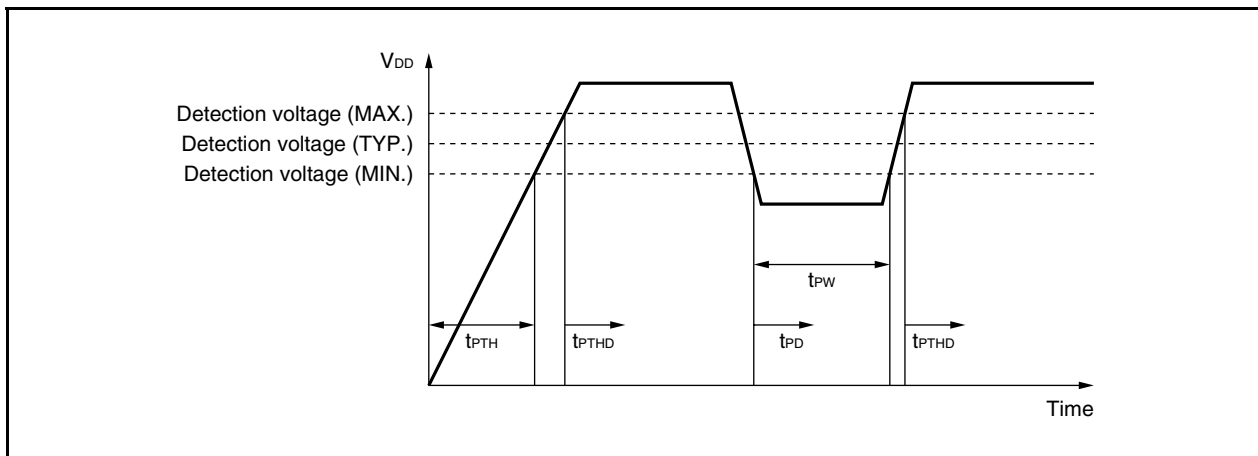
(h) POC circuit characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|------------|---|-------|------|------|------|
| Detection voltage | V_{POCO} | | 3.5 | 3.7 | 3.9 | V |
| Power supply startup time | t_{PTH} | $V_{DD} = 0$ V \rightarrow 3.5 V | 0.002 | | | ms |
| Response delay time 1 ^{Note 1} | t_{PTHD} | In case of power on. After V_{DD} reaches 3.9 V. | | | 3.0 | ms |
| Response delay time 2 ^{Note 2} | t_{PD} | In case of power off. After V_{DD} drops 3.5 V. | | | 1 | ms |
| Minimum V_{DD} width | t_{PW} | | 0.2 | | | ms |

Notes 1. From detect voltage to release reset signal.

2. From detect voltage to output reset signal.

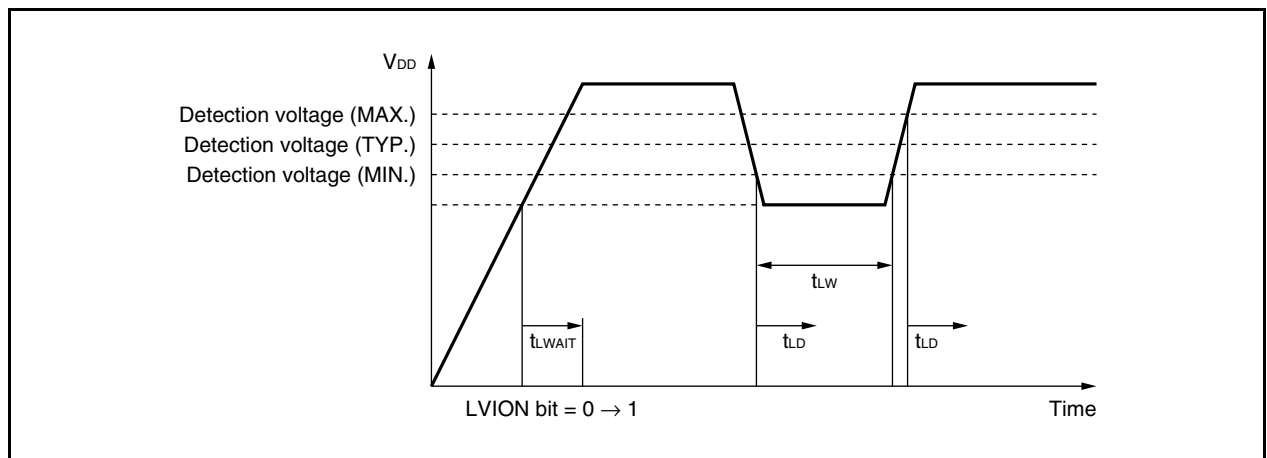


(i) LVI circuit characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|-------------|--|------|------|------|------|
| Detection voltage | V_{LV10} | | 4.2 | 4.4 | 4.6 | V |
| | V_{LV11} | | 4.0 | 4.2 | 4.4 | V |
| Response time ^{Note 1} | t_{LD} | After V_{DD} reaches V_{LV10}/V_{LV11} (Max.). After V_{DD} drops V_{LV10}/V_{LV11} (Min.). | | 0.2 | 2.0 | ms |
| Minimum V_{DD} width | t_{LW} | | 0.2 | | | ms |
| Reference voltage stabilization wait time ^{Note 2} | t_{LWAIT} | After V_{DD} reaches 3.5 V. After LVION bit (LVIM.bit7) = 0 \rightarrow 1 | | 0.1 | 0.2 | ms |

- Notes**
1. The time required to output an interrupt/reset after the detection voltage is detected.
 2. Unnecessary when the POC function is used.

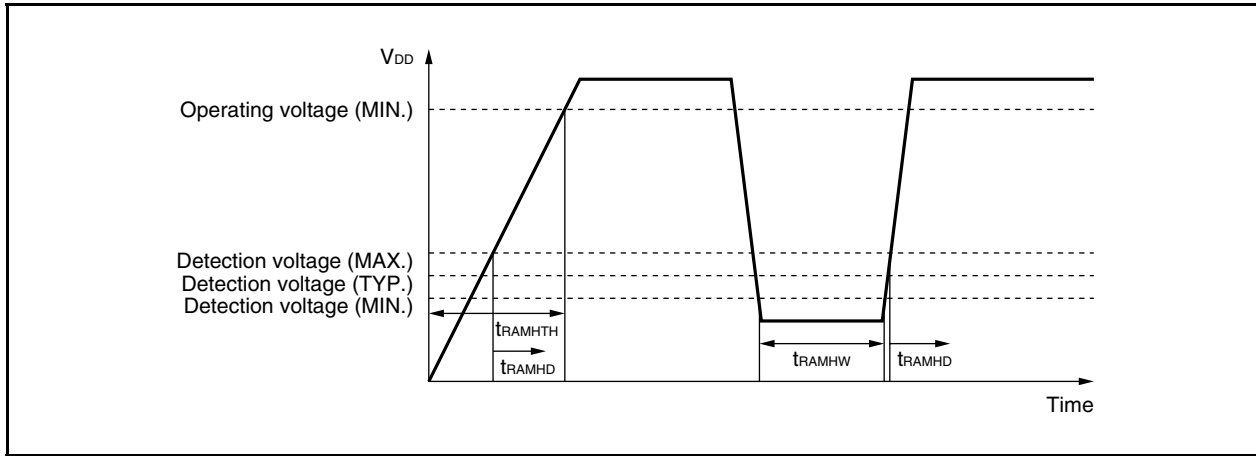


(j) RAM retention flag characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 1.9$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------------------|--------------|---|-------|------|-------|------|
| Detection voltage | V_{RAMH} | | 1.9 | 2.0 | 2.1 | V |
| Supply voltage rise time | t_{RAMHTH} | $V_{DD} = 0$ V \rightarrow 3.5 V | 0.002 | | 1,800 | ms |
| Response time ^{Note} | t_{RAMHD} | After the supply voltage reaches the detection voltage (MAX.) | | 0.2 | 2.0 | ms |
| Minimum V_{DD} width | t_{RAMHW} | | 0.2 | | | ms |

Note Time required to set the RAMF bit after the detection voltage is detected.



(k) Flash memory programming characteristics

(i) Basic characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------------|----------------------------|---|--------------|------|--------------|------------------|
| Operating frequency | f_{CPU} | | 4 | | 20 | MHz |
| Supply voltage | V_{DD} | | 3.5 | | 5.5 | V |
| Number of writes | C_{WRT} ^{Note} | | | | 100 | Times |
| Input voltage, high | V_{IH} | FLMD0 | $0.8EV_{DD}$ | | EV_{DD} | V |
| Input voltage, low | V_{IL} | FLMD0 | EV_{SS} | | $0.2EV_{DD}$ | V |
| Write time + erase time | t_{WRT} + t_{ERASE} | Flash: 256 KB ($\mu\text{PD70F3235}$) 384 KB ($\mu\text{PD70F3236}$) | | | T.B.D | s |
| Programming temperature | t_{PRG} | | -40 | | +85 | $^\circ\text{C}$ |

Note The initial write when the product is shipped, any erase → write set of operations, or any programming operation is counted as one rewrite.

Example: P: Write, E: Erase

Shipped product → P → E → P → E → P: 3 rewrites

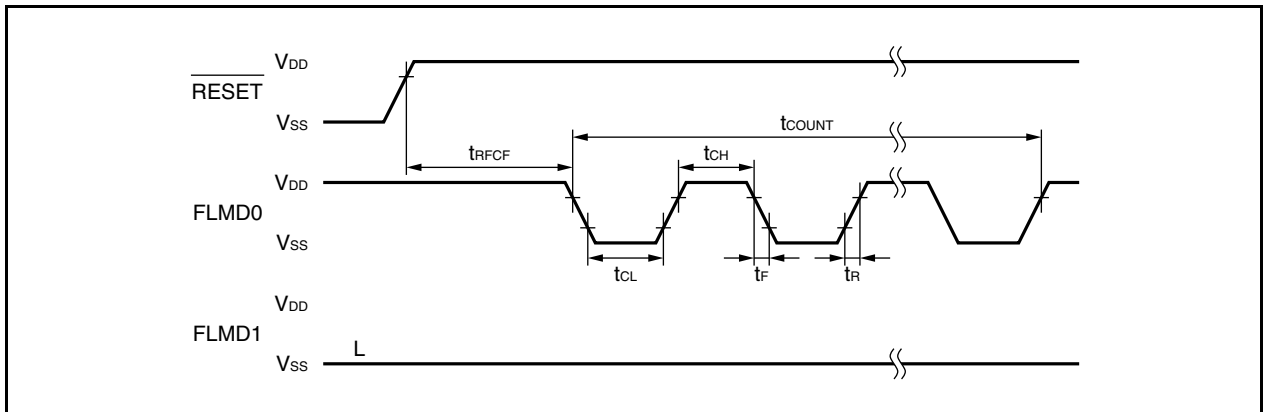
Shipped product → E → P → E → P → E → P: 3 rewrites

(ii) Serial Write Operation Characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|-------------|------------|---------------------|------|------|---------------|
| FLMD0 setup time from $\overline{\text{RESET}}\uparrow$ | t_{RFCF} | | $5000/f_x + \alpha$ | | | s |
| Count execution time | t_{COUNT} | | | | 3 | ms |
| FLMD0 high-level width | t_{CH} | | 10 | | 100 | μs |
| FLMD0 low-level width | t_{CL} | | 10 | | 100 | μs |
| FLMD rise time | t_R | | | | 50 | ns |
| FLMD fall time | t_F | | | | 50 | ns |

Note “ ” represents the oscillation stabilization time.



1.2 Electrical Specifications of (A1)-Grade

1.2.1 Absolute maximum ratings

Absolute Maximum Ratings (T_A = 25°C): Flash memory products (1/2)

| Parameter | Symbol | Conditions | Ratings | Unit |
|----------------------|--------------------|---|--|------|
| Supply voltage | V _{DD} | V _{DD} = EV _{DD} = BV _{DD} | -0.5 to +6.5 | V |
| | BV _{DD} | V _{DD} = EV _{DD} = BV _{DD} | -0.5 to +6.5 | V |
| | EV _{DD} | V _{DD} = EV _{DD} = BV _{DD} | -0.5 to +6.5 | V |
| | AV _{REF0} | | -0.5 to +6.5 | V |
| | V _{SS} | V _{SS} = EV _{SS} = BV _{SS} = AV _{SS} | -0.5 to +0.5 | V |
| | AV _{SS} | V _{SS} = EV _{SS} = BV _{SS} = AV _{SS} | -0.5 to +0.5 | V |
| | BV _{SS} | V _{SS} = EV _{SS} = BV _{SS} = AV _{SS} | -0.5 to +0.5 | V |
| | EV _{SS} | V _{SS} = EV _{SS} = BV _{SS} = AV _{SS} | -0.5 to +0.5 | V |
| Input voltage | V _{I1} | P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P90 to P915, RESET, FLMD0 | -0.5 to EV _{DD} + 0.5 ^{Note} | V |
| | V _{I2} | PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL13 | -0.5 to BV _{DD} + 0.5 ^{Note} | V |
| | V _{I3} | X1, X2, XT1, XT2 | -0.5 to V _{RO} + 0.5 ^{Note} | V |
| Analog input voltage | V _{IAN} | P70 to P715 | -0.5 to AV _{REF0} + 0.5 ^{Note} | V |

Note Be sure not to exceed the absolute maximum ratings (MAX. value) of each supply voltage.

Cautions 1. Avoid direct connections among the IC device output (or I/O) pins and between V_{DD} or V_{CC} and GND.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Absolute maximum ratings (T_A = 25°C): Flash memory products (2/2)

| Parameter | Symbol | Conditions | Ratings | Unit | |
|-------------------------------|------------------|--|-------------------|----------------------|----|
| Output current, low | I _{OL} | P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P90 to P915 | Per pin | 4 | mA |
| | | | Total of all pins | 50 ^{Note1} | mA |
| | | P70 to P715 | Per pin | 4 | mA |
| | | | Total of all pins | 20 ^{Note2} | mA |
| | | PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL13 | Per pin | 4 | mA |
| | | | Total of all pins | 50 ^{Note1} | mA |
| Output current, high | I _{OH} | P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P90 to P915 | Per pin | -4 | mA |
| | | | Total of all pins | -50 ^{Note1} | mA |
| | | P70 to P715 | Per pin | -4 | mA |
| | | | Total of all pins | -20 ^{Note2} | mA |
| | | PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL13 | Per pin | -4 | mA |
| | | | Total of all pins | -50 ^{Note1} | mA |
| Operating ambient temperature | T _A | Normal operating mode | -40 to +110 | °C | |
| | | Flash programming mode | -40 to +85 | °C | |
| Storage temperature | T _{stg} | | -40 to +125 | °C | |

Notes 1. This value is a value at the time of T_A = 25 °C. At the time of T_A = 110 °C, This value is 20 mA/-20 mA.

2. This value is a value at the time of T_A = 25 °C. At the time of T_A = 110 °C, This value is 10 mA/-10 mA.

Cautions 1. Avoid direct connections among the IC device output (or I/O) pins and between V_{DD} or V_{CC} and GND.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Absolute Maximum Ratings (T_A = 25°C): Mask ROM products (1/2)

| Parameter | Symbol | Conditions | Ratings | Unit |
|----------------------|--------------------|---|--|------|
| Supply voltage | V _{DD} | V _{DD} = EV _{DD} = BV _{DD} | -0.5 to +6.5 | V |
| | BV _{DD} | V _{DD} = EV _{DD} = BV _{DD} | -0.5 to +6.5 | V |
| | EV _{DD} | V _{DD} = EV _{DD} = BV _{DD} | -0.5 to +6.5 | V |
| | AV _{REF0} | | -0.5 to +6.5 | V |
| | V _{SS} | V _{SS} = EV _{SS} = BV _{SS} = AV _{SS} | -0.5 to +0.5 | V |
| | AV _{SS} | V _{SS} = EV _{SS} = BV _{SS} = AV _{SS} | -0.5 to +0.5 | V |
| | BV _{SS} | V _{SS} = EV _{SS} = BV _{SS} = AV _{SS} | -0.5 to +0.5 | V |
| | EV _{SS} | V _{SS} = EV _{SS} = BV _{SS} = AV _{SS} | -0.5 to +0.5 | V |
| Input voltage | V _{I1} | P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P90 to P915, $\overline{\text{RESET}}$, IC | -0.5 to EV _{DD} + 0.5 ^{Note} | V |
| | V _{I2} | PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL13 | -0.5 to BV _{DD} + 0.5 ^{Note} | V |
| | V _{I3} | X1, X2, XT1, XT2 | -0.5 to V _{RO} + 0.5 ^{Note} | V |
| Analog input voltage | V _{IAN} | P70 to P715 | -0.5 to AV _{REF0} + 0.5 ^{Note} | V |

Note Be sure not to exceed the absolute maximum ratings (MAX. value) of each supply voltage.

Cautions 1. Avoid direct connections among the IC device output (or I/O) pins and between V_{DD} or V_{CC} and GND.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Absolute maximum ratings (T_A = 25°C): Mask ROM products (2/2)

| Parameter | Symbol | Conditions | Ratings | Unit | |
|-------------------------------|------------------|--|-------------------|----------------------|----|
| Output current, low | I _{OL} | P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P90 to P915 | Per pin | 4 | mA |
| | | | Total of all pins | 50 ^{Note1} | mA |
| | | P70 to P715 | Per pin | 4 | mA |
| | | | Total of all pins | 20 ^{Note2} | mA |
| | | PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL13 | Per pin | 4 | mA |
| | | | Total of all pins | 50 ^{Note1} | mA |
| Output current, high | I _{OH} | P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P90 to P915 | Per pin | -4 | mA |
| | | | Total of all pins | -50 ^{Note1} | mA |
| | | P70 to P715 | Per pin | -4 | mA |
| | | | Total of all pins | -20 ^{Note2} | mA |
| | | PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL13 | Per pin | -4 | mA |
| | | | Total of all pins | -50 ^{Note1} | mA |
| Operating ambient temperature | T _A | | -40 to +110 | °C | |
| Storage temperature | T _{stg} | | -65 to +110 | °C | |

Notes 1. This value is a value at the time of T_A = 25 °C. At the time of T_A = 110 °C, This value is 20 mA/-20 mA.

2. This value is a value at the time of T_A = 25 °C. At the time of T_A = 110 °C, This value is 10 mA/-10 mA.

Cautions 1. Avoid direct connections among the IC device output (or I/O) pins and between V_{DD} or V_{CC} and GND.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

1.2.2 Capacitance

($T_A = 25^\circ\text{C}$, $V_{DD} = EV_{DD} = AV_{REF0} = BV_{DD} = AV_{REF1} = V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0\text{ V}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-----------------|----------|--|------|------|------|------|
| I/O capacitance | C_{IO} | $f_x = 1\text{ MHz}$, Unmeasured pins returned to 0 V. | | | 10 | pF |

1.2.3 Operating conditions

($T_A = -40\text{ to }+110^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0\text{ V}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---------------------------------|-----------|--|----------------------|------|----------------------|------|
| Internal system clock frequency | f_{CLK} | REGC Capacity = $4.7\ \mu\text{F}$ at operation with main clock | 4 | | 20 | MHz |
| | | REGC Capacity = $4.7\ \mu\text{F}$ at operation with subclock (RC resonator) | 12.5 ^{Note} | | 27.5 ^{Note} | kHz |

Note The internal system clock frequency is half the oscillation frequency.

1.2.4 Oscillator Characteristics

Main clock oscillator characteristics

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V)

| Resonator | Recommended Circuit | Parameter | Conditions | MIN. | TYP. | MAX. | Unit |
|--------------------------|---------------------|--|-------------------------|-----------------------|---------------|------|------|
| Ceramic resonator | | Oscillation frequency (fx) ^{Note 1} | | 4 | | 5 | MHz |
| | | Oscillation stabilization time ^{Note 2} | After reset release | | $2^{16}/f_x$ | | s |
| | | | After STOP mode release | 0.5 ^{Note 3} | Note 4 | | ms |
| After IDLE2 mode release | 0.35 | Note 4 | | ms | | | |
| Crystal resonator | | Oscillation frequency (fx) ^{Note 1} | | 4 | | 5 | MHz |
| | | Oscillation stabilization time ^{Note 2} | After reset release | | $2^{16}/f_x$ | | s |
| | | | After STOP mode release | 0.5 ^{Note 3} | Note 4 | | ms |
| After IDLE2 mode release | 350 | Note 4 | | μs | | | |

- Notes**
1. Indicates only oscillator characteristics.
 2. Time required to stabilize the crystal resonator after reset or STOP mode is released.
 3. Time required to stabilize access to the internal flash memory.
 4. The value differs depending on the OSTS register settings.

Cautions 1. When using the main clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
 - Do not cross the wiring with the other signal lines.
 - Do not route the wiring near a signal line through which a high fluctuating current flows.
 - Always make the ground point of the oscillator capacitor the same potential as V_{SS}.
 - Do not ground the capacitor to a ground pattern through which a high current flows.
 - Do not fetch signals from the oscillator.
2. When the main clock is stopped and the device is operating on the subclock, wait until the oscillation stabilization time has been secured by the program before switching back to the main clock.

Subclock Oscillator Characteristics

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V)

| Resonator | Recommended Circuit | Parameter | Conditions | MIN. | TYP. | MAX. | Unit |
|--------------|---------------------|---|---|------|------|------|---------------|
| RC resonator | | Oscillation frequency (f_{XT}) <small>Notes 1, 4</small> | $R = 390\text{ k}\Omega \pm 5\%$ <small>Note 3</small> $C = 47\text{ pF} \pm 10\%$ <small>Note 3</small> | 25 | 40 | 55 | kHz |
| | | Oscillation stabilization time <small>Note 2</small> | | | | 100 | μs |

- Notes**
1. Indicates only oscillator characteristics. Refer to **27. 2. 10 AC Characteristics** for CPU operating clock.
 2. Time required from when V_{DD} reaches oscillation voltage range (MIN.: 3.5 V) to when the crystal resonator stabilizes.
 3. In order to avoid the influence of wiring capacity, shorten wiring as much as possible.
 4. RC oscillation frequency is 40 kHz (Typ.). This clock is divided (1/2) internally. In case of RC oscillator, internal system clock frequency (f_{XT}) is 12.5 kHz (Min.), 20 kHz (Typ.), and 27.5 kHz (Max.).

Cautions 1. When using the subclock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
 - Do not cross the wiring with the other signal lines.
 - Do not route the wiring near a signal line through which a high fluctuating current flows.
 - Always make the ground point of the oscillator capacitor the same potential as V_{SS} .
 - Do not ground the capacitor to a ground pattern through which a high current flows.
 - Do not fetch signals from the oscillator.
2. The subclock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main clock oscillator. Particular care is therefore required with the wiring method when the subclock is used.

1.2.5 PLL Characteristics

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|------------------|-----------|------------------------------------|------|------|------|---------------|
| Input frequency | f_x | | 4 | | 5 | MHz |
| Output frequency | f_{xx} | | 16 | | 20 | MHz |
| Clock time | t_{PLL} | After V_{DD} reaches MIN.: 3.5 V | | | 800 | μs |

1.2.6 Ring-OSC Characteristics

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V)

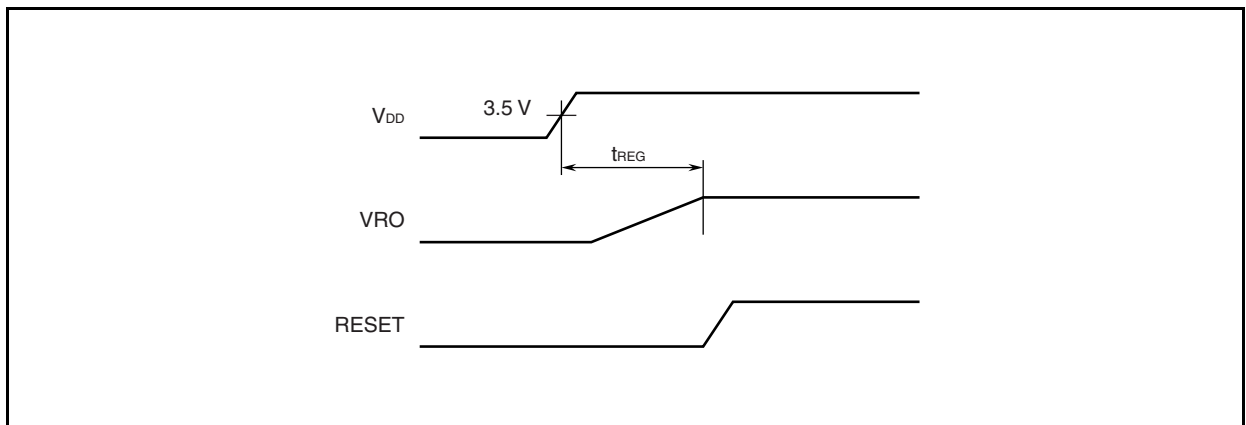
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|------------------|--------|------------|------|------|------|------|
| Output frequency | f_r | | 100 | 200 | 400 | kHz |

1.2.7 Voltage Regulator Characteristics

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD}$, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-----------------------------|-----------|--|------|------|------|------|
| Input voltage | V_{DD} | | 3.5 | | 5.5 | V |
| Output voltage | V_{RO} | | | 2.5 | | V |
| Lock time ^{Note 1} | t_{REG} | After V_{DD} reaches MIN.: 3.5 V Connect $C = 4.7 \mu\text{F} \pm 20\%$ to REGC pin | | | 1 | ms |

Note 1. The lock time does not have to be considered for devices that have POC.



1.2.8 DC Characteristics

(1) Input/Output level

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0\text{ V}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|---|-----------|---|---------------------------|-------------------|----------------|-------------|---|
| Input voltage, high | V_{IH1} | P30, P34, P38, P41, P98, P911 | $0.7EV_{DD}$ | | EV_{DD} | V | |
| | V_{IH2} | P00 to P06, P10, P11, P31 to P33, P35, P39, P40, P42, P50 to P55, P90 to P97, P99, P910, P912 to P915 | $0.8EV_{DD}$ | | EV_{DD} | V | |
| | V_{IH3} | PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL13 | $0.7BV_{DD}$ | | BV_{DD} | V | |
| | V_{IH4} | P70 to P715 | $0.7AV_{REF0}$ | | AV_{REF0} | V | |
| | V_{IH5} | RESET, FLMD0 | $0.8EV_{DD}$ | | EV_{DD} | V | |
| Input voltage, low | V_{IL1} | P30, P34, P38, P41, P98, P911 | EV_{SS} | | $0.3EV_{DD}$ | V | |
| | V_{IL2} | P00 to P06, P10, P11, P31 to P33, P35, P39, P40, P42, P50 to P55, P90 to P97, P99, P910, P912 to P915 | EV_{SS} | | $0.2EV_{DD}$ | V | |
| | V_{IL3} | PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL13 | BV_{SS} | | $0.3BV_{DD}$ | V | |
| | V_{IL4} | P70 to P715 | AV_{SS} | | $0.3AV_{REF0}$ | V | |
| | V_{IL5} | RESET, FLMD0 | EV_{SS} | | $0.2EV_{DD}$ | V | |
| Output voltage, high <small>Note 1</small> | V_{OH1} | P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P90 to P915 | $I_{OH} = -1.0\text{ mA}$ | $EV_{DD} - 1.0$ | | EV_{DD} | V |
| | | | $I_{OH} = -0.1\text{ mA}$ | $EV_{DD} - 0.5$ | | EV_{DD} | V |
| | V_{OH2} | PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL13 | $I_{OH} = -1.0\text{ mA}$ | $BV_{DD} - 1.0$ | | BV_{DD} | V |
| | | | $I_{OH} = -0.1\text{ mA}$ | $BV_{DD} - 0.5$ | | BV_{DD} | V |
| | V_{OH3} | P70 to P715 | $I_{OH} = -1.0\text{ mA}$ | $AV_{REF0} - 1.0$ | | AV_{REF0} | V |
| | | | $I_{OH} = -0.1\text{ mA}$ | $AV_{REF0} - 0.5$ | | AV_{REF0} | V |
| Output voltage, low <small>Note 1</small> | V_{OL1} | P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P90 to P915 | $I_{OL} = 1.0\text{ mA}$ | 0 | | 0.4 | V |
| | V_{OL2} | PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL13 | $I_{OL} = 1.0\text{ mA}$ | 0 | | 0.4 | V |
| | V_{OL3} | P70 to P715 | $I_{OL} = 1.0\text{ mA}$ | 0 | | 0.4 | V |
| Pull-up resistor | R_1 | $V_I = 0\text{ V}$ | 10 | 30 | 100 | $k\Omega$ | |
| Pull-down resistor <small>Note 2</small> | R_2 | $V_I = V_{DD}$ | 10 | 30 | 100 | $k\Omega$ | |

Notes 1. Total I_{OH}/I_{OL} (Max.) is 20 mA/-20 mA each power supply terminal (EV_{DD} , BV_{DD} and AV_{REF0}).

2. DRST pin only (OCDM0 is the control register).

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

(2) Pin leakage current

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0\text{ V}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|------------------------------|-------------------|-----------------------------------|------------------------------|------|------|------|----|
| Input leakage current, high | I _{LIH1} | V _{IN} = V _{DD} | Analog pins | | | +0.3 | μA |
| | | | Other pins ^{Note 1} | | | +2.0 | |
| Input leakage current, low | I _{LIL1} | V _{IN} = 0 V | Analog pins | | | -0.3 | μA |
| | | | Other pins ^{Note 1} | | | -2.0 | |
| Output leakage current, high | I _{LOH1} | V _O = V _{DD} | Analog pins | | | +0.3 | μA |
| | | | Other pins | | | +2.0 | |
| Output leakage current, low | I _{LOL1} | V _O = 0 V | Analog pins | | | -0.2 | μA |
| | | | Other pins | | | -2.0 | |

Note 1. For flash memory product, specification of FLMD0 is as follows:

Input leakage current, high: 4 μA

Input leakage current, low: -4 μA

(3) Supply current

Supply current (V850ES/FG2: μ PD70F3236, μ PD70F3235, μ PD70F3234)

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|--|------------------|---|--|------|------|------|---------|
| Flash memory products supply current ^{Note 1} | I _{DD1} | Normal operation | f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions operating | | 30 | 45 | mA |
| | | | f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions stopped | | 22 | | mA |
| | I _{DD2} | HALT mode | f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions operating | | 18 | 30 | mA |
| | | | f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions stopped | | 11 | | mA |
| | I _{DD3} | IDLE1 mode | f _{xx} = 5 MHz (OSC = 5 MHz), PLL off | | 0.6 | 1.2 | mA |
| | I _{DD4} | IDLE2 mode | f _{xx} = 5 MHz (OSC = 5 MHz), PLL off | | 0.25 | 0.9 | mA |
| | I _{DD5} | Subclock operation mode ^{Notes 2, 3} | RC resonator f _{XT} = 40 kHz ^{Note 4} | | 200 | 600 | μ A |
| | I _{DD6} | Sub-IDLE mode ^{Notes 2, 3} | RC resonator f _{XT} = 40 kHz ^{Note 4} | | 35 | 340 | μ A |
| | I _{DD7} | Stop mode ^{Notes 2, 5} | POC stopped, Ring-OSC stopped | | 7 | 250 | μ A |
| | | | POC operating, Ring-OSC stopped | | 10 | 255 | μ A |
| | | | POC stopped, Ring-OSC operating | | 15 | 265 | μ A |
| | | | POC operating, Ring-OSC operating | | 18 | 270 | μ A |

Notes 1. Total current of V_{DD}, EV_{DD}, and BV_{DD} (all ports stopped).

The current of AV_{REF0} and the port buffer current including the current flowing through the on-chip pull-up/pull-down resistors are not included.

2. When the main OSC is stopped.
3. POC operating, Ring-OSC operating.
4. The RC oscillation frequency is 40 kHz (TYP.). This clock is internally divided by 2.
5. When the sub-OSC is not used.

Supply current (V850ES/FG2: μ PD703235, μ PD703234)

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|------------------|--|---|------|------|---------|---------|
| Mask ROM products supply current ^{Note 1} | I _{DD1} | Normal operation | f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions operating | | 25 | 40 | mA |
| | | | f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions stopped | | 20 | | mA |
| | I _{DD2} | HALT mode | f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions operating | | 14 | 26 | mA |
| | | | f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions stopped | | 9 | | mA |
| | I _{DD3} | IDLE1 mode | f _{xx} = 5 MHz (OSC = 5 MHz), PLL off | | 0.25 | 0.9 | mA |
| | I _{DD4} | IDLE2 mode | f _{xx} = 5 MHz (OSC = 5 MHz), PLL off | | 0.2 | 0.9 | mA |
| | I _{DD5} | Subclock operation mode ^{Notes 2, 3} | RC resonator f _{XT} = 40 kHz ^{Note 4} | | 50 | 550 | μ A |
| | I _{DD6} | Sub-IDLE mode ^{Notes 2, 3} | RC resonator f _{XT} = 40 kHz ^{Note 4} | | 35 | 340 | μ A |
| | I _{DD7} | Stop mode ^{Notes 2, 5} | POC stopped, Ring-OSC stopped | | 7 | 250 | μ A |
| | | | POC operating, Ring-OSC stopped | | 10 | 255 | μ A |
| POC stopped, Ring-OSC operating | | | | 15 | 265 | μ A | |
| POC operating, Ring-OSC operating | | | | 18 | 270 | μ A | |

Notes 1. Total current of V_{DD}, EV_{DD}, and BV_{DD} (all ports stopped).

The current of AV_{REF0} and the port buffer current including the current flowing through the on-chip pull-up/pull-down resistors are not included.

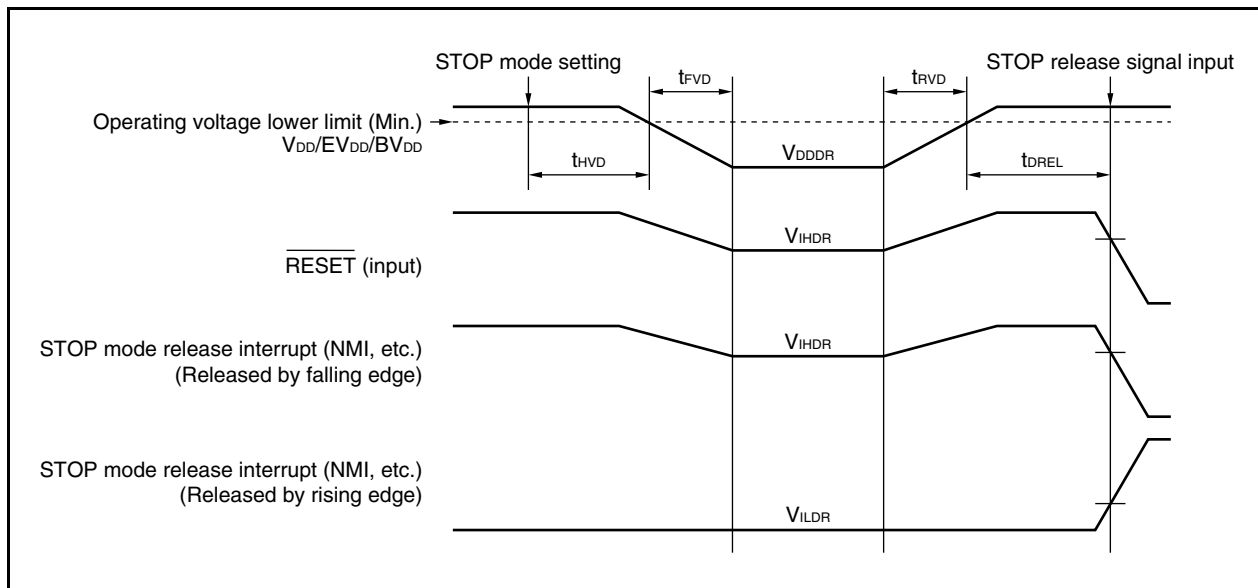
2. When the main OSC is stopped.
3. POC operating, Ring-OSC operating.
4. The RC oscillation frequency is 40 kHz(TYP.). This clock is internally divided by 2.
5. When the sub-OSC is not used.

1.2.9 Data Retention Characteristics

STOP Mode ($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 1.9$ V to 5.5 V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V)

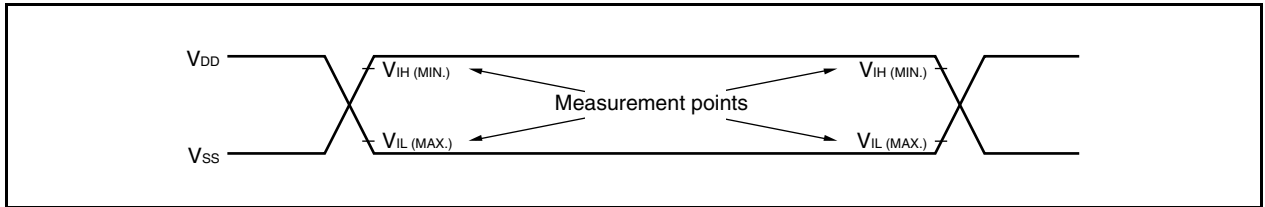
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|------------------------------------|------------|------------------------------------|---------------|------|---------------|---------------|
| Data retention voltage | V_{DDDR} | In STOP mode | 1.9 | | 5.5 | V |
| Data retention current | I_{DDDR} | $V_{DDDR} = 2.0$ V | | 10 | 230 | μA |
| Supply voltage rise time | t_{rVD} | | 1 | | | μs |
| Supply voltage fall time | t_{fVD} | | 1 | | | μs |
| Supply voltage retention time | t_{HVD} | After STOP mode release | 0 | | | ms |
| STOP release signal input time | t_{dREL} | After V_{DD} reaches MIN.: 3.5 V | 0 | | | μs |
| Data retention input voltage, high | V_{IHDR} | All input ports | $0.9V_{DDDR}$ | | V_{DDDR} | V |
| Data retention input voltage, low | V_{ILDR} | All input ports | 0 | | $0.1V_{DDDR}$ | V |

Caution Shifting to STOP mode and restoring from STOP mode must be performed within the rated operating range.

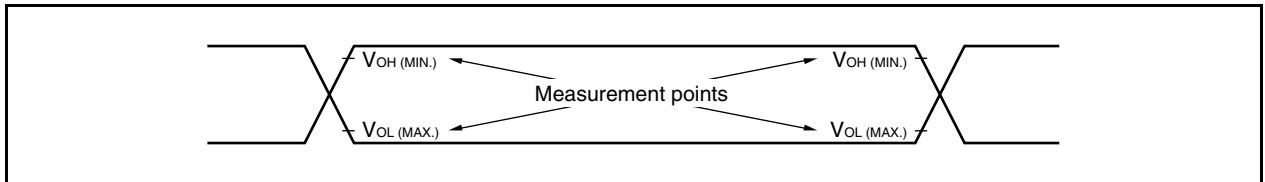


1.2.10 AC Characteristics

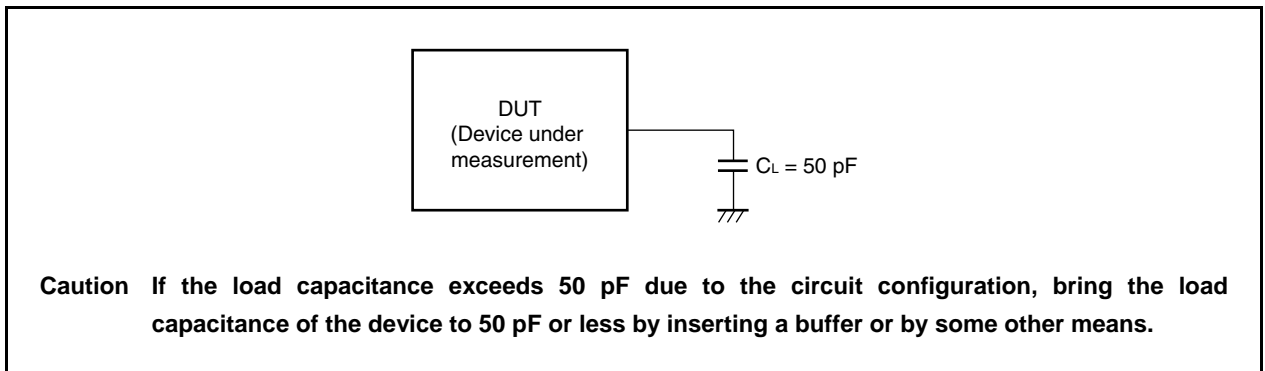
AC Test Input Measurement Points (V_{DD} , AV_{DD} , EV_{DD} , BV_{DD})



AC Test Output Measurement Points



Load Conditions

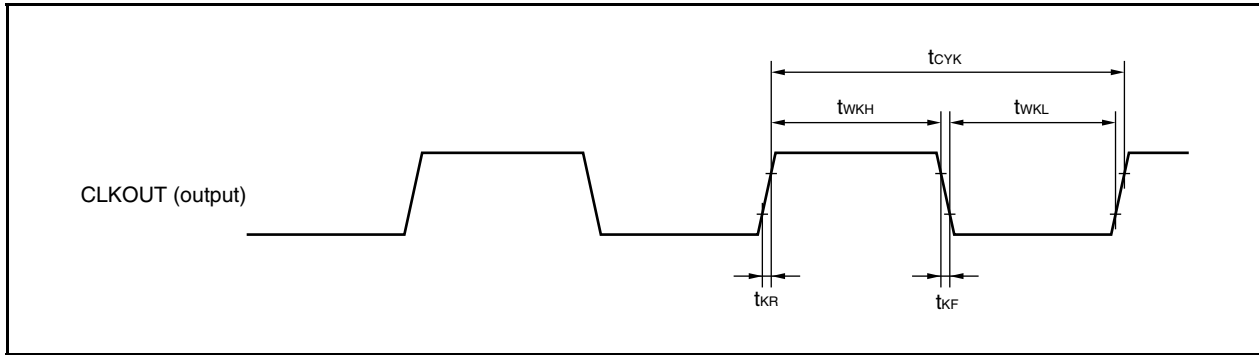


(1) CLKOUT output timing

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0\text{ V}$, $C_L = 50\text{ pF}$)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|------------------|-----------|------------|------------------|------------------|------|
| Output cycle | t_{CYK} | | 50 ns | 80 μs | |
| High-level width | t_{WKH} | | $t_{CYK}/2 - 15$ | | ns |
| Low-level width | t_{WKL} | | $t_{CYK}/2 - 15$ | | ns |
| Rise time | t_{KR} | | | 15 | ns |
| Fall time | t_{KF} | | | 15 | ns |

Clock Timing



(2) Basic Operation

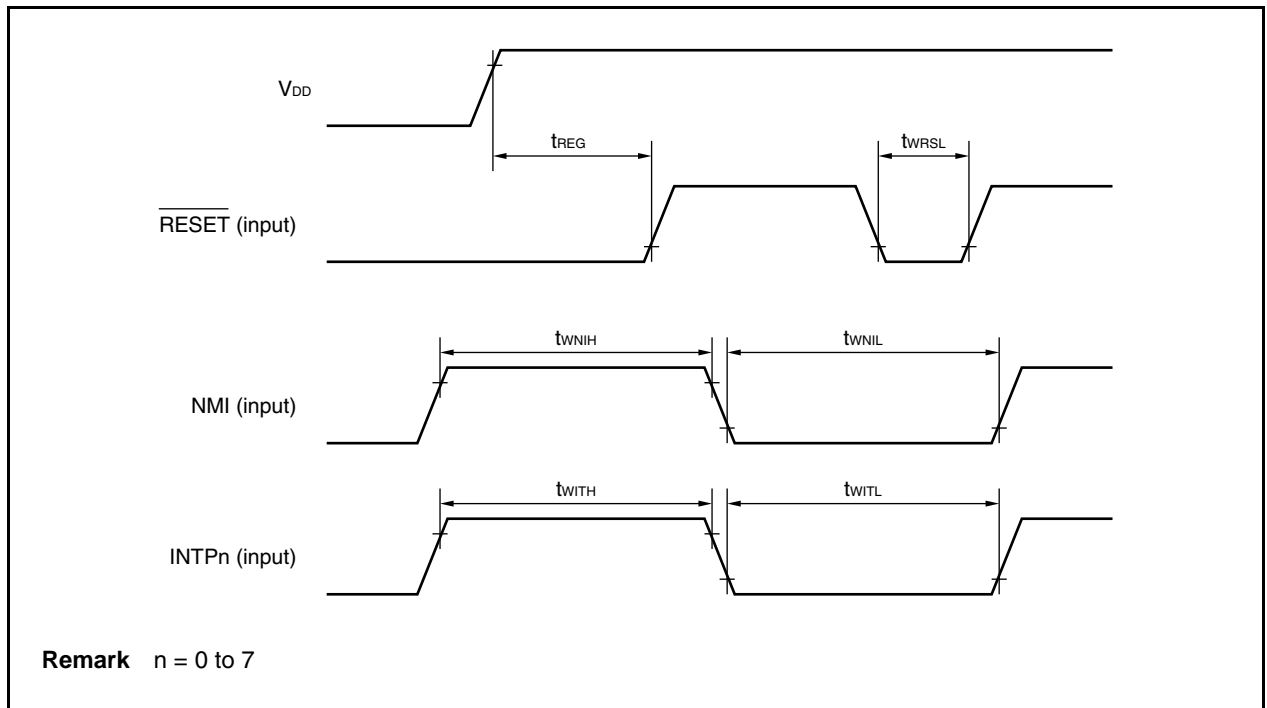
(a) Reset, Interrupt timing

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0\text{ V}$, $C_L = 50\text{ pF}$)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|--|------------|---------------------------------------|---------------|------|------|
| RESET low-level width | t_{WRSL} | | 500 | | ns |
| NMI high-level width | t_{WNIH} | Analog noise elimination | 500 | | ns |
| NMI low-level width | t_{WNIL} | Analog noise elimination | 500 | | ns |
| INTP _n ^{Note 1} high-level width | t_{WITH} | Analog noise elimination (n = 0 to 7) | 500 | | ns |
| | | Digital noise elimination (n = 3) | Note 2 | | ns |
| INTP _n ^{Note 1} low-level width | t_{WITL} | Analog noise elimination (n = 0 to 7) | 1 | | ns |
| | | Digital noise elimination (n = 3) | Note 2 | | ns |

- Notes**
- ADTRG is same spec (P03/INTP0/ADTRG). \overline{DRST} is same spec (P05/INTP2/ \overline{DRST}).
 - $2T_{\text{samp}} + 20$ or $3T_{\text{samp}} + 20$
 T_{samp} : Sampling clock for noise elimination

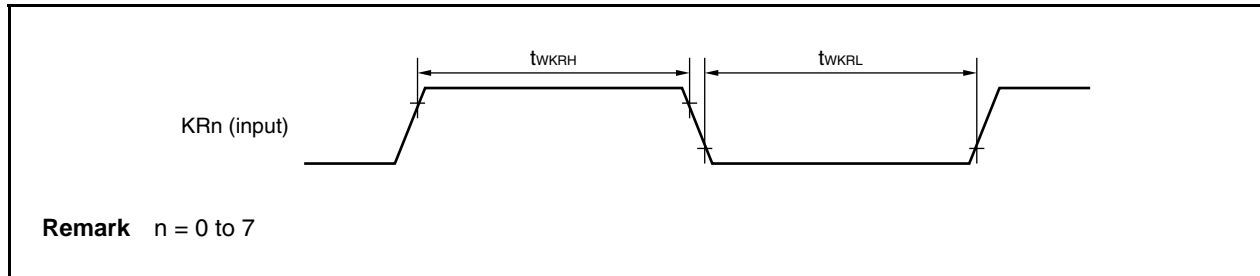
Reset/Interrupt



(b) Key return timing

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0\text{ V}$, $C_L = 50\text{ pF}$)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|----------------------------|------------|---|------|------|------|
| KRn input high-level width | t_{WKRH} | Analog noise elimination ($n = 0$ to 7) | 500 | | ns |
| KRn input low-level width | t_{WKRL} | | 500 | | ns |

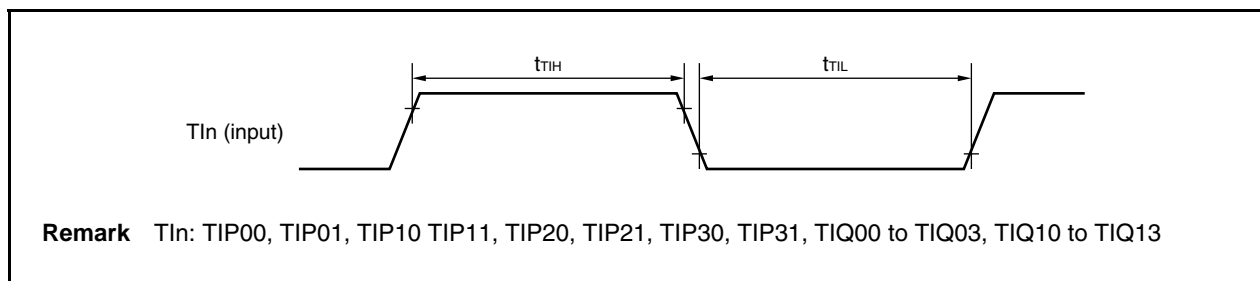


(c) Timer input timing

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0\text{ V}$, $C_L = 50\text{ pF}$)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|----------------------|-----------|---|-------------|------|------|
| TIn high-level width | t_{TIH} | TIP00, TIP01, TIP10, TIP11, TIP20, TIP21, TIP30, TIP31, | Note | | ns |
| TIn low-level width | t_{TIL} | TIQ00 to TIQ03, TIQ10 to TIQ13 | Note | | ns |

Note $2T_{\text{samp}} + 20$ or $3T_{\text{samp}} + 20$
 T_{samp} : Sampling clock for noise elimination



(d) CSIB timing

(i) Master mode

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|---|-------------|------------|-------------------|------|------|
| \overline{SCKBn} cycle time | t_{KCYn} | | 125 | | ns |
| \overline{SCKBn} high-level width | t_{KHn} | | $t_{KCYn}/2 - 15$ | | ns |
| \overline{SCKBn} low-level width | t_{KLn} | | $t_{KCYn}/2 - 15$ | | ns |
| SIBn setup time (to $\overline{SCKBn}\uparrow$) | t_{SIKn} | | 30 | | ns |
| SIBn hold time (from $\overline{SCKBn}\uparrow$) | t_{SIn} | | 25 | | ns |
| Output delay time from $\overline{SCKBn}\downarrow$ to SOBn | t_{KSOIn} | | | 25 | ns |

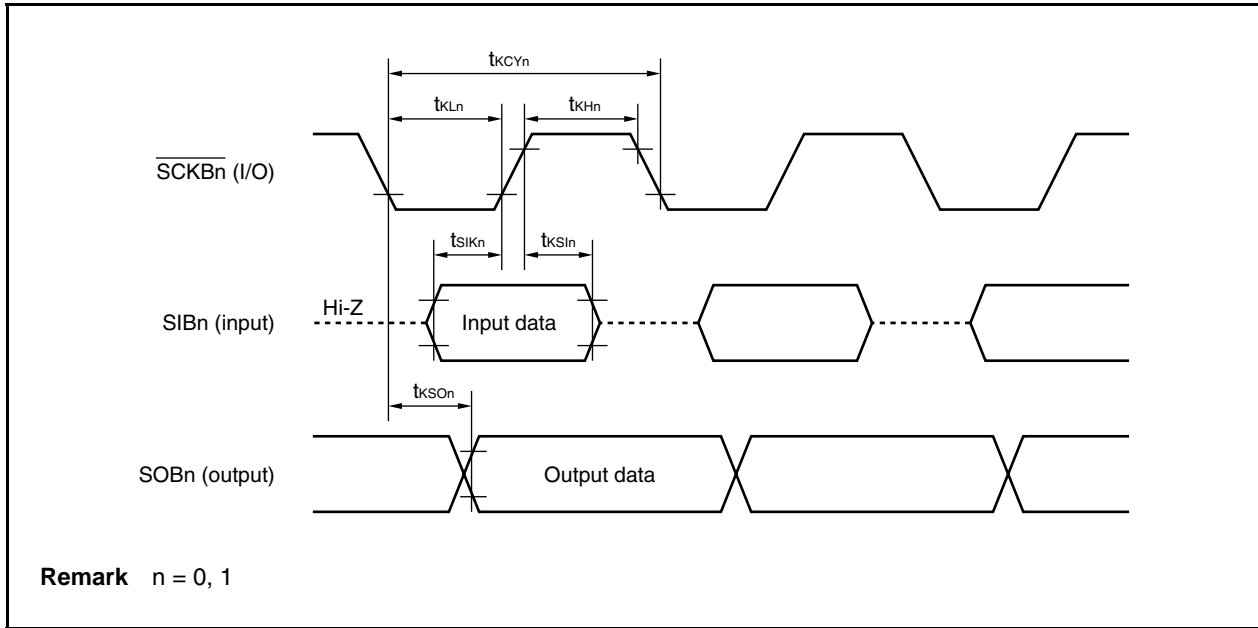
Remark n = 0, 1

(ii) Slave mode

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|---|-------------|------------|------|------|------|
| \overline{SCKBn} cycle time | t_{KCYn} | | 200 | | ns |
| \overline{SCKBn} high-level width | t_{KHn} | | 90 | | ns |
| \overline{SCKBn} low-level width | t_{KLn} | | 90 | | ns |
| SIBn setup time (to $\overline{SCKBn}\uparrow$) | t_{SIKn} | | 50 | | ns |
| SIBn hold time (from $\overline{SCKBn}\uparrow$) | t_{SIn} | | 50 | | ns |
| Output delay time from $\overline{SCKBn}\downarrow$ to SOBn | t_{KSOIn} | | | 50 | ns |

Remark n = 0, 1



(e) UART timing

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V \leq $AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

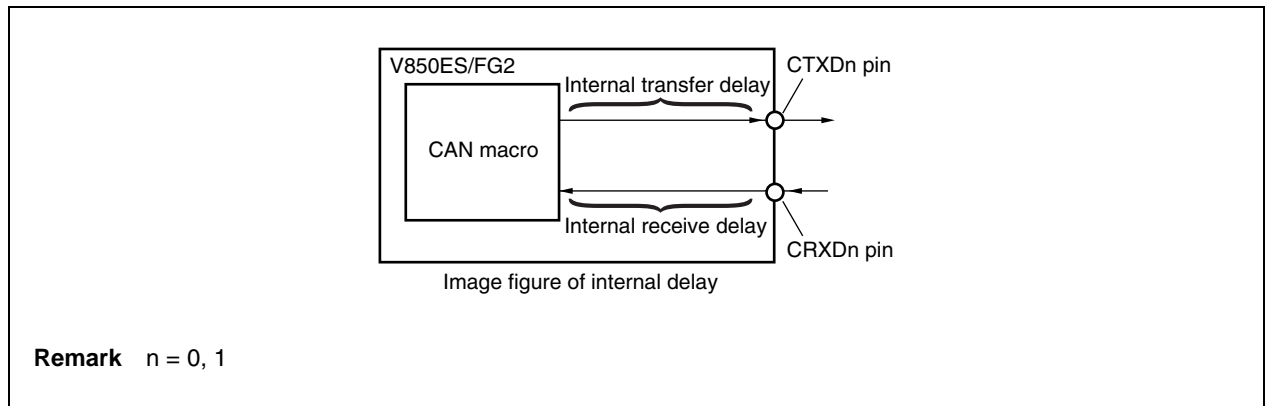
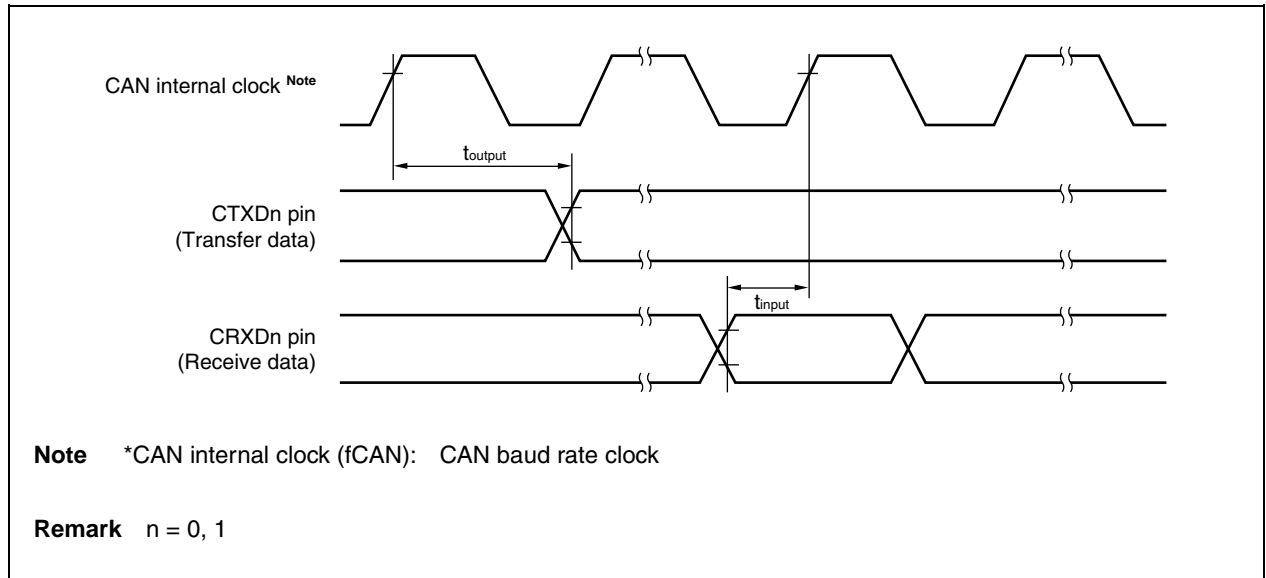
| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|--------------------|--------|------------|------|-------|------|
| Communication rate | | | | 312.5 | kbps |
| ASCK0 cycle time | | | | 10 | MHz |

(f) CAN timing

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0\text{ V}$, $C_L = 50\text{ pF}$)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|-------------------------------------|--------|------------|------|------|------|
| Transfer rate | | | | 1 | Mbps |
| Internal delay time ^{Note} | | | | 100 | ns |

Note Internal delay time (t_{NODE}) = Internal transfer delay time (t_{OUTPUT}) + Internal receive delay time (t_{INPUT})



(g) A/D converter

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------------------|-------------|---------------------------------|-----------|------------|-------------|---------------|
| Resolution | | | | | 10 | bit |
| Overall error ^{Note} | | $4.0 \leq AV_{REF0} \leq 5.5$ V | | ± 0.15 | ± 0.3 | %FSR |
| Conversion time | t_{CONV} | | 3.1 | | 16 | μs |
| Analog input voltage | V_{IAN} | | AV_{SS} | | AV_{REF0} | V |
| AV_{REF0} current | I_{AREF0} | When using A/D converter | | 5 | 10 | mA |
| | | When not using A/D converter | | 1 | 10 | μA |

Note Excluding quantization error ($\pm 0.05\%$ FSR). Indicates the ratio to the full-scale value (%FSR).

Remark FSR: Full Scale Range

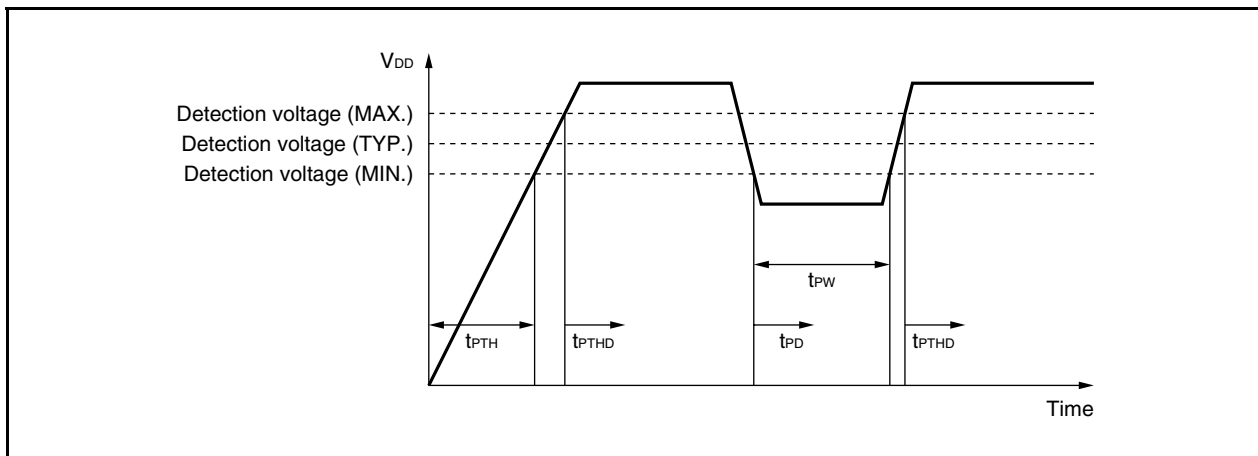
(h) POC circuit characteristics

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|------------|---|-------|------|------|------|
| Detection voltage | V_{POCO} | | 3.5 | 3.7 | 3.9 | V |
| Power supply startup time | t_{PTH} | $V_{DD} = 0$ V \rightarrow 3.5 V | 0.002 | | | ms |
| Response delay time 1 ^{Note 1} | t_{PTHD} | In case of power on. After V_{DD} reaches 3.9 V. | | | 3.0 | ms |
| Response delay time 2 ^{Note 2} | t_{PD} | In case of power off. After V_{DD} drops 3.5 V. | | | 1 | ms |
| Minimum V_{DD} width | t_{PW} | | 0.2 | | | ms |

Notes 1. From detect voltage to release reset signal.

2. From detect voltage to output reset signal.



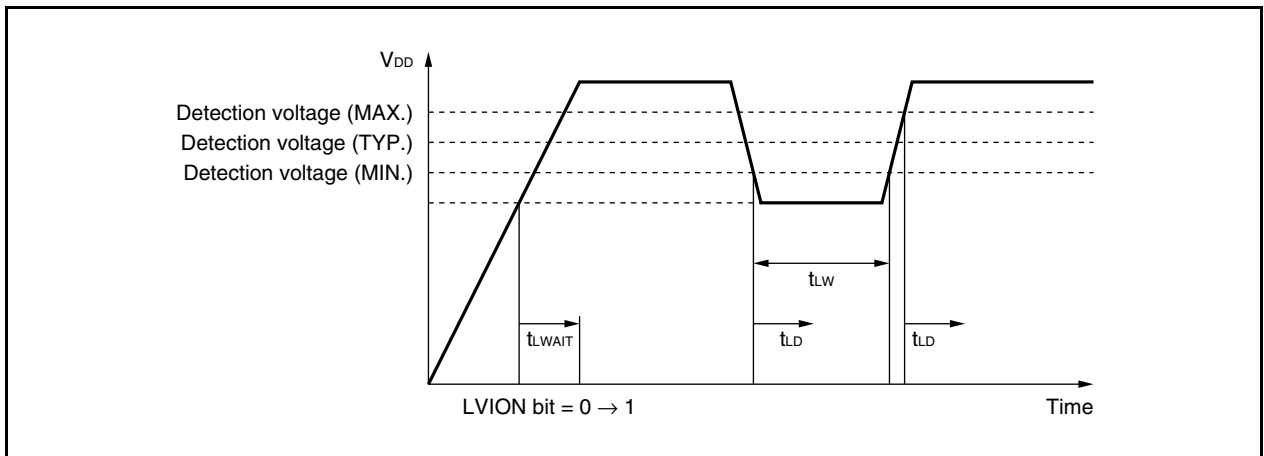
(i) LVI circuit characteristics

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0\text{ V}$, $C_L = 50\text{ pF}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|-------------|--|------|------|------|------|
| Detection voltage | V_{LV10} | | 4.2 | 4.4 | 4.6 | V |
| | V_{LV11} | | 4.0 | 4.2 | 4.4 | V |
| Response time ^{Note 1} | t_{LD} | After V_{DD} reaches V_{LV10}/V_{LV11} (Max.). After V_{DD} drops V_{LV10}/V_{LV11} (Min.). | | 0.2 | 2.0 | ms |
| Minimum V_{DD} width | t_{LW} | | 0.2 | | | ms |
| Reference voltage stabilization wait time ^{Note 2} | t_{LWAIT} | After V_{DD} reaches 3.5 V. After LVION bit (LVIM.bit7) = 0 → 1 | | 0.1 | 0.2 | ms |

Notes 1. The time required to output an interrupt/reset after the detection voltage is detected.

2. Unnecessary when the POC function is used.

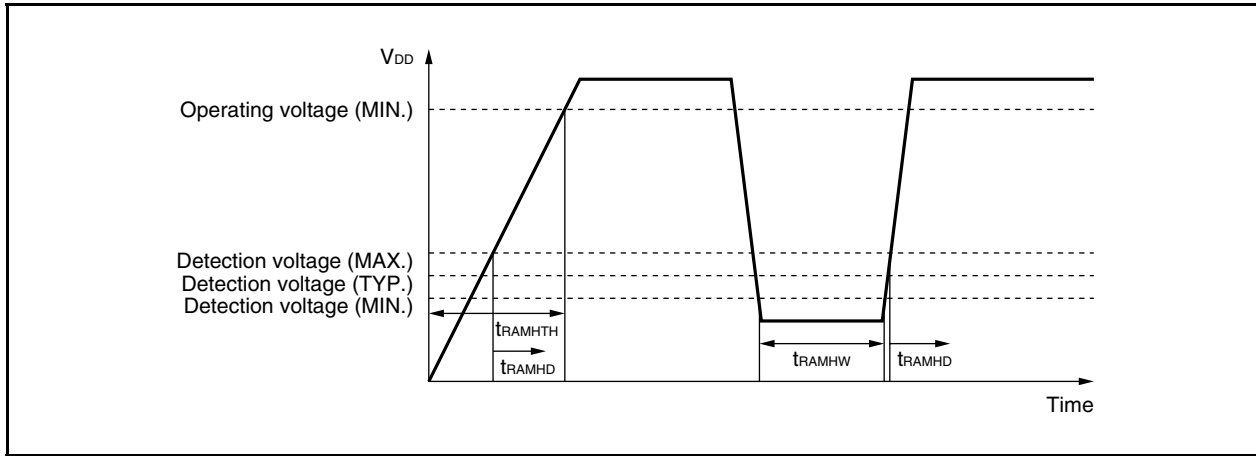


(j) RAM retention flag characteristics

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 1.9$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------------------|--------------|---|-------|------|-------|------|
| Detection voltage | V_{RAMH} | | 1.9 | 2.0 | 2.1 | V |
| Supply voltage rise time | t_{RAMHTH} | $V_{DD} = 0$ V \rightarrow 3.5 V | 0.002 | | 1,800 | ms |
| Response time ^{Note} | t_{RAMHD} | After the supply voltage reaches the detection voltage (MAX.) | | 0.2 | 2.0 | ms |
| Minimum V_{DD} width | t_{RAMHW} | | 0.2 | | | ms |

Note Time required to set the RAMF bit after the detection voltage is detected.



(k) Flash memory programming characteristics

(i) Basic characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------------|----------------------------|---|--------------|------|--------------|------------------|
| Operating frequency | f_{CPU} | | 4 | | 20 | MHz |
| Supply voltage | V_{DD} | | 3.5 | | 5.5 | V |
| Number of writes | C_{WRT} ^{Note} | | | | 100 | Times |
| Input voltage, high | V_{IH} | FLMD0 | $0.8EV_{DD}$ | | EV_{DD} | V |
| Input voltage, low | V_{IL} | FLMD0 | EV_{SS} | | $0.2EV_{DD}$ | V |
| Write time + erase time | t_{WRT} + t_{ERASE} | Flash: 256 KB (μ PD70F3235) 384 KB (μ PD70F3236) | | | T.B.D | s |
| Programming temperature | t_{PRG} | | -40 | | +85 | $^\circ\text{C}$ |

Note The initial write when the product is shipped, any erase → write set of operations, or any programming operation is counted as one rewrite.

Example: P: Write, E: Erase

Shipped product → P → E → P → E → P: 3 rewrites

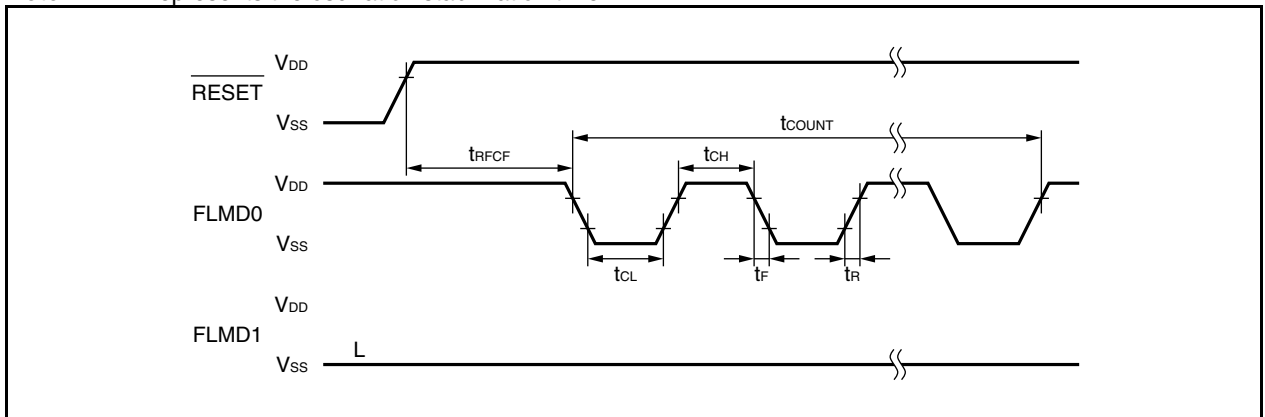
Shipped product → E → P → E → P → E → P: 3 rewrites

(ii) Serial Write Operation Characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|-------------|------------|---------------------|------|------|---------------|
| FLMD0 setup time from $\overline{\text{RESET}}\uparrow$ | t_{RFCF} | | $5000/f_x + \alpha$ | | | s |
| Count execution time | t_{COUNT} | | | | 3 | ms |
| FLMD0 high-level width | t_{CH} | | 10 | | 100 | μs |
| FLMD0 low-level width | t_{CL} | | 10 | | 100 | μs |
| FLMD rise time | t_R | | | | 50 | ns |
| FLMD fall time | t_F | | | | 50 | ns |

Note “ ” represents the oscillation stabilization time.



1.3 Electrical Specifications of (A2)-Grade

1.3.1 Absolute maximum ratings

Absolute Maximum Ratings (T_A = 25°C): Flash memory products (1/2)

| Parameter | Symbol | Conditions | Ratings | Unit |
|----------------------|--------------------|---|--|------|
| Supply voltage | V _{DD} | V _{DD} = EV _{DD} = BV _{DD} | -0.5 to +6.5 | V |
| | BV _{DD} | V _{DD} = EV _{DD} = BV _{DD} | -0.5 to +6.5 | V |
| | EV _{DD} | V _{DD} = EV _{DD} = BV _{DD} | -0.5 to +6.5 | V |
| | AV _{REF0} | | -0.5 to +6.5 | V |
| | V _{SS} | V _{SS} = EV _{SS} = BV _{SS} = AV _{SS} | -0.5 to +0.5 | V |
| | AV _{SS} | V _{SS} = EV _{SS} = BV _{SS} = AV _{SS} | -0.5 to +0.5 | V |
| | BV _{SS} | V _{SS} = EV _{SS} = BV _{SS} = AV _{SS} | -0.5 to +0.5 | V |
| | EV _{SS} | V _{SS} = EV _{SS} = BV _{SS} = AV _{SS} | -0.5 to +0.5 | V |
| Input voltage | V _{I1} | P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P90 to P915, RESET, FLMD0 | -0.5 to EV _{DD} + 0.5 ^{Note} | V |
| | V _{I2} | PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL13 | -0.5 to BV _{DD} + 0.5 ^{Note} | V |
| | V _{I3} | X1, X2, XT1, XT2 | -0.5 to V _{RO} + 0.5 ^{Note} | V |
| Analog input voltage | V _{IAN} | P70 to P715 | -0.5 to AV _{REF0} + 0.5 ^{Note} | V |

Note Be sure not to exceed the absolute maximum ratings (MAX. value) of each supply voltage.

Cautions 1. Avoid direct connections among the IC device output (or I/O) pins and between V_{DD} or V_{CC} and GND.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Absolute maximum ratings (T_A = 25°C): Flash memory products (2/2)

| Parameter | Symbol | Conditions | Ratings | Unit | |
|-------------------------------|------------------|--|-------------------|----------------------|----|
| Output current, low | I _{OL} | P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P90 to P915 | Per pin | 4 | mA |
| | | | Total of all pins | 50 ^{Note1} | mA |
| | | P70 to P715 | Per pin | 4 | mA |
| | | | Total of all pins | 20 ^{Note2} | mA |
| | | PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL13 | Per pin | 4 | mA |
| | | | Total of all pins | 50 ^{Note1} | mA |
| Output current, high | I _{OH} | P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P90 to P915 | Per pin | -4 | mA |
| | | | Total of all pins | -50 ^{Note1} | mA |
| | | P70 to P715 | Per pin | -4 | mA |
| | | | Total of all pins | -20 ^{Note2} | mA |
| | | PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL13 | Per pin | -4 | mA |
| | | | Total of all pins | -50 ^{Note1} | mA |
| Operating ambient temperature | T _A | Normal operating mode | -40 to +125 | °C | |
| | | Flash programming mode | -40 to +85 | °C | |
| Storage temperature | T _{stg} | | -40 to +125 | °C | |

- Notes**
1. This value is a value at the time of T_A = 25 °C. At the time of T_A = 125 °C, This value is 20 mA/-20 mA.
 2. This value is a value at the time of T_A = 25 °C. At the time of T_A = 125 °C, This value is 10 mA/-10 mA.

- Cautions**
1. Avoid direct connections among the IC device output (or I/O) pins and between V_{DD} or V_{CC} and GND.
 2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Absolute Maximum Ratings (T_A = 25°C): Mask ROM products (1/2)

| Parameter | Symbol | Conditions | Ratings | Unit |
|----------------------|--------------------|---|--|------|
| Supply voltage | V _{DD} | V _{DD} = EV _{DD} = BV _{DD} | -0.5 to +6.5 | V |
| | BV _{DD} | V _{DD} = EV _{DD} = BV _{DD} | -0.5 to +6.5 | V |
| | EV _{DD} | V _{DD} = EV _{DD} = BV _{DD} | -0.5 to +6.5 | V |
| | AV _{REF0} | | -0.5 to +6.5 | V |
| | V _{SS} | V _{SS} = EV _{SS} = BV _{SS} = AV _{SS} | -0.5 to +0.5 | V |
| | AV _{SS} | V _{SS} = EV _{SS} = BV _{SS} = AV _{SS} | -0.5 to +0.5 | V |
| | BV _{SS} | V _{SS} = EV _{SS} = BV _{SS} = AV _{SS} | -0.5 to +0.5 | V |
| | EV _{SS} | V _{SS} = EV _{SS} = BV _{SS} = AV _{SS} | -0.5 to +0.5 | V |
| Input voltage | V _{I1} | P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P90 to P915, $\overline{\text{RESET}}$, IC | -0.5 to EV _{DD} + 0.5 ^{Note} | V |
| | V _{I2} | PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL13 | -0.5 to BV _{DD} + 0.5 ^{Note} | V |
| | V _{I3} | X1, X2, XT1, XT2 | -0.5 to V _{RO} + 0.5 ^{Note} | V |
| Analog input voltage | V _{IAN} | P70 to P715 | -0.5 to AV _{REF0} + 0.5 ^{Note} | V |

Note Be sure not to exceed the absolute maximum ratings (MAX. value) of each supply voltage.

Cautions 1. Avoid direct connections among the IC device output (or I/O) pins and between V_{DD} or V_{CC} and GND.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Absolute maximum ratings (T_A = 25°C): Mask ROM products (2/2)

| Parameter | Symbol | Conditions | Ratings | Unit | |
|-------------------------------|------------------|--|-------------------|----------------------|----|
| Output current, low | I _{OL} | P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P90 to P915 | Per pin | 4 | mA |
| | | | Total of all pins | 50 ^{Note1} | mA |
| | | P70 to P715 | Per pin | 4 | mA |
| | | | Total of all pins | 20 ^{Note2} | mA |
| | | PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL13 | Per pin | 4 | mA |
| | | | Total of all pins | 50 ^{Note1} | mA |
| Output current, high | I _{OH} | P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P90 to P915 | Per pin | -4 | mA |
| | | | Total of all pins | -50 ^{Note1} | mA |
| | | P70 to P715 | Per pin | -4 | mA |
| | | | Total of all pins | -20 ^{Note2} | mA |
| | | PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL13 | Per pin | -4 | mA |
| | | | Total of all pins | -50 ^{Note1} | mA |
| Operating ambient temperature | T _A | | -40 to +125 | °C | |
| Storage temperature | T _{stg} | | -65 to +150 | °C | |

Notes 1. This value is a value at the time of T_A = 25 °C. At the time of T_A = 125 °C, This value is 20 mA/-20 mA.

2. This value is a value at the time of T_A = 25 °C. At the time of T_A = 125 °C, This value is 10 mA/-10 mA.

Cautions 1. Avoid direct connections among the IC device output (or I/O) pins and between V_{DD} or V_{CC} and GND.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

1.3.2 Capacitance

($T_A = 25^\circ\text{C}$, $V_{DD} = EV_{DD} = AV_{REF0} = BV_{DD} = AV_{REF1} = V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0\text{ V}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-----------------|----------|--|------|------|------|------|
| I/O capacitance | C_{IO} | $f_x = 1\text{ MHz}$, Unmeasured pins returned to 0 V. | | | 10 | pF |

1.3.3 Operating conditions

($T_A = -40\text{ to }+125^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0\text{ V}$)

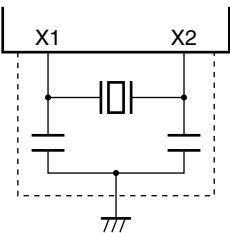
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---------------------------------|-----------|--|----------------------|------|----------------------|------|
| Internal system clock frequency | f_{CLK} | REGC Capacity = $4.7\ \mu\text{F}$, at operation with main clock | 4 | | 20 | MHz |
| | | REGC Capacity = $4.7\ \mu\text{F}$, at operation with subclock (RC resonator) | 12.5 ^{Note} | | 27.5 ^{Note} | kHz |

Note The internal system clock frequency is half the oscillation frequency.

1.3.4 Oscillator Characteristics

Main clock oscillator characteristics

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V)

| Resonator | Recommended Circuit | Parameter | Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------|---|--|--------------------------|-----------------------|---------------|------|---------------|
| Ceramic resonator |  | Oscillation frequency (fx) ^{Note 1} | | 4 | | 5 | MHz |
| | | Oscillation stabilization time ^{Note 2} | After reset release | | $2^{16}/f_x$ | | s |
| | | | After STOP mode release | 0.5 ^{Note 3} | Note 4 | | ms |
| Crystal resonator | | Oscillation frequency (fx) ^{Note 1} | | 4 | | 5 | MHz |
| | | Oscillation stabilization time ^{Note 2} | After reset release | | $2^{16}/f_x$ | | s |
| | | | After STOP mode release | 0.5 ^{Note 3} | Note 4 | | ms |
| | | | After IDLE2 mode release | 350 | Note 4 | | μs |

- Notes**
1. Indicates only oscillator characteristics.
 2. Time required to stabilize the crystal resonator after reset or STOP mode is released.
 3. Time required to stabilize access to the internal flash memory.
 4. The value differs depending on the OSTS register settings.

Cautions 1. When using the main clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
 - Do not cross the wiring with the other signal lines.
 - Do not route the wiring near a signal line through which a high fluctuating current flows.
 - Always make the ground point of the oscillator capacitor the same potential as V_{SS}.
 - Do not ground the capacitor to a ground pattern through which a high current flows.
 - Do not fetch signals from the oscillator.
2. When the main clock is stopped and the device is operating on the subclock, wait until the oscillation stabilization time has been secured by the program before switching back to the main clock.

Subclock Oscillator Characteristics

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V)

| Resonator | Recommended Circuit | Parameter | Conditions | MIN. | TYP. | MAX. | Unit |
|--------------|---------------------|---|---|------|------|------|---------------|
| RC resonator | | Oscillation frequency (f_{XT}) <small>Notes 1, 4</small> | $R = 390\text{ k}\Omega \pm 5\%$ <small>Note 3</small> $C = 47\text{ pF} \pm 10\%$ <small>Note 3</small> | 25 | 40 | 55 | kHz |
| | | Oscillation stabilization time <small>Note 2</small> | | | | 100 | μs |

- Notes**
1. Indicates only oscillator characteristics. Refer to **27. 3. 10 AC Characteristics** for CPU operating clock.
 2. Time required from when V_{DD} reaches oscillation voltage range (MIN.: 3.5 V) to when the crystal resonator stabilizes.
 3. In order to avoid the influence of wiring capacity, shorten wiring as much as possible.
 4. RC oscillation frequency is 40 kHz (Typ.). This clock is divided (1/2) internally. In case of RC oscillator, internal system clock frequency (f_{XT}) is 12.5 kHz (Min.), 20 kHz (Typ.), and 27.5 kHz (Max.).

Cautions 1. When using the subclock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
 - Do not cross the wiring with the other signal lines.
 - Do not route the wiring near a signal line through which a high fluctuating current flows.
 - Always make the ground point of the oscillator capacitor the same potential as V_{SS} .
 - Do not ground the capacitor to a ground pattern through which a high current flows.
 - Do not fetch signals from the oscillator.
2. The subclock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main clock oscillator. Particular care is therefore required with the wiring method when the subclock is used.

1.3.5 PLL Characteristics

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|------------------|-----------|------------------------------------|------|------|------|---------------|
| Input frequency | f_x | | 4 | | 5 | MHz |
| Output frequency | f_{xx} | | 16 | | 20 | MHz |
| Clock time | t_{PLL} | After V_{DD} reaches MIN.: 3.5 V | | | 800 | μs |

1.3.6 Ring-OSC Characteristics

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V)

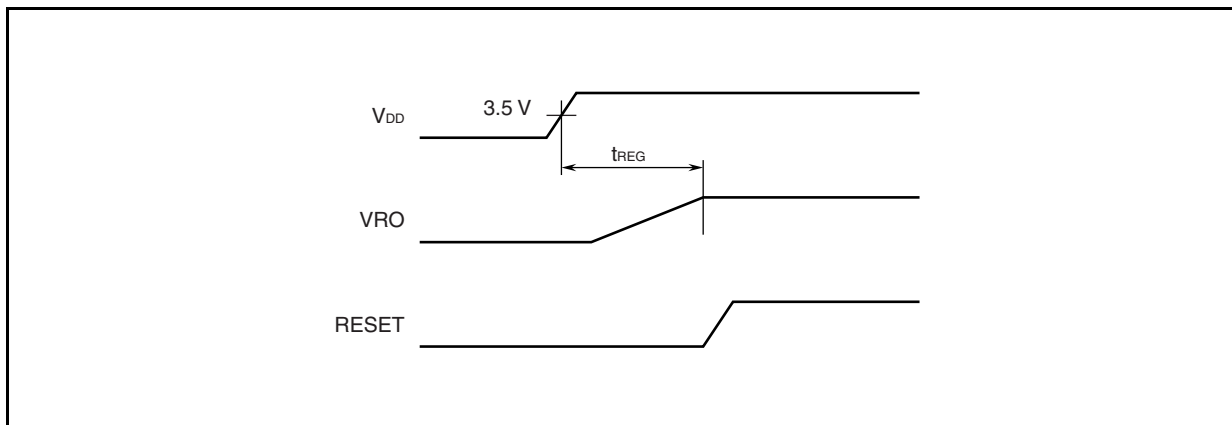
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|------------------|--------|------------|------|------|------|------|
| Output frequency | f_r | | 100 | 200 | 400 | kHz |

1.3.7 Voltage Regulator Characteristics

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD}$, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-----------------------------|-----------|--|------|------|------|------|
| Input voltage | V_{DD} | | 3.5 | | 5.5 | V |
| Output voltage | V_{RO} | | | 2.5 | | V |
| Lock time ^{Note 1} | t_{REG} | After V_{DD} reaches MIN.: 3.5 V Connect C = 4.7 mF \pm 20% to REGC pin | | | 1 | ms |

Note 1. The lock time does not have to be considered for devices that have POC.



1.3.8 DC Characteristics

(1) Input/Output level

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|---|-----------|---|--------------------|-------------------|----------------|-------------|---|
| Input voltage, high | V_{IH1} | P30, P34, P38, P41, P98, P911 | $0.7EV_{DD}$ | | EV_{DD} | V | |
| | V_{IH2} | P00 to P06, P10, P11, P31 to P33, P35, P39, P40, P42, P50 to P55, P90 to P97, P99, P910, P912 to P915 | $0.8EV_{DD}$ | | EV_{DD} | V | |
| | V_{IH3} | PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL13 | $0.7BV_{DD}$ | | BV_{DD} | V | |
| | V_{IH4} | P70 to P715 | $0.7AV_{REF0}$ | | AV_{REF0} | V | |
| | V_{IH5} | RESET, FLMD0 | $0.8EV_{DD}$ | | EV_{DD} | V | |
| Input voltage, low | V_{IL1} | P30, P34, P38, P41, P98, P911 | EV_{SS} | | $0.3EV_{DD}$ | V | |
| | V_{IL2} | P00 to P06, P10, P11, P31 to P33, P35, P39, P40, P42, P50 to P55, P90 to P97, P99, P910, P912 to P915 | EV_{SS} | | $0.2EV_{DD}$ | V | |
| | V_{IL3} | PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL13 | BV_{SS} | | $0.3BV_{DD}$ | V | |
| | V_{IL4} | P70 to P715 | AV_{SS} | | $0.3AV_{REF0}$ | V | |
| | V_{IL5} | RESET, FLMD0 | EV_{SS} | | $0.2EV_{DD}$ | V | |
| Output voltage, high <small>Note 1</small> | V_{OH1} | P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P90 to P915 | $I_{OH} = -1.0$ mA | $EV_{DD} - 1.0$ | | EV_{DD} | V |
| | | | $I_{OH} = -0.1$ mA | $EV_{DD} - 0.5$ | | EV_{DD} | V |
| | V_{OH2} | PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL13 | $I_{OH} = -1.0$ mA | $BV_{DD} - 1.0$ | | BV_{DD} | V |
| | | | $I_{OH} = -0.1$ mA | $BV_{DD} - 0.5$ | | BV_{DD} | V |
| | V_{OH3} | P70 to P715 | $I_{OH} = -1.0$ mA | $AV_{REF0} - 1.0$ | | AV_{REF0} | V |
| | | | $I_{OH} = -0.1$ mA | $AV_{REF0} - 0.5$ | | AV_{REF0} | V |
| Output voltage, low <small>Note 1</small> | V_{OL1} | P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P90 to P915 | $I_{OL} = 1.0$ mA | 0 | | 0.4 | V |
| | V_{OL2} | PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL13 | $I_{OL} = 1.0$ mA | 0 | | 0.4 | V |
| | V_{OL3} | P70 to P715 | $I_{OL} = 1.0$ mA | 0 | | 0.4 | V |
| Pull-up resistor | R_1 | $V_I = 0$ V | 10 | 30 | 100 | k Ω | |
| Pull-down resistor <small>Note 2</small> | R_2 | $V_I = V_{DD}$ | 10 | 30 | 100 | k Ω | |

- Notes 1.** Total I_{OH}/I_{OL} (Max.) of EV_{DD} is 20 mA/-20 mA.
 Total I_{OH}/I_{OL} (Max.) of AV_{REF0} is 10 mA/-10 mA.
2. DRST pin only (OCDM0 is the control register).

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

(2) Pin leakage current

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|------------------------------|-------------------|-----------------------------------|-------------|------|------|------|---------------|
| Input leakage current, high | I _{LIH1} | V _{IN} = V _{DD} | Analog pins | | | +1.0 | μA |
| | | | Other pins | | | +5.0 | |
| Input leakage current, low | I _{LIL1} | V _{IN} = 0 V | Analog pins | | | -1.0 | μA |
| | | | Other pins | | | -5.0 | |
| Output leakage current, high | I _{LOH1} | V _O = V _{DD} | Analog pins | | | +1.0 | μA |
| | | | Other pins | | | +5.0 | |
| Output leakage current, low | I _{LOL1} | V _O = 0 V | Analog pins | | | -1.0 | μA |
| | | | Other pins | | | -5.0 | |

(3) Supply current

Supply current (V850ES/FG: μ PD70F3236, μ PD70F3235, μ PD70F3234)

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|--|------------------|---|---|------|------|------|---------|
| Flash memory products supply current ^{Note 1} | I _{DD1} | Normal operation, | f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions operating | | 30 | 45 | mA |
| | | | f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions stopped | | 22 | | mA |
| | I _{DD2} | HALT mode | f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions operating | | 18 | 30 | mA |
| | | | f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions stopped | | 11 | | mA |
| | I _{DD3} | IDLE1 mode | f _{xx} = 5 MHz (OSC = 5 MHz), PLL off | | 0.6 | 1.5 | mA |
| | I _{DD4} | IDLE2 mode | f _{xx} = 5 MHz (OSC = 5 MHz), PLL off | | 0.25 | 1.15 | mA |
| | I _{DD5} | Subclock operation mode ^{Notes 2, 3} | RC resonator f _{XT} = 40 kHz ^{Note 4} | | 200 | 850 | μ A |
| | I _{DD6} | Sub-IDLE mode ^{Notes 2, 3} | RC resonator f _{XT} = 40 kHz ^{Note 4} | | 35 | 590 | μ A |
| | I _{DD7} | Stop mode ^{Notes 2, 5} | POC stopped, Ring-OSC stopped | | 7 | 500 | μ A |
| | | | POC operating, Ring-OSC stopped | | 10 | 505 | μ A |
| | | | POC stopped, Ring-OSC operating | | 15 | 515 | μ A |
| | | | POC operating, Ring-OSC operating | | 18 | 520 | μ A |

Notes 1. Total current of V_{DD}, EV_{DD}, and BV_{DD} (all ports stopped).

The current of AV_{REF0} and the port buffer current including the current flowing through the on-chip pull-up/pull-down resistors are not included.

2. When the main OSC is stopped.
3. POC operating, Ring-OSC operating.
4. The RC oscillation frequency is 40 kHz(TYP.). This clock is internally divided by 2.
5. When the sub-OSC is not used.

Supply current (V850ES/FG2: μ PD703235, μ PD703234)

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|---|------------------|--|---|------|------|---------|---------|
| Mask ROM products supply current ^{Note 1} | I _{DD1} | Normal operation, f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions operating | | 25 | 40 | mA | |
| | | | | 20 | | mA | |
| | I _{DD2} | HALT mode | f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions operating | | 14 | 26 | mA |
| | | | f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions stopped | | 9 | | mA |
| | I _{DD3} | IDLE1 mode | f _{xx} = 5 MHz (OSC = 5 MHz), PLL off | | 0.25 | 1.15 | mA |
| | I _{DD4} | IDLE2 mode | f _{xx} = 5 MHz (OSC = 5 MHz), PLL off | | 0.2 | 1.15 | mA |
| | I _{DD5} | Subclock operation mode ^{Notes 2, 3} | RC resonator f _{XT} = 40 kHz ^{Note 4} | | 50 | 800 | μ A |
| | I _{DD6} | Sub-IDLE mode ^{Notes 2, 3} | RC resonator f _{XT} = 40 kHz ^{Note 4} | | 35 | 590 | μ A |
| | I _{DD7} | Stop mode ^{Notes 2, 5} | POC stopped, Ring-OSC stopped | | 7 | 500 | μ A |
| | | | POC operating, Ring-OSC stopped | | 10 | 505 | μ A |
| POC stopped, Ring-OSC operating | | | | 15 | 515 | μ A | |
| POC operating, Ring-OSC operating | | | | 18 | 520 | μ A | |

Notes 1. Total current of V_{DD}, EV_{DD}, and BV_{DD} (all ports stopped).

The current of AV_{REF0} and the port buffer current including the current flowing through the on-chip pull-up/pull-down resistors are not included.

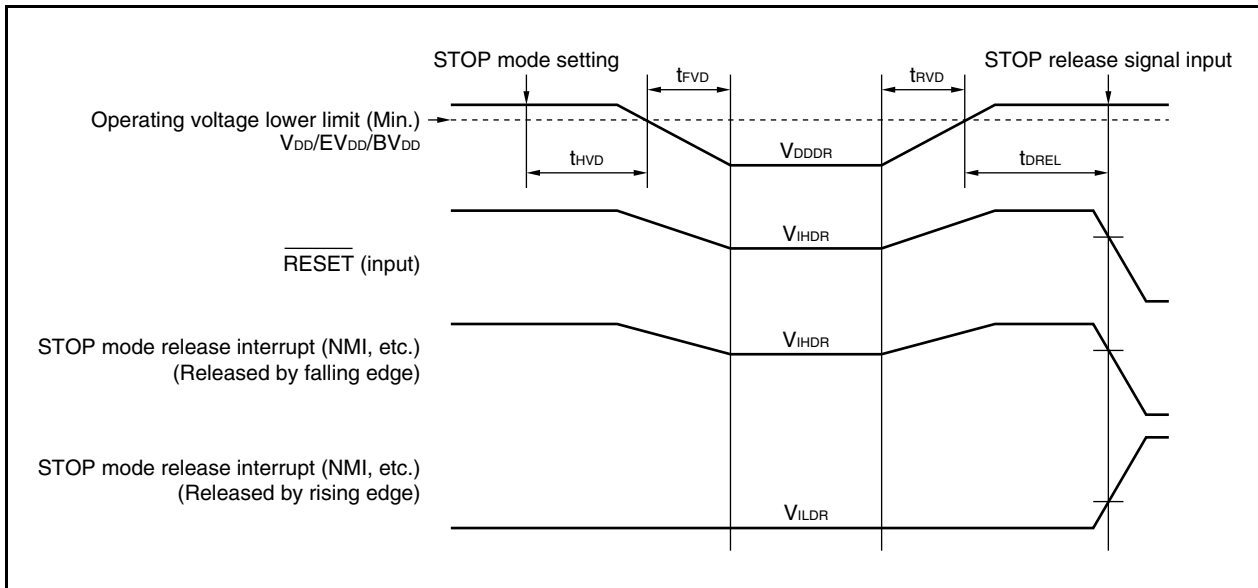
2. When the main OSC is stopped.
3. POC operating, Ring-OSC operating.
4. The RC oscillation frequency is 40 kHz (TYP.). This clock is internally divided by 2.
5. When the sub-OSC is not used.

1.3.9 Data Retention Characteristics

STOP Mode ($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 1.9$ V to 5.5 V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V)

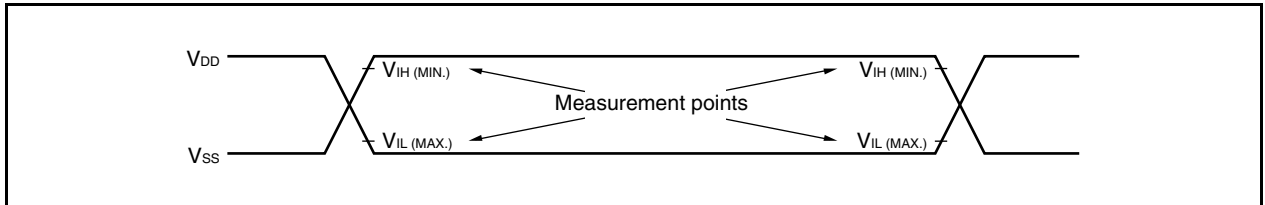
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|------------------------------------|------------|------------------------------------|---------------|------|---------------|---------------|
| Data retention voltage | V_{DDDR} | In STOP mode | 1.9 | | 5.5 | V |
| Data retention current | I_{DDDR} | $V_{DDDR} = 2.0$ V | | 6 | 450 | μA |
| Supply voltage rise time | t_{rVD} | | 1 | | | μs |
| Supply voltage fall time | t_{fVD} | | 1 | | | μs |
| Supply voltage retention time | t_{HVD} | After STOP mode release | 0 | | | ms |
| STOP release signal input time | t_{dREL} | After V_{DD} reaches MIN.: 3.5 V | 0 | | | μs |
| Data retention input voltage, high | V_{IHDR} | All input ports | $0.9V_{DDDR}$ | | V_{DDDR} | V |
| Data retention input voltage, low | V_{ILDR} | All input ports | 0 | | $0.1V_{DDDR}$ | V |

Caution Shifting to STOP mode and restoring from STOP mode must be performed within the rated operating range.

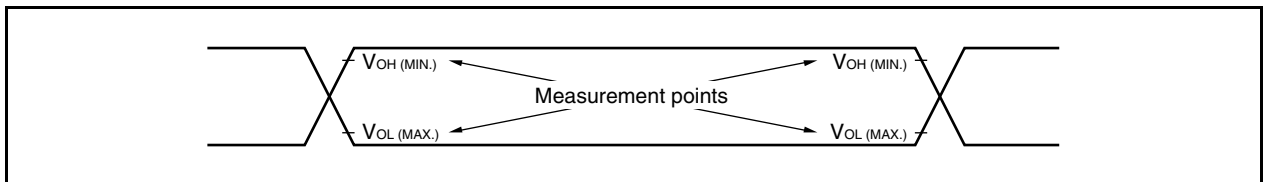


1.3.10 AC Characteristics

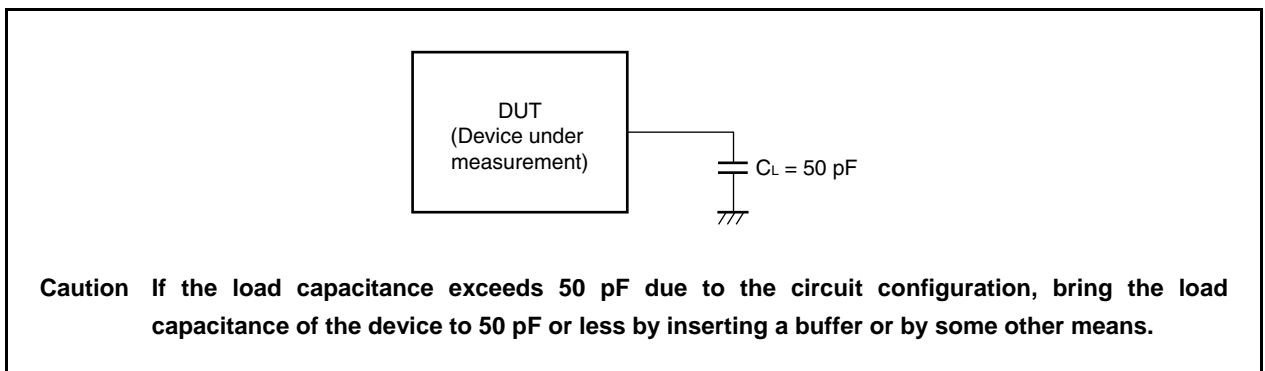
AC Test Input Measurement Points (V_{DD} , AV_{DD} , EV_{DD} , BV_{DD})



AC Test Output Measurement Points



Load Conditions

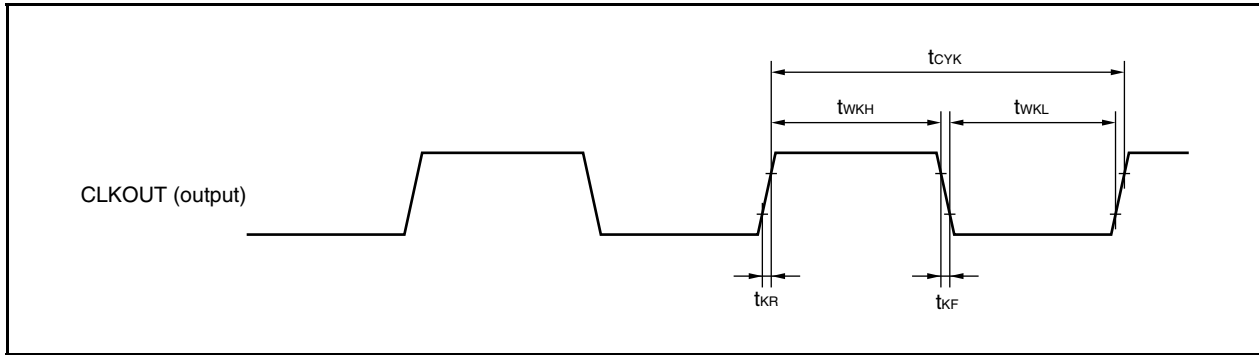


(1) CLKOUT output timing

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|------------------|-----------|------------|------------------|------------------|------|
| Output cycle | t_{CYK} | | 50 ns | 80 μs | |
| High-level width | t_{WKH} | | $t_{CYK}/2 - 15$ | | ns |
| Low-level width | t_{WKL} | | $t_{CYK}/2 - 15$ | | ns |
| Rise time | t_{KR} | | | 15 | ns |
| Fall time | t_{KF} | | | 15 | ns |

Clock Timing



(2) Basic Operation

(a) Reset, Interrupt timing

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0\text{ V}$, $C_L = 50\text{ pF}$)

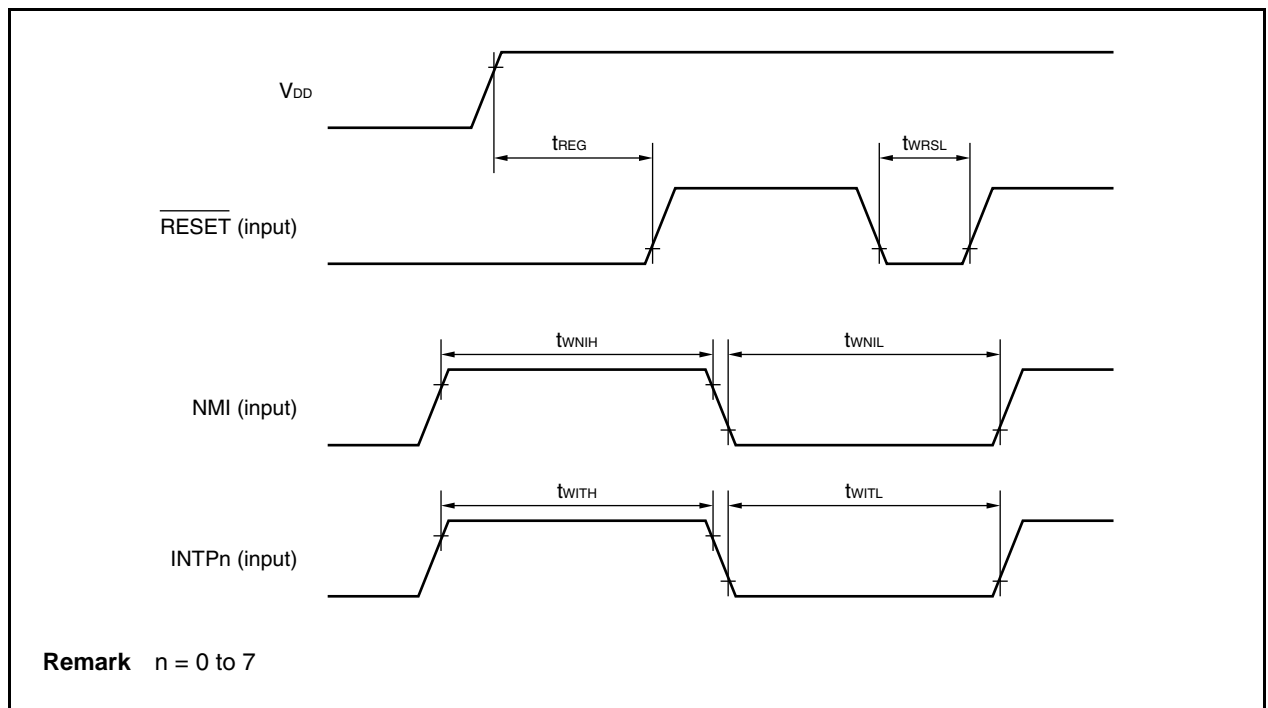
| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|--|------------|---------------------------------------|---------------|------|------|
| RESET low-level width | t_{WRSL} | | 500 | | ns |
| NMI high-level width | t_{WNIH} | Analog noise elimination | 500 | | ns |
| NMI low-level width | t_{WNIL} | Analog noise elimination | 500 | | ns |
| INTP _n ^{Note 1} high-level width | t_{WITH} | Analog noise elimination (n = 0 to 7) | 500 | | ns |
| | | Digital noise elimination (n = 3) | Note 2 | | ns |
| INTP _n ^{Note 1} low-level width | t_{WITL} | Analog noise elimination (n = 0 to 7) | 1 | | ns |
| | | Digital noise elimination (n = 3) | Note 2 | | ns |

Notes 1. ADTRG is same spec (P03/INTP0/ADTRG). \overline{DRST} is same spec (P05/INTP2/ \overline{DRST}).

2. $2T_{\text{samp}} + 20$ or $3T_{\text{samp}} + 20$

T_{samp} : Sampling clock for noise elimination

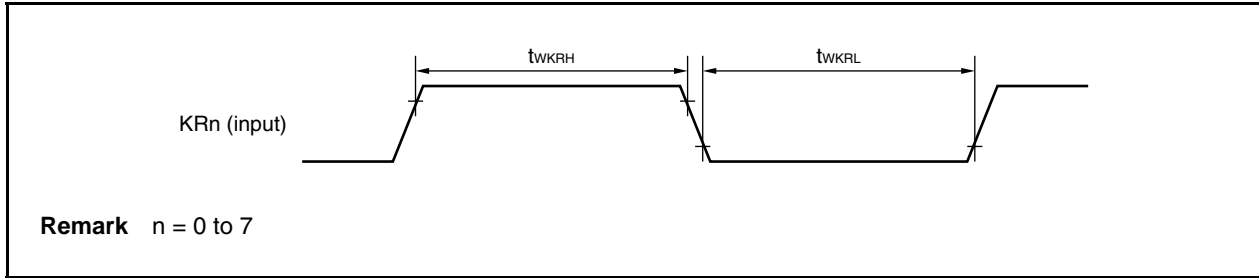
Reset/Interrupt



(b) Key return timing

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0\text{ V}$, $C_L = 50\text{ pF}$)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|----------------------------|------------|---|------|------|------|
| KRn input high-level width | t_{WKRH} | Analog noise elimination ($n = 0$ to 7) | 500 | | ns |
| KRn input low-level width | t_{WKRL} | | 500 | | ns |

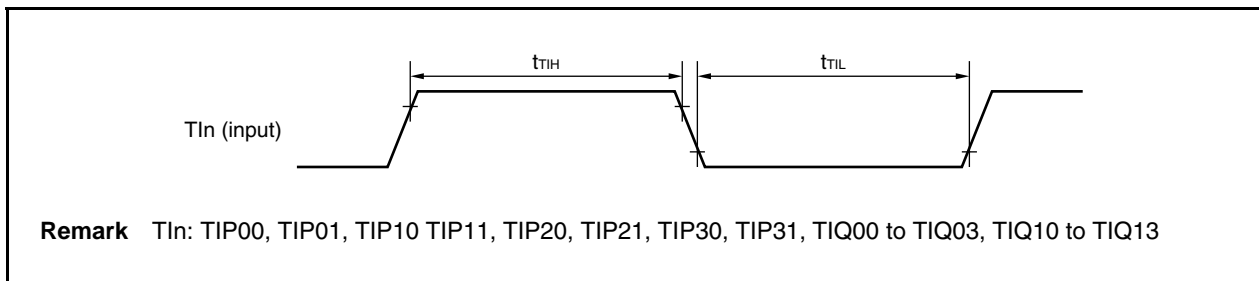


(c) Timer input timing

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0\text{ V}$, $C_L = 50\text{ pF}$)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|----------------------|-----------|---|-------------|------|------|
| TIn high-level width | t_{TIH} | TIP00, TIP01, TIP10, TIP11, TIP20, TIP21, TIP30, TIP31, | Note | | ns |
| TIn low-level width | t_{TIL} | TIQ00 to TIQ03, TIQ10 to TIQ13 | Note | | ns |

Note $2T_{\text{samp}} + 20$ or $3T_{\text{samp}} + 20$
 T_{samp} : Sampling clock for noise elimination



(d) CSIB timing

(i) Master mode

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V \leq $AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|--|--------------------|------------|--------------------------|------|------|
| $\overline{\text{SCKBn}}$ cycle time | t_{KCYn} | | 125 | | ns |
| $\overline{\text{SCKBn}}$ high-level width | t_{KHn} | | $t_{\text{KCYn}}/2 - 15$ | | ns |
| $\overline{\text{SCKBn}}$ low-level width | t_{KLn} | | $t_{\text{KCYn}}/2 - 15$ | | ns |
| SIBn setup time (to $\overline{\text{SCKBn}}\uparrow$) | t_{SIKn} | | 30 | | ns |
| SIBn hold time (from $\overline{\text{SCKBn}}\uparrow$) | t_{SIn} | | 25 | | ns |
| Output delay time from $\overline{\text{SCKBn}}\downarrow$ to SOBn | t_{KSOIn} | | | 25 | ns |

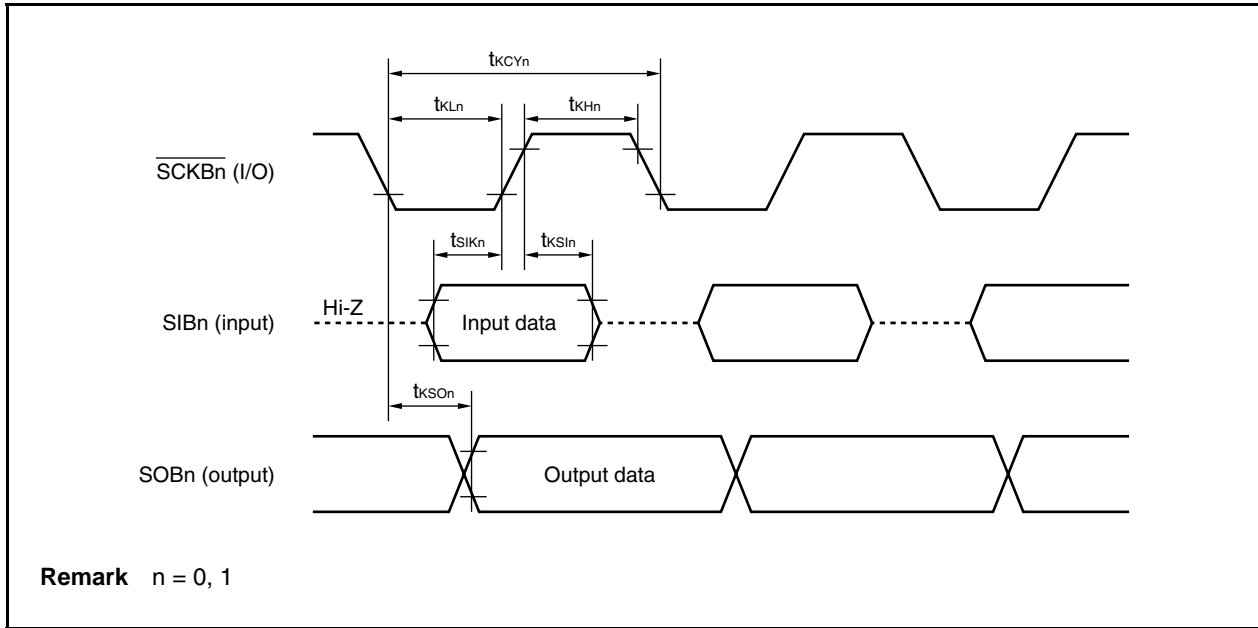
Remark n = 0, 1

(ii) Slave mode

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V \leq $AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|--|--------------------|------------|------|------|------|
| $\overline{\text{SCKBn}}$ cycle time | t_{KCYn} | | 200 | | ns |
| $\overline{\text{SCKBn}}$ high-level width | t_{KHn} | | 90 | | ns |
| $\overline{\text{SCKBn}}$ low-level width | t_{KLn} | | 90 | | ns |
| SIBn setup time (to $\overline{\text{SCKBn}}\uparrow$) | t_{SIKn} | | 50 | | ns |
| SIBn hold time (from $\overline{\text{SCKBn}}\uparrow$) | t_{SIn} | | 50 | | ns |
| Output delay time from $\overline{\text{SCKBn}}\downarrow$ to SOBn | t_{KSOIn} | | | 50 | ns |

Remark n = 0, 1



(e) UART timing

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V \leq $AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

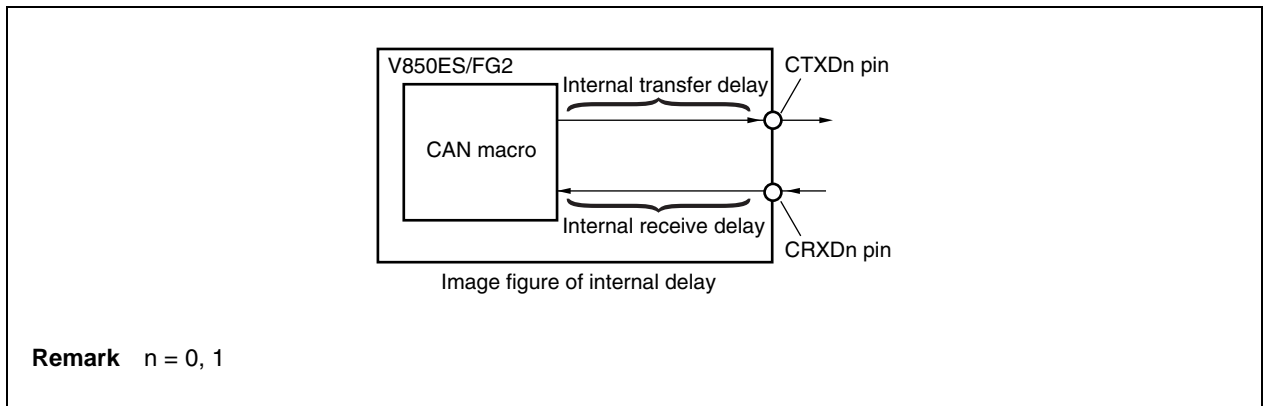
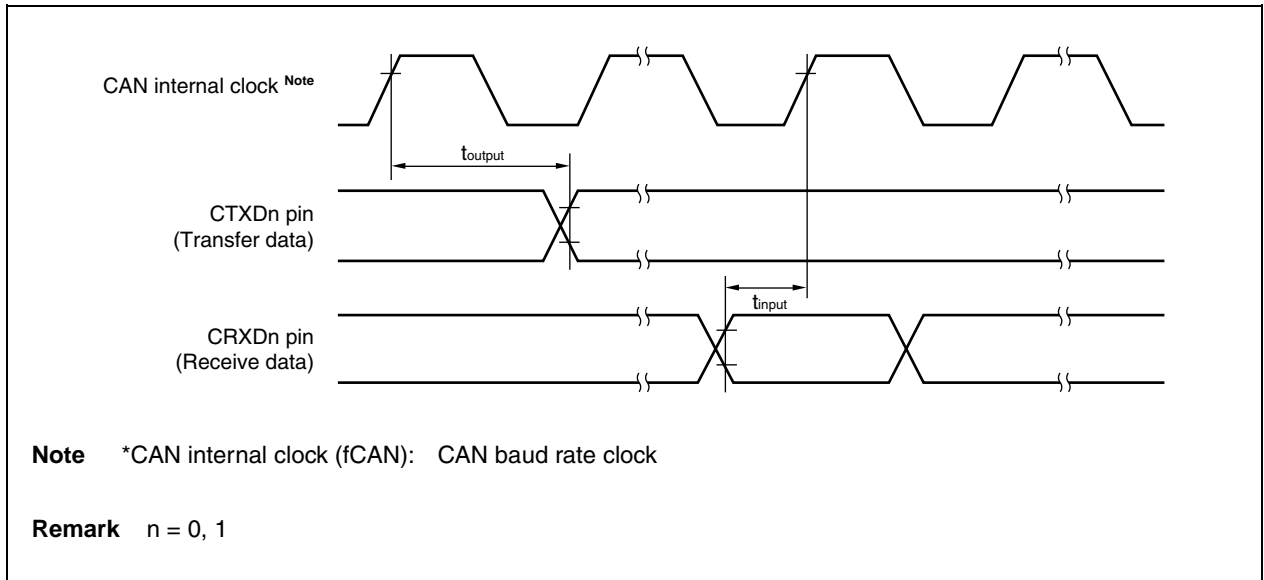
| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|--------------------|--------|------------|------|-------|------|
| Communication rate | | | | 312.5 | kbps |
| ASCK0 cycle time | | | | 10 | MHz |

(f) CAN timing

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0\text{ V}$, $C_L = 50\text{ pF}$)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|-------------------------------------|--------|------------|------|------|------|
| Transfer rate | | | | 1 | Mbps |
| Internal delay time ^{Note} | | | | 100 | ns |

Note Internal delay time (t_{NODE}) = Internal transfer delay time (t_{OUTPUT}) + Internal receive delay time (t_{INPUT})



(g) A/D converter

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------------------|-------------|---------------------------------|-----------|------------|-------------|---------------|
| Resolution | | | | | 10 | bit |
| Overall error ^{Note} | | $4.0 \leq AV_{REF0} \leq 5.5$ V | | ± 0.15 | ± 0.35 | %FSR |
| Conversion time | t_{CONV} | | 3.1 | | 16 | μs |
| Analog input voltage | V_{IAN} | | AV_{SS} | | AV_{REF0} | V |
| AV_{REF0} current | I_{AREF0} | When using A/D converter | | 5 | 10 | mA |
| | | When not using A/D converter | | 1 | 10 | μA |

Note Excluding quantization error ($\pm 0.05\%$ FSR). Indicates the ratio to the full-scale value (%FSR).

Remark FSR: Full Scale Range

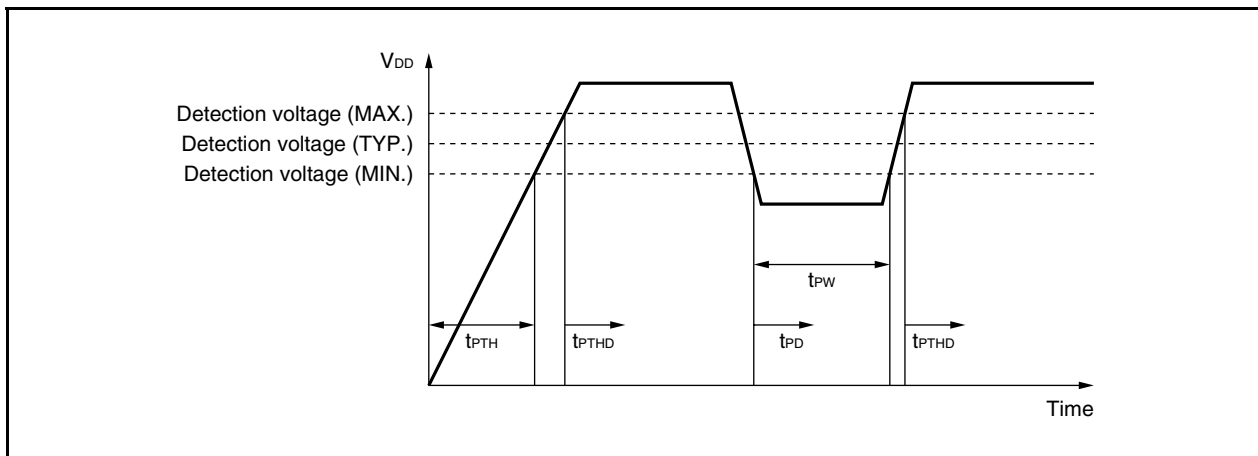
(h) POC circuit characteristics

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--|------------|---|-------|------|------|------|
| Detection voltage | V_{POCO} | | 3.5 | 3.7 | 3.9 | V |
| Power supply startup time | t_{PTH} | $V_{DD} = 0$ V \rightarrow 3.5 V | 0.002 | | | ms |
| Response delay time 1 ^{Note} 1 | t_{PTH1} | In case of power on. After V_{DD} reaches 3.9 V. | | | 3.0 | ms |
| Response delay time 2 ^{Note} 2 | t_{PD} | In case of power off. After V_{DD} drops 3.5 V. | | | 1 | ms |
| Minimum V_{DD} width | t_{PW} | | 0.2 | | | ms |

Notes 1. From detect voltage to release reset signal.

2. From detect voltage to output reset signal.

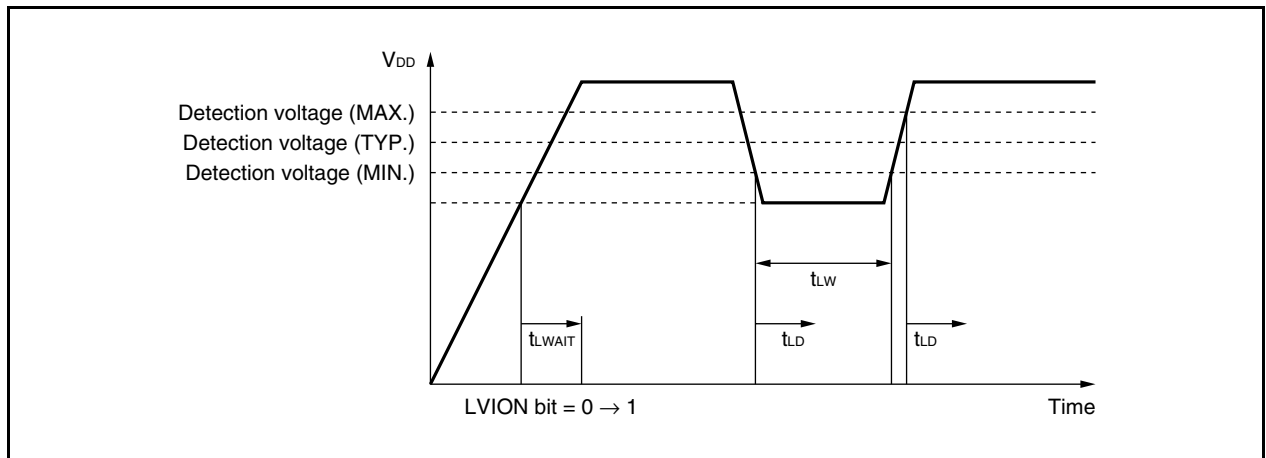


(i) LVI circuit characteristics

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0\text{ V}$, $C_L = 50\text{ pF}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|-------------|--|------|------|------|------|
| Detection voltage | V_{LV10} | | 4.2 | 4.4 | 4.6 | V |
| | V_{LV11} | | 4.0 | 4.2 | 4.4 | V |
| Response time ^{Note 1} | t_{LD} | After V_{DD} reaches V_{LV10}/V_{LV11} (Max.). After V_{DD} drops V_{LV10}/V_{LV11} (Min.). | | 0.2 | 2.0 | ms |
| Minimum V_{DD} width | t_{LW} | | 0.2 | | | ms |
| Reference voltage stabilization wait time ^{Note 2} | t_{LWAIT} | After V_{DD} reaches 3.5 V. After LVION bit (LVIM.bit7) = 0 → 1 | | 0.1 | 0.2 | ms |

- Notes**
1. The time required to output an interrupt/reset after the detection voltage is detected.
 2. Unnecessary when the POC function is used.

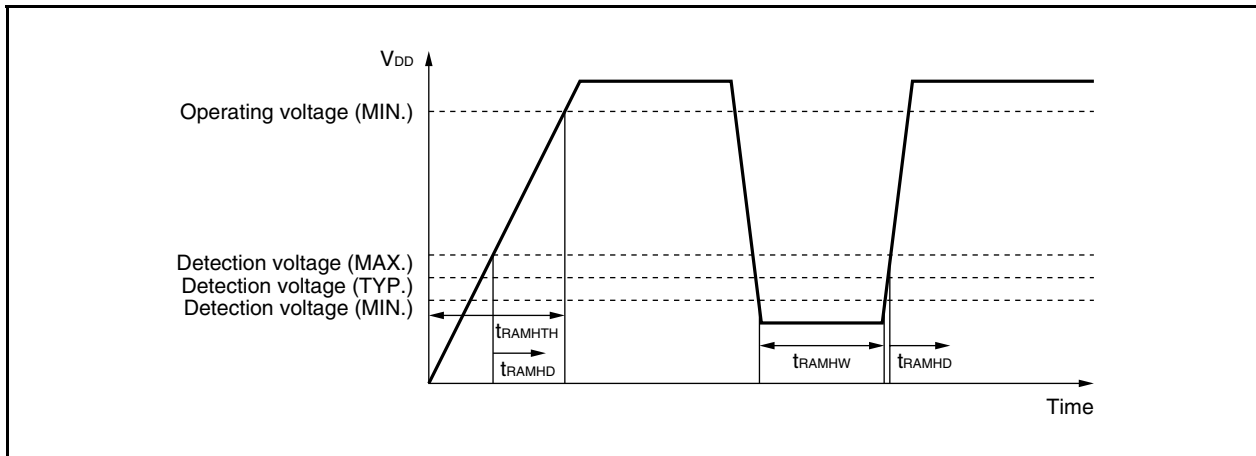


(j) RAM retention flag characteristics

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 1.9$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------------------|--------------|---|-------|------|-------|------|
| Detection voltage | V_{RAMH} | | 1.9 | 2.0 | 2.1 | V |
| Supply voltage rise time | t_{RAMHTH} | $V_{DD} = 0$ V \rightarrow 3.5 V | 0.002 | | 1,800 | ms |
| Response time ^{Note} | t_{RAMHD} | After the supply voltage reaches the detection voltage (MAX.) | | 0.2 | 2.0 | ms |
| Minimum V_{DD} width | t_{RAMHW} | | 0.2 | | | ms |

Note Time required to set the RAMF bit after the detection voltage is detected.



(k) Flash memory programming characteristics

(i) Basic characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------------|----------------------------|---|--------------|------|--------------|------------------|
| Operating frequency | f_{CPU} | | 4 | | 20 | MHz |
| Supply voltage | V_{DD} | | 3.5 | | 5.5 | V |
| Number of writes | C_{WRT} ^{Note} | | | | 100 | Times |
| Input voltage, high | V_{IH} | FLMD0 | $0.8EV_{DD}$ | | EV_{DD} | V |
| Input voltage, low | V_{IL} | FLMD0 | EV_{SS} | | $0.2EV_{SS}$ | V |
| Write time + erase time | t_{WRT} + t_{ERASE} | Flash: 256 KB ($\mu\text{PD70F3235}$) 384 KB ($\mu\text{PD70F3236}$) | | | T.B.D | s |
| Programming temperature | t_{PRG} | | -40 | | +85 | $^\circ\text{C}$ |

Note The initial write when the product is shipped, any erase → write set of operations, or any programming operation is counted as one rewrite.

Example: P: Write, E: Erase

Shipped product → P → E → P → E → P: 3 rewrites

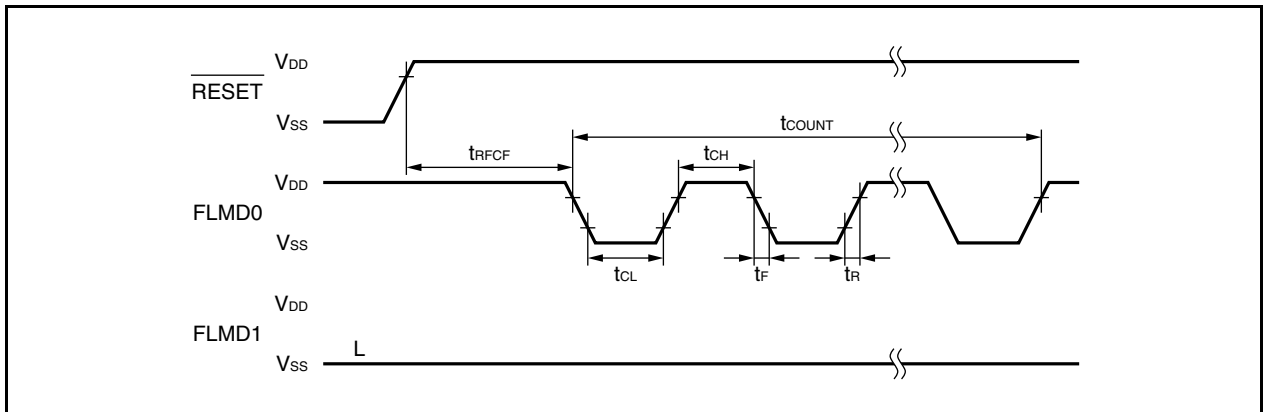
Shipped product → E → P → E → P → E → P: 3 rewrites

(ii) Serial Write Operation Characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = BV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|-------------|------------|---------------------|------|------|---------------|
| FLMD0 setup time from $\overline{\text{RESET}}\uparrow$ | t_{RFCF} | | $5000/f_x + \alpha$ | | | s |
| Count execution time | t_{COUNT} | | | | 3 | ms |
| FLMD0 high-level width | t_{CH} | | 10 | | 100 | μs |
| FLMD0 low-level width | t_{CL} | | 10 | | 100 | μs |
| FLMD rise time | t_R | | | | 50 | ns |
| FLMD fall time | t_F | | | | 50 | ns |

Note “ ” represents the oscillation stabilization time.



2. Injected Current Specification

2.1 Injected Current Specification of (A)-Grade

2.1.1 Absolute Maximum Ratings

(Ta = +25 °C)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|--|-------------|--------------------|---------|------|------|------|----|
| Pos. Overload Current $V_{IN} > V_{DD}$ | I_{INJPM} | Digital input pins | Per pin | | | 4 | mA |
| | | | Total | | | 50 | mA |
| | | Analog input pins | Per pin | | | 4 | mA |
| | | | Total | | | 20 | mA |
| Neg. Overload Current $V_{IN} < V_{SS}$ | I_{INJNM} | Digital input pins | Per pin | | | -4 | mA |
| | | | Total | | | -50 | mA |
| | | Analog input pins | Per pin | | | -4 | mA |
| | | | Total | | | -20 | mA |

Caution: Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter.

Remark: Analog input pins are pins of Port7 and Port12. Digital input pins are pins except analog input pins.

2.1.2 DC Characteristics for overload current

(Ta = -40 to +85 °C, $V_{DD}=EV_{DD}=BV_{DD}=3.5V$ to $5.5V$, $AV_{REF0}=4.0V$ to $5.5V$, $V_{SS}=EV_{SS}=BV_{SS}=AV_{SS}=0V$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|--|------------|-------------------------------------|---------|------|------|------|----|
| Pos. Overload Current $V_{IN} > V_{DD}$ | I_{INJP} | Digital input pins | Per pin | | | 2 | mA |
| | | | Total | | | 16 | mA |
| | | Analog input pins | Per pin | | | 0.5 | mA |
| | | | Total | | | 2 | mA |
| Neg. Overload Current $V_{IN} < V_{SS}$ | I_{INJN} | Digital input pins ^{Note1} | Per pin | | | -0.3 | mA |
| | | | Total | | | -2.4 | mA |
| | | Analog input pins | Per pin | | | -0.3 | mA |
| | | | Total | | | -1.2 | mA |

Remark(s):

1. Analog input pins are pins of Port7 and Port12. Digital input pins are pins except analog input pins.
2. These specifications are not tested in outgoing inspection, but specified based on the device characterization.
3. Refer to the next pages for Input leakage current and A/D characteristics.

Note(s):

1. In case of using Sub clock, an adjacent pin of XT2 pin is the following specification.

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--|------------|--|------|------|------|------|
| Neg. Overload Current $V_{IN} < V_{SS}$ | I_{INJN} | an adjacent pin of XT2 pin ^{Note2} | | | -0.1 | mA |

Note(s):

2. An adjacent pin of XT2 pin is as follows:

V850ES/FE2: P00 pin, V850ES/FF2: P05 pin, V850ES/FG2: P02 pin, V850ES/FJ2: P02 pin

2.1.3 DC Characteristics for pins influenced by injected current on an adjacent pin

(Ta = -40 to +85 °C, V_{DD}=EV_{DD}=BV_{DD} = 3.5V to 5.5V, AV_{REF0} = 4.0V to 5.5V, V_{SS}=EV_{SS}=BV_{SS}=AV_{SS}=0V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|-------------------------------|------------------|----------------------------------|--|------|------|------|----|
| Input leakage current High | I _{LIH} | V _I = V _{DD} | Digital input pins I _{INIP} : 2mA(per pin), 4mA(total) | | - | 0.5 | uA |
| | | | Analog input pins I _{INIP} : 0.5mA(per pin), 1mA(total) | | - | 0.2 | uA |
| Input leakage current Low | I _{LIL} | V _I = 0 | Digital input pins I _{ININ} : -0.3mA(per pin), -0.6mA(total) | | 5 | 40 | uA |
| | | | I _{ININ} : -0.1mA(per pin), -0.2mA(total) | | 1 | 10 | uA |
| | | | Analog input pins I _{ININ} : -0.3mA(per pin), -0.6mA(total) | | 5 | 40 | uA |
| | | | I _{ININ} : -0.1mA(per pin), -0.2mA(total) | | 1 | 10 | uA |

Remark(s):

1. Analog input pins are pins of Port7 and Port12. Digital input pins are pins except analog input pins.
2. These specifications are not tested in outgoing inspection, but specified based on the device characterization.
3. Measurement conditions are shown in [Figure 1](#).
4. TYP. is the value of Ta=+25 °C.

2.1.4 A/D converter influenced by injected current on an adjacent pin

(Ta = -40 to +85 °C, V_{DD}=EV_{DD}=BV_{DD}= 3.5V to 5.5V, AV_{REF0}= 4.0V to 5.5V, V_{SS}=EV_{SS}=BV_{SS}=AV_{SS}=0V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|--------|--|------|------|----------|------|
| Degradation of Overall error ^{Note1} | | I _{INJP} : 0.5mA(per pin), 1mA(total) | | | +/- 0.10 | %FSR |
| | | I _{INJN} : -0.3mA(per pin), -0.6mA(total) | | | +/- 0.25 | %FSR |

Remark(s):

1. These specifications are not tested in outgoing inspection, but specified based on the device characterization.
2. Measurement conditions are shown in Figure 1.

Note(s):

This value is the degradation by injected current on an adjacent pin. Therefore, this value is added to the specification of A/D converter's overall error defined separately as the electrical specifications.

Caution(s):

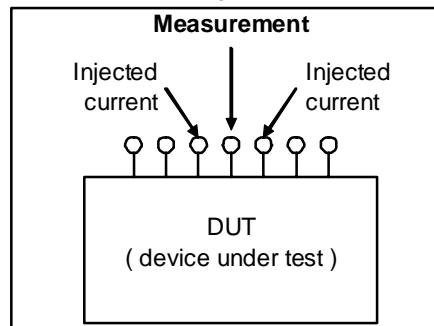
When there is a leakage current, the effect on the ADC accuracy depends on the external analog source impedance.

Example) Conditions: AVREF0 = 5.0V, external analog source impedance = 10K ohm

If there is a leakage current of 10uA by injected current, the effect on the ADC accuracy is

$$10(\mu\text{A}) \times 10\text{K}(\text{ohm}) / 5(\text{V}) = 2\% \text{FSR}$$

Figure 1



2.2 Injected Current Specification of (A1)-Grade

2.2.1 Absolute Maximum Ratings

(Ta = +25 °C)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|--|-------------|--------------------|---------|------|------|------|----|
| Pos. Overload Current $V_{IN} > V_{DD}$ | I_{INJPM} | Digital input pins | Per pin | | | 4 | mA |
| | | | Total | | | 50 | mA |
| | | Analog input pins | Per pin | | | 4 | mA |
| | | | Total | | | 20 | mA |
| Neg. Overload Current $V_{IN} < V_{SS}$ | I_{INJNM} | Digital input pins | Per pin | | | -4 | mA |
| | | | Total | | | -50 | mA |
| | | Analog input pins | Per pin | | | -4 | mA |
| | | | Total | | | -20 | mA |

Caution: Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter.

Remark: Analog input pins are pins of Port7 and Port12. Digital input pins are pins except analog input pins.

2.2.2 DC Characteristics for overload current

(Ta = -40 to +110 °C, $V_{DD}=EV_{DD}=BV_{DD}=3.5V$ to $5.5V$, $AV_{REF}=4.0V$ to $5.5V$, $V_{SS}=EV_{SS}=BV_{SS}=AV_{SS}=0V$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|--|------------|-------------------------------------|---------|------|------|------|----|
| Pos. Overload Current $V_{IN} > V_{DD}$ | I_{INJP} | Digital input pins | Per pin | | | 2 | mA |
| | | | Total | | | 16 | mA |
| | | Analog input pins | Per pin | | | 0.5 | mA |
| | | | Total | | | 2 | mA |
| Neg. Overload Current $V_{IN} < V_{SS}$ | I_{INJN} | Digital input pins ^{Note1} | Per pin | | | -0.3 | mA |
| | | | Total | | | -2.4 | mA |
| | | Analog input pins | Per pin | | | -0.3 | mA |
| | | | Total | | | -1.2 | mA |

Remark(s):

1. Analog input pins are pins of Port7 and Port12. Digital input pins are pins except analog input pins.
2. These specifications are not tested in outgoing inspection, but specified based on the device characterization.
3. Refer to the next pages for Input leakage current and A/D characteristics.

Note(s):

1. In case of using Sub clock, an adjacent pin of XT2 pin is the following specification.

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--|------------|--|------|------|------|------|
| Neg. Overload Current $V_{IN} < V_{SS}$ | I_{INJN} | an adjacent pin of XT2 pin ^{Note2} | | | -0.1 | mA |

Note(s):

2. An adjacent pin of XT2 pin is as follows.

V850ES/FE2: P00 pin, V850ES/FF2: P05 pin, V850ES/FG2: P02 pin, V850ES/FJ2: P02 pin

2.2.3 DC Characteristics for pins influenced by injected current on an adjacent pin

(Ta = -40 to +110 °C, V_{DD}=EV_{DD}=BV_{DD} = 3.5V to 5.5V, AV_{REF0} = 4.0V to 5.5V, V_{SS}=EV_{SS}=BV_{SS}=AV_{SS}=0V)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|-------------------------------|------------------|----------------------------------|--|------|------|------|------|
| Input leakage current High | I _{LH} | V _I = V _{DD} | Digital input pins I _{INIP} : 2mA(per pin), 4mA(total) | | - | 2 | uA |
| | | | Analog input pins I _{INIP} : 0.5mA(per pin), 1mA(total) | | - | 2 | uA |
| Input leakage current Low | I _{LIL} | V _I = 0 | Digital input pins I _{ININ} : -0.3mA(per pin), -0.6mA(total) | | 5 | 60 | uA |
| | | | I _{ININ} : -0.1mA(per pin), -0.2mA(total) | | 1 | 15 | uA |
| | | | Analog input pins I _{ININ} : -0.3mA(per pin), -0.6mA(total) | | 5 | 60 | uA |
| | | | I _{ININ} : -0.1mA(per pin), -0.2mA(total) | | 1 | 15 | uA |

Remark(s):

1. Analog input pins are pins of Port7 and Port12. Digital input pins are pins except analog input pins.
2. These specifications are not tested in outgoing inspection, but specified based on the device characterization.
3. Measurement conditions are shown in Figure 2.
4. TYP. is the value of Ta=+25 °C.

2.2.4 A/D converter influenced by injected current on an adjacent pin

(Ta = -40 to +110 °C, V_{DD}=EV_{DD}=BV_{DD} = 3.5V to 5.5V, AV_{REF0} = 4.0V to 5.5V, V_{SS}=EV_{SS}=BV_{SS}=AV_{SS}=0V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|--------|--|------|------|----------|------|
| Degradation of Overall error ^{Note1} | | I _{INJP} : 0.5mA(per pin), 1mA(total) | | | +/- 0.10 | %FSR |
| | | I _{INJN} : -0.3mA(per pin), -0.6mA(total) | | | +/- 0.25 | %FSR |

Remark(s):

1. These specifications are not tested in outgoing inspection, but specified based on the device characterization.
2. Measurement conditions are shown in Figure 2.

Note(s):

This value is the degradation by injected current on an adjacent pin. Therefore, this value is added to the specification of A/D converter's overall error defined separately as the electrical specifications.

Caution(s):

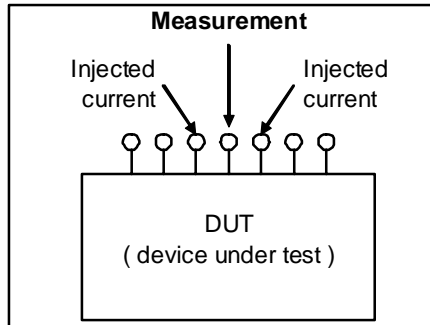
When there is a leakage current, the effect on the ADC accuracy depends on the external analog source impedance.

Example) Conditions: AVREF0 = 5.0V, external analog source impedance = 10K ohm

If there is a leakage current of 10uA by injected current, the effect on the ADC accuracy is

$$10(\mu\text{A}) \times 10\text{K}(\text{ohm}) / 5(\text{V}) = 2\% \text{FSR}$$

Figure 2



2.3 Injected Current Specification of (A2)-Grade

2.3.1 Absolute Maximum Ratings

(Ta = +25 °C)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|--|-------------|--------------------|---------|------|------|------|----|
| Pos. Overload Current $V_{IN} > V_{DD}$ | I_{INJPM} | Digital input pins | Per pin | | | 4 | mA |
| | | | Total | | | 50 | mA |
| | | Analog input pins | Per pin | | | 4 | mA |
| | | | Total | | | 20 | mA |
| Neg. Overload Current $V_{IN} < V_{SS}$ | I_{INJNM} | Digital input pins | Per pin | | | -4 | mA |
| | | | Total | | | -50 | mA |
| | | Analog input pins | Per pin | | | -4 | mA |
| | | | Total | | | -20 | mA |

Caution: Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter.

Remark: Analog input pins are pins of Port7 and Port12. Digital input pins are pins except analog input pins.

2.3.2 DC Characteristics for overload current

(Ta = -40 to +125 °C, $V_{DD}=EV_{DD}=BV_{DD}=3.5V$ to $5.5V$, $AV_{REF}=4.0V$ to $5.5V$, $V_{SS}=EV_{SS}=BV_{SS}=AV_{SS}=0V$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|--|------------|-------------------------------------|---------|------|------|------|----|
| Pos. Overload Current $V_{IN} > V_{DD}$ | I_{INJP} | Digital input pins | Per pin | | | 2 | mA |
| | | | Total | | | 16 | mA |
| | | Analog input pins | Per pin | | | 0.5 | mA |
| | | | Total | | | 2 | mA |
| Neg. Overload Current $V_{IN} < V_{SS}$ | I_{INJN} | Digital input pins ^{Note1} | Per pin | | | -0.3 | mA |
| | | | Total | | | -2.4 | mA |
| | | Analog input pins | Per pin | | | -0.3 | mA |
| | | | Total | | | -1.2 | mA |

Remark(s):

1. Analog input pins are pins of Port7 and Port12. Digital input pins are pins except analog input pins.
2. These specifications are not tested in outgoing inspection, but specified based on the device characterization.
3. Refer to the next pages for Input leakage current and A/D characteristics.

Note(s):

1. In case of using Sub clock, an adjacent pin of XT2 pin is the following specification.

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--|------------|--|------|------|------|------|
| Neg. Overload Current $V_{IN} < V_{SS}$ | I_{INJN} | an adjacent pin of XT2 pin ^{Note2} | | | -0.1 | mA |

Note(s):

2. An adjacent pin of XT2 pin is as follows.

V850ES/FE2: P00 pin, V850ES/FF2: P05 pin, V850ES/FG2: P02 pin, V850ES/FJ2: P02 pin

2.3.3 DC Characteristics for pins influenced by injected current on an adjacent pin

(Ta = -40 to +125 °C, V_{DD}=EV_{DD}=BV_{DD}= 3.5V to 5.5V, AV_{BEF0}= 4.0V to 5.5V, V_{SS}=EV_{SS}=BV_{SS}=AV_{SS}=0V)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|-------------------------------|------------------|----------------------------------|--|------|------|------|------|
| Input leakage current High | I _{LIH} | V _I = V _{DD} | Digital input pins I _{INIP} : 2mA(per pin), 4mA(total) | | - | 5 | uA |
| | | | Analog input pins I _{INIP} : 0.5mA(per pin), 1mA(total) | | - | 3 | uA |
| Input leakage current Low | I _{LIL} | V _I = 0 | Digital input pins I _{ININ} : -0.3mA(per pin), -0.6mA(total) | | 5 | 60 | uA |
| | | | I _{ININ} : -0.1mA(per pin), -0.2mA(total) | | 1 | 15 | uA |
| | | | Analog input pins I _{ININ} : -0.3mA(per pin), -0.6mA(total) | | 5 | 60 | uA |
| | | | I _{ININ} : -0.1mA(per pin), -0.2mA(total) | | 1 | 15 | uA |

Remark(s):

1. Analog input pins are pins of Port7 and Port12. Digital input pins are pins except analog input pins.
2. These specifications are not tested in outgoing inspection, but specified based on the device characterization.
3. Measurement conditions are shown in [Figure 3](#).
4. TYP. is the value of Ta=+25 °C.

2.3.4 A/D converter influenced by injected current on an adjacent pin

(Ta = -40 to +125 °C, V_{DD}=EV_{DD}=BV_{DD}= 3.5V to 5.5V, AV_{REF0} = 4.0V to 5.5V, V_{SS}=EV_{SS}=BV_{SS}=AV_{SS}=0V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|--------|--|------|------|----------|------|
| Degradation of Overall error ^{Note1} | | I _{INJP} : 0.5mA(per pin), 1mA(total) | | | +/- 0.10 | %FSR |
| | | I _{INJN} : -0.3mA(per pin), -0.6mA(total) | | | +/- 0.25 | %FSR |

Remark(s):

1. These specifications are not tested in outgoing inspection, but specified based on the device characterization.
2. Measurement conditions are shown in [Figure 3](#).

Note(s):

This value is the degradation by injected current on an adjacent pin. Therefore, this value is added to the specification of A/D converter's overall error defined separately as the electrical specifications.

Caution(s):

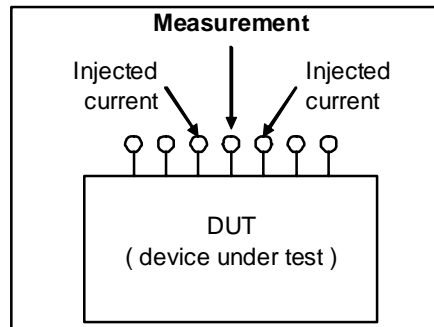
When there is a leakage current, the effect on the ADC accuracy depends on the external analog source impedance.

Example) Conditions: AVREF0 = 5.0V, external analog source impedance = 10K ohm

If there is a leakage current of 10uA by injected current, the effect on the ADC accuracy is

$$10(\mu\text{A}) \times 10\text{K}(\text{ohm}) / 5(\text{V}) = 2\% \text{FSR}$$

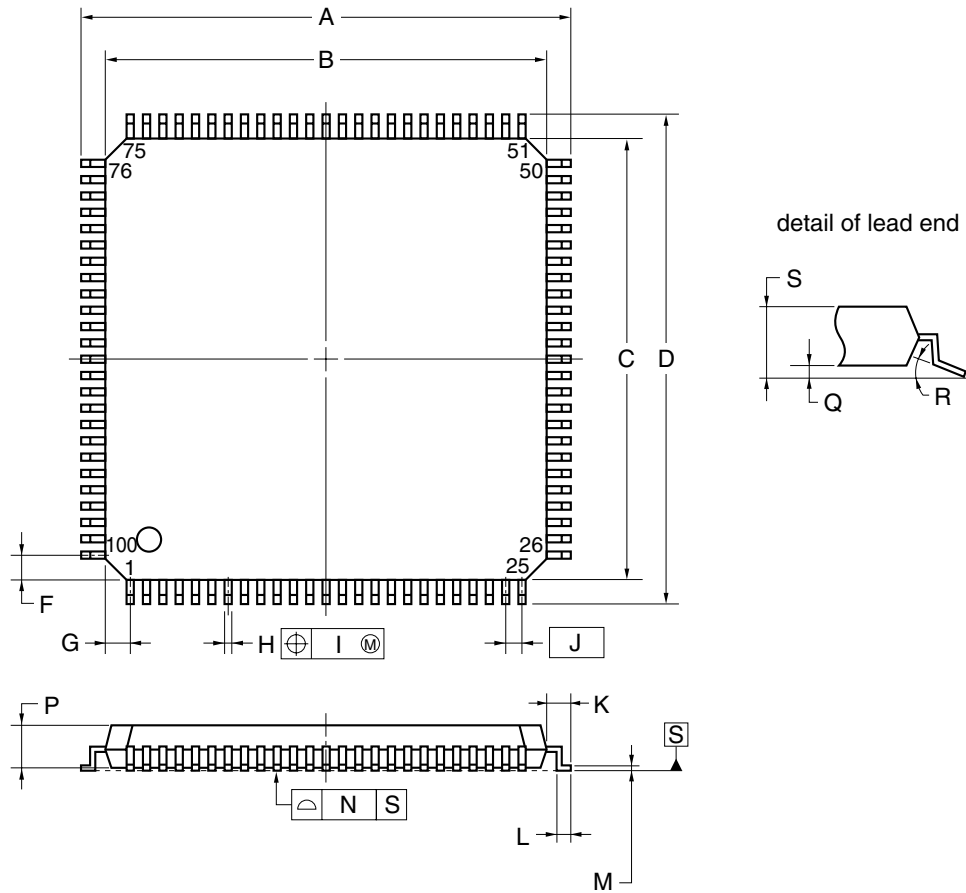
Figure 3



3. Package Drawings

Figure 3-1: Package Drawing

100-PIN PLASTIC LQFP (FINE PITCH) (14x14)



NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS |
|------|--|
| A | 16.00±0.20 |
| B | 14.00±0.20 |
| C | 14.00±0.20 |
| D | 16.00±0.20 |
| F | 1.00 |
| G | 1.00 |
| H | 0.22 ^{+0.05} _{-0.04} |
| I | 0.08 |
| J | 0.50 (T.P.) |
| K | 1.00±0.20 |
| L | 0.50±0.20 |
| M | 0.17 ^{+0.03} _{-0.07} |
| N | 0.08 |
| P | 1.40±0.05 |
| Q | 0.10±0.05 |
| R | 3° ^{+7°} _{-3°} |
| S | 1.60 MAX. |

S100GC-50-8EU, 8EA-2

4. Recommended Soldering Conditions

Table 4-1: Soldering Conditions

(1) μ PD70F3236MxGC(Ax)-8EA, μ PD70F3235MxGC(Ax)-8EA, μ PD70F3234MxGC(Ax)-8EA

| Soldering Method | Soldering Condition | Symbol of Recommended Soldering Condition |
|------------------|---|---|
| Infrared Reflow | Package Peak Temperature: 235°C Time: 30 seconds max. (210°C min.) Count: 3 max Exposure Limit: 7 days ^{Note} | IR35-207-3 |

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period. After that, prebaking is necessary at 125 °C for 20 to 72 hours.