

To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

Send any inquiries to <http://www.renesas.com/inquiry>.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: “Standard”, “High Quality”, and “Specific”. The recommended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as “Specific” without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as “Specific” or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is “Standard” unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.
 - “Standard”: Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.
 - “High Quality”: Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.
 - “Specific”: Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.



MOS Integrated Circuit

V850ES/FE2

32-bit single-chip micro controller

INTRODUCTION

The V850ES/FE2 are 32-bit single-chip microcontrollers that include the V850ES CPU core and integrate peripheral functions such as timers/counters, serial interfaces, and an A/D converter. These microcontrollers also incorporate a CAN (Controller Area Network) as an automotive LAN.

In addition to highly real-time responsive, 1-clock-pitch basic instructions, these microcontrollers have instructions ideal for digital servo applications, such as multiplication instructions using a hardware multiplier, sum-of-products operation instructions, and bit manipulation instructions. These microcontrollers can also realize a real-time control system that is highly cost effective and can be used in automotive instrumentation fields.

FEATURES

- Number of instructions: 83
- Minimum instruction execution time: 50 ns (main clock (fxx) = 20 MHz)
- General-purpose registers: 32 bits × 32
- Power-on clear function
- Low-voltage detection function
- Ring-OSC: 200 kHz (TYP.)
- Internal memory:
 - RAM: 4/6 KB
 - Flash memory: 128KB
 - Mask ROM: 64/128KB
- Interrupts/exceptions :
 - Non-maskable interrupts : 1 source
 - Maskable interrupts : 43 sources
 - Software exceptions: 2 sources
 - Exception trap: 1 source
- I/O lines I/O ports: 51
- Timer/counters:
 - 16-bit interval timer M (TMM): 1 ch
 - 16-bit timer/event counter P (TMP): 4 ch
 - 16-bit timer/event counter Q (TMQ): 1 ch
- Watch timer: 1 ch
- Watchdog timer 2: 1 ch
- Serial interface (SIO):
 - Asynchronous serial interface A (UART): 2 ch
 - 3-wire variable-length serial interface B (CSIB): 2 ch
- CAN controller: 1 ch
- A/D converter 10-bit resolution: 10 ch
- Clock generator Main clock/subclock operation:
 - CPU clock in seven steps (fxx, fxx/2, fxx/4, fxx/8, fxx/16, fxx/32, fxt)
 - Clock-through mode/PLL mode selectable
 - Internal oscillator: 200 kHz (TYP.)
- Power save function: HALT/IDLE1/IDLE2/software STOP/subclock/sub-IDLE modes
- Package: 64-pin plastic LQFP (fine pitch) (10 × 10)

Part Number	Internal ROM	Internal RAM	CAN I/F
uPD703230	64KB (Mask ROM)	4KB	1 channel
uPD703231	128KB (Mask ROM)	6KB	1 channel
uPD70F3231	128KB (Flash)	6KB	1 channel

Table of Contents

1. Electrical Specifications 4

 1.1 Electrical Specifications of (A)-Grade 4

 1.1.1 Absolute maximum ratings 4

 1.1.2 Capacitance 8

 1.1.3 Operating conditions 8

 1.1.4 Oscillator Characteristics 9

 1.1.5 PLL Characteristics 11

 1.1.6 Ring-OSC Characteristics 11

 1.1.7 Voltage Regulator Characteristics 11

 1.1.8 DC Characteristics 12

 1.1.9 Data Retention Characteristics 17

 1.1.10 AC Characteristics 18

 1.2 Electrical Specifications of (A1)-Grade 29

 1.2.1 Absolute maximum ratings 29

 1.2.2 Capacitance 33

 1.2.3 Operating conditions 33

 1.2.4 Oscillator Characteristics 34

 1.2.5 PLL Characteristics 36

 1.2.6 Ring-OSC Characteristics 36

 1.2.7 Voltage Regulator Characteristics 36

 1.2.8 DC Characteristics 37

 1.2.9 Data Retention Characteristics 42

 1.2.10 AC Characteristics 43

 1.3 Electrical Specifications of (A2)-Grade 54

 1.3.1 Absolute maximum ratings 54

 1.3.2 Capacitance 58

 1.3.3 Operating conditions 58

 1.3.4 Oscillator Characteristics 59

 1.3.5 PLL Characteristics 61

 1.3.6 Ring-OSC Characteristics 61

 1.3.7 Voltage Regulator Characteristics 61

 1.3.8 DC Characteristics 62

 1.3.9 Data Retention Characteristics 67

 1.3.10 AC Characteristics 68

2. Injected Current Specification 79

 2.1 Injected Current Specification of (A)-Grade 79

 2.1.1 Absolute Maximum Ratings 79

 2.1.2 DC Characteristics for overload current 79

 2.1.3 DC Characteristics for pins influenced by injected current on an adjacent pin 80

 2.1.4 A/D converter influenced by injected current on an adjacent pin 81

 2.2 Injected Current Specification of (A1)-Grade 82

 2.2.1 Absolute Maximum Ratings 82

 2.2.2 DC Characteristics for overload current 82

 2.2.3 DC Characteristics for pins influenced by injected current on an adjacent pin 83

 2.2.4 A/D converter influenced by injected current on an adjacent pin 84

 2.3 Injected Current Specification of (A2)-Grade 85

 2.3.1 Absolute Maximum Ratings 85

2.3.2 DC Characteristics for overload current85

2.3.3 DC Characteristics for pins influenced by injected current on an adjacent pin.....86

2.3.4 A/D converter influenced by injected current on an adjacent pin87

3. Package Drawing88

Figure 3-1: Package Drawing88

4. Recommended Soldering Conditions89

Table 4-1: Soldering Conditions.....89

1. Electrical Specifications

1.1 Electrical Specifications of (A)-Grade

1.1.1 Absolute maximum ratings

Absolute maximum ratings (Flash memory product) (T_A = 25°C) (1/2)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{DD}	V _{DD} = EV _{DD}	-0.5 to +6.5	V
	EV _{DD}	V _{DD} = EV _{DD}	-0.5 to +6.5	V
	AV _{REF0}		-0.5 to +6.5	V
	V _{SS}	V _{SS} = EV _{SS} = AV _{SS}	-0.5 to +0.5	V
	AV _{SS}	V _{SS} = EV _{SS} = AV _{SS}	-0.5 to +0.5	V
	EV _{SS}	V _{SS} = EV _{SS} = AV _{SS}	-0.5 to +0.5	V
Input voltage	V _{I1}	P00 to P06, P30 to P35, P40 to P42, P50 to P55, P90, P91, P96 to P99, P913 to P915, <u>RESET</u> , FLMD0, PCM0, PCM1, PDL0 to PDL7	-0.5 to EV _{DD} + 0.5 ^{Note}	V
	V _{I3}	X1, X2, XT1, XT2	-0.5 to V _{RO} + 0.5 ^{Note}	V
Analog input voltage	V _{IAN}	P70 to P79	-0.5 to AV _{REF0} + 0.5 ^{Note}	V

Note Be sure not to exceed the absolute maximum ratings (MAX. value) of each supply voltage.

- Cautions**
1. Avoid direct connections among the IC device output (or I/O) pins and between V_{DD} or V_{CC} and GND.
 2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Absolute maximum ratings (Flash memory product) (T_A = 25°C) (2/2)

Parameter	Symbol	Conditions	Ratings	Unit	
Output current, low	I _{OL}	P00 to P06, P30 to P35, P40 to P42, P50 to P55, P90, P91, P96 to P99, P913 to P915, PCM0, PCM1 PDL0 to PDL7	Per pin	4	mA
			Total of all pins	50	mA
		P70 to P79	Per pin	4	mA
			Total of all pins	20	mA
Output current, high	I _{OH}	P00 to P06, P30 to P35, P40 to P42, P50 to P55, P90, P91, P96 to P99, P913 to P915, PCM0, PCM1 PDL0 to PDL7	Per pin	-4	mA
			Total of all pins	-50	mA
		P70 to P79	Per pin	-4	mA
			Total of all pins	-20	mA
Operating ambient temperature	T _A	Normal operating mode	-40 to +85	°C	
		Flash programming mode			
Storage temperature	T _{stg}		-40 to +125	°C	

- Cautions**
- 1. Avoid direct connections among the IC device output (or I/O) pins and between V_{DD} or V_{CC} and GND.**
 - 2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Absolute maximum ratings (Mask ROM product) (T_A = 25°C) (1/2)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{DD}	V _{DD} = EV _{DD}	-0.5 to +6.5	V
	EV _{DD}	V _{DD} = EV _{DD}	-0.5 to +6.5	V
	AV _{REF0}		-0.5 to +6.5	V
	V _{SS}	V _{SS} = EV _{SS} = AV _{SS}	-0.5 to +0.5	V
	AV _{SS}	V _{SS} = EV _{SS} = AV _{SS}	-0.5 to +0.5	V
	EV _{SS}	V _{SS} = EV _{SS} = AV _{SS}	-0.5 to +0.5	V
Input voltage	V _{I1}	P00 to P06, P30 to P35, P40 to P42, P50 to P55, P90, P91, P96 to P99, P913 to P915, RESET, PCM0, PCM1, PDL0 to PDL7	-0.5 to EV _{DD} + 0.5 ^{Note}	V
	V _{I3}	X1, X2, XT1, XT2	-0.5 to V _{RO} + 0.5 ^{Note}	V
Analog input voltage	V _{IAN}	P70 to P79	-0.5 to AV _{REF0} + 0.5 ^{Note}	V

Note Be sure not to exceed the absolute maximum ratings (MAX. value) of each supply voltage.

Cautions 1. Avoid direct connections among the IC device output (or I/O) pins and between V_{DD} or V_{CC} and GND.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Absolute maximum ratings (Mask ROM product) (T_A = 25°C) (2/2)

Parameter	Symbol	Conditions	Ratings	Unit	
Output current, low	I _{OL}	P00 to P06, P30 to P35, P40 to P42, P50 to P55, P90, P91, P96 to P99, P913 to P915, PCM0, PCM1 PDL0 to PDL7	Per pin	4	mA
			Total of all pins	50	mA
		P70 to P79	Per pin	4	mA
			Total of all pins	20	mA
Output current, high	I _{OH}	P00 to P06, P30 to P35, P40 to P42, P50 to P55, P90, P91, P96 to P99, P913 to P915, PCM0, PCM1 PDL0 to PDL7	Per pin	-4	mA
			Total of all pins	-50	mA
		P70 to P79	Per pin	-4	mA
			Total of all pins	-20	mA
Operating ambient temperature	T _A		-40 to +85	°C	
Storage temperature	T _{stg}		-65 to +150	°C	

- Cautions**
1. Avoid direct connections among the IC device output (or I/O) pins and between V_{DD} or V_{CC} and GND.
 2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

1.1.2 Capacitance

($T_A = 25^\circ\text{C}$, $V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1} = V_{SS} = EV_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
I/O capacitance	C_{IO}	$f_x = 1\text{ MHz}$, Unmeasured pins returned to 0 V.			10	pF

1.1.3 Operating conditions

($T_A = -40\text{ to }+85^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = AV_{SS} = 0\text{ V}$)

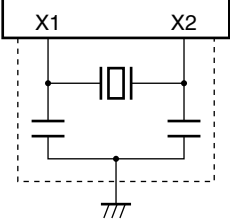
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Internal system clock frequency	f_{CLK}	REGC Capacity = $4.7\ \mu\text{F}$, at operation with main clock	4		20	MHz
		REGC Capacity = $4.7\ \mu\text{F}$, at operation with subclock (crystal resonator)	32		35	kHz
		REGC Capacity = $4.7\ \mu\text{F}$, at operation with subclock (RC resonator)	12.5 ^{Note}		27.5 ^{Note}	kHz

Note The internal system clock frequency is half the oscillation frequency.

1.1.4 Oscillator Characteristics

Main clock oscillator characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = AV_{SS} = 0\text{ V}$)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (fx) ^{Note 1}		4		5	MHz
		Oscillation stabilization time ^{Note 2}	After reset release		$2^{16}/f_x$		s
			After STOP mode release	0.5 ^{Note 3}	Note 4		ms
After IDLE2 mode release	0.35	Note 4		ms			
Crystal resonator		Oscillation frequency (fx) ^{Note 1}		4		5	MHz
		Oscillation stabilization time ^{Note 2}	After reset release		$2^{16}/f_x$		s
			After STOP mode release	0.5 ^{Note 3}	Note 4		ms
After IDLE2 mode release	350	Note 4		μs			

Notes 1. Indicates only oscillator characteristics.

2. Time required to stabilize the crystal resonator after reset or STOP mode is released.

3. Time required to stabilize access to the internal flash memory.

4. The value differs depending on the OSTS register settings.

Cautions 1. When using the main clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
- Do not cross the wiring with the other signal lines.
- Do not route the wiring near a signal line through which a high fluctuating current flows.
- Always make the ground point of the oscillator capacitor the same potential as V_{SS} .
- Do not ground the capacitor to a ground pattern through which a high current flows.
- Do not fetch signals from the oscillator.

2. When the main clock is stopped and the device is operating on the subclock, wait until the oscillation stabilization time has been secured by the program before switching back to the main clock.

Subclock oscillator characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = AV_{SS} = 0\text{ V}$)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator Note 5		Oscillation frequency (f_{XT}) Note 1		32	32.768	35	kHz
		Oscillation stabilization time Note 2				10	s
RC resonator		Oscillation frequency (f_{XT}) Notes 1, 4	$R = 390\text{ k}\Omega \pm 5\%$ Note 3 $C = 47\text{ pF} \pm 10\%$ Note 3	25	40	55	kHz
		Oscillation stabilization time Note 2				100	μs

- Notes**
1. Indicates only oscillator characteristics. Refer to **26. 1. 10 AC Characteristics** for CPU operating clock.
 2. Time required from when V_{DD} reaches oscillation voltage range (MIN.: 3.5 V) to when the crystal resonator stabilizes.
 3. In order to avoid the influence of wiring capacity, shorten wiring as much as possible.
 4. RC oscillation frequency is 40 kHz (Typ.). This clock is divided (1/2) internally. In case of RC oscillator, internal system clock frequency (f_{XT}) is 12.5 kHz (Min.), 20 kHz (Typ.), and 27.5 kHz (Max.).
 5. The values of capacitors $C1'$, $C2'$ and resistors $R'1$ depend on the resonator used and must be specified in cooperation with the manufacturer.

Cautions 1. When using the subclock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
 - Do not cross the wiring with the other signal lines.
 - Do not route the wiring near a signal line through which a high fluctuating current flows.
 - Always make the ground point of the oscillator capacitor the same potential as V_{SS} .
 - Do not ground the capacitor to a ground pattern through which a high current flows.
 - Do not fetch signals from the oscillator.
2. The subclock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main clock oscillator. Particular care is therefore required with the wiring method when the subclock is used.

1.1.5 PLL Characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input frequency	f_x		4		5	MHz
Output frequency	f_{xx}		16		20	MHz
Lock time	t_{PLL}	After V_{DD} reaches MIN.: 3.5 V			800	μs

1.1.6 Ring-OSC Characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD}$, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V)

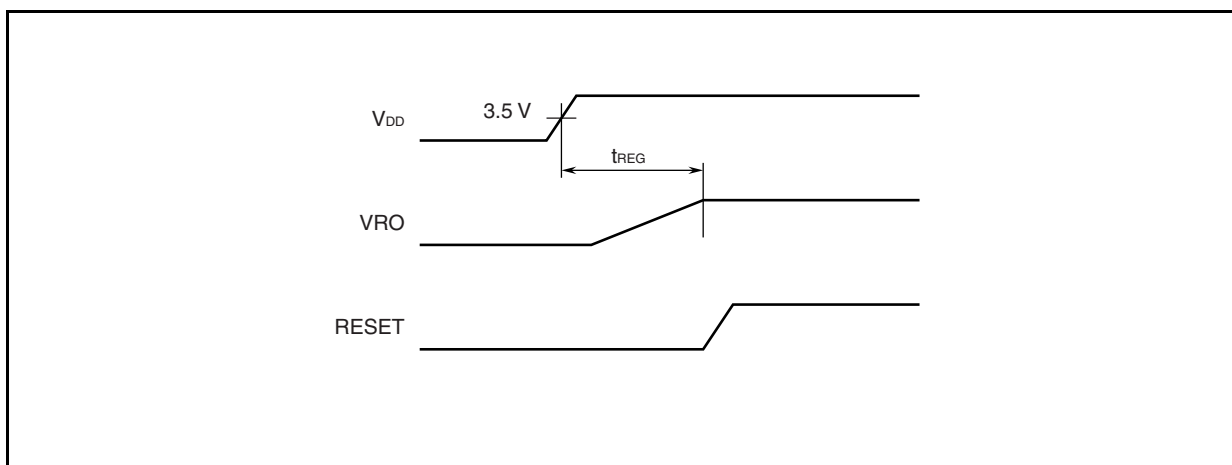
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output frequency	f_r		100	200	400	kHz

1.1.7 Voltage Regulator Characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD}$, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage	V_{DD}		3.5		5.5	V
Output voltage	V_{RO}			2.5		V
Lock time ^{Note 1}	t_{REG}	After V_{DD} reaches MIN.: 3.5 V Connect $C = 4.7 \mu\text{F} \pm 20\%$ to REGC pin			1	ms

Note 1. The lock time does not have to be considered for devices that have POC.



1.1.8 DC Characteristics

(1) Input/Output level

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = AV_{SS} = 0\text{ V}$)

(1/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P30, P34, P41, P98, PCM0, PCM1, PDL0-PDL7	$0.7EV_{DD}$		EV_{DD}	V
	V_{IH2}	P00 to P06, P31 to P33, P35, P40, P42, P50 to P55, P90, P91, P96, P97, P99, P910, P913 to P915	$0.8EV_{DD}$		EV_{DD}	V
	V_{IH4}	P70 to P79	$0.7AV_{REF0}$		AV_{REF0}	V
	V_{IH5}	$\overline{\text{RESET}}$, FLMD0	$0.8EV_{DD}$		EV_{DD}	V
Input voltage, low	V_{IL1}	P30, P34, P41, P98, PCM0, PCM1, PDL0-PDL7	EV_{SS}		$0.3EV_{DD}$	V
	V_{IL2}	P00 to P06, P31 to P33, P35, P40, P42, P50 to P55, P90, P91, P96, P97, P99, P910, P913 to P915	EV_{SS}		$0.2EV_{DD}$	V
	V_{IL4}	P70 to P79	AV_{SS}		$0.3AV_{REF0}$	V
	V_{IL5}	$\overline{\text{RESET}}$, FLMD0	EV_{SS}		$0.2EV_{DD}$	V

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = AV_{SS} = 0\text{ V}$)

(2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Output voltage, high <small>Note 1</small>	V _{OH1}	P00 to P06, P30 to P35, P40 to P42, P50 to P55, P90, P91, P96, P99, P913 to P915, PCM0, PCM1, PDL0 to PDL7	I _{OH} = -1.0 mA	EV _{DD} - 1.0		EV _{DD}	V
			I _{OH} = -0.1 mA	EV _{DD} - 0.5		EV _{DD}	V
	V _{OH3}	P70 to P79	I _{OH} = -1.0 mA	AV _{REF0} - 1.0		AV _{REF0}	V
			I _{OH} = -0.1 mA	AV _{REF0} - 0.5		AV _{REF0}	V
Output voltage, low <small>Note 1</small>	V _{OL1}	P00 to P06, P30 to P35, P40 to P42, P50 to P55, P90, P91, P96, P99, P913 to P915, PCM0, PCM1, PDL0 to PDL7	I _{OL} = 1.0 mA	0		0.4	V
			I _{OL} = 1.0 mA	0		0.4	V
Pull-up resistor	R ₁	V _I = 0 V	10	30	100	kΩ	
Pull-down resistor <small>Note 2</small>	R ₂	V _I = V _{DD}	10	30	100	kΩ	

Notes 1. Total I_{OH}/I_{OL} (Max.) is 20 mA/-20 mA each power supply terminal (EV_{DD} and AV_{REF0}).

2. When used as \overline{DRST} pin (Flash memory product only) (OCDM0 is the control register).

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

(2) Pin leakage current

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Input leakage current, high	I _{LIH1}	V _{IN} = V _{DD}	Analog pins			+0.2	μA
			Other pins ^{Note 1}			+0.5	
Input leakage current, low	I _{LIL1}	V _{IN} = 0 V	Analog pins			-0.2	μA
			Other pins ^{Note 1}			-0.5	
Output leakage current, high	I _{LOH1}	V _O = V _{DD}	Analog pins			+0.2	μA
			Other pins			+0.5	
Output leakage current, low	I _{LOL1}	V _O = 0 V	Analog pins			-0.2	μA
			Other pins			-0.5	

Note 1. For flash memory product, specification of FLMD0 is as follows:

Input leakage current, high: 2 μA

Input leakage current, low: -2 μA

(3) Supply current

Supply current (V850ES/FE2: μ PD70F3231)

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Flash memory products supply current ^{Note 1}	I _{DD1}	Normal operation	f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions operating		25	40	mA
			f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions stopped		20		mA
	I _{DD2}	HALT mode	f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions operating		14	24	mA
			f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions stopped		9		mA
	I _{DD3}	IDLE1 mode	f _{xx} = 5 MHz (OSC = 5 MHz), PLL off		0.6	0.9	mA
	I _{DD4}	IDLE2 mode	f _{xx} = 5 MHz (OSC = 5 MHz), PLL off		0.25	0.7	mA
	I _{DD5}	Subclock operation mode ^{Notes 2, 3}	Crystal resonator f _{XT} = 32.768 kHz		200	400	μ A
			RC resonator ^{Note 4} f _{XT} = 40 kHz		200	400	μ A
	I _{DD6}	Sub-IDLE mode ^{Notes 2, 3}	Crystal resonator f _{XT} = 32.768 kHz		20	120	μ A
			RC resonator ^{Note 4} f _{XT} = 40 kHz		35	140	μ A
	I _{DD7}	Stop mode ^{Notes 2, 5}	POC stopped, Ring-OSC stopped		7	50	μ A
			POC operating, Ring-OSC stopped		10	55	μ A
			POC stopped, Ring-OSC operating		15	65	μ A
			POC operating, Ring-OSC operating		18	70	μ A

Notes 1. Total current of V_{DD} and EV_{DD} (all ports stopped). The current of AV_{REF0} and the port buffer current including the current flowing through the on-chip pull-up/pull-down resistors are not included.

2. When the main OSC is stopped.

3. POC operating, Ring-OSC operating.

4. The RC oscillation frequency is 40 kHz(TYP.). This clock is internally divided by 2.

5. When the sub-OSC is not used.

Supply current (V850ES/FE2: μ PD703231, μ PD703230)

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Mask ROM products supply current ^{Note 1}	I _{DD1}	Normal operation,	f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions operating		20	35	mA
			f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions stopped		16		mA
	I _{DD2}	HALT mode	f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions operating		12	22	mA
			f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions stopped		8		mA
	I _{DD3}	IDLE1 mode	f _{xx} = 5 MHz (OSC = 5 MHz), PLL off		0.25	0.7	mA
	I _{DD4}	IDLE2 mode	f _{xx} = 5 MHz (OSC = 5 MHz), PLL off		0.2	0.7	mA
	I _{DD5}	Subclock operation mode ^{Notes 2, 3}	Crystal resonator f _{XT} = 32.768 kHz		50	350	μ A
	I _{DD6}	Sub-IDLE mode ^{Notes 2, 3}	Crystal resonator f _{XT} = 32.768 kHz		20	120	μ A
			RC resonator f _{XT} = 40 kHz ^{Note 4}		35	140	μ A
	I _{DD7}	Stop mode ^{Notes 2, 5}	POC stopped, Ring-OSC stopped		7	50	μ A
			POC operating, Ring-OSC stopped		10	55	μ A
			POC stopped, Ring-OSC operating		15	65	μ A
			POC operating, Ring-OSC operating		18	70	μ A

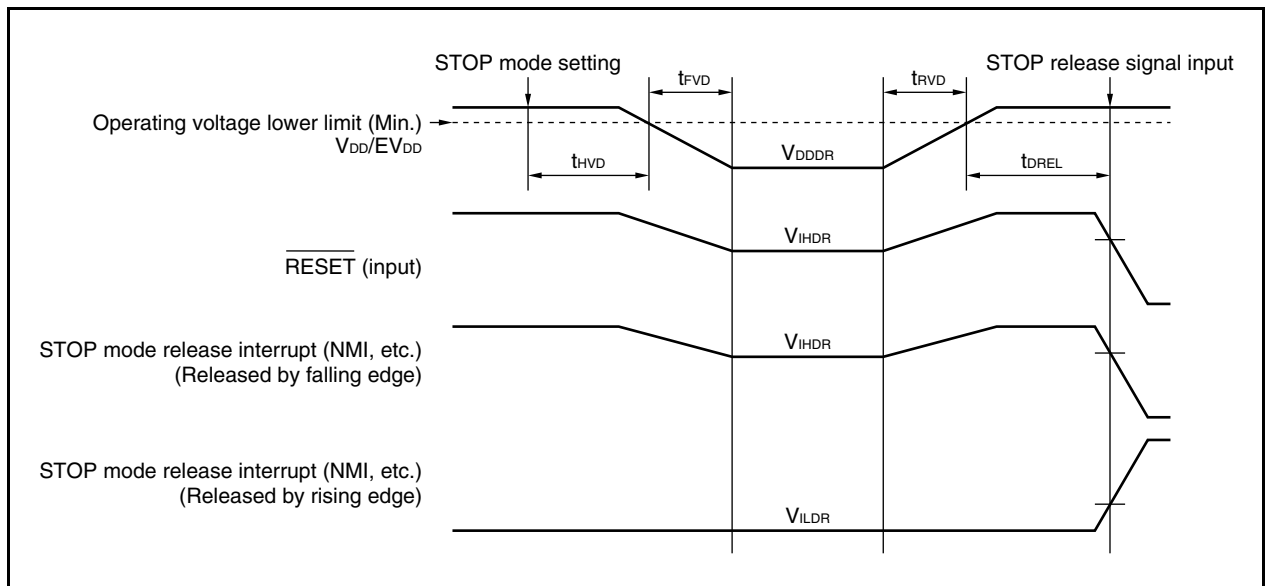
- Notes**
1. Total current of V_{DD} and EV_{DD} (all ports stopped). The current of AV_{REF0} and the port buffer current including the current flowing through the on-chip pull-up/pull-down resistors are not included.
 2. When the main OSC is stopped.
 3. POC operating, Ring-OSC operating.
 4. The RC oscillation frequency is 40 kHz (TYP.). This clock is internally divided by 2.
 5. When the sub-OSC is not used.

1.1.9 Data Retention Characteristics

STOP Mode ($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = 1.9$ V to 5.5 V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V)

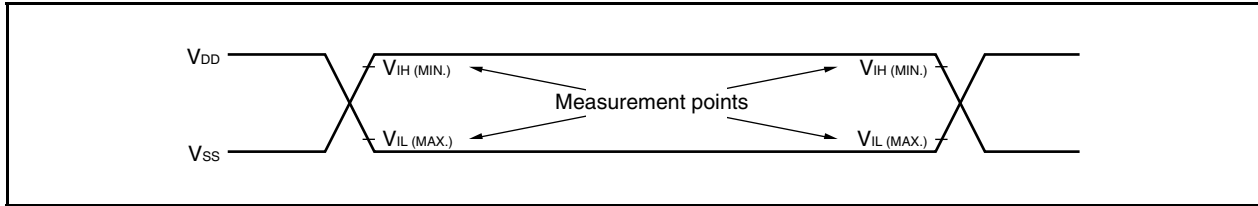
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}	In STOP mode	1.9		5.5	V
Data retention current	I_{DDDR}	$V_{DDDR} = 2.0$ V		6	45	μA
Supply voltage rise time	t_{rVD}		1			μs
Supply voltage fall time	t_{fVD}		1			μs
Supply voltage retention time	t_{HVD}	After STOP mode release	0			ms
STOP release signal input time	t_{DREL}	After V_{DD} reaches MIN.: 3.5 V	0			μs
Data retention input voltage, high	V_{IHDR}	All input ports	$0.9V_{DDDR}$		V_{DDDR}	V
Data retention input voltage, low	V_{ILDR}	All input ports	0		$0.1V_{DDDR}$	V

Caution Shifting to STOP mode and restoring from STOP mode must be performed within the rated operating range.

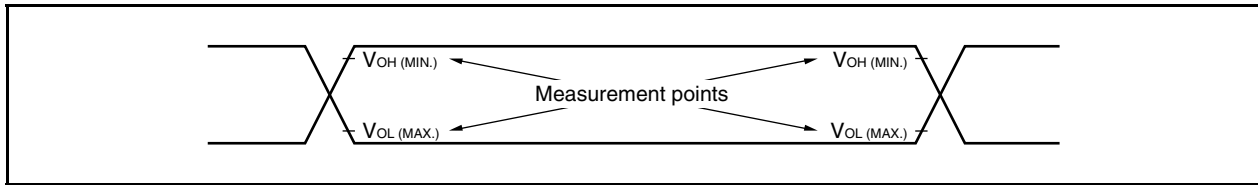


1.1.10 AC Characteristics

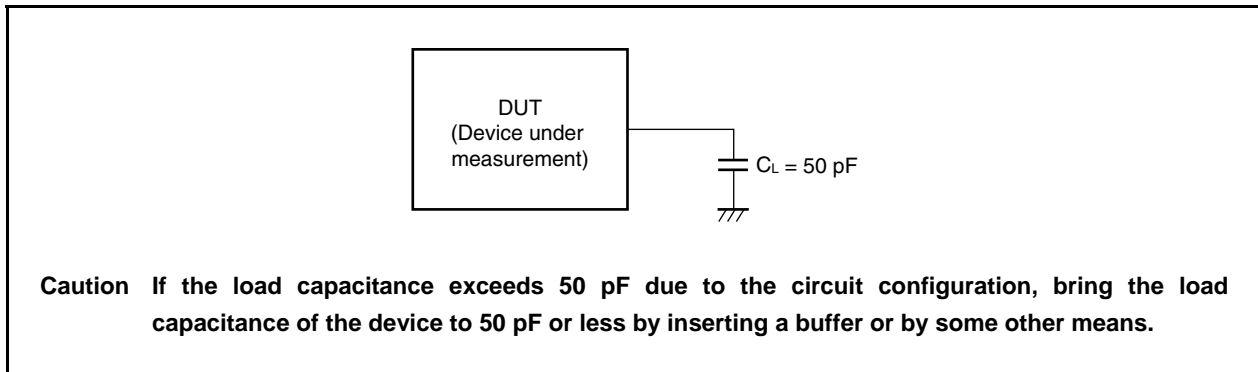
AC Test Input Measurement Points (V_{DD} , AV_{DD} , EV_{DD})



AC Test Output Measurement Points



Load Conditions

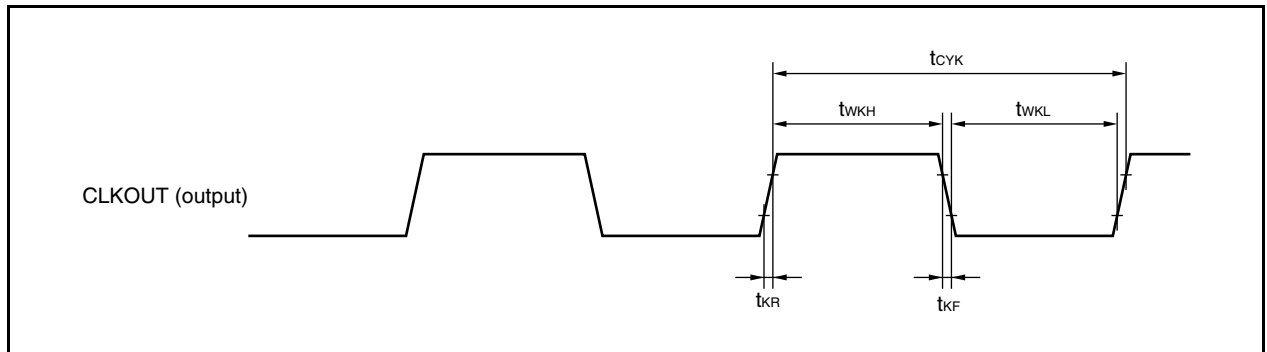


(1) CLKOUT output timing

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Output cycle	t_{CYK}		50 ns	80 μs	
High-level width	t_{WKH}		$t_{CYK}/2 - 15$		ns
Low-level width	t_{WKL}		$t_{CYK}/2 - 15$		ns
Rise time	t_{KR}			15	ns
Fall time	t_{KF}			15	ns

Clock Timing



(2) Basic Operation

(a) Reset, Interrupt timing

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = AV_{SS} = 0\text{ V}$, $C_L = 50\text{ pF}$)

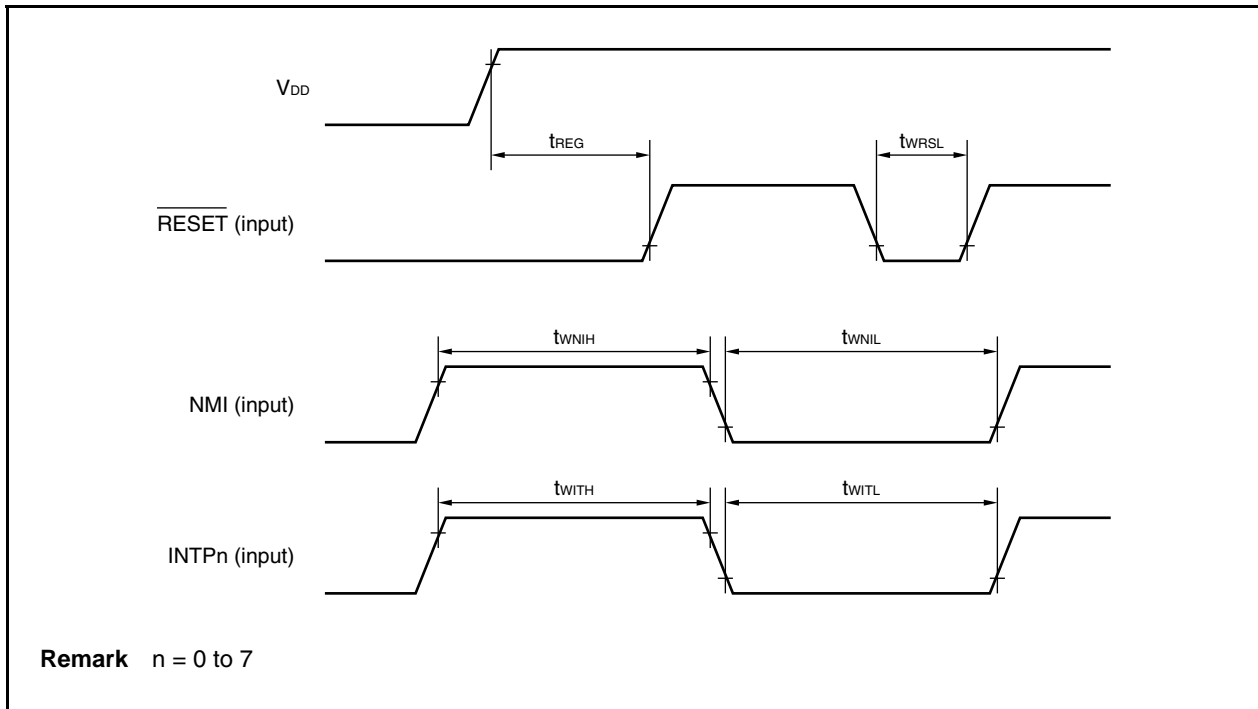
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ low-level width	t_{WRSL}		500		ns
NMI high-level width	t_{WNH}	Analog noise elimination	500		ns
NMI low-level width	t_{WNL}	Analog noise elimination	500		ns
INTP _n ^{Note 1} high-level width	t_{WITH}	Analog noise elimination (n = 0 to 7)	500		ns
		Digital noise elimination (n = 3)	Note 2		ns
INTP _n ^{Note 1} low-level width	t_{WITL}	Analog noise elimination (n = 0 to 7)	500		ns
		Digital noise elimination (n = 3)	Note 2		ns

Notes 1. ADTRG is same spec (P03/INTP0/ADTRG). $\overline{\text{DRST}}$ is same spec (P05/INTP2/DRST).

2. $2T_{\text{samp}} + 20$ or $3T_{\text{samp}} + 20$

T_{samp} : Sampling clock for noise elimination

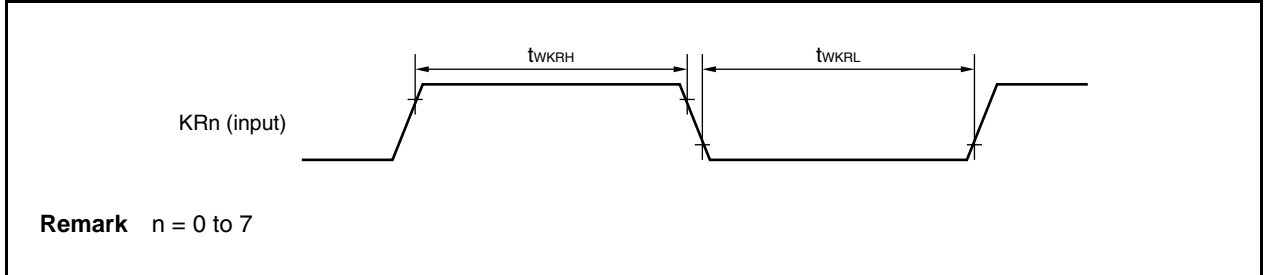
Reset/Interrupt



(b) Key return timing

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = AV_{SS} = 0\text{ V}$, $C_L = 50\text{ pF}$)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
KRn input high-level width	t_{WKRH}	Analog noise elimination ($n = 0$ to 7)	500		ns
KRn input low-level width	t_{WKRL}		500		ns



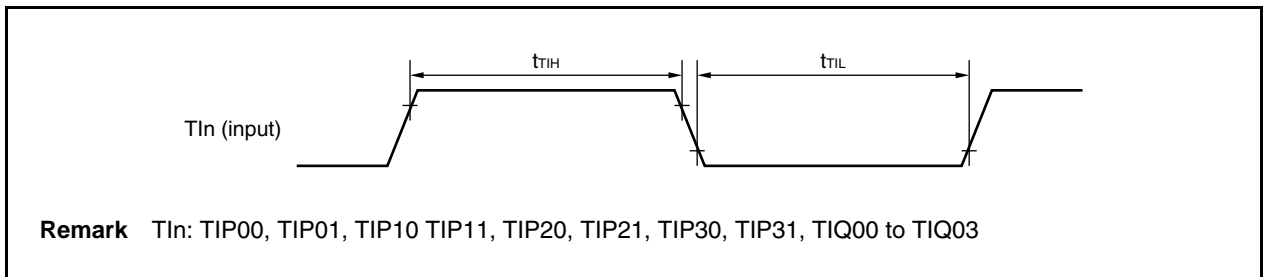
(c) Timer input timing

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = AV_{SS} = 0\text{ V}$, $C_L = 50\text{ pF}$)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
TIn high-level width	t_{TIH}	TIP00, TIP01, TIP10, TIP11, TIP20, TIP21, TIP30, TIP31, TIQ00 to TIQ03	Note		ns
TIn low-level width	t_{TIL}	TIQ03	Note		ns

Note $2T_{\text{samp}} + 20$ or $3T_{\text{samp}} + 20$

T_{samp} : Sampling clock for noise elimination



(d) CSIB timing

(i) Master mode

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
\overline{SCKBn} cycle time	t_{KCYn}		125		ns
\overline{SCKBn} high-level width	t_{KHn}		$t_{KCYn}/2 - 15$		ns
\overline{SCKBn} low-level width	t_{KLn}		$t_{KCYn}/2 - 15$		ns
SIBn setup time (to $\overline{SCKBn}\uparrow$)	t_{SIKn}		30		ns
SIBn hold time (from $\overline{SCKBn}\uparrow$)	t_{SIn}		25		ns
Output delay time from $\overline{SCKBn}\downarrow$ to SOBn	$t_{KSO n}$			25	ns

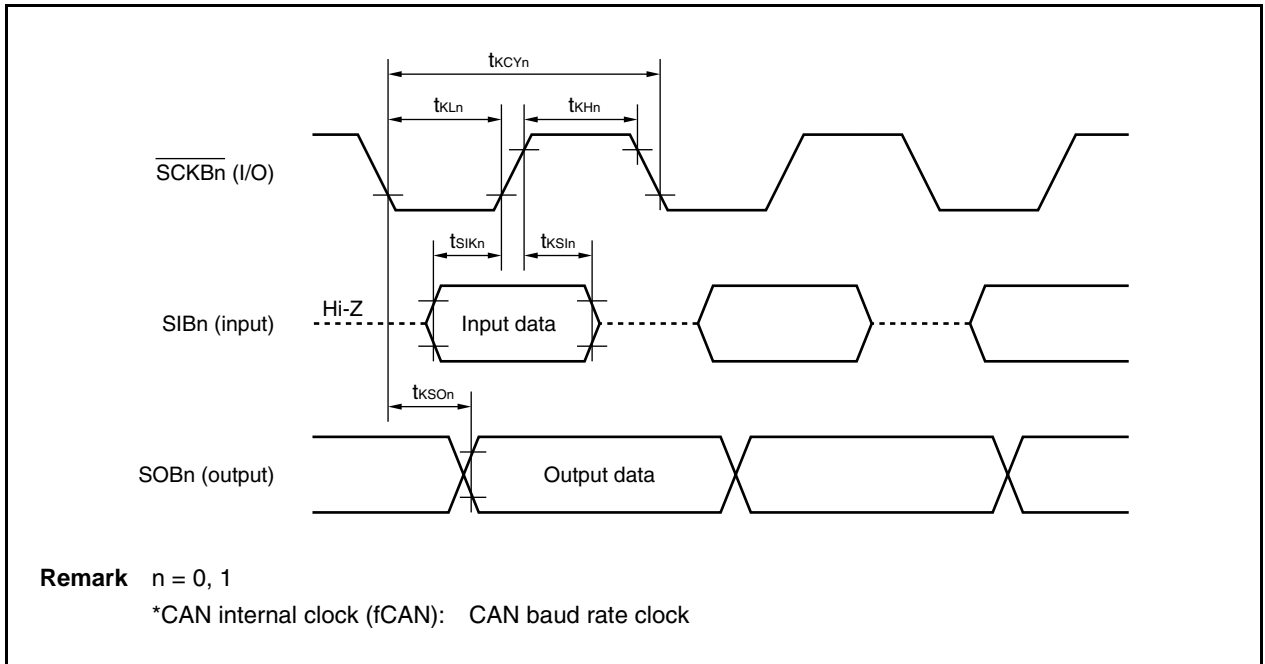
Remark n = 0, 1

(ii) Slave mode

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
\overline{SCKBn} cycle time	t_{KCYn}		200		ns
\overline{SCKBn} high-level width	t_{KHn}		90		ns
\overline{SCKBn} low-level width	t_{KLn}		90		ns
SIBn setup time (to $\overline{SCKBn}\uparrow$)	t_{SIKn}		50		ns
SIBn hold time (from $\overline{SCKBn}\uparrow$)	t_{SIn}		50		ns
Output delay time from $\overline{SCKBn}\downarrow$ to SOBn	$t_{KSO n}$			50	ns

Remark n = 0, 1



(e) UART timing

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V \leq $AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

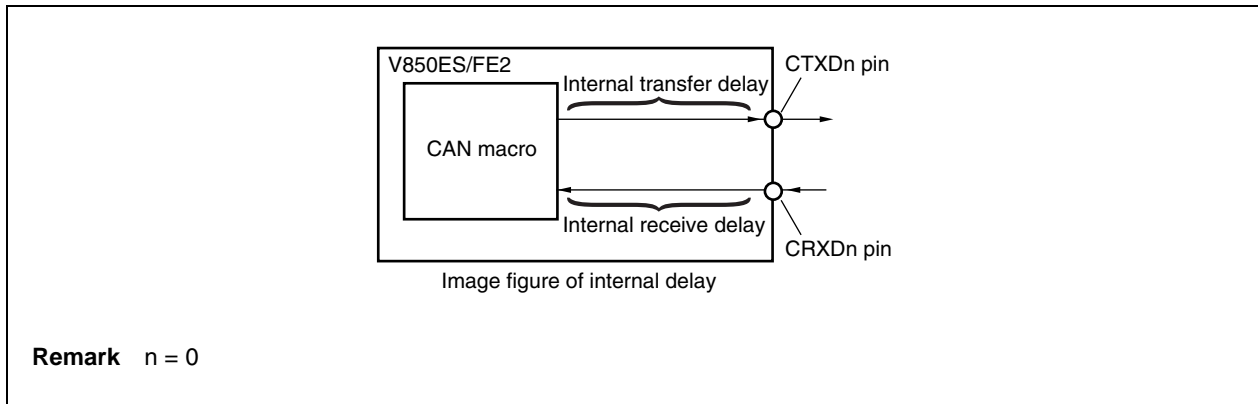
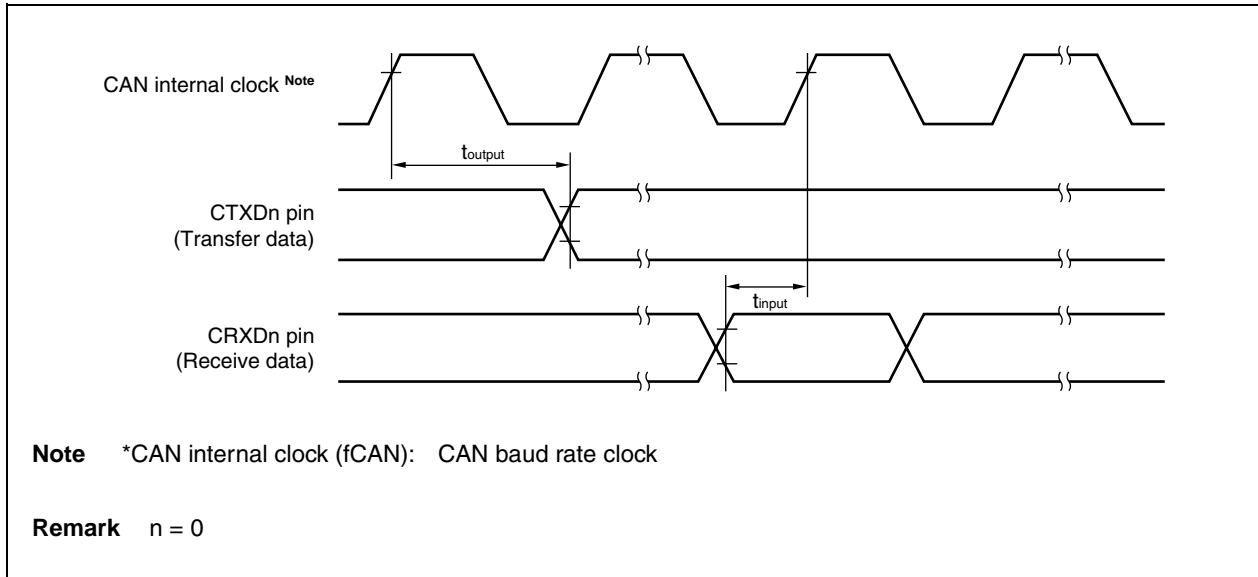
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Communication rate				312.5	kbps
ASCK0 cycle time				10	MHz

(f) CAN timing

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = AV_{SS} = 0\text{ V}$, $C_L = 50\text{ pF}$)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Transfer rate				1	Mbps
Internal delay time ^{Note}				100	ns

Note Internal delay time (t_{NODE}) = Internal transfer delay time (t_{OUTPUT}) + Internal receive delay time (t_{INPUT})



(g) A/D converter

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					10	bit
Overall error ^{Note}		$4.0 \leq AV_{REF0} \leq 5.5$ V		± 0.15	± 0.3	%FSR
Conversion time	t_{CONV}		3.1		16	μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF0}	V
AV _{REF0} current	I_{AREF0}	When using A/D converter		5	10	mA
		When not using A/D converter		1	10	μA

Note Excluding quantization error ($\pm 0.05\%$ FSR). Indicates the ratio to the full-scale value (%FSR).

Remark FSR: Full Scale Range

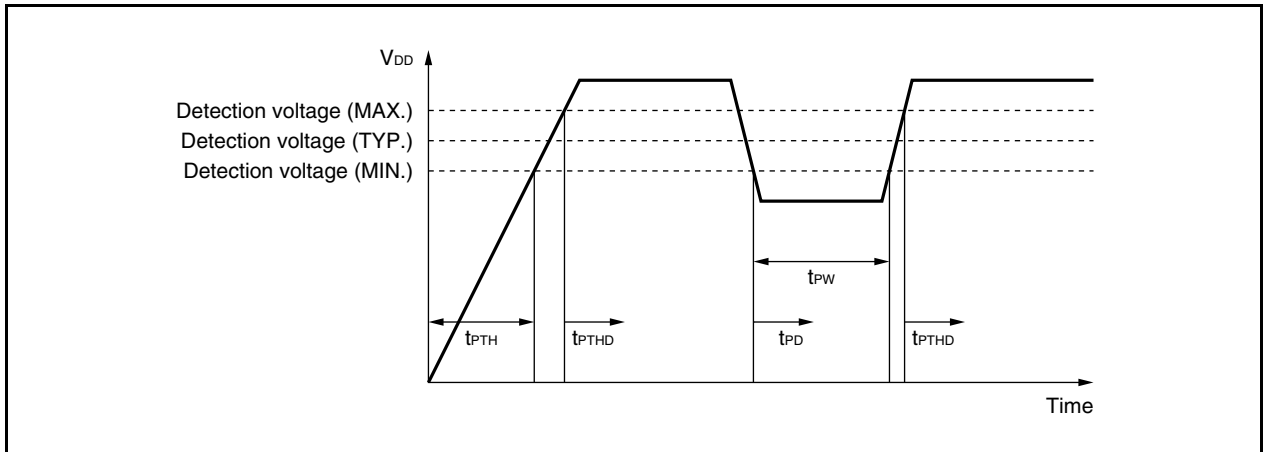
(h) POC circuit characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POC0}		3.5	3.7	3.9	V
Power supply startup time	t_{PTH}	$V_{DD} = 0$ V \rightarrow 3.5 V	0.002			ms
Response delay time 1 ^{Note 1}	t_{PTH0}	In case of power on. After V_{DD} reaches 3.9 V.			3.0	ms
Response delay time 2 ^{Note 2}	t_{PD}	In case of power off. After V_{DD} drops 3.5 V.			1	ms
Minimum V_{DD} width	t_{PW}		0.2			ms

Notes 1. From detect voltage to release reset signal.

2. From detect voltage to output reset signal.

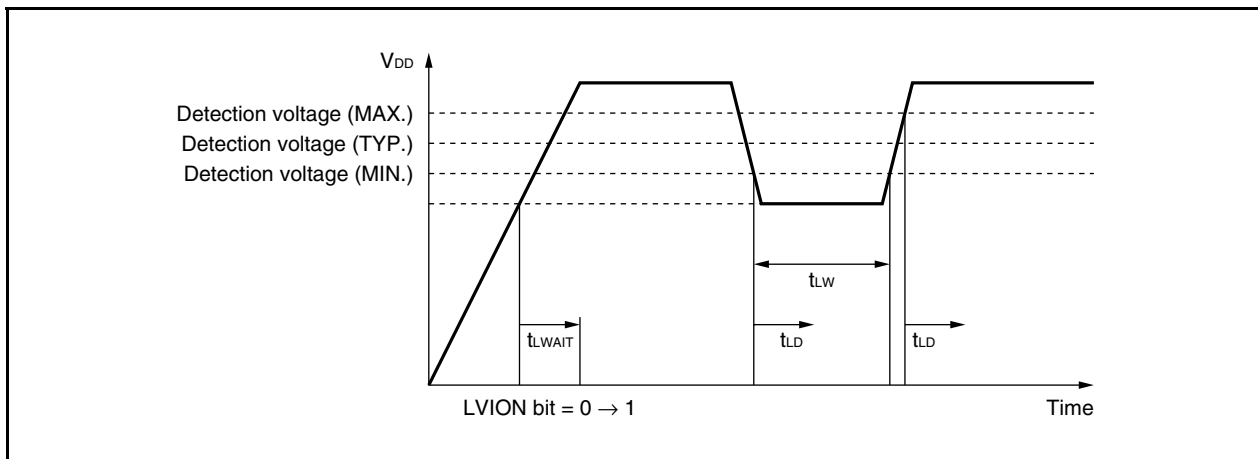


(i) LVI circuit characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = AV_{SS} = 0\text{ V}$, $C_L = 50\text{ pF}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{LV10}		4.2	4.4	4.6	V
	V_{LV11}		4.0	4.2	4.4	V
Response time ^{Note 1}	t_{LD}	After V_{DD} reaches V_{LV10}/V_{LV11} (Max.). After V_{DD} drops V_{LV10}/V_{LV11} (Min.).		0.2	2.0	ms
Minimum V_{DD} width	t_{LW}		0.2			ms
Reference voltage stabilization wait time ^{Note 2}	t_{LWAIT}	After V_{DD} reaches 3.5 V. After LVION bit (LVIM.bit7) = 0 \rightarrow 1		0.1	0.2	ms

- Notes**
1. The time required to output an interrupt/reset after the detection voltage is detected.
 2. Unnecessary when the POC function is used.

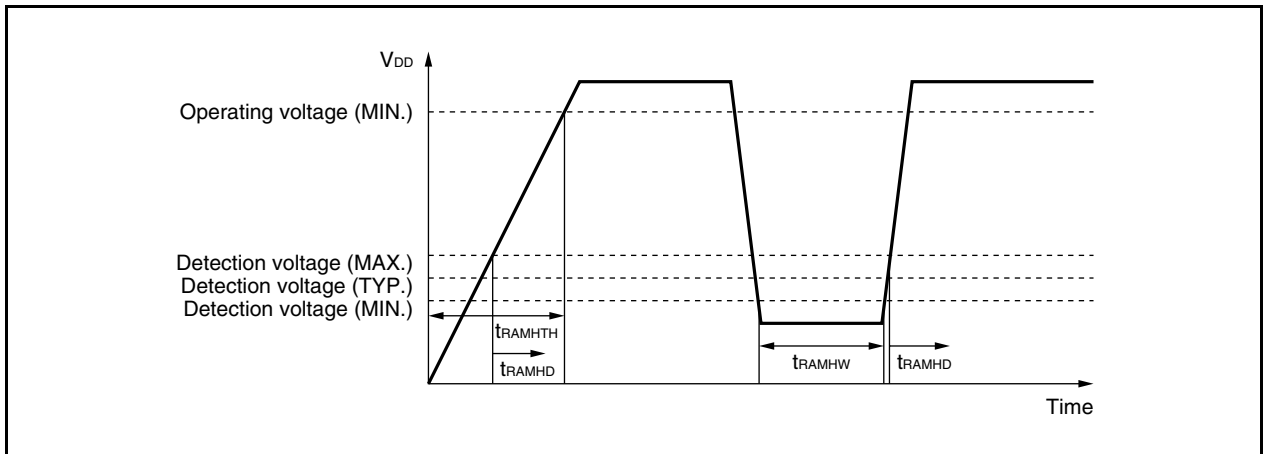


(j) RAM retention flag characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = 1.9$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{RAMH}		1.9	2.0	2.1	V
Supply voltage rise time	t_{RAMHTH}	$V_{DD} = 0$ V \rightarrow 3.5 V	0.002		1,800	ms
Response time ^{Note}	t_{RAMHD}	After the supply voltage reaches the detection voltage (MAX.)		0.2	2.0	ms
Minimum V_{DD} width	t_{RAMHW}		0.2			ms

Note Time required to set the RAMF bit after the detection voltage is detected.



(k) Flash memory programming characteristics

(i) Basic characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = AV_{SS} = 0\text{ V}$, $C_L = 50\text{ pF}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	f_{CPU}		4		20	MHz
Supply voltage	V_{DD}		3.5		5.5	V
Number of writes	C_{WRT} Note				100	Times
Input voltage, high	V_{IH}	FLMD0	$0.8EV_{DD}$		EV_{DD}	V
Input voltage, low	V_{IL}	FLMD0	EV_{SS}		$0.2EV_{DD}$	V
Write time + erase time	t_{WRT} + t_{ERASE}	Flash: 128 KB ($\mu\text{PD70F3231}$)			T.B.D	s
Programming temperature	t_{PRG}		-40		+85	$^\circ\text{C}$

Note The initial write when the product is shipped, any erase → write set of operations, or any programming operation is counted as one rewrite.

Example: P: Write, E: Erase

Shipped product → P → E → P → E → P: 3 rewrites

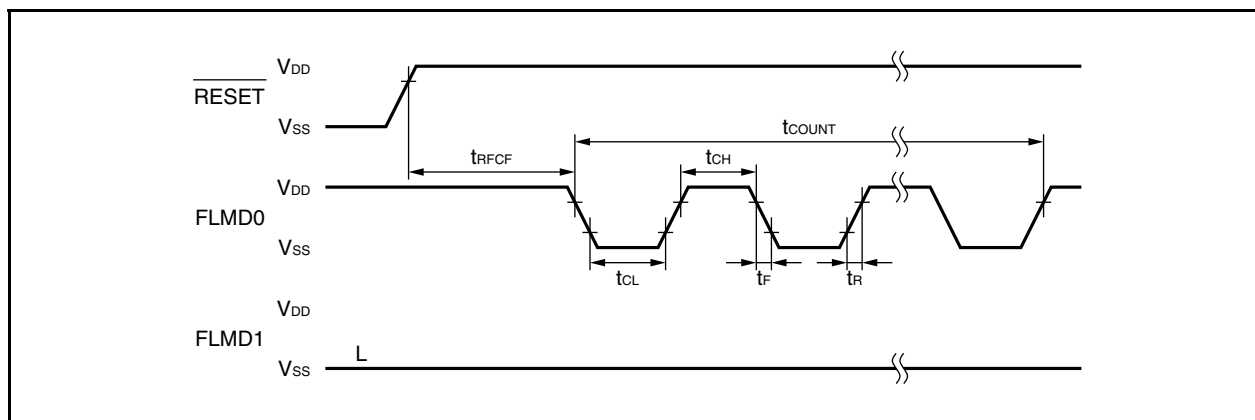
Shipped product → E → P → E → P → E → P: 3 rewrites

(ii) Serial Write Operation Characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = AV_{SS} = 0\text{ V}$, $C_L = 50\text{ pF}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
FLMD0 setup time from $\overline{\text{RESET}}\uparrow$	t_{RFCF}		$500/f_x + \alpha$			s
Count execution time	t_{COUNT}				3	ms
FLMD0 high-level width	t_{CH}		10		100	μs
FLMD0 low-level width	t_{CL}		10		100	μs
FLMD rise time	t_R				50	ns
FLMD fall time	t_F				50	ns

Note “ ” represents the oscillation stabilization time.



1.2 Electrical Specifications of (A1)-Grade

1.2.1 Absolute maximum ratings

Absolute Maximum Ratings (Flash memory product) (T_A = 25°C) (1/2)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{DD}	V _{DD} = EV _{DD}	-0.5 to +6.5	V
	EV _{DD}	V _{DD} = EV _{DD}	-0.5 to +6.5	V
	AV _{REF0}		-0.5 to +6.5	V
	V _{SS}	V _{SS} = EV _{SS} = AV _{SS}	-0.5 to +0.5	V
	AV _{SS}	V _{SS} = EV _{SS} = AV _{SS}	-0.5 to +0.5	V
	EV _{SS}	V _{SS} = EV _{SS} = AV _{SS}	-0.5 to +0.5	V
Input voltage	V _{I1}	P00 to P06, P30 to P35, P40 to P42, P50 to P55, P90, P91, P96 to P99, P913 to P915, RESET, FLMD0, PCMO, PCM1, PDL0 to PDL7	-0.5 to EV _{DD} + 0.5 ^{Note}	V
	V _{I3}	X1, X2, XT1, XT2	-0.5 to V _{RO} + 0.5 ^{Note}	V
Analog input voltage	V _{IAN}	P70 to P79	-0.5 to AV _{REF0} + 0.5 ^{Note}	V

Note Be sure not to exceed the absolute maximum ratings (MAX. value) of each supply voltage.

- Cautions**
1. Avoid direct connections among the IC device output (or I/O) pins and between V_{DD} or V_{CC} and GND.
 2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Absolute maximum ratings (Flash memory product) (T_A = 25°C) (2/2)

Parameter	Symbol	Conditions	Ratings	Unit	
Output current, low	I _{OL}	P00 to P06, P30 to P35, P40 to P42, P50 to P55, P90, P91, P96 to P99, P913 to P915, PCM0, PCM1 PDL0 to PDL7	Per pin	4	mA
			Total of all pins	50 ^{Note 1}	mA
		P70 to P79	Per pin	4	mA
			Total of all pins	20 ^{Note 2}	mA
Output current, high	I _{OH}	P00 to P06, P30 to P35, P40 to P42, P50 to P55, P90, P91, P96 to P99, P913 to P915, PCM0, PCM1 PDL0 to PDL7	Per pin	-4	mA
			Total of all pins	-50 ^{Note 1}	mA
		P70 to P79	Per pin	-4	mA
			Total of all pins	-20 ^{Note 2}	mA
Operating ambient temperature	T _A	Normal operating mode	-40 to +110	°C	
		Flash programming mode	-40 to +85		
Storage temperature	T _{stg}		-40 to +125	°C	

Notes 1. At T_A = 25°C. 20 mA/-20 mA at T_A = 110°C.

2. At T_A = 25°C. 10 mA/-10 mA at T_A = 110°C.

Cautions 1. Avoid direct connections among the IC device output (or I/O) pins and between V_{DD} or V_{CC} and GND.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Absolute Maximum Ratings (Mask ROM product) (T_A = 25°C) (1/2)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{DD}	V _{DD} = EV _{DD}	-0.5 to +6.5	V
	EV _{DD}	V _{DD} = EV _{DD}	-0.5 to +6.5	V
	AV _{REF0}		-0.5 to +6.5	V
	V _{SS}	V _{SS} = EV _{SS} = AV _{SS}	-0.5 to +0.5	V
	AV _{SS}	V _{SS} = EV _{SS} = AV _{SS}	-0.5 to +0.5	V
	EV _{SS}	V _{SS} = EV _{SS} = AV _{SS}	-0.5 to +0.5	V
Input voltage	V _{I1}	P00 to P06, P30 to P35, P40 to P42, P50 to P55, P90, P91, P96 to P99, P913 to P915, <u>RESET</u> , PCM0, PCM1, PDL0 to PDL7	-0.5 to EV _{DD} + 0.5 ^{Note}	V
	V _{I3}	X1, X2, XT1, XT2	-0.5 to V _{RO} + 0.5 ^{Note}	V
Analog input voltage	V _{IAN}	P70 to P79	-0.5 to AV _{REF0} + 0.5 ^{Note}	V

Note Be sure not to exceed the absolute maximum ratings (MAX. value) of each supply voltage.

- Cautions**
1. Avoid direct connections among the IC device output (or I/O) pins and between V_{DD} or V_{CC} and GND.
 2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Absolute maximum ratings (Mask ROM product) (T_A = 25°C) (2/2)

Parameter	Symbol	Conditions	Ratings	Unit	
Output current, low	I _{OL}	P00 to P06, P30 to P35, P40 to P42, P50 to P55, P90, P91, P96 to P99, P913 to P915, PCM0, PCM1 PDL0 to PDL7	Per pin	4	mA
			Total of all pins	50 ^{Note 1}	mA
		P70 to P79	Per pin	4	mA
			Total of all pins	20 ^{Note 2}	mA
Output current, high	I _{OH}	P00 to P06, P30 to P35, P40 to P42, P50 to P55, P90, P91, P96 to P99, P913 to P915, PCM0, PCM1 PDL0 to PDL7	Per pin	-4	mA
			Total of all pins	-50 ^{Note 1}	mA
		P70 to P79	Per pin	-4	mA
			Total of all pins	-20 ^{Note 2}	mA
Operating ambient temperature	T _A		-40 to +110	°C	
Storage temperature	T _{stg}		-65 to +150	°C	

- Notes 1.** At T_A = 25°C. 20 mA/-20 mA at T_A = 110°C.
2. At T_A = 25°C. 10 mA/-10 mA at T_A = 110°C.

- Cautions 1.** Avoid direct connections among the IC device output (or I/O) pins and between V_{DD} or V_{CC} and GND.
2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

1.2.2 Capacitance

($T_A = 25^\circ\text{C}$, $V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1} = V_{SS} = EV_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
I/O capacitance	C_{IO}	$f_x = 1\text{ MHz}$, Unmeasured pins returned to 0 V.			10	pF

1.2.3 Operating conditions

($T_A = -40\text{ to }+110^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Internal system clock frequency	f_{CLK}	REGC Capacity = 4.7 μF at operation with main clock	4		20	MHz
		REGC Capacity = 4.7 μF at operation with subclock (RC resonator)	12.5 ^{Note}		27.5 ^{Note}	kHz

Note The internal system clock frequency is half the oscillation frequency.

1.2.4 Oscillator Characteristics

Main clock oscillator characteristics

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit	
Ceramic resonator		Oscillation frequency (fx) ^{Note 1}		4		5	MHz	
		Oscillation stabilization time ^{Note 2}	After reset release		$2^{16}/f_x$		s	
			After STOP mode release	0.5 ^{Note 3}	Note 4		ms	
After IDLE2 mode release			0.35	Note 4		ms		
Crystal resonator			Oscillation frequency (fx) ^{Note 1}		4		5	MHz
			Oscillation stabilization time ^{Note 2}	After reset release		$2^{16}/f_x$		s
	After STOP mode release			0.5 ^{Note 3}	Note 4		ms	
After IDLE2 mode release	350			Note 4		μs		

Notes 1. Indicates only oscillator characteristics.

2. Time required to stabilize the crystal resonator after reset or STOP mode is released.
3. Time required to stabilize access to the internal flash memory.
4. The value differs depending on the OSTS register settings.

Cautions 1. When using the main clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
 - Do not cross the wiring with the other signal lines.
 - Do not route the wiring near a signal line through which a high fluctuating current flows.
 - Always make the ground point of the oscillator capacitor the same potential as V_{SS}.
 - Do not ground the capacitor to a ground pattern through which a high current flows.
 - Do not fetch signals from the oscillator.
2. When the main clock is stopped and the device is operating on the subclock, wait until the oscillation stabilization time has been secured by the program before switching back to the main clock.

Subclock Oscillator Characteristics

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = AV_{SS} = 0\text{ V}$)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
RC resonator		Oscillation frequency (f_{XT}) <small>Notes^{1, 4}</small>	$R = 390\text{ k}\Omega \pm 5\%$ <small>Note³</small> $C = 47\text{ pF} \pm 10\%$ <small>Note³</small>	25	40	55	kHz
		Oscillation stabilization time <small>Note²</small>				100	μs

- Notes**
- Indicates only oscillator characteristics. Refer to **26. 2. 10 AC Characteristics** for CPU operating clock.
 - Time required from when V_{DD} reaches oscillation voltage range (MIN.: 3.5 V) to when the crystal resonator stabilizes.
 - In order to avoid the influence of wiring capacity, shorten wiring as much as possible.
 - RC oscillation frequency is 40 kHz (Typ.). This clock is divided (1/2) internally. In case of RC oscillator, internal system clock frequency (f_{XT}) is 12.5 kHz (Min.), 20 kHz (Typ.), and 27.5 kHz (Max.).

Cautions 1. When using the subclock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
 - Do not cross the wiring with the other signal lines.
 - Do not route the wiring near a signal line through which a high fluctuating current flows.
 - Always make the ground point of the oscillator capacitor the same potential as V_{SS} .
 - Do not ground the capacitor to a ground pattern through which a high current flows.
 - Do not fetch signals from the oscillator.
2. The subclock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main clock oscillator. Particular care is therefore required with the wiring method when the subclock is used.

1.2.5 PLL Characteristics

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input frequency	f_x		4		5	MHz
Output frequency	f_{xx}		16		20	MHz
Lock time	t_{PLL}	After V_{DD} reaches MIN.: 3.5 V			800	μs

1.2.6 Ring-OSC Characteristics

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V)

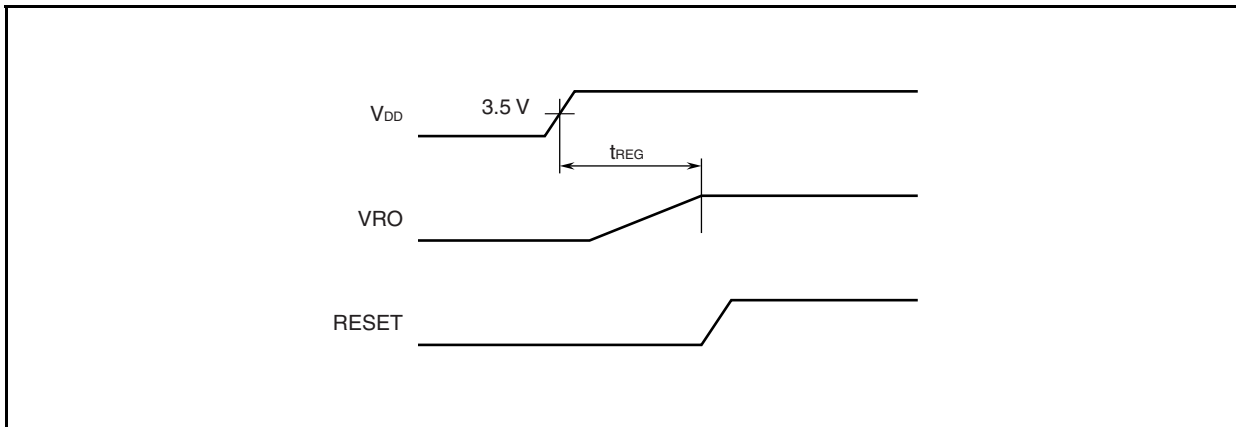
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output frequency	f_r		100	200	400	kHz

1.2.7 Voltage Regulator Characteristics

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD}$, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage	V_{DD}		3.5		5.5	V
Output voltage	V_{RO}			2.5		V
Lock time ^{Note 1}	t_{REG}	After V_{DD} reaches MIN.: 3.5 V Connect $C = 4.7 \mu\text{F} \pm 20\%$ to REGC pin			1	ms

Note 1. The lock time does not have to be considered for devices that have POC.



1.2.8 DC Characteristics

(1) Input/Output level

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V)

(1/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P30, P34, P41, P98, PCM0, PCM1, PDL0-PDL7	$0.7EV_{DD}$		EV_{DD}	V
	V_{IH2}	P00 to P06, P31 to P33, P35, P40, P42, P50 to P55, P90, P91, P96, P97, P99, P910, P913 to P915	$0.8EV_{DD}$		EV_{DD}	V
	V_{IH4}	P70 to P79	$0.7AV_{REF0}$		AV_{REF0}	V
	V_{IH5}	$\overline{\text{RESET}}$, FLMD0	$0.8EV_{DD}$		EV_{DD}	V
Input voltage, low	V_{IL1}	P30, P34, P41, P98, PCM0, PCM1, PDL0-PDL7	EV_{SS}		$0.3EV_{DD}$	V
	V_{IL2}	P00 to P06, P31 to P33, P35, P40, P42, P50 to P55, P90, P91, P96, P97, P99, P910, P913 to P915	EV_{SS}		$0.2EV_{DD}$	V
	V_{IL4}	P70 to P79	AV_{SS}		$0.3AV_{REF0}$	V
	V_{IL5}	$\overline{\text{RESET}}$, FLMD0	EV_{SS}		$0.2EV_{DD}$	V

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V)

(2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Output voltage, high <small>Note 1</small>	V _{OH1}	P00 to P06, P30 to P35, P40 to P42, P50 to P55, P90, P91, P96, P99, P913 to P915, PCM0, PCM1, PDL0 to PDL7	I _{OH} = -1.0 mA	EV _{DD} - 1.0		EV _{DD}	V
			I _{OH} = -0.1 mA	EV _{DD} - 0.5		EV _{DD}	V
	V _{OH3}	P70 to P79	I _{OH} = -1.0 mA	AV _{REF0} - 1.0		AV _{REF0}	V
			I _{OH} = -0.1 mA	AV _{REF0} - 0.5		AV _{REF0}	V
Output voltage, low <small>Note 1</small>	V _{OL1}	P00 to P06, P30 to P35, P40 to P42, P50 to P55, P90, P91, P96, P99, P913 to P915, PCM0, PCM1, PDL0 to PDL7	I _{OL} = 1.0 mA	0		0.4	V
			I _{OL} = 1.0 mA	0		0.4	V
Pull-up resistor	R ₁	V _I = 0 V	10	30	100	kΩ	
Pull-down resistor <small>Note 2</small>	R ₂	V _I = V _{DD}	10	30	100	kΩ	

Notes 1. Total I_{OH}/I_{OL} (Max.) is 20 mA/-20 mA each power supply terminal (EV_{DD} and AV_{REF0}).

2. When used as \overline{DRST} pin (Flash memory product only) (OCDM0 is the control register).

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

(2) Pin leakage current

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Input leakage current, high	I _{LIH1}	V _{IN} = V _{DD}	Analog pins			+0.3	μA
			Other pins ^{Note 1}			+2.0	
Input leakage current, low	I _{LIL1}	V _{IN} = 0 V	Analog pins			-0.3	μA
			Other pins ^{Note 1}			-2.0	
Output leakage current, high	I _{LOH1}	V _O = V _{DD}	Analog pins			+0.3	μA
			Other pins			+2.0	
Output leakage current, low	I _{LOL1}	V _O = 0 V	Analog pins			-0.2	μA
			Other pins			-2.0	

Note 1. For flash memory product, specification of FLMD0 is as follows:

Input leakage current, high: 4 μA

Input leakage current, low: -4 μA

(3) Supply current

Supply current (V850ES/FE2: μ PD70F3231)

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Flash memory products supply current ^{Note 1}	I _{DD1}	Normal operation	f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions operating		25	40	mA
			f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions stopped		20		mA
	I _{DD2}	HALT mode	f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions operating		14	26	mA
			f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions stopped		9		mA
	I _{DD3}	IDLE1 mode	f _{xx} = 5 MHz (OSC = 5 MHz), PLL off		0.6	1.2	mA
	I _{DD4}	IDLE2 mode	f _{xx} = 5 MHz (OSC = 5 MHz), PLL off		0.25	0.9	mA
	I _{DD5}	Subclock operation mode ^{Notes 2, 3}	RC resonator f _{XT} = 40 kHz ^{Note 4}		200	600	μ A
	I _{DD6}	Sub-IDLE mode ^{Notes 2, 3}	RC resonator f _{XT} = 40 kHz ^{Note 4}		35	340	μ A
	I _{DD7}	Stop mode ^{Notes 2, 5}	POC stopped, Ring-OSC stopped		7	250	μ A
			POC operating, Ring-OSC stopped		10	255	μ A
			POC stopped, Ring-OSC operating		15	265	μ A
			POC operating, Ring-OSC operating		18	270	μ A

- Notes**
1. Total current of V_{DD} and EV_{DD} (all ports stopped). The current of AV_{REF0} and the port buffer current including the current flowing through the on-chip pull-up/pull-down resistors are not included.
 2. When the main OSC is stopped.
 3. POC operating, Ring-OSC operating.
 4. The RC oscillation frequency is 40 kHz (TYP.). This clock is internally divided by 2.
 5. When the sub-OSC is not used.

Supply current (V850ES/FE2: μ PD703231, μ PD703230)

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Mask ROM products supply current ^{Note 1}	I _{DD1}	Normal operation,	f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions operating		20	35	mA
			f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions stopped		16		mA
	I _{DD2}	HALT mode	f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions operating		12	24	mA
			f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions stopped		8		mA
	I _{DD3}	IDLE1 mode	f _{xx} = 5 MHz (OSC = 5 MHz), PLL off		0.25	0.9	mA
	I _{DD4}	IDLE2 mode	f _{xx} = 5 MHz (OSC = 5 MHz), PLL off		0.2	0.9	mA
	I _{DD5}	Subclock operation mode ^{Notes 2, 3}	RC resonator f _{XT} = 40 kHz ^{Note 4}		50	550	μ A
	I _{DD6}	Sub-IDLE mode ^{Notes 2, 3}	RC resonator f _{XT} = 40 kHz ^{Note 4}		35	340	μ A
	I _{DD7}	Stop mode ^{Notes 2, 5}	POC stopped, Ring-OSC stopped		7	250	μ A
			POC operating, Ring-OSC stopped		10	255	μ A
			POC stopped, Ring-OSC operating		15	265	μ A
			POC operating, Ring-OSC operating		18	270	μ A

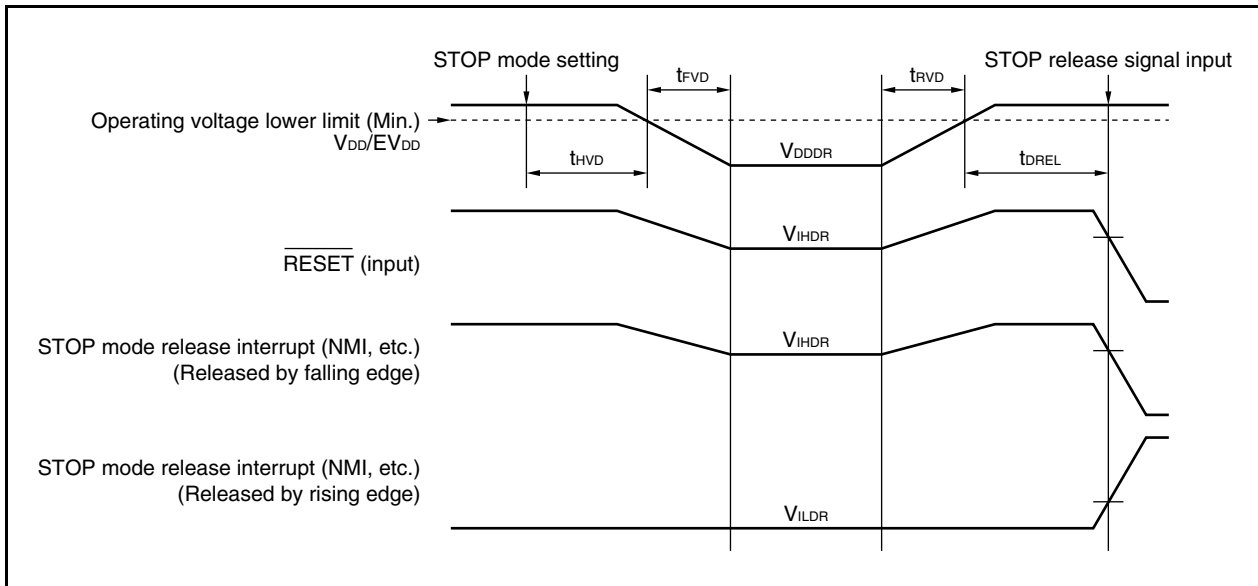
- Notes**
1. Total current of V_{DD} and EV_{DD} (all ports stopped). The current of AV_{REF0} and the port buffer current including the current flowing through the on-chip pull-up/pull-down resistors are not included.
 2. When the main OSC is stopped.
 3. POC operating, Ring-OSC operating.
 4. The RC oscillation frequency is 40 kHz(TYP.). This clock is internally divided by 2.
 5. When the sub-OSC is not used.

1.2.9 Data Retention Characteristics

STOP Mode ($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = 1.9$ V to 5.5 V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V)

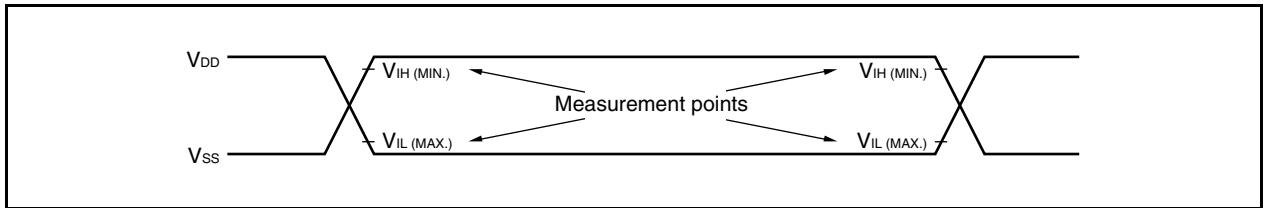
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}	In STOP mode	1.9		5.5	V
Data retention current	I_{DDDR}	$V_{DDDR} = 2.0$ V		6	230	μA
Supply voltage rise time	t_{rVD}		1			μs
Supply voltage fall time	t_{fVD}		1			μs
Supply voltage retention time	t_{HVD}	After STOP mode release	0			ms
STOP release signal input time	t_{DREL}	After V_{DD} reaches MIN.: 3.5 V	0			μs
Data retention input voltage, high	V_{IHDR}	All input ports	$0.9V_{DDDR}$		V_{DDDR}	V
Data retention input voltage, low	V_{ILDR}	All input ports	0		$0.1V_{DDDR}$	V

Caution Shifting to STOP mode and restoring from STOP mode must be performed within the rated operating range.

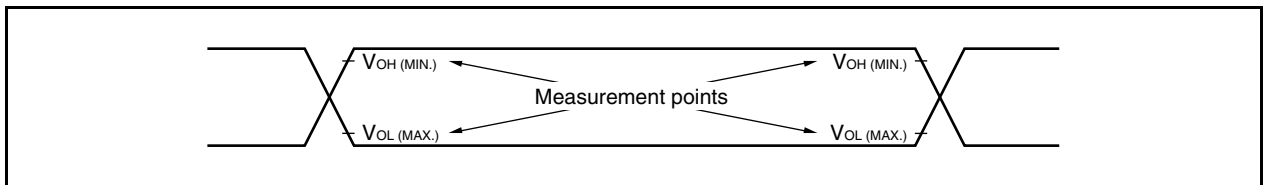


1.2.10 AC Characteristics

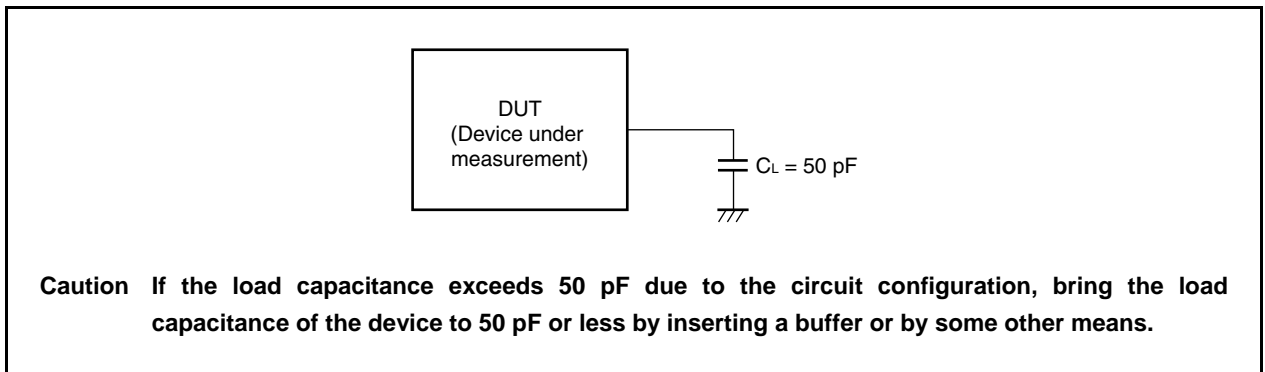
AC Test Input Measurement Points (V_{DD} , AV_{DD} , EV_{DD})



AC Test Output Measurement Points



Load Conditions

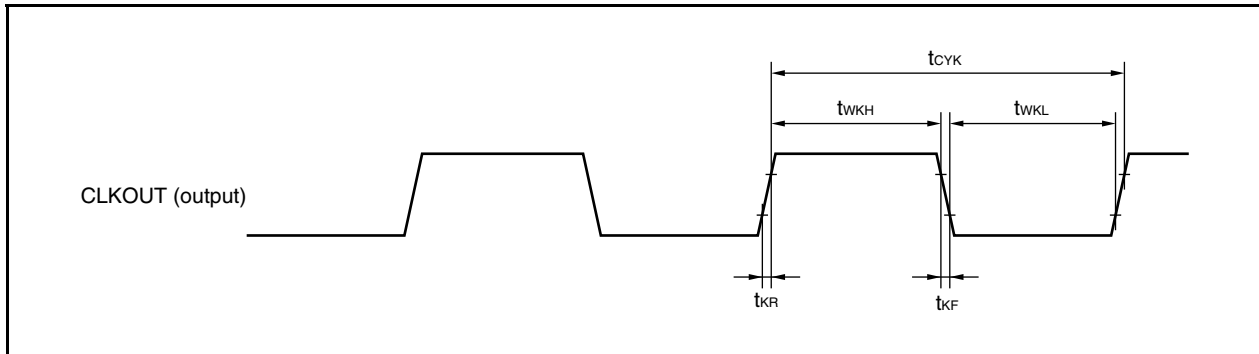


(1) CLKOUT output timing

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = AV_{SS} = 0\text{ V}$, $C_L = 50\text{ pF}$)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Output cycle	t_{CYK}		50 ns	80 μs	
High-level width	t_{WKH}		$t_{CYK}/2 - 15$		ns
Low-level width	t_{WKL}		$t_{CYK}/2 - 15$		ns
Rise time	t_{KR}			15	ns
Fall time	t_{KF}			15	ns

Clock Timing



(2) Basic Operation

(a) Reset, Interrupt timing

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V \leq $AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

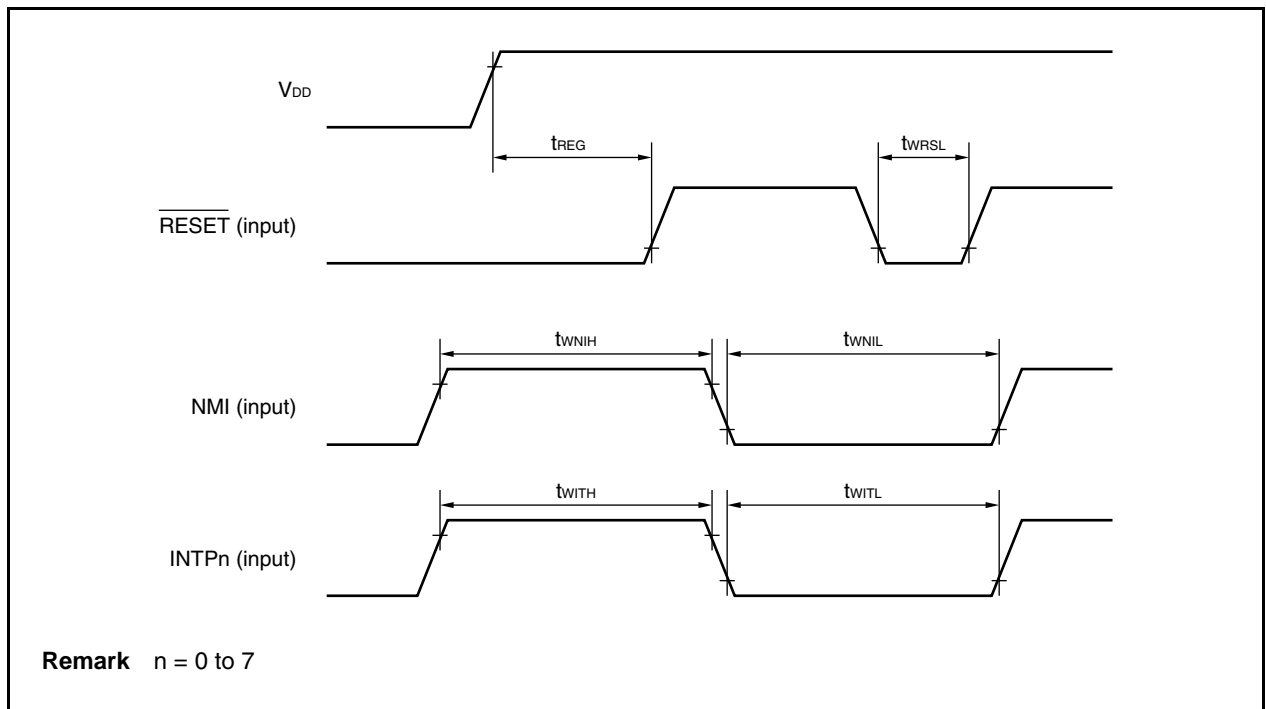
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
RESET low-level width	t_{WRSL}		500		ns
NMI high-level width	t_{WNIH}	Analog noise elimination	500		ns
NMI low-level width	t_{WNIL}	Analog noise elimination	500		ns
INTP _n ^{Note 1} high-level width	t_{WITH}	Analog noise elimination (n = 0 to 7)	500		ns
		Digital noise elimination (n = 3)	Note 2		ns
INTP _n ^{Note 1} low-level width	t_{WITL}	Analog noise elimination (n = 0 to 7)	500		ns
		Digital noise elimination (n = 3)	Note 2		ns

Notes 1. ADTRG is same spec (P03/INTP0/ADTRG). \overline{DRST} is same spec (P05/INTP2/DRST).

2. $2T_{\text{samp}} + 20$ or $3T_{\text{samp}} + 20$

T_{samp} : Sampling clock for noise elimination

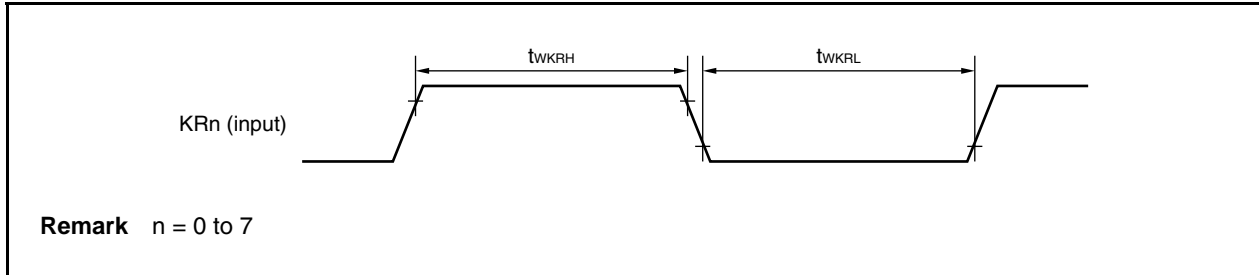
Reset/Interrupt



(b) Key return timing

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
KRn input high-level width	t_{WKRH}	Analog noise elimination ($n = 0$ to 7)	500		ns
KRn input low-level width	t_{WKRL}		500		ns

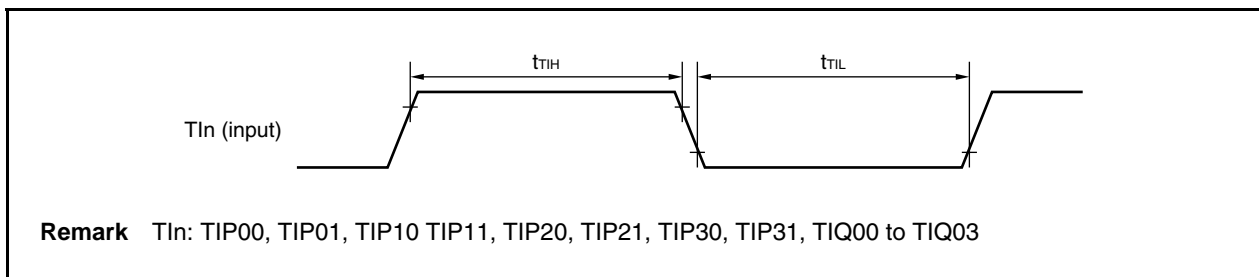


(c) Timer input timing

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
TIn high-level width	t_{TIH}	TIP00, TIP01, TIP10, TIP11, TIP20, TIP21, TIP30, TIP31, TIQ00 to TIQ03	Note		ns
TIn low-level width	t_{TIL}		Note		ns

Note $2T_{\text{samp}} + 20$ or $3T_{\text{samp}} + 20$
 T_{samp} : Sampling clock for noise elimination



(d) CSIB timing

(i) Master mode

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{SCKBn}}$ cycle time	t_{KCYn}		125		ns
$\overline{\text{SCKBn}}$ high-level width	t_{KHn}		$t_{\text{KCYn}}/2 - 15$		ns
$\overline{\text{SCKBn}}$ low-level width	t_{KLn}		$t_{\text{KCYn}}/2 - 15$		ns
SIBn setup time (to $\overline{\text{SCKBn}}\uparrow$)	t_{SIKn}		30		ns
SIBn hold time (from $\overline{\text{SCKBn}}\uparrow$)	t_{SIn}		25		ns
Output delay time from $\overline{\text{SCKBn}}\downarrow$ to SOBn	$t_{\text{KSO n}}$			25	ns

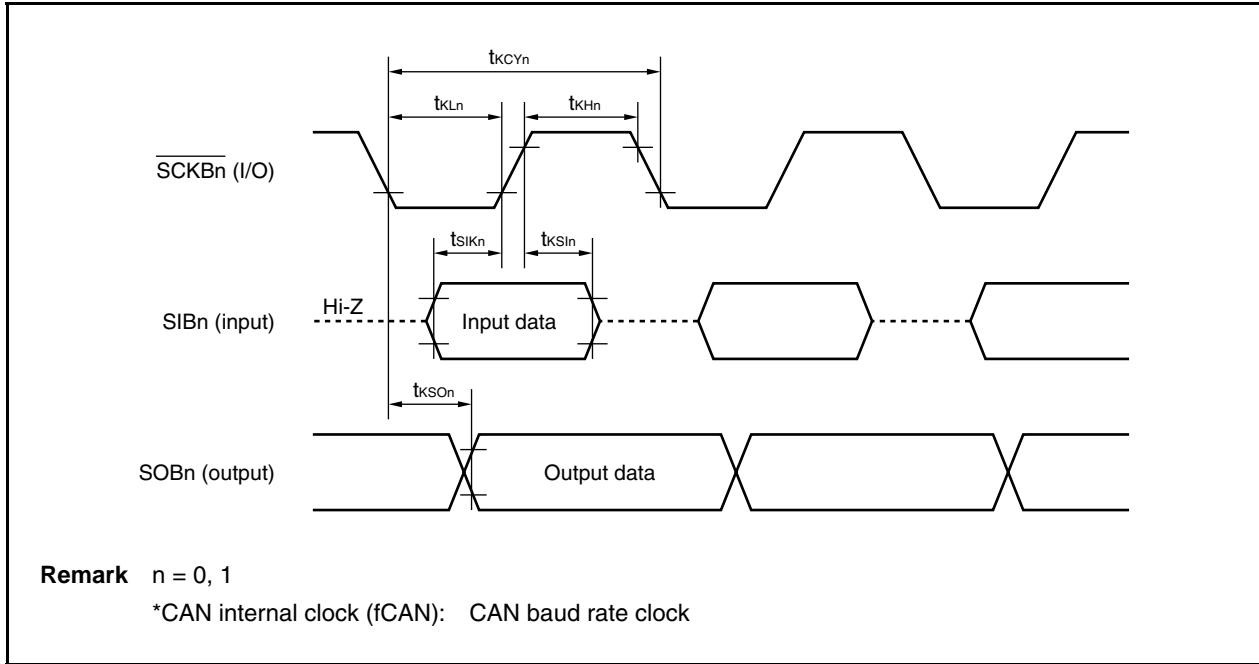
Remark n = 0, 1

(ii) Slave mode

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{SCKBn}}$ cycle time	t_{KCYn}		200		ns
$\overline{\text{SCKBn}}$ high-level width	t_{KHn}		90		ns
$\overline{\text{SCKBn}}$ low-level width	t_{KLn}		90		ns
SIBn setup time (to $\overline{\text{SCKBn}}\uparrow$)	t_{SIKn}		50		ns
SIBn hold time (from $\overline{\text{SCKBn}}\uparrow$)	t_{SIn}		50		ns
Output delay time from $\overline{\text{SCKBn}}\downarrow$ to SOBn	$t_{\text{KSO n}}$			50	ns

Remark n = 0, 1



(e) UART timing

($T_A = -40$ to $+110^\circ\text{C}$, $V_{\text{DD}} = \text{EV}_{\text{DD}} = 3.5$ V to 5.5 V, 4.0 V \leq $\text{AV}_{\text{REF0}} \leq 5.5$ V, $V_{\text{SS}} = \text{EV}_{\text{SS}} = \text{AV}_{\text{SS}} = 0$ V, $C_L = 50$ pF)

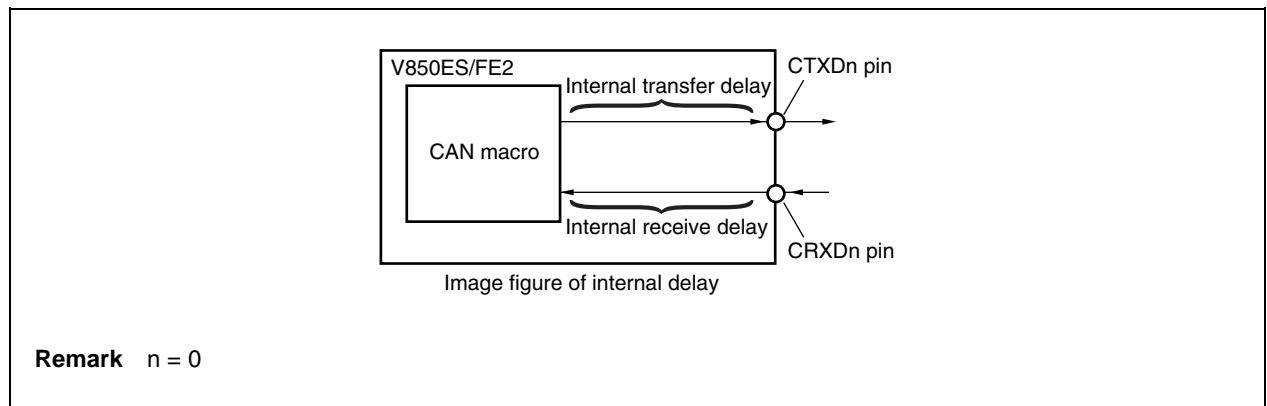
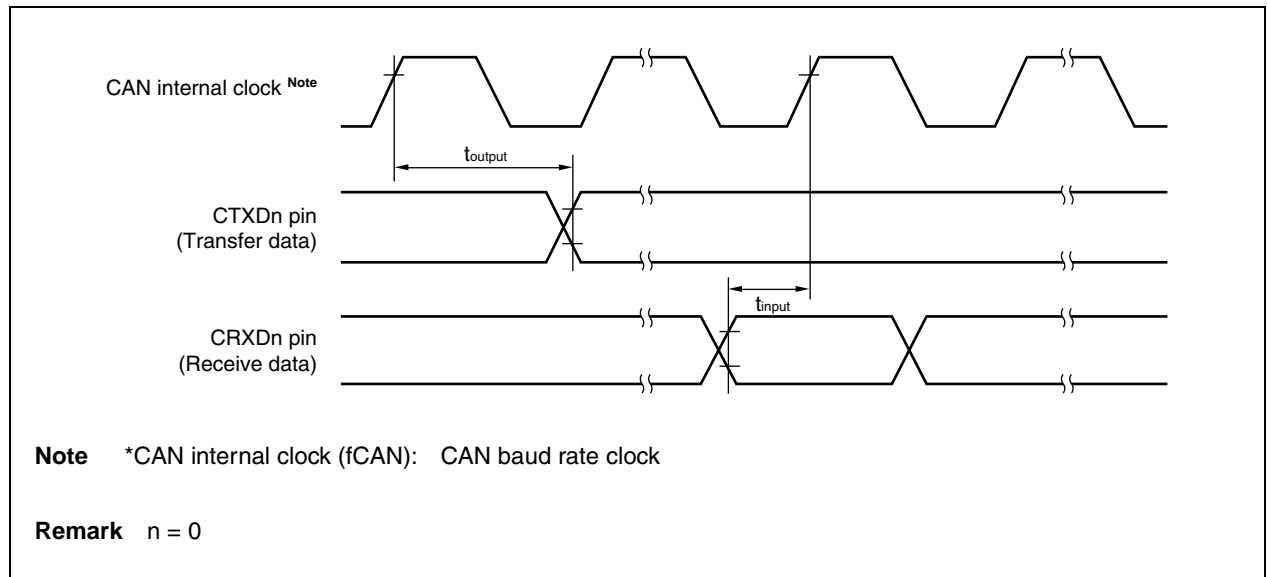
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Communication rate				312.5	kbps
ASCK0 cycle time				10	MHz

(f) CAN timing

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Transfer rate				1	Mbps
Internal delay time ^{Note}				100	ns

Note Internal delay time (t_{NODE}) = Internal transfer delay time (t_{OUTPUT}) + Internal receive delay time (t_{INPUT})



(g) A/D converter

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					10	bit
Overall error ^{Note}		$4.0 \leq AV_{REF0} \leq 5.5$ V		± 0.15	± 0.3	%FSR
Conversion time	t_{CONV}		3.1		16	μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF0}	V
AV _{REF0} current	I_{AREF0}	When using A/D converter		5	10	mA
		When not using A/D converter		1	10	μA

Note Excluding quantization error ($\pm 0.05\%$ FSR). Indicates the ratio to the full-scale value (%FSR).

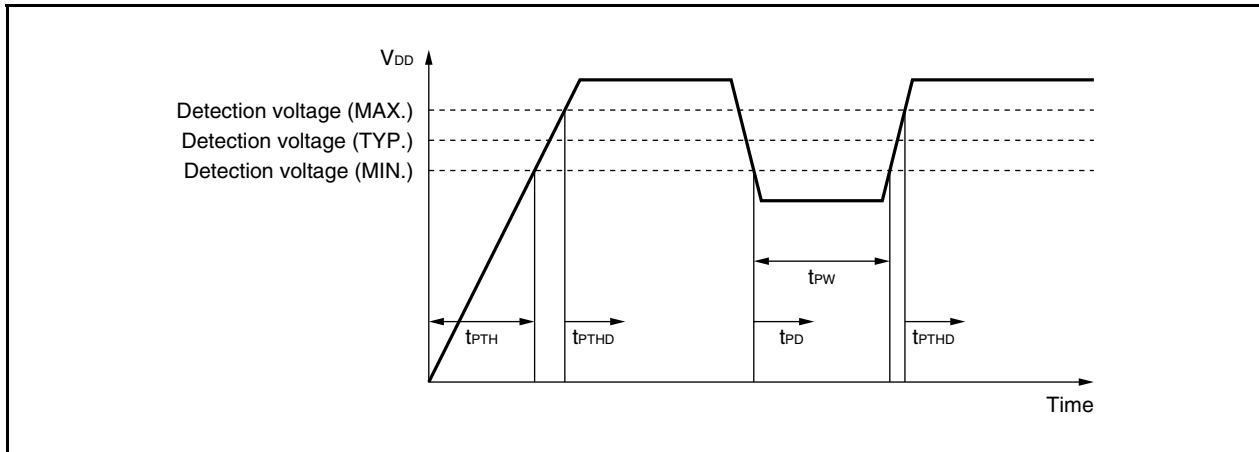
Remark FSR: Full Scale Range

(h) POC circuit characteristics

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POCO}		3.5	3.7	3.9	V
Power supply startup time	t_{PTH}	$V_{DD} = 0$ V \rightarrow 3.5 V	0.002			ms
Response delay time 1 ^{Note 1}	t_{PTHD}	In case of power on. After V_{DD} reaches 3.9 V.			3.0	ms
Response delay time 2 ^{Note 2}	t_{PD}	In case of power off. After V_{DD} drops 3.5 V.			1	ms
Minimum V_{DD} width	t_{PW}		0.2			ms

- Notes 1.** From detect voltage to release reset signal.
2. From detect voltage to output reset signal.

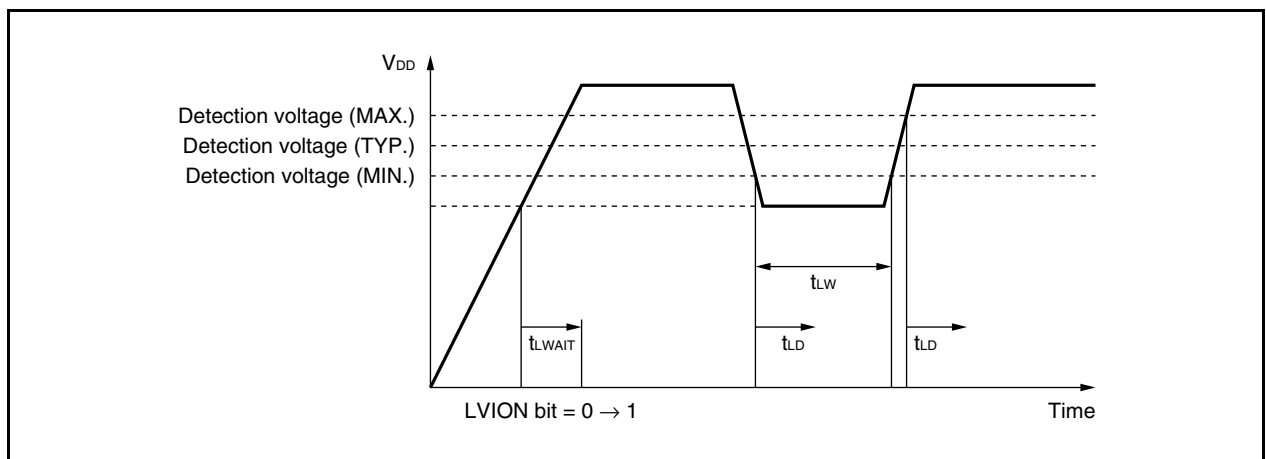


(i) LVI circuit characteristics

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{LV10}		4.2	4.4	4.6	V
	V_{LV11}		4.0	4.2	4.4	V
Response time ^{Note 1}	t_{LD}	After V_{DD} reaches V_{LV10}/V_{LV11} (Max.). After V_{DD} drops V_{LV10}/V_{LV11} (Min.).		0.2	2.0	ms
Minimum V_{DD} width	t_{LW}		0.2			ms
Reference voltage stabilization wait time ^{Note 2}	t_{LWAIT}	After V_{DD} reaches 3.5 V. After LVION bit (LVIM.bit7) = 0 \rightarrow 1		0.1	0.2	ms

- Notes**
1. The time required to output an interrupt/reset after the detection voltage is detected.
 2. Unnecessary when the POC function is used.

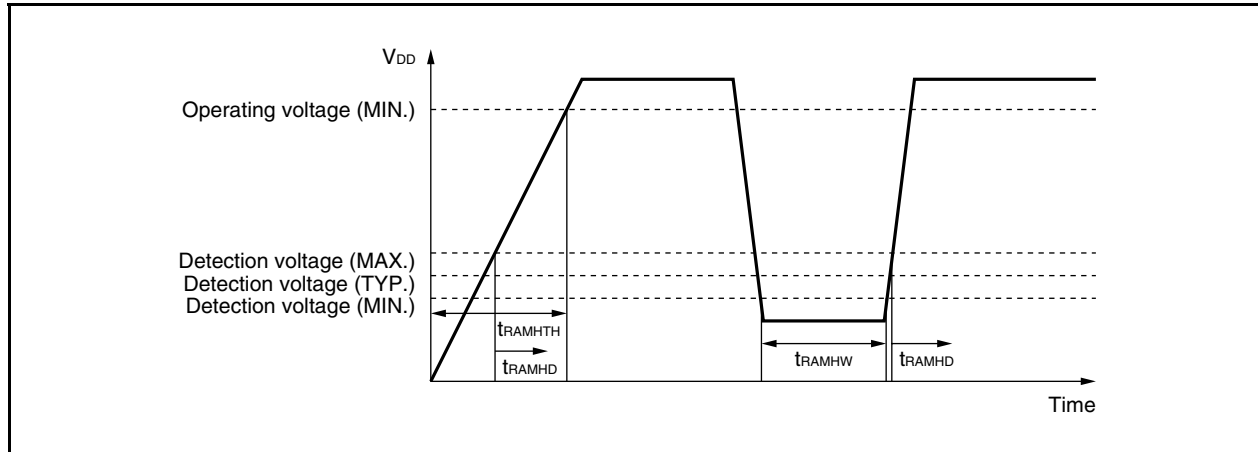


(j) RAM retention flag characteristics

($T_A = -40$ to $+110^\circ\text{C}$, $V_{DD} = EV_{DD} = 1.9$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{RAMH}		1.9	2.0	2.1	V
Supply voltage rise time	t_{RAMHTH}	$V_{DD} = 0$ V \rightarrow 3.5 V	0.002		1,800	ms
Response time ^{Note}	t_{RAMHD}	After the supply voltage reaches the detection voltage (MAX.)		0.2	2.0	ms
Minimum V_{DD} width	t_{RAMHW}		0.2			ms

Note Time required to set the RAMF bit after the detection voltage is detected.



(k) Flash memory programming characteristics

(i) Basic characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	f_{CPU}		4		20	MHz
Supply voltage	V_{DD}		3.5		5.5	V
Number of writes	C_{WRT} Note				100	Times
Input voltage, high	V_{IH}	FLMD0	$0.8EV_{DD}$		EV_{DD}	V
Input voltage, low	V_{IL}	FLMD0	EV_{SS}		$0.2EV_{DD}$	V
Write time + erase time	t_{WRT} + t_{ERASE}	Flash: 128 KB ($\mu\text{PD70F3231}$)			T.B.D	s
Programming temperature	t_{PRG}		-40		+85	$^\circ\text{C}$

Note The initial write when the product is shipped, any erase → write set of operations, or any programming operation is counted as one rewrite.

Example: P: Write, E: Erase

Shipped product → P → E → P → E → P: 3 rewrites

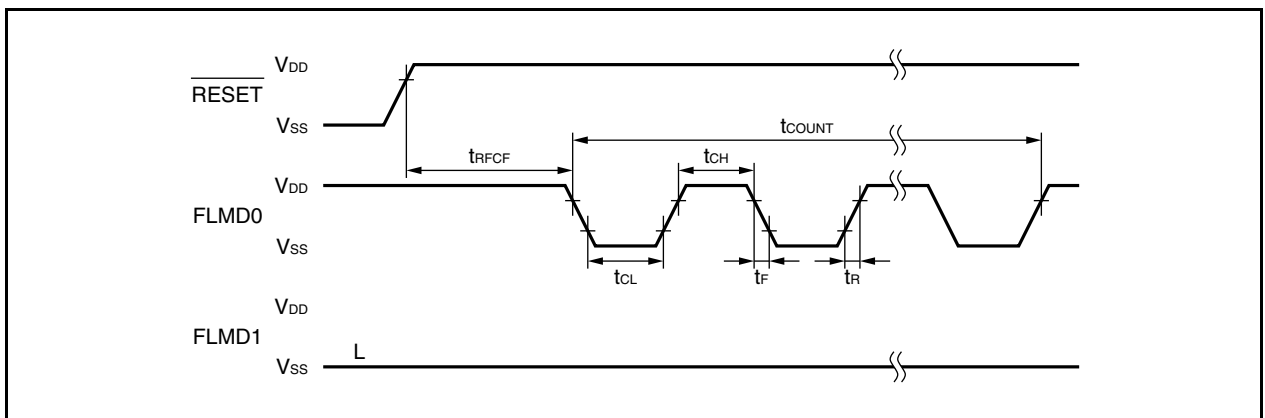
Shipped product → E → P → E → P → E → P: 3 rewrites

(ii) Serial Write Operation Characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
FLMD0 setup time from $\overline{\text{RESET}}\uparrow$	t_{RFCF}		$500/f_x + \alpha$			s
Count execution time	t_{COUNT}				3	ms
FLMD0 high-level width	t_{CH}		10		100	μs
FLMD0 low-level width	t_{CL}		10		100	μs
FLMD rise time	t_R				50	ns
FLMD fall time	t_F				50	ns

Note “ ” represents the oscillation stabilization time.



1.3 Electrical Specifications of (A2)-Grade

1.3.1 Absolute maximum ratings

Absolute Maximum Ratings (Flash memory product) (T_A = 25°C) (1/2)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{DD}	V _{DD} = EV _{DD}	-0.5 to +6.5	V
	EV _{DD}	V _{DD} = EV _{DD}	-0.5 to +6.5	V
	AV _{REF0}		-0.5 to +6.5	V
	V _{SS}	V _{SS} = EV _{SS} = AV _{SS}	-0.5 to +0.5	V
	AV _{SS}	V _{SS} = EV _{SS} = AV _{SS}	-0.5 to +0.5	V
	EV _{SS}	V _{SS} = EV _{SS} = AV _{SS}	-0.5 to +0.5	V
Input voltage	V _{I1}	P00 to P06, P30 to P35, P40 to P42, P50 to P55, P90, P91, P96 to P99, P913 to P915, $\overline{\text{RESET}}$, FLMD0, PCM0, PCM1, PDL0 to PDL7	-0.5 to EV _{DD} + 0.5 ^{Note}	V
	V _{I3}	X1, X2, XT1, XT2	-0.5 to V _{RO} + 0.5 ^{Note}	V
Analog input voltage	V _{IAN}	P70 to P79	-0.5 to AV _{REF0} + 0.5 ^{Note}	V

Note Be sure not to exceed the absolute maximum ratings (MAX. value) of each supply voltage.

- Cautions**
1. Avoid direct connections among the IC device output (or I/O) pins and between V_{DD} or V_{CC} and GND.
 2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Absolute maximum ratings (Flash memory product) (T_A = 25°C) (2/2)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, low	I _{OL}	P00 to P06, P30 to P35, P40 to P42, P50 to P55, P90, P91, P96 to P99, P913 to P915, PCM0, PCM1 PDL0 to PDL7	Per pin	4	mA
			Total of all pins	50 ^{Note 1}	mA
		P70 to P79	Per pin	4	mA
			Total of all pins	20 ^{Note 2}	mA
Output current, high	I _{OH}	P00 to P06, P30 to P35, P40 to P42, P50 to P55, P90, P91, P96 to P99, P913 to P915, PCM0, PCM1 PDL0 to PDL7	Per pin	-4	mA
			Total of all pins	-50 ^{Note 1}	mA
		P70 to P79	Per pin	-4	mA
			Total of all pins	-20 ^{Note 2}	mA
Operating ambient temperature	T _A	Normal operating mode	-40 to +125		°C
		Flash programming mode	-40 to +85		
Storage temperature	T _{stg}			-40 to +125	°C

Notes 1. At T_A = 25°C. 20 mA/-20 mA at T_A = 125°C.

2. At T_A = 25°C. 10 mA/-10 mA at T_A = 125°C.

- Cautions 1.** Avoid direct connections among the IC device output (or I/O) pins and between V_{DD} or V_{CC} and GND.
- 2.** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Absolute Maximum Ratings (Mask ROM product) (T_A = 25°C) (1/2)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{DD}	V _{DD} = EV _{DD}	-0.5 to +6.5	V
	EV _{DD}	V _{DD} = EV _{DD}	-0.5 to +6.5	V
	AV _{REF0}		-0.5 to +6.5	V
	V _{SS}	V _{SS} = EV _{SS} = AV _{SS}	-0.5 to +0.5	V
	AV _{SS}	V _{SS} = EV _{SS} = AV _{SS}	-0.5 to +0.5	V
	EV _{SS}	V _{SS} = EV _{SS} = AV _{SS}	-0.5 to +0.5	V
Input voltage	V _{I1}	P00 to P06, P30 to P35, P40 to P42, P50 to P55, P90, P91, P96 to P99, P913 to P915, RESET, PCM0, PCM1, PDL0 to PDL7	-0.5 to EV _{DD} + 0.5 ^{Note}	V
	V _{I3}	X1, X2, XT1, XT2	-0.5 to V _{RO} + 0.5 ^{Note}	V
Analog input voltage	V _{IAN}	P70 to P79	-0.5 to AV _{REF0} + 0.5 ^{Note}	V

Note Be sure not to exceed the absolute maximum ratings (MAX. value) of each supply voltage.

- Cautions**
1. Avoid direct connections among the IC device output (or I/O) pins and between V_{DD} or V_{CC} and GND.
 2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Absolute maximum ratings (Mask ROM product) (T_A = 25°C) (2/2)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, low	I _{OL}	P00 to P06, P30 to P35, P40 to P42, P50 to P55, P90, P91, P96 to P99, P913 to P915, PCM0, PCM1 PDL0 to PDL7	Per pin	4	mA
			Total of all pins	50 ^{Note 1}	mA
		P70 to P79	Per pin	4	mA
			Total of all pins	20 ^{Note 2}	mA
Output current, high	I _{OH}	P00 to P06, P30 to P35, P40 to P42, P50 to P55, P90, P91, P96 to P99, P913 to P915, PCM0, PCM1 PDL0 to PDL7	Per pin	-4	mA
			Total of all pins	-50 ^{Note 1}	mA
		P70 to P79	Per pin	-4	mA
			Total of all pins	-20 ^{Note 2}	mA
Operating ambient temperature	T _A			-40 to +125	°C
Storage temperature	T _{stg}			-65 to +150	°C

- Notes**
- At T_A = 25°C. 20 mA/-20 mA at T_A = 125°C.
 - At T_A = 25°C. 10 mA/-10 mA at T_A = 125°C.

- Cautions**
- Avoid direct connections among the IC device output (or I/O) pins and between V_{DD} or V_{CC} and GND.
 - Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

1.3.2 Capacitance

($T_A = 25^\circ\text{C}$, $V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1} = V_{SS} = EV_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
I/O capacitance	C_{IO}	$f_x = 1\text{ MHz}$, Unmeasured pins returned to 0 V.			10	pF

1.3.3 Operating conditions

($T_A = -40\text{ to }+125^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Internal system clock frequency	f_{CLK}	REGC Capacity = $4.7\ \mu\text{F}$, at operation with main clock	4		20	MHz
		REGC Capacity = $4.7\ \mu\text{F}$, at operation with subclock (RC resonator)	12.5		27.5	kHz

Note The internal system clock frequency is half the oscillation frequency.

1.3.4 Oscillator Characteristics

Main clock oscillator characteristics

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = AV_{SS} = 0\text{ V}$)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (fx) ^{Note 1}		4		5	MHz
		Oscillation stabilization time ^{Note 2}	After reset release		$2^{16}/f_x$		s
			After STOP mode release	0.5 ^{Note 3}	Note 4		ms
After IDLE2 mode release	0.35	Note 4		ms			
Crystal resonator		Oscillation frequency (fx) ^{Note 1}		4		5	MHz
		Oscillation stabilization time ^{Note 2}	After reset release		$2^{16}/f_x$		s
			After STOP mode release	0.5 ^{Note 3}	Note 4		ms
After IDLE2 mode release	350	Note 4		μs			

- Notes**
1. Indicates only oscillator characteristics.
 2. Time required to stabilize the crystal resonator after reset or STOP mode is released.
 3. Time required to stabilize access to the internal flash memory.
 4. The value differs depending on the OSTS register settings.

Cautions 1. When using the main clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
 - Do not cross the wiring with the other signal lines.
 - Do not route the wiring near a signal line through which a high fluctuating current flows.
 - Always make the ground point of the oscillator capacitor the same potential as V_{SS} .
 - Do not ground the capacitor to a ground pattern through which a high current flows.
 - Do not fetch signals from the oscillator.
2. When the main clock is stopped and the device is operating on the subclock, wait until the oscillation stabilization time has been secured by the program before switching back to the main clock.

Subclock Oscillator Characteristics

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
RC resonator		Oscillation frequency (f_{XT}) Notes 1, 4	$R = 390\text{ k}\Omega \pm 5\%$ Note 3 $C = 47\text{ pF} \pm 10\%$ Note 3	25	40	55	kHz
		Oscillation stabilization time Note 2				100	μs

- Notes**
1. Indicates only oscillator characteristics. Refer to **26. 3. 10 AC Characteristics** for CPU operating clock.
 2. Time required from when V_{DD} reaches oscillation voltage range (MIN.: 3.5 V) to when the crystal resonator stabilizes.
 3. In order to avoid the influence of wiring capacity, shorten wiring as much as possible.
 4. RC oscillation frequency is 40 kHz (Typ.). This clock is divided (1/2) internally. In case of RC oscillator, internal system clock frequency (f_{XT}) is 12.5 kHz (Min.), 20 kHz (Typ.), and 27.5 kHz (Max.).

Cautions 1. When using the subclock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
 - Do not cross the wiring with the other signal lines.
 - Do not route the wiring near a signal line through which a high fluctuating current flows.
 - Always make the ground point of the oscillator capacitor the same potential as V_{SS} .
 - Do not ground the capacitor to a ground pattern through which a high current flows.
 - Do not fetch signals from the oscillator.
2. The subclock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main clock oscillator. Particular care is therefore required with the wiring method when the subclock is used.

1.3.5 PLL Characteristics

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input frequency	f_x		4		5	MHz
Output frequency	f_{xx}		16		20	MHz
Lock time	t_{PLL}	After V_{DD} reaches MIN.: 3.5 V			800	μs

1.3.6 Ring-OSC Characteristics

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V)

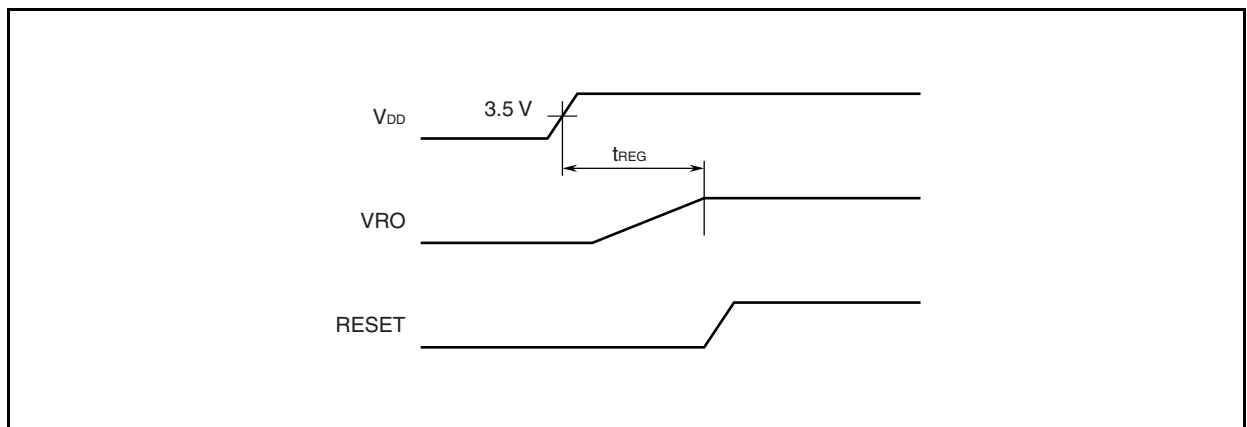
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output frequency	f_r		100	200	400	kHz

1.3.7 Voltage Regulator Characteristics

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD}$, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage	V_{DD}		3.5		5.5	V
Output voltage	V_{RO}			2.5		V
Lock time ^{Note 1}	t_{REG}	After V_{DD} reaches MIN.: 3.5 V Connect $C = 4.7$ mF $\pm 20\%$ to REGC pin			1	ms

Note 1. The lock time does not have to be considered for devices that have POC.



1.3.8 DC Characteristics

(1) Input/Output level

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V)

(1/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P30, P34, P41, P98, PCM0, PCM1, PDL0-PDL7	$0.7EV_{DD}$		EV_{DD}	V
	V_{IH2}	P00 to P06, P31 to P33, P35, P40, P42, P50 to P55, P90, P91, P96, P97, P99, P910, P913 to P915	$0.8EV_{DD}$		EV_{DD}	V
	V_{IH4}	P70 to P79	$0.7AV_{REF0}$		AV_{REF0}	V
	V_{IH5}	$\overline{\text{RESET}}$, FLMD0	$0.8EV_{DD}$		EV_{DD}	V
Input voltage, low	V_{IL1}	P30, P34, P41, P98, PCM0, PCM1, PDL0-PDL7	EV_{SS}		$0.3EV_{DD}$	V
	V_{IL2}	P00 to P06, P31 to P33, P35, P40, P42, P50 to P55, P90, P91, P96, P97, P99, P910, P913 to P915	EV_{SS}		$0.2EV_{DD}$	V
	V_{IL4}	P70 to P79	AV_{SS}		$0.3AV_{REF0}$	V
	V_{IL5}	$\overline{\text{RESET}}$, FLMD0	EV_{SS}		$0.2EV_{DD}$	V

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V)

(2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Output voltage, high <small>Note 1</small>	V _{OH1}	P00 to P06, P30 to P35, P40 to P42, P50 to P55, P90, P91, P96, P99, P913 to P915, PCM0, PCM1, PDL0 to PDL7	I _{OH} = -1.0 mA	EV _{DD} - 1.0		EV _{DD}	V
			I _{OH} = -0.1 mA	EV _{DD} - 0.5		EV _{DD}	V
	V _{OH3}	P70 to P79	I _{OH} = -1.0 mA	AV _{REF0} - 1.0		AV _{REF0}	V
			I _{OH} = -0.1 mA	AV _{REF0} - 0.5		AV _{REF0}	V
Output voltage, low <small>Note 1</small>	V _{OL1}	P00 to P06, P30 to P35, P40 to P42, P50 to P55, P90, P91, P96, P99, P913 to P915, PCM0, PCM1, PDL0 to PDL7	I _{OL} = 1.0 mA	0		0.4	V
			I _{OL} = 1.0 mA	0		0.4	V
	V _{OL3}	P70 to P79	I _{OL} = 1.0 mA	0		0.4	V
Pull-up resistor	R ₁	V _I = 0 V	10	30	100	kΩ	
Pull-down resistor <small>Note 2</small>	R ₂	V _I = V _{DD}	10	30	100	kΩ	

Notes 1. Total I_{OH}/I_{OL} (Max.) is 20 mA/-20 mA each power supply terminal (EV_{DD} and AV_{REF0}).

2. When used as \overline{DRST} pin (Flash memory product only) (OCDM0 is the control register).

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

(2) Pin leakage current

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input leakage current, high	I _{LIH1}	V _{IN} = V _{DD}	Analog pins		+1.0	μA
			Other pins		+5.0	
Input leakage current, low	I _{LIL1}	V _{IN} = 0 V	Analog pins		-1.0	μA
			Other pins		-5.0	
Output leakage current, high	I _{LOH1}	V _O = V _{DD}	Analog pins		+1.0	μA
			Other pins		+5.0	
Output leakage current, low	I _{LOL1}	V _O = 0 V	Analog pins		-1.0	μA
			Other pins		-5.0	

(3) Supply current

Supply current (V850ES/FE2: μ PD70F3231)

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Flash memory products supply current ^{Note 1}	I _{DD1}	Normal operation,	f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions operating		25	40	mA
			f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions stopped		20		mA
	I _{DD2}	HALT mode	f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions operating		14	26	mA
			f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions stopped		9		mA
	I _{DD3}	IDLE1 mode	f _{xx} = 5 MHz (OSC = 5 MHz), PLL off		0.6	1.5	mA
	I _{DD4}	IDLE2 mode	f _{xx} = 5 MHz (OSC = 5 MHz), PLL off		0.25	1.15	mA
	I _{DD5}	Subclock operation mode ^{Notes 2, 3}	RC resonator f _{XT} = 40 kHz ^{Note 4}		200	850	μ A
	I _{DD6}	Sub-IDLE mode ^{Notes 2, 3}	RC resonator f _{XT} = 40 kHz ^{Note 4}		35	590	μ A
	I _{DD7}	Stop mode ^{Notes 2, 5}	POC stopped, Ring-OSC stopped		7	500	μ A
			POC operating, Ring-OSC stopped		10	505	μ A
POC stopped, Ring-OSC operating				15	515	μ A	
POC operating, Ring-OSC operating				18	520	μ A	

- Notes**
1. Total current of V_{DD} and EV_{DD} (all ports stopped). The current of AV_{REF0} and the port buffer current including the current flowing through the on-chip pull-up/pull-down resistors are not included.
 2. When the main OSC is stopped.
 3. POC operating, Ring-OSC operating.
 4. The RC oscillation frequency is 40 kHz(TYP.). This clock is internally divided by 2.
 5. When the sub-OSC is not used.

Supply current (V850ES/FE2: μ PD703231, μ PD703230)

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Mask ROM products supply current ^{Note 1}	I _{DD1}	Normal operation,	f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions operating		20	35	mA
			f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions stopped		16		mA
	I _{DD2}	HALT mode	f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions operating		12	24	mA
			f _{xx} = 20 MHz (OSC = 5 MHz), all peripheral functions stopped		8		mA
	I _{DD3}	IDLE1 mode	f _{xx} = 5 MHz (OSC = 5 MHz), PLL off		0.25	1.15	mA
	I _{DD4}	IDLE2 mode	f _{xx} = 5 MHz (OSC = 5 MHz), PLL off		0.2	1.15	mA
	I _{DD5}	Subclock operation mode ^{Notes 2, 3}	RC resonator f _{XT} = 40 kHz ^{Note 4}		50	800	μ A
	I _{DD6}	Sub-IDLE mode ^{Notes 2, 3}	RC resonator f _{XT} = 40 kHz ^{Note 4}		35	590	μ A
	I _{DD7}	Stop mode ^{Notes 2, 5}	POC stopped, Ring-OSC stopped		7	500	μ A
			POC operating, Ring-OSC stopped		10	505	μ A
			POC stopped, Ring-OSC operating		15	515	μ A
			POC operating, Ring-OSC operating		18	520	μ A

Notes 1. Total current of V_{DD} and EV_{DD} (all ports stopped). The current of AV_{REF0} and the port buffer current including the current flowing through the on-chip pull-up/pull-down resistors are not included.

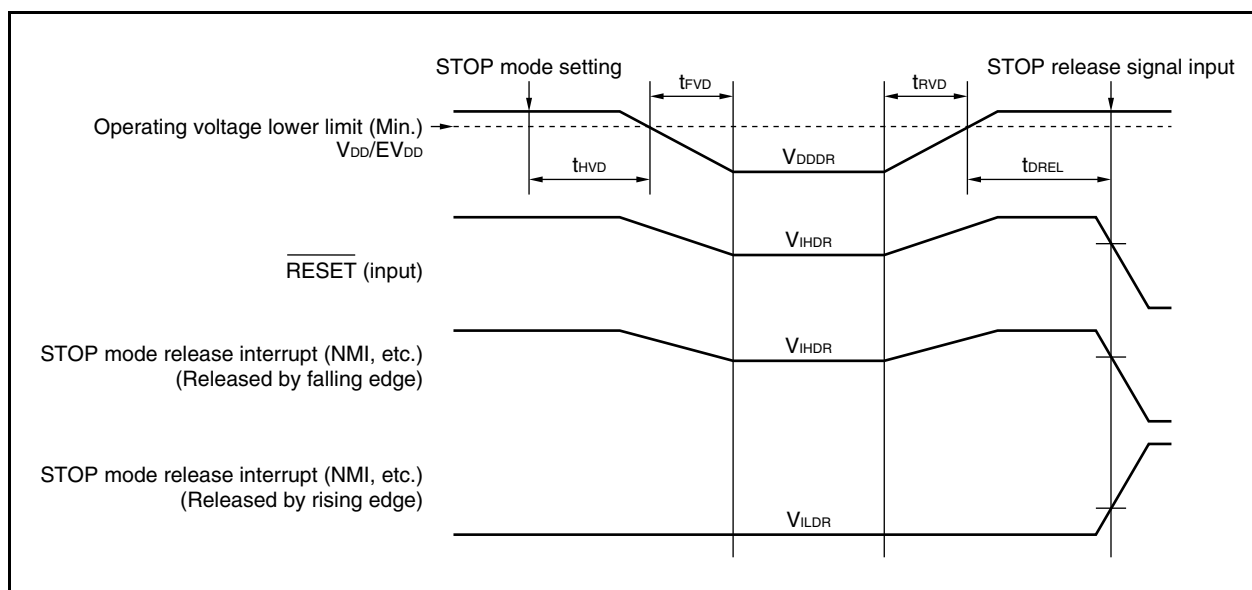
- 2. When the main OSC is stopped.
- 3. POC operating, Ring-OSC operating.
- 4. The RC oscillation frequency is 40 kHz(TYP.). This clock is internally divided by 2.
- 5. When the sub-OSC is not used.

1.3.9 Data Retention Characteristics

STOP Mode ($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = 1.9$ V to 5.5 V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V)

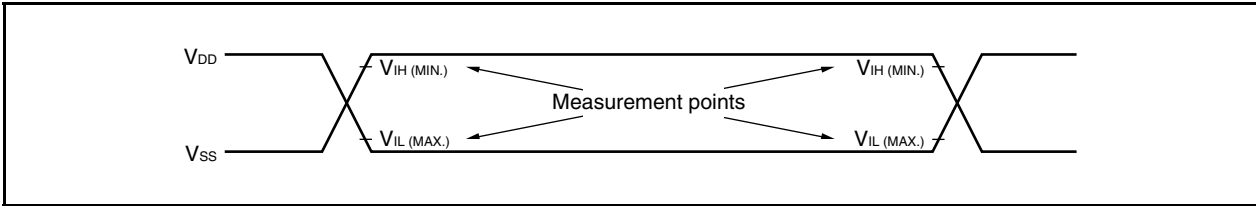
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}	In STOP mode	1.9		5.5	V
Data retention current	I_{DDDR}	$V_{DDDR} = 2.0$ V		6	450	μA
Supply voltage rise time	t_{rVD}		1			μs
Supply voltage fall time	t_{fVD}		1			μs
Supply voltage retention time	t_{HVD}	After STOP mode release	0			ms
STOP release signal input time	t_{DREL}	After V_{DD} reaches MIN.: 3.5 V	0			μs
Data retention input voltage, high	V_{IHDR}	All input ports	$0.9V_{DDDR}$		V_{DDDR}	V
Data retention input voltage, low	V_{ILDR}	All input ports	0		$0.1V_{DDDR}$	V

Caution Shifting to STOP mode and restoring from STOP mode must be performed within the rated operating range.

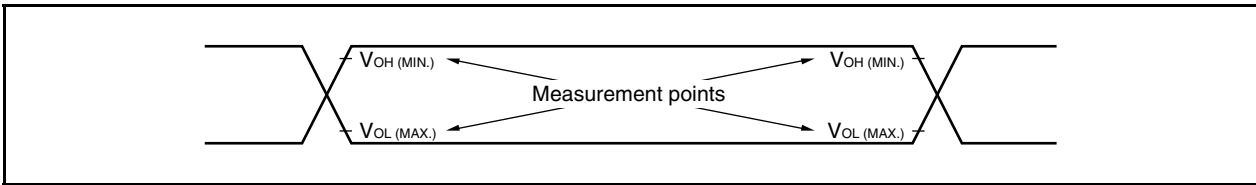


1.3.10 AC Characteristics

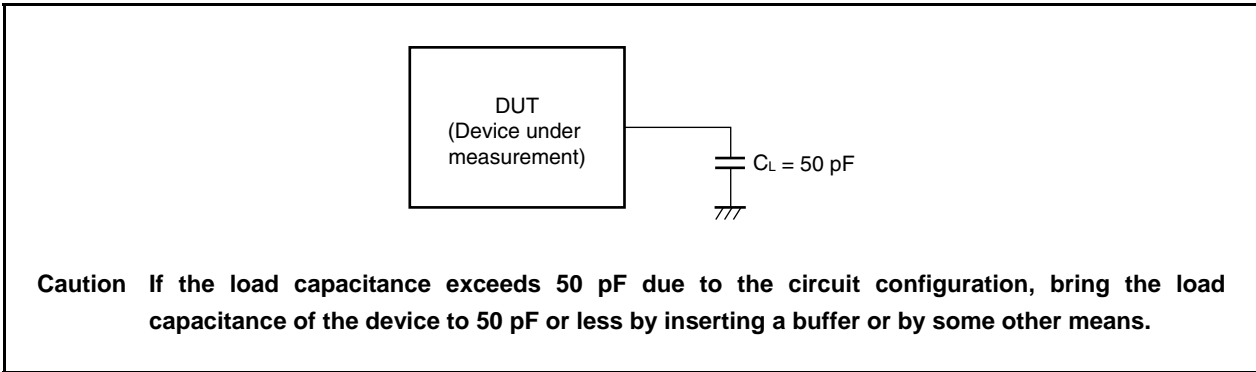
AC Test Input Measurement Points (V_{DD} , AV_{DD} , EV_{DD})



AC Test Output Measurement Points



Load Conditions

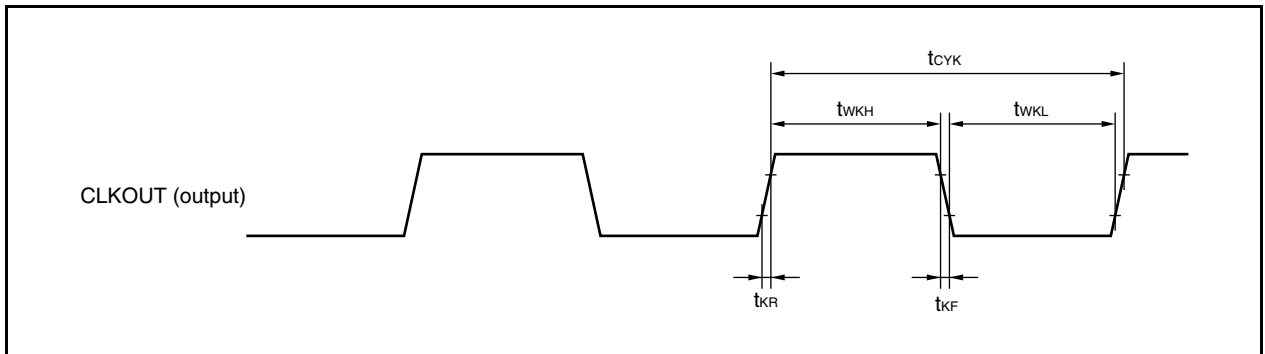


(1) CLKOUT output timing

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Output cycle	t_{CYK}		50 ns	80 μs	
High-level width	t_{WKH}		$t_{CYK}/2 - 15$		ns
Low-level width	t_{WKL}		$t_{CYK}/2 - 15$		ns
Rise time	t_{KR}			15	ns
Fall time	t_{KF}			15	ns

Clock Timing



(2) Basic Operation

(a) Reset, Interrupt timing

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

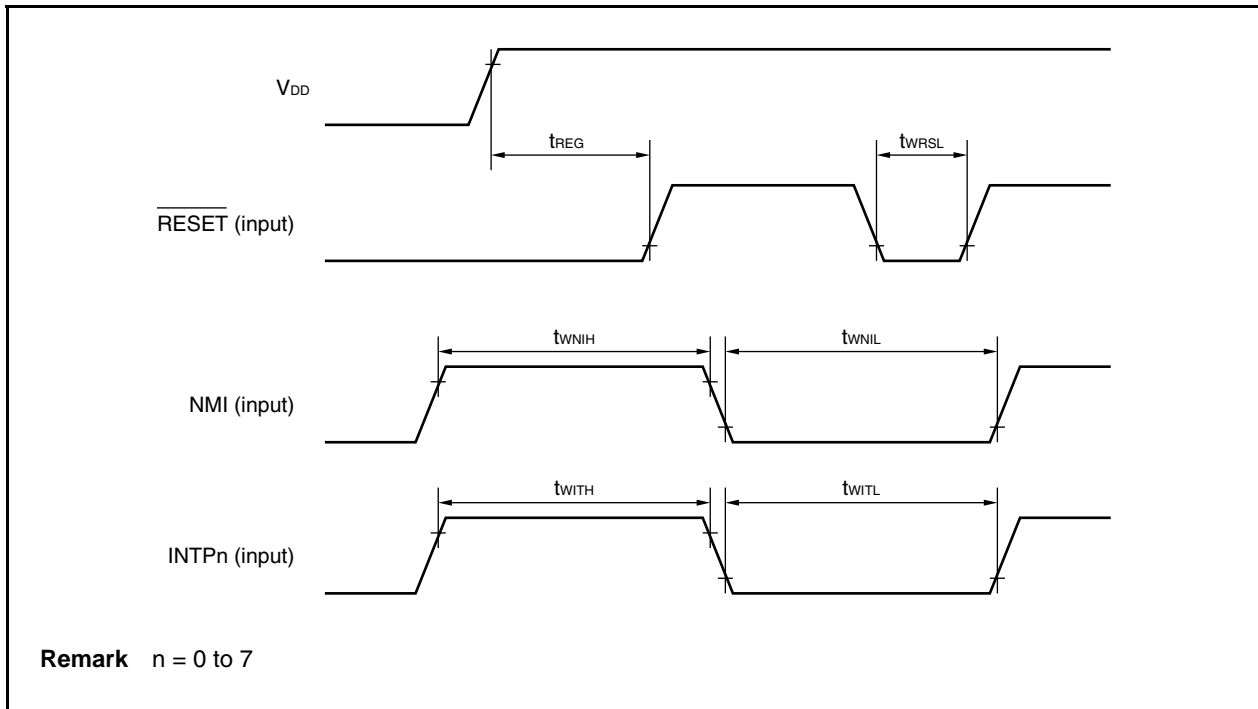
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ low-level width	t_{WRSL}		500		ns
NMI high-level width	t_{WNIH}	Analog noise elimination	500		ns
NMI low-level width	t_{WNIL}	Analog noise elimination	500		ns
INTP _n ^{Note 1} high-level width	t_{WITH}	Analog noise elimination (n = 0 to 7)	500		ns
		Digital noise elimination (n = 3)	Note 2		ns
INTP _n ^{Note 1} low-level width	t_{WITL}	Analog noise elimination (n = 0 to 7)	500		ns
		Digital noise elimination (n = 3)	Note 2		ns

Notes 1. ADTRG is same spec (P03/INTP0/ADTRG). $\overline{\text{DRST}}$ is same spec (P05/INTP2/DRST).

2. $2T_{\text{samp}} + 20$ or $3T_{\text{samp}} + 20$

T_{samp} : Sampling clock for noise elimination

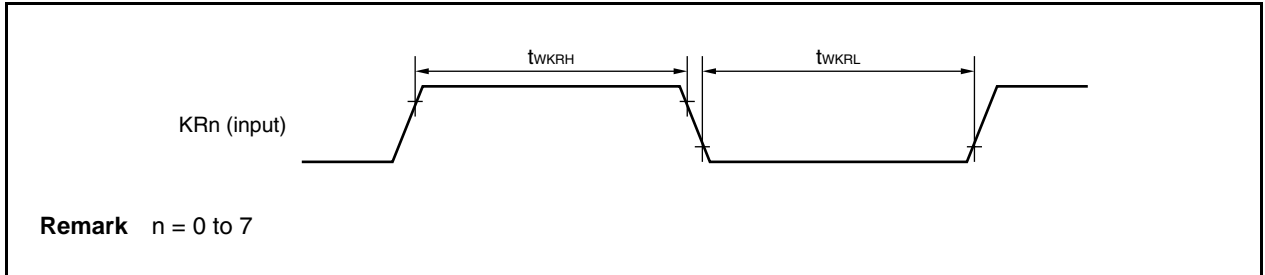
Reset/Interrupt



(b) Key return timing

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
KRn input high-level width	t_{WKRH}	Analog noise elimination ($n = 0$ to 7)	500		ns
KRn input low-level width	t_{WKRL}		500		ns

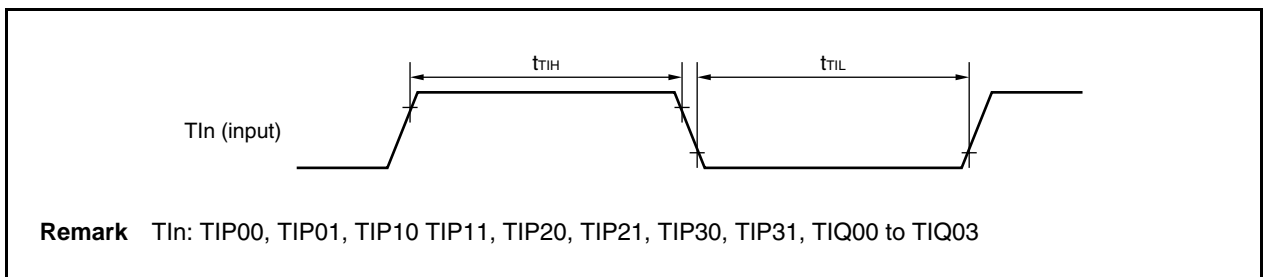


(c) Timer input timing

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
TIn high-level width	t_{TIH}	TIP00, TIP01, TIP10, TIP11, TIP20, TIP21, TIP30, TIP31, TIQ00 to TIQ03	Note		ns
TIn low-level width	t_{TIL}	TIQ03	Note		ns

Note $2T_{\text{samp}} + 20$ or $3T_{\text{samp}} + 20$
 T_{samp} : Sampling clock for noise elimination



(d) CSIB timing

(i) Master mode

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{SCKBn}}$ cycle time	t_{KCYn}		125		ns
$\overline{\text{SCKBn}}$ high-level width	t_{KHn}		$t_{\text{KCYn}}/2 - 15$		ns
$\overline{\text{SCKBn}}$ low-level width	t_{KLn}		$t_{\text{KCYn}}/2 - 15$		ns
SIBn setup time (to $\overline{\text{SCKBn}}\uparrow$)	t_{SIKn}		30		ns
SIBn hold time (from $\overline{\text{SCKBn}}\uparrow$)	t_{SIn}		25		ns
Output delay time from $\overline{\text{SCKBn}}\downarrow$ to SOBn	$t_{\text{KSO n}}$			25	ns

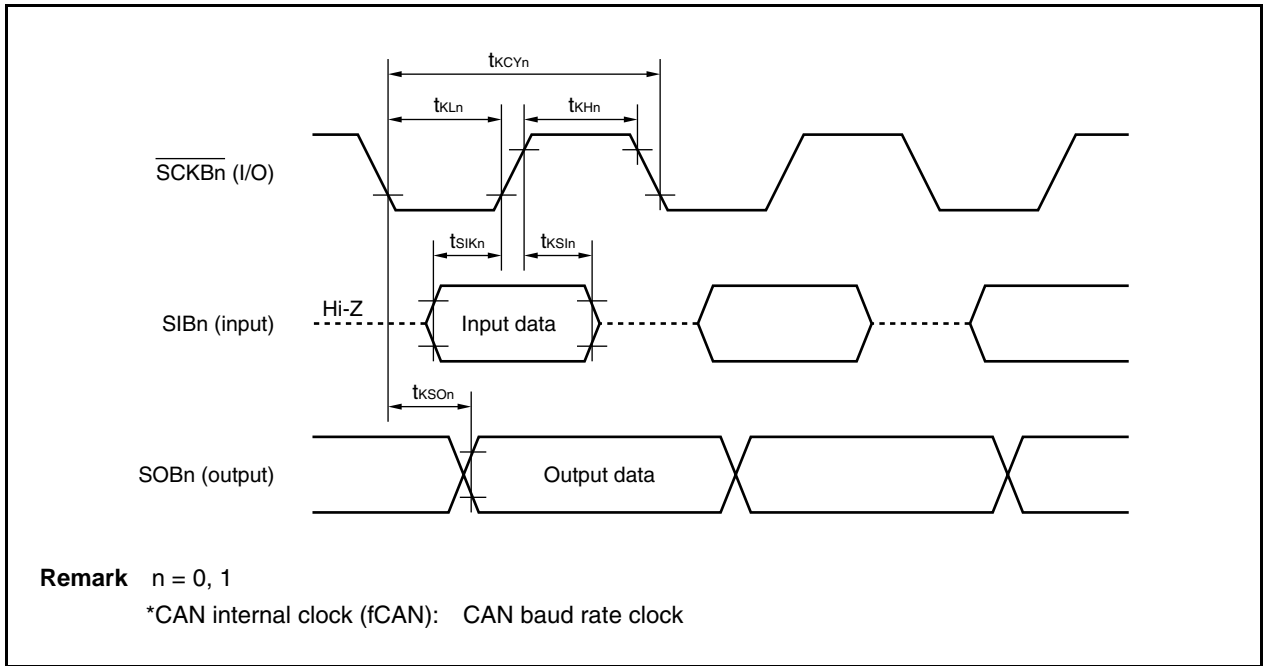
Remark n = 0, 1

(ii) Slave mode

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{SCKBn}}$ cycle time	t_{KCYn}		200		ns
$\overline{\text{SCKBn}}$ high-level width	t_{KHn}		90		ns
$\overline{\text{SCKBn}}$ low-level width	t_{KLn}		90		ns
SIBn setup time (to $\overline{\text{SCKBn}}\uparrow$)	t_{SIKn}		50		ns
SIBn hold time (from $\overline{\text{SCKBn}}\uparrow$)	t_{SIn}		50		ns
Output delay time from $\overline{\text{SCKBn}}\downarrow$ to SOBn	$t_{\text{KSO n}}$			50	ns

Remark n = 0, 1



(e) UART timing

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

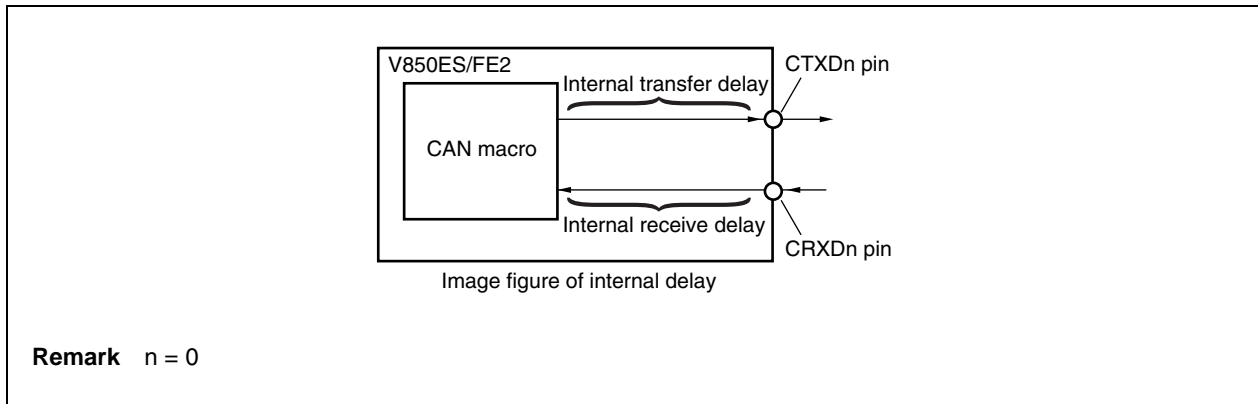
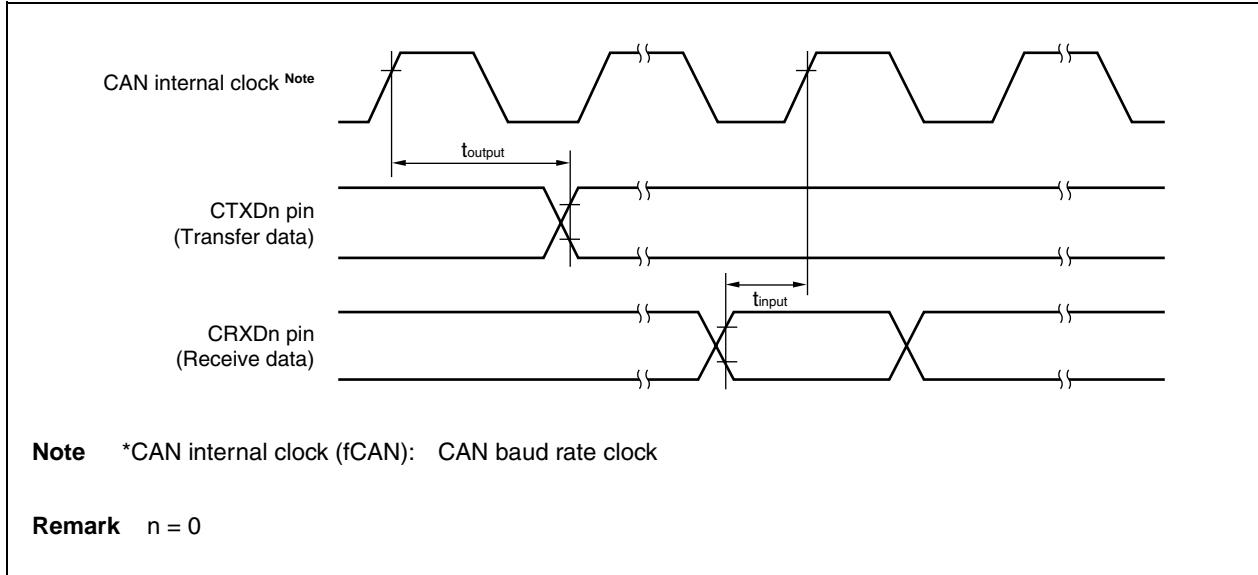
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Communication rate				312.5	kbps
ASCK0 cycle time				10	MHz

(f) CAN timing

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = AV_{SS} = 0\text{ V}$, $C_L = 50\text{ pF}$)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Transfer rate				1	Mbps
Internal delay time ^{Note}				100	ns

Note Internal delay time (t_{NODE}) = Internal transfer delay time (t_{OUTPUT}) + Internal receive delay time (t_{INPUT})



(g) A/D converter

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					10	bit
Overall error ^{Note}		$4.0 \leq AV_{REF0} \leq 5.5$ V		± 0.15	± 0.35	%FSR
Conversion time	t_{CONV}		3.1		16	μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF0}	V
AV _{REF0} current	I_{AREF0}	When using A/D converter		5	10	mA
		When not using A/D converter		1	10	μA

Note Excluding quantization error ($\pm 0.05\%$ FSR). Indicates the ratio to the full-scale value (%FSR).

Remark FSR: Full Scale Range

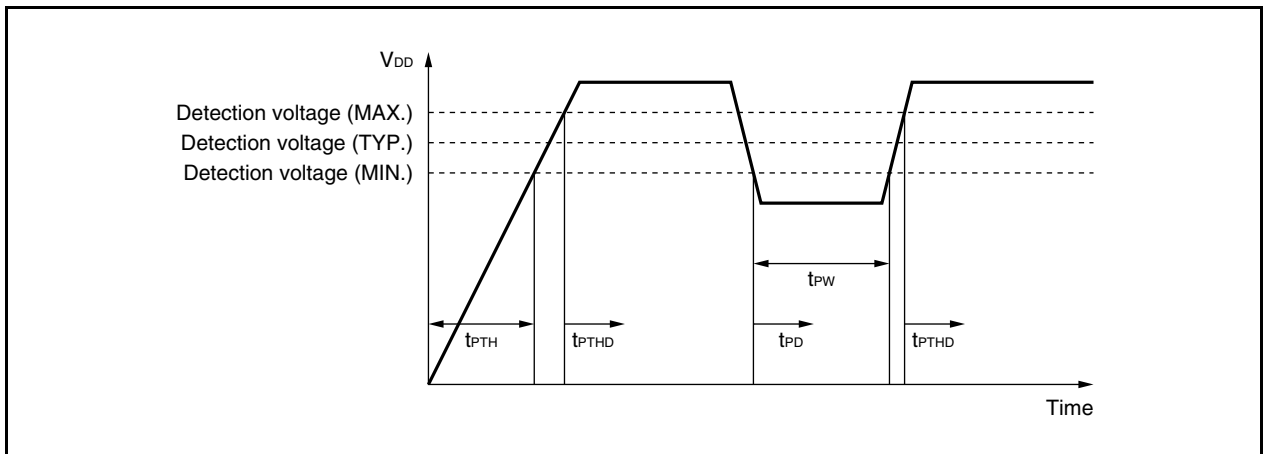
(h) POC circuit characteristics

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POCO}		3.5	3.7	3.9	V
Power supply startup time	t_{PTH}	$V_{DD} = 0$ V \rightarrow 3.5 V	0.002			ms
Response delay time 1 ^{Note} ₁	t_{PTHD}	In case of power on. After V_{DD} reaches 3.9 V.			3.0	ms
Response delay time 2 ^{Note} ₂	t_{PD}	In case of power off. After V_{DD} drops 3.5 V.			1	ms
Minimum V_{DD} width	t_{PW}		0.2			ms

Notes 1. From detect voltage to release reset signal.

2. From detect voltage to output reset signal.

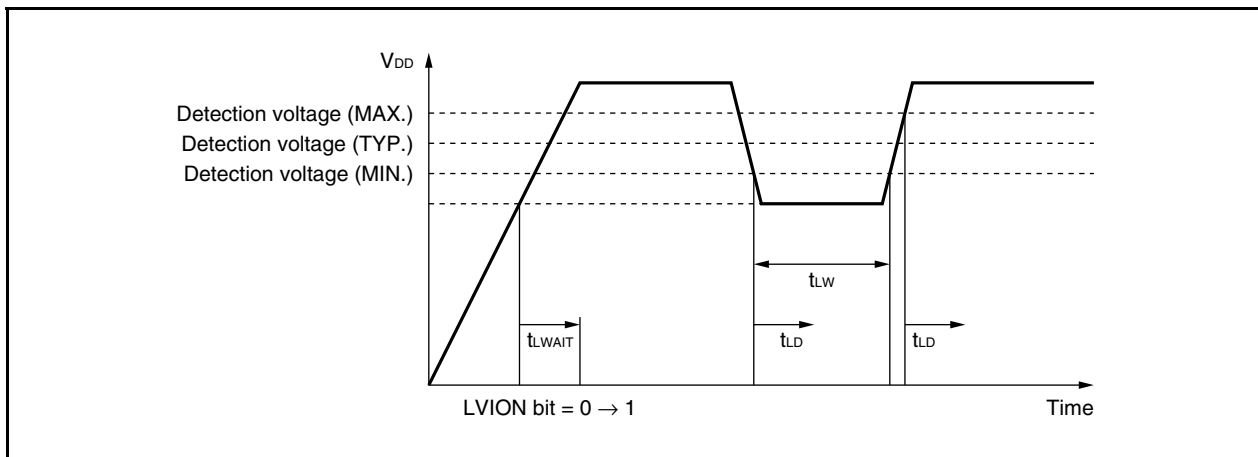


(i) LVI circuit characteristics

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5\text{ V to }5.5\text{ V}$, $4.0\text{ V} \leq AV_{REF0} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = AV_{SS} = 0\text{ V}$, $C_L = 50\text{ pF}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{LV10}		4.2	4.4	4.6	V
	V_{LV11}		4.0	4.2	4.4	V
Response time ^{Note 1}	t_{LD}	After V_{DD} reaches V_{LV10}/V_{LV11} (Max.). After V_{DD} drops V_{LV10}/V_{LV11} (Min.).		0.2	2.0	ms
Minimum V_{DD} width	t_{LW}		0.2			ms
Reference voltage stabilization wait time ^{Note 2}	t_{LWAIT}	After V_{DD} reaches 3.5 V. After LVION bit (LVIM.bit7) = 0 \rightarrow 1		0.1	0.2	ms

- Notes**
1. The time required to output an interrupt/reset after the detection voltage is detected.
 2. Unnecessary when the POC function is used.

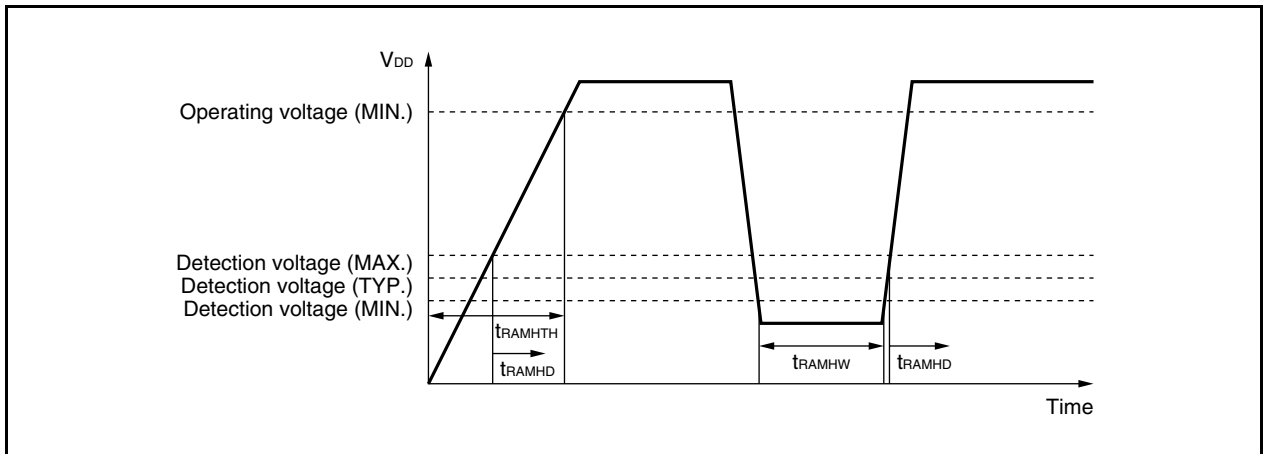


(j) RAM retention flag characteristics

($T_A = -40$ to $+125^\circ\text{C}$, $V_{DD} = EV_{DD} = 1.9$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{RAMH}		1.9	2.0	2.1	V
Supply voltage rise time	t_{RAMHTH}	$V_{DD} = 0$ V \rightarrow 3.5 V	0.002		1,800	ms
Response time ^{Note}	t_{RAMHD}	After the supply voltage reaches the detection voltage (MAX.)		0.2	2.0	ms
Minimum V_{DD} width	t_{RAMHW}		0.2			ms

Note Time required to set the RAMF bit after the detection voltage is detected.



(k) Flash memory programming characteristics

(i) Basic characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	f_{CPU}		4		20	MHz
Supply voltage	V_{DD}		3.5		5.5	V
Number of writes	C_{WRT} Note				100	Times
Input voltage, high	V_{IH}	FLMD0	$0.8EV_{DD}$		EV_{DD}	V
Input voltage, low	V_{IL}	FLMD0	EV_{SS}		$0.2EV_{DD}$	V
Write time + erase time	t_{WRT} + t_{ERASE}	Flash: 128 KB (μ PD70F3231)			T.B.D	s
Programming temperature	t_{PRG}		-40		+85	$^\circ\text{C}$

Note The initial write when the product is shipped, any erase → write set of operations, or any programming operation is counted as one rewrite.

Example: P: Write, E: Erase

Shipped product → P → E → P → E → P: 3 rewrites

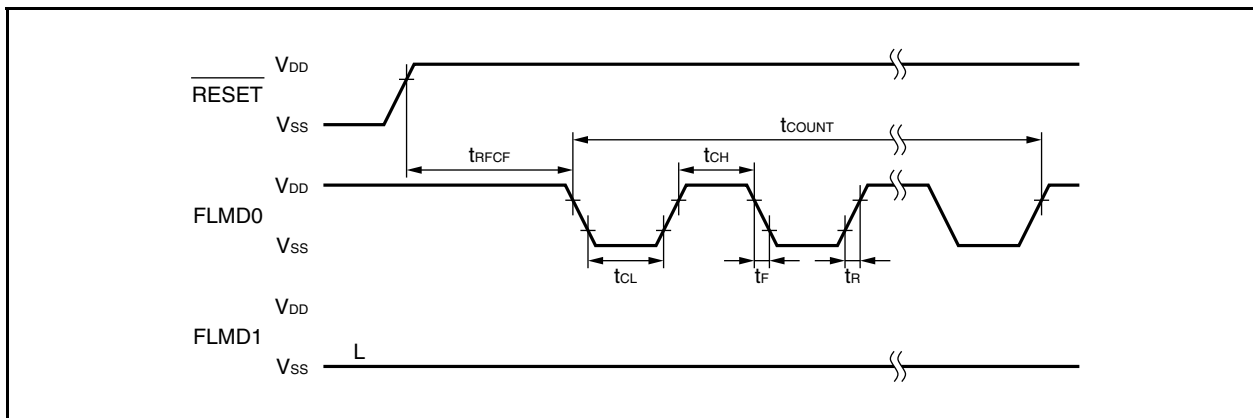
Shipped product → E → P → E → P → E → P: 3 rewrites

(ii) Serial Write Operation Characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = EV_{DD} = 3.5$ V to 5.5 V, 4.0 V $\leq AV_{REF0} \leq 5.5$ V, $V_{SS} = EV_{SS} = AV_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
FLMD0 setup time from $\overline{\text{RESET}}\uparrow$	t_{RFCF}		$500/f_x + \alpha$			s
Count execution time	t_{COUNT}				3	ms
FLMD0 high-level width	t_{CH}		10		100	μs
FLMD0 low-level width	t_{CL}		10		100	μs
FLMD rise time	t_R				50	ns
FLMD fall time	t_F				50	ns

Note “ ” represents the oscillation stabilization time.



2. Injected Current Specification

2.1 Injected Current Specification of (A)-Grade

2.1.1 Absolute Maximum Ratings

(Ta = +25 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Pos. Overload Current $V_{IN} > V_{DD}$	I_{INJPM}	Digital input pins	Per pin			4	mA
			Total			50	mA
		Analog input pins	Per pin			4	mA
			Total			20	mA
Neg. Overload Current $V_{IN} < V_{SS}$	I_{INJNM}	Digital input pins	Per pin			-4	mA
			Total			-50	mA
		Analog input pins	Per pin			-4	mA
			Total			-20	mA

Caution: Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter.

Remark: Analog input pins are pins of Port7 and Port12. Digital input pins are pins except analog input pins.

2.1.2 DC Characteristics for overload current

(Ta = -40 to +85 °C, $V_{DD}=EV_{DD}=BV_{DD}=3.5V$ to $5.5V$, $AV_{REF0}=4.0V$ to $5.5V$, $V_{SS}=EV_{SS}=BV_{SS}=AV_{SS}=0V$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Pos. Overload Current $V_{IN} > V_{DD}$	I_{INJP}	Digital input pins	Per pin			2	mA
			Total			16	mA
		Analog input pins	Per pin			0.5	mA
			Total			2	mA
Neg. Overload Current $V_{IN} < V_{SS}$	I_{INJN}	Digital input pins ^{Note1}	Per pin			-0.3	mA
			Total			-2.4	mA
		Analog input pins	Per pin			-0.3	mA
			Total			-1.2	mA

Remark(s):

1. Analog input pins are pins of Port7 and Port12. Digital input pins are pins except analog input pins.
2. These specifications are not tested in outgoing inspection, but specified based on the device characterization.
3. Refer to the next pages for Input leakage current and A/D characteristics.

Note(s):

1. In case of using Sub clock, an adjacent pin of XT2 pin is the following specification.

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Neg. Overload Current $V_{IN} < V_{SS}$	I_{INJN}	an adjacent pin of XT2 pin ^{Note2}			-0.1	mA

Note(s):

2. An adjacent pin of XT2 pin is as follows:

V850ES/FE2: P00 pin, V850ES/FF2: P05 pin, V850ES/FG2: P02 pin, V850ES/FJ2: P02 pin

2.1.3 DC Characteristics for pins influenced by injected current on an adjacent pin

(Ta = -40 to +85 °C, V_{DD}=EV_{DD}=BV_{DD}= 3.5V to 5.5V, AV_{REF}= 4.0V to 5.5V, V_{SS}=EV_{SS}=BV_{SS}=AV_{SS}=0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input leakage current High	I _{LH}	V _I = V _{DD}	Digital input pins I _{IN,IP} : 2mA(per pin), 4mA(total)	-	0.5	uA
			Analog input pins I _{IN,IP} : 0.5mA(per pin), 1mA(total)	-	0.2	uA
Input leakage current Low	I _{LIL}	V _I = 0	Digital input pins I _{IN,IN} : -0.3mA(per pin), -0.6mA(total)	5	40	uA
			I _{IN,IN} : -0.1mA(per pin), -0.2mA(total)	1	10	uA
			Analog input pins I _{IN,IN} : -0.3mA(per pin), -0.6mA(total)	5	40	uA
			I _{IN,IN} : -0.1mA(per pin), -0.2mA(total)	1	10	uA

Remark(s):

1. Analog input pins are pins of Port7 and Port12. Digital input pins are pins except analog input pins.
2. These specifications are not tested in outgoing inspection, but specified based on the device characterization.
3. Measurement conditions are shown in [Figure 1](#).
4. TYP. is the value of Ta=+25 °C.

2.1.4 A/D converter influenced by injected current on an adjacent pin

(Ta = -40 to +85 °C, V_{DD}=EV_{DD}=BV_{DD}= 3.5V to 5.5V, AV_{REF0}= 4.0V to 5.5V, V_{SS}=EV_{SS}=BV_{SS}=AV_{SS}=0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Degradation of Overall error ^{Note1}		I _{INJP} : 0.5mA(per pin), 1mA(total)			+/- 0.10	%FSR
		I _{INJN} : -0.3mA(per pin), -0.6mA(total)			+/- 0.25	%FSR

Remark(s):

1. These specifications are not tested in outgoing inspection, but specified based on the device characterization.
2. Measurement conditions are shown in [Figure 1](#).

Note(s):

This value is the degradation by injected current on an adjacent pin. Therefore, this value is added to the specification of A/D converter's overall error defined separately as the electrical specifications.

Caution(s):

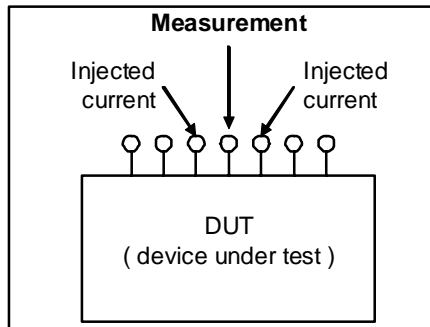
When there is a leakage current, the effect on the ADC accuracy depends on the external analog source impedance.

Example) Conditions: AVREF0 = 5.0V, external analog source impedance = 10K ohm

If there is a leakage current of 10uA by injected current, the effect on the ADC accuracy is

$$10(\mu\text{A}) \times 10\text{K}(\text{ohm}) / 5(\text{V}) = 2\% \text{FSR}$$

Figure 1



2.2 Injected Current Specification of (A1)-Grade

2.2.1 Absolute Maximum Ratings

(Ta = +25 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Pos. Overload Current $V_{IN} > V_{DD}$	I_{INJPM}	Digital input pins	Per pin			4	mA
			Total			50	mA
		Analog input pins	Per pin			4	mA
			Total			20	mA
Neg. Overload Current $V_{IN} < V_{SS}$	I_{INJNM}	Digital input pins	Per pin			-4	mA
			Total			-50	mA
		Analog input pins	Per pin			-4	mA
			Total			-20	mA

Caution: Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter.

Remark: Analog input pins are pins of Port7 and Port12. Digital input pins are pins except analog input pins.

2.2.2 DC Characteristics for overload current

(Ta = -40 to +110 °C, $V_{DD}=EV_{DD}=BV_{DD}=3.5V$ to $5.5V$, $AV_{REF0}=4.0V$ to $5.5V$, $V_{SS}=EV_{SS}=BV_{SS}=AV_{SS}=0V$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Pos. Overload Current $V_{IN} > V_{DD}$	I_{INJP}	Digital input pins	Per pin			2	mA
			Total			16	mA
		Analog input pins	Per pin			0.5	mA
			Total			2	mA
Neg. Overload Current $V_{IN} < V_{SS}$	I_{INJN}	Digital input pins ^{Note1}	Per pin			-0.3	mA
			Total			-2.4	mA
		Analog input pins	Per pin			-0.3	mA
			Total			-1.2	mA

Remark(s):

1. Analog input pins are pins of Port7 and Port12. Digital input pins are pins except analog input pins.
2. These specifications are not tested in outgoing inspection, but specified based on the device characterization.
3. Refer to the next pages for Input leakage current and A/D characteristics.

Note(s):

1. In case of using Sub clock, an adjacent pin of XT2 pin is the following specification.

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Neg. Overload Current $V_{IN} < V_{SS}$	I_{INJN}	an adjacent pin of XT2 pin ^{Note2}			-0.1	mA

Note(s):

2. An adjacent pin of XT2 pin is as follows.

V850ES/FE2: P00 pin, V850ES/FF2: P05 pin, V850ES/FG2: P02 pin, V850ES/FJ2: P02 pin

2.2.3 DC Characteristics for pins influenced by injected current on an adjacent pin

(Ta = -40 to +110 °C, V_{DD}=EV_{DD}=BV_{DD}= 3.5V to 5.5V, AV_{REF0}= 4.0V to 5.5V, V_{SS}=EV_{SS}=BV_{SS}=AV_{SS}=0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Input leakage current High	I _{LIH}	V _I = V _{DD}	Digital input pins I _{IN,IP} : 2mA(per pin), 4mA(total)		-	2	uA
			Analog input pins I _{IN,IP} : 0.5mA(per pin), 1mA(total)		-	2	uA
Input leakage current Low	I _{LIL}	V _I = 0	Digital input pins I _{IN,IN} : -0.3mA(per pin), -0.6mA(total)		5	60	uA
			I _{IN,IN} : -0.1mA(per pin), -0.2mA(total)		1	15	uA
			Analog input pins I _{IN,IN} : -0.3mA(per pin), -0.6mA(total)		5	60	uA
			I _{IN,IN} : -0.1mA(per pin), -0.2mA(total)		1	15	uA

Remark(s):

1. Analog input pins are pins of Port7 and Port12. Digital input pins are pins except analog input pins.
2. These specifications are not tested in outgoing inspection, but specified based on the device characterization.
3. Measurement conditions are shown in Figure 2.
4. TYP. is the value of Ta=+25 °C.

2.2.4 A/D converter influenced by injected current on an adjacent pin

(Ta = -40 to +110 °C, V_{DD}=EV_{DD}=BV_{DD} = 3.5V to 5.5V, AV_{REF0} = 4.0V to 5.5V, V_{SS}=EV_{SS}=BV_{SS}=AV_{SS}=0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Degradation of Overall error ^{Note1}		I _{INJP} : 0.5mA(per pin), 1mA(total)			+/- 0.10	%FSR
		I _{INJN} : -0.3mA(per pin), -0.6mA(total)			+/- 0.25	%FSR

Remark(s):

1. These specifications are not tested in outgoing inspection, but specified based on the device characterization.
2. Measurement conditions are shown in Figure 2.

Note(s):

This value is the degradation by injected current on an adjacent pin. Therefore, this value is added to the specification of A/D converter's overall error defined separately as the electrical specifications.

Caution(s):

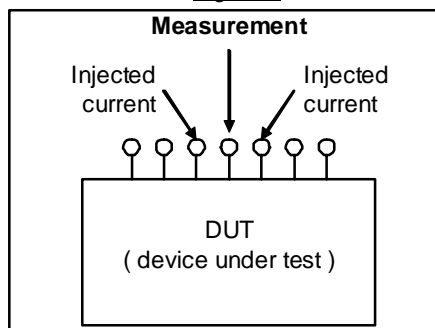
When there is a leakage current, the effect on the ADC accuracy depends on the external analog source impedance.

Example) Conditions: AVREF0 = 5.0V, external analog source impedance = 10K ohm

If there is a leakage current of 10uA by injected current, the effect on the ADC accuracy is

$$10(\mu\text{A}) \times 10\text{K}(\text{ohm}) / 5(\text{V}) = 2 \text{ \%FSR}$$

Figure 2



2.3 Injected Current Specification of (A2)-Grade

2.3.1 Absolute Maximum Ratings

(Ta = +25 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Pos. Overload Current $V_{IN} > V_{DD}$	I_{INJPM}	Digital input pins	Per pin			4	mA
			Total			50	mA
		Analog input pins	Per pin			4	mA
			Total			20	mA
Neg. Overload Current $V_{IN} < V_{SS}$	I_{INJNM}	Digital input pins	Per pin			-4	mA
			Total			-50	mA
		Analog input pins	Per pin			-4	mA
			Total			-20	mA

Caution: Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter.

Remark: Analog input pins are pins of Port7 and Port12. Digital input pins are pins except analog input pins.

2.3.2 DC Characteristics for overload current

(Ta = -40 to +125 °C, $V_{DD}=EV_{DD}=BV_{DD}=3.5V$ to $5.5V$, $AV_{REF0}=4.0V$ to $5.5V$, $V_{SS}=EV_{SS}=BV_{SS}=AV_{SS}=0V$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Pos. Overload Current $V_{IN} > V_{DD}$	I_{INJP}	Digital input pins	Per pin			2	mA
			Total			16	mA
		Analog input pins	Per pin			0.5	mA
			Total			2	mA
Neg. Overload Current $V_{IN} < V_{SS}$	I_{INJN}	Digital input pins ^{Note1}	Per pin			-0.3	mA
			Total			-2.4	mA
		Analog input pins	Per pin			-0.3	mA
			Total			-1.2	mA

Remark(s):

- Analog input pins are pins of Port7 and Port12. Digital input pins are pins except analog input pins.
- These specifications are not tested in outgoing inspection, but specified based on the device characterization.
- Refer to the next pages for Input leakage current and A/D characteristics.

Note(s):

- In case of using Sub clock, an adjacent pin of XT2 pin is the following specification.

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Neg. Overload Current $V_{IN} < V_{SS}$	I_{INJN}	an adjacent pin of XT2 pin ^{Note2}			-0.1	mA

Note(s):

- An adjacent pin of XT2 pin is as follows.

V850ES/FE2: P00 pin, V850ES/FF2: P05 pin, V850ES/FG2: P02 pin, V850ES/FJ2: P02 pin

2.3.3 DC Characteristics for pins influenced by injected current on an adjacent pin

(Ta = -40 to +125 °C, V_{DD}=E_{V_{DD}}=B_{V_{DD}}= 3.5V to 5.5V, A_{V_{REF0}}= 4.0V to 5.5V, V_{SS}=E_{V_{SS}}=B_{V_{SS}}=A_{V_{SS}}=0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Input leakage current High	I _{LIH}	V _I = V _{DD}	Digital input pins I _{IN,IP} : 2mA(per pin), 4mA(total)		-	5	uA
			Analog input pins I _{IN,IP} : 0.5mA(per pin), 1mA(total)		-	3	uA
Input leakage current Low	I _{LIL}	V _I = 0	Digital input pins I _{IN,IN} : -0.3mA(per pin), -0.6mA(total)		5	60	uA
			I _{IN,IN} : -0.1mA(per pin), -0.2mA(total)		1	15	uA
			Analog input pins I _{IN,IN} : -0.3mA(per pin), -0.6mA(total)		5	60	uA
			I _{IN,IN} : -0.1mA(per pin), -0.2mA(total)		1	15	uA

Remark(s):

1. Analog input pins are pins of Port7 and Port12. Digital input pins are pins except analog input pins.
2. These specifications are not tested in outgoing inspection, but specified based on the device characterization.
3. Measurement conditions are shown in [Figure 3](#).
4. TYP. is the value of Ta=+25 °C.

2.3.4 A/D converter influenced by injected current on an adjacent pin

(Ta = -40 to +125 °C, V_{DD}=EV_{DD}=BV_{DD}= 3.5V to 5.5V, AV_{REF0}= 4.0V to 5.5V, V_{SS}=EV_{SS}=BV_{SS}=AV_{SS}=0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Degradation of Overall error ^{Note1}		I _{INJP} : 0.5mA(per pin), 1mA(total)			+/- 0.10	%FSR
		I _{INJN} : -0.3mA(per pin), -0.6mA(total)			+/- 0.25	%FSR

Remark(s):

1. These specifications are not tested in outgoing inspection, but specified based on the device characterization.
2. Measurement conditions are shown in [Figure 3](#).

Note(s):

This value is the degradation by injected current on an adjacent pin. Therefore, this value is added to the specification of A/D converter's overall error defined separately as the electrical specifications.

Caution(s):

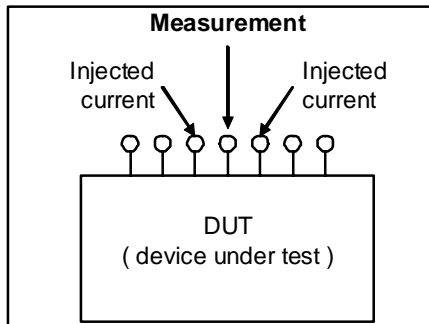
When there is a leakage current, the effect on the ADC accuracy depends on the external analog source impedance.

Example) Conditions: AVREF0 = 5.0V, external analog source impedance = 10K ohm

If there is a leakage current of 10uA by injected current, the effect on the ADC accuracy is

$$10(\mu\text{A}) \times 10\text{K}(\text{ohm}) / 5(\text{V}) = 2 \text{ \%FSR}$$

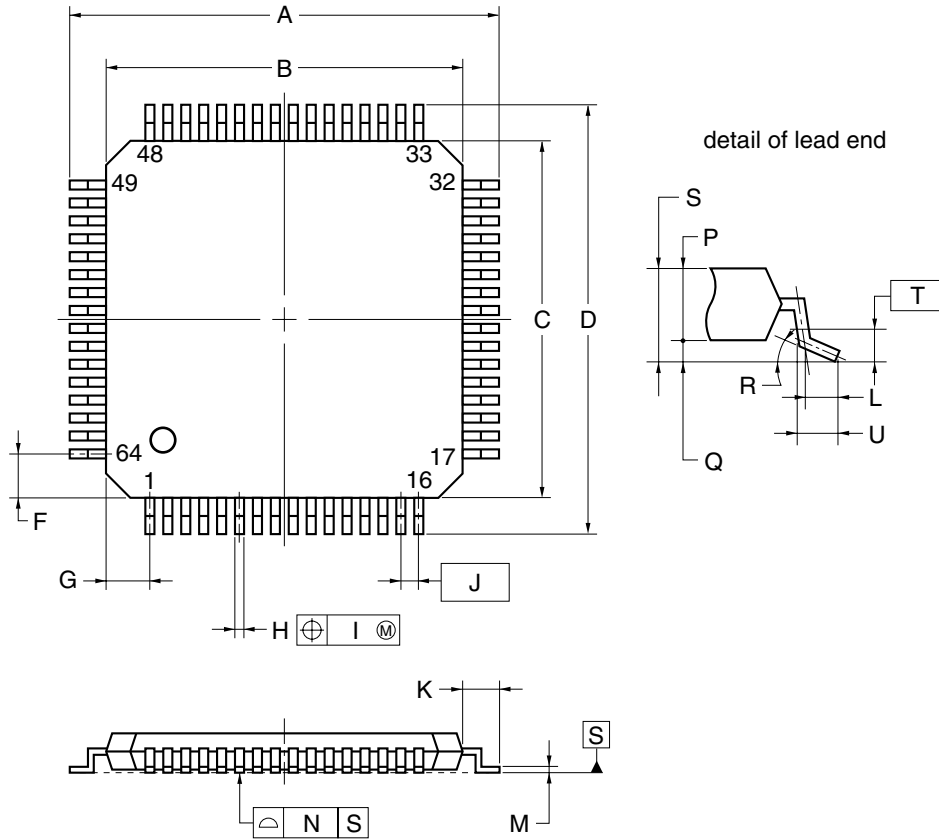
Figure 3



3. Package Drawing

Figure 3-1: Package Drawing

64-PIN PLASTIC TQFP (FINE PITCH) (10x10)



NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	12.0±0.2
B	10.0±0.2
C	10.0±0.2
D	12.0±0.2
F	1.25
G	1.25
H	0.22±0.05
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5
M	0.17 ^{+0.03} _{-0.07}
N	0.08
P	1.0
Q	0.1±0.05
R	3° ^{+4°} _{-3°}
S	1.10±0.10
T	0.25
U	0.6±0.15

S64GB-50-YEU-1

4. Recommended Soldering Conditions

Table 4-1: Soldering Conditions

(1) μ PD70F3231MxGB(Ax)-8EU

Soldering Method	Soldering Condition	Symbol of Recommended Soldering Condition
Infrared Reflow	Package Peak Temperature: 260°C Time: 30 seconds max. (210°C min.) Count: 3 max Exposure Limit: 7 days ^{Note}	IR60-207-3

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period. After that, prebaking is necessary at 125 °C for 20 to 72 hours.

(2) μ PD70F3231MxGB(Ax)-UEU

Soldering Method	Soldering Condition	Symbol of Recommended Soldering Condition
Infrared Reflow	Package Peak Temperature: 235°C Time: 30 seconds max. (210°C min.) Count: 3 max Exposure Limit: 7 days ^{Note}	IR35-207-3

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period. After that, prebaking is necessary at 125 °C for 20 to 72 hours.