NEC

MOS INTEGRATED CIRCUIT
μPD800232

ERTEC 400
Enhanced Real-Time Ethernet Controller with 32-bit RISC CPU Core

DESCRIPTION

ERTEC 400 is a powerful communication block for development of Ethernet-based automation products. ERTEC 400 contains a 32-bit RISC processor, an external memory interface with SDRAM and SRAM controller, a PCI/LBU interface, a 4-channel real-time Ethernet interface, synchronous and asynchronous serial ports, and general purpose I/Os. Its robust construction, specific automation functions, and openness to the IT world are distinguishing features. The ERTEC 400 is housed in a 304-pin plastic FBGA package (19 mm × 19 mm).

Detailed functions are described in the following user's manual. Be sure to read this manual when you design your systems.

Preliminary User's Manual ERTEC 400 : A17812EE2V0UM00

FEATURES

- ARM946E-S core with max. 150 MHz
  - 8 kBytes of instruction cache
  - 4 kBytes of data cache
  - 4 kBytes of D-TCM
  - Memory protection unit
  - On-chip debug and trace functionality via JTAG interface
  - ETM9 embedded trace macrocell
  - Interrupt controller for 16 IRQs and 8 FIQs
- Internal Multilayer AHB bus running at 50 MHz
- 8 kBytes of internal SRAM accessible by ARM946 core, IRT and PCI/LBU interface
- External memory interface (EMIF) supports up to 256 MBytes of SDRAM and up to 64 MBytes for static memories and I/O with 4 chip selects
- Integrated PLL to generate internal clocks for ARM946E-S, AHB, APB and IRT switch
- Predefined Boot ROM content supporting different download sources
- 32-bit/66 MHz PCI Rev. 2.2 interface
  - supports power management V1.1
  - 3.3 V interface level (5 V tolerant)
  - master/target capability
  - host bridge functionality
- Local bus unit (LBU) with 16-bit data bus to connect external host with access to internal ERTEC 400 resources
- IRT switch block with 4 Ethernet ports (10/100 Mbps) supporting RT and IRT traffic
  - autonegotiation, broadcast filter
  - 192 kBytes internal communication SRAM
- Two UARTs (16550 like) and one SPI interface
- Two 32-bit timers with prescaler, one 32-bit F-timer and two watchdog timers
- Max. 32 GPIOs, partly usable as interrupts
- 1.5 V (logic) and 3.3 V (I/O) power supply
- Temperature range: T_A = -40 to 85°C
- Compact 304-pin plastic FBGA package

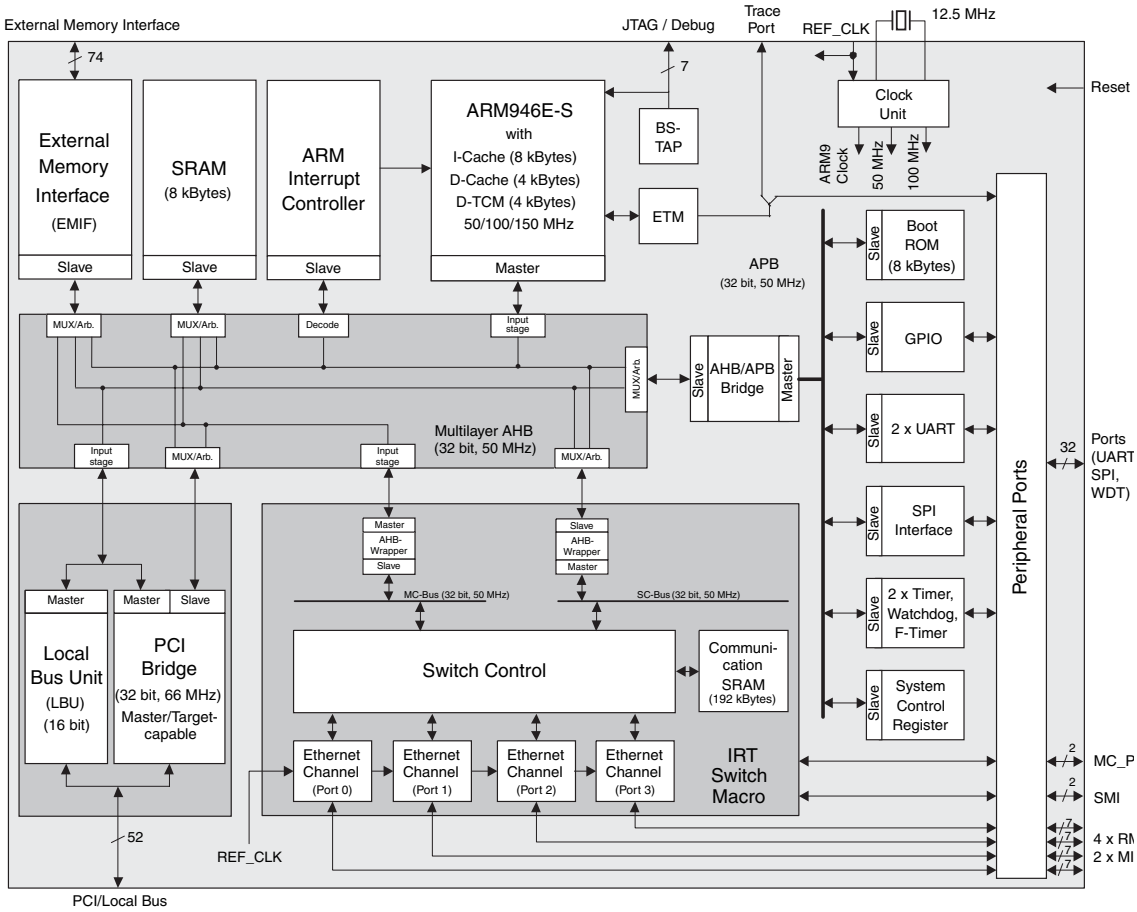
ORDERING INFORMATION

Device	Part Number	Package
ERTEC 400	μPD800232F1-014-HN2-A	P-FBGA304, 19 × 19 mm

Remark: Products with -A at the end of the part number are lead-free products.

Document No. A17813EE2V0DS00
Data Published: November 2009

INTERNAL BLOCK DIAGRAM



PIN IDENTIFICATION

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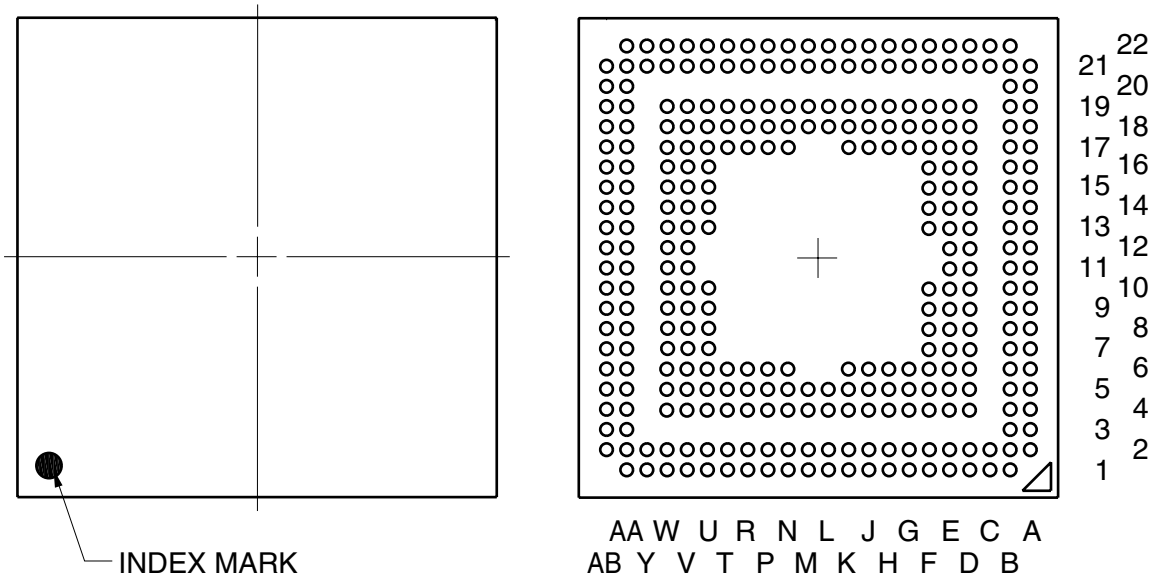
A(23:0)	:	Address bus	PAR	:	PCI parity
D(31:0)	:	Data bus	SERR_N	:	PCI system error
WR_N	:	Write strobe	PERR_N	:	PCI parity error
RD_N	:	Read strobe	STOP_N	:	PCI stop
CLK_SDRAM	:	Clock to SDRAM	DEVSEL_N	:	PCI device select
BE(3:0)_DQM(3:0)_N	:	Byte enable	TRDY_N	:	PCI target ready
CS_SDRAM_N	:	Chip select to SDRAM	IRDY_N	:	PCI initiator ready
RAS_SDRAM_N	:	Row address strobe to SDRAM	FRAME_N	:	PCI cycle frame
CAS_SDRAM_N	:	Column address strobe to SDRAM	LBU_AB(20:0)	:	LBU address bus
WE_SDRAM_N	:	RD/WR SDRAM	LBU_DB(15:0)	:	LBU data bus
CS_PER(3:0)_N	:	Chip select	LBU_WR_N	:	LBU write control
RDY_PER_N	:	Ready signal	LBU_RD_N	:	LBU read control
DTR_N	:	Direction signal for external driver or scan clock	LBU_BE(1:0)_N	:	LBU byte enable
OE_DRIVER_N	:	Enable signal for external driver or scan clock	LBU_SEG_(1:0)	:	LBU page selection
BOOT(2:0)	:	Boot mode	LBU_IRQ_(1:0)_N	:	LBU interrupt request
CONFIG(4:0)	:	System configuration	LBU_RDY_N	:	LBU ready signal
GPIO(31:0)	:	GPIO pins	LBU_CS_M_N	:	LBU chip select to ERTEC 400 internal resources
TXD(2:1)	:	UART transmit data output	LBU_CS_R_N	:	LBU chip select to page configuration registers
RXD(2:1)	:	UART receive data input	LBU_CFG	:	LBU separate RD/WR
DCD(2:1)_N	:	UART carrier detection signal	LBU_POL_RDY	:	LBU polarity selection for pin LBU_RDY_N
DSR(2:1)_N	:	UART data set ready signal	SSPRXD	:	SPI receive data
CTS(2:1)_N	:	UART transmit enable signal	SSPTXD	:	SPI transmit data
AD(31:0)	:	PCI address data bits	SCLKOUT	:	SPI clock out
IDSEL	:	PCI initialization device select	SFRMOUT	:	SPI serial frame output
CBE(3:0)_N	:	PCI byte enable	SFRMIN	:	SPI serial frame input
PME_N	:	PCI power management	SCLKIN	:	SPI clock in
REQ_N	:	PCI request	SSPCTLOE	:	SPI clock and serial frame output enable
GNT_N	:	PCI grant	SSPOE	:	SPI output enable
CLK_PCI	:	PCI clock	TXD_P(3:0) 0	:	(R)MII transmit data bit 0
RES_PCI_N	:	PCI reset	TXD_P(3:0) 1	:	(R)MII transmit data bit 1
INTA_N	:	PCI interrupt INTA_N	TXD_P(1:0) 2	:	MII transmit data bit 2
INTB_N	:	PCI interrupt INTB_N	TXD_P(1:0) 3	:	MII transmit data bit 3
M66EN	:	PCI clock selection	RXD_P(3:0) 0	:	(R)MII receive data bit 0

RXD_P(3:0) 1	:	(R)MII receive data bit 1	TRST_N	:	JTAG reset
RXD_P(1:0) 2	:	MII receive data bit 2	TCK	:	JTAG clock
RXD_P(1:0) 3	:	MII receive data bit 3	TDI	:	JTAG data in
TX_EN_P(3:0)	:	(R)MII transmit enable	TMS	:	JTAG test mode select
TX_ERR_P(1:0)	:	MII transmit error	TDO	:	JTAG data out
CRS_DV_P(3:0)	:	RMII carrier sense/data valid	DBGREQ	:	Debug request to ARM9
RX_ER_P(3:0)	:	(R)MII receive error	DBGACK	:	Debug acknowledge
CRS_P(1:0)	:	MII carrier sense	TAP_SEL	:	Select TAP controller
RX_DV_P(1:0)	:	MII receive data valid	CLKP_A	:	Quartz connection
COL_P(1:0)	:	MII collision	CLKP_B	:	Quartz connection
RX_CLK_P(1:0)	:	MII receive clock	REF_CLK	:	Reference clock input
TX_CLK_P(1:0)	:	MII transmit clock	F_CLK	:	Clock for F-counter
SMI_MDC	:	(R)MII SMI clock	RESET_N	:	HW reset
SMI_MDIO	:	(R)MII SMI input/output	WDOUT0_N	:	Watchdog output
RES_PHY_N	:	Reset to PHY	VDD Core	:	Power supply for core, 1.5 V
PLL_EXT_IN_N	:	MC_PLL input signal	GND Core	:	GND for core
TGEN_OUT1_N	:	MC_PLL output signal	VDD IO	:	Power supply for IO, 3.3 V
TRACEPKT(7:0)	:	Trace pins of ETM	GND IO	:	GND for IO
ETMEXTOUT	:	ETM output signal	P5V_PCI	:	Power supply for PCI, 5 V
ETMEXTIN1	:	ETM input signal	AVDD	:	Analog power supply for PLL, 1.5 V
PIPESTA(2:0)	:	Trace pipeline status	AGND	:	Analog GND for PLL
TRACESYNC	:	Trace sync signal	AVDD_PCI	:	Analog power supply for PLL in PCI I/F, 1.5 V
TRACECLK	:	ETM trace or scan clock	AGND_PCI	:	Analog GND for PLL in PCI I/F

PIN CONFIGURATION

- 304-Pin Plastic FBGA (19 mm × 19 mm)



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Pin Number	Pin Name	Pin Number	Pin Name
A2	AD1/LBU_DB1	A21	GND IO
A3	VDD IO	B1	A0
A4	AD7/LBU_DB7	B2	AD2/LBU_DB2
A5	VDD IO	B3	AD3/LBU_DB3
A6	AD12/LBU_DB12	B4	AD5/LBU_DB5
A7	GND IO	B5	AD8/LBU_DB8
A8	VDD IO	B6	AD10/LBU_DB10
A9	PERR_N/LBU_RD_N	B7	AD14/LBU_DB14
A10	IRDY_N/LBU_AB3	B8	CBE1_N/LBU_BE1_N
A11	VDD IO	B9	SERR_N/LBU_POL_RDY
A12	FRAME_N/LBU_AB4	B10	DEVSEL_N/LBU_AB1
A13	CBE2_N/LBU_AB5	B11	VDD Core
A14	AD19/LBU_AB9	B12	AD16/LBU_AB6
A15	VDD IO	B13	AD17/LBU_AB7
A16	CBE3_N/LBU_AB15	B14	AD21/LBU_AB11
A17	AD27/LBU_AB19	B15	AD23/LBU_AB13
A18	VDD IO	B16	AD25/LBU_AB17
A19	REQ_N/LBU_CS_M_N	B17	AD29/LBU_SEG_0
A20	VDD IO	B18	AD31/LBU_CS_R_N

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Pin Number	Pin Name	Pin Number	Pin Name
B19	CLK_PCI	E15	P5V_PCI
B20	INTB_N/LBU_IRQ1_N	E16	GND IO
B21	RXD_P3(1)/RXD_P1(3)	E17	RES_PCI_N
B22	RXD_P3(0)/RXD_P1(2)	E18	VDD Core
C1	A2	E19	VDD Core
C2	A1	E21	RX_ER_P3/COL_P1
C21	TXD_P3(1)/TXD_P1(3)	E22	RXD_P2(1)/RXD_P1(1)
C22	TXD_P3(0)/TXD_P1(2)	F1	A7
D1	A4	F2	A6
D2	A3	F4	A16/BOOT0
D4	AD0/LBU_DB0	F5	A15
D5	AD4/LBU_DB4	F6	VDD Core
D6	VDD Core	F7	GND IO
D7	CBE0_N/LBU_BE0_N	F8	P5V_PCI
D8	AD9/LBU_DB9	F9	AD15/LBU_DB15
D9	VDD Core	F10	GND Core
D10	STOP_N/LBU_AB00	F13	GND IO
D11	TRDY_N/LBU_AB2	F14	AD24/LBU_AB16
D12	P5V_PCI	F15	AD28/LBU_AB20
D13	IDSEL/LBU_AB14	F16	GND Core
D14	AD30/LBU_SEG_1	F17	VDD Core
D15	VDD Core	F18	GND IO
D16	PME_N/LBU_RDY_N	F19	CRS_DV_P3/RX_DV_P1
D17	GNT_N/LBU_CFG	F21	RXD_P2(0)/RXD_P1(0)
D18	INTA_N/LBU_IRQ0_N	F22	AVDD_PCI
D19	M66EN	G1	A9
D21	TX_EN_P3/TX_ERR_P1	G2	A8
D22	VDD IO	G4	A17/BOOT1
E1	VDD IO	G5	GND IO
E2	A5	G6	GND Core
E4	A14	G17	GND Core
E5	VDD Core	G18	CRS_DV_P2/CRS_P1
E6	GND Core	G19	CRS_DV_P1/RX_DV_P0
E7	AD6/LBU_DB6	G21	AGND_PCI
E8	AD11/LBU_DB11	G22	TXD_P2(1)/TXD_P1(1)
E9	AD13/LBU_DB13	H1	A11
E10	PAR/LBU_WR_N	H2	A10
E11	AD18/LBU_AB8	H4	VDD Core
E12	AD20/LBU_AB10	H5	A20/CONFIG1
E13	AD22/LBU_AB12	H6	A19/CONFIG0
E14	AD26/LBU_AB18	H17	leave open

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Pin Number	Pin Name	Pin Number	Pin Name
H18	RX_CLK_P1	N2	D0
H19	CRS_DV_P0/CRS_P0	N4	D18
H21	TXD_P2(0)/TXD_P1(0)	N5	VDD Core
H22	TX_EN_P2/TX_EN_P1	N6	D16
J1	A13	N17	GPIO4
J2	A12	N18	SMI_MDIO
J4	A18/BOOT2	N19	VDD Core
J5	A22/CONFIG3	N21	TXD_P0(1)/TXD_P0(1)
J6	A21/CONFIG2	N22	RXD_P0(0)/RXD_P0(0)
J17	TX_CLK_P1	P1	D1
J18	RX_ER_P2/RX_ER_P1	P2	D2
J19	VDD Core	P4	VDD Core
J21	RXD_P1(1)/RXD_P0(3)	P5	D19
J22	VDD IO	P6	GND IO
K1	RAS_SDRAM_N	P17	leave open
K2	CS_SDRAM_N	P18	VDD Core
K4	VDD Core	P19	GPIO5
K5	A23/CONFIG4	P21	TX_EN_P0/TX_EN_P0
K6	GND Core	P22	TXD_P0(0)/TXD_P0(0)
K17	TX_CLK_P0	R1	VDD IO
K18	RX_ER_P0/RX_ER_P0	R2	D3
K19	RX_CLK_P0	R4	D21
K21	RXD_P1(0)/RXD_P0(2)	R5	D22
K22	GND IO	R6	D20
L1	VDD IO	R17	GND IO
L2	CLK_SDRAM	R18	VDD Core
L4	CAS_SDRAM_N	R19	GPIO6
L5	BE2_DQM2_N	R21	RES_PHY_N
L18	GND Core	R22	REF_CLK
L19	VDD Core	T1	D4
L21	TXD_P1(1)/TXD_P0(3)	T2	D5
L22	TXD_P1(0)/TXD_P0(2)	T4	BE3_DQM3_N
M1	GND IO	T5	D23
M2	WE_SDRAM_N	T6	GND IO
M4	VDD Core	T17	GND Core
M5	D17	T18	GND IO
M18	SMI_MDC	T19	GPIO7
M19	TX_EN_P1/TX_ERR_P0	T21	GPIO0
M21	RXD_P0(1)/RXD_P0(1)	T22	VDD IO
M22	RX_ER_P1/COL_P0	U1	GND Core
N1	BE0_DQM0_N	U2	D6

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Pin Number	Pin Name	Pin Number	Pin Name
U4	VDD Core	W7	VDD Core
U5	GND Core	W8	VDD Core
U6	VDD Core	W9	GPIO28
U7	GND Core	W10	GPIO27
U8	DTR_N	W11	AVDD
U9	GND Core	W12	CLKP_B
U10	AGND	W13	GPIO12/CTS1_N/ ETMEXTOUT
U13	GND Core	W14	VDD Core
U14	GND Core	W15	VDD Core
U15	GPIO14/RXD2	W16	GPIO15/DCD2_N/WDOUT0_N
U16	GND IO	W17	VDD Core
U17	VDD Core	W18	TDI
U18	GND Core	W19	TCK
U19	TMS	W21	DBGREQ
U21	GPIO1	W22	GPIO18/SSPRXD
U22	GND IO	Y1	VDD IO
V1	BE1_DQM1_N	Y2	D10
V2	D7	Y21	PIPESTA0
V4	D24	Y22	GPIO23/SCLKIN/DBGACK
V5	VDD Core	AA1	D11
V6	CS_PER3_N	AA2	D13
V7	GND IO	AA3	D15
V8	OE_DRIVER_N	AA4	D26
V9	GND Core	AA5	D28
V10	GPIO29	AA6	D30
V11	GPIO30	AA7	CS_PER1_N
V12	GPIO31	AA8	RDY_PER_N
V13	GND IO	AA9	WR_N
V14	VDD Core	AA10	GPIO25/TGEN_OUT1_N
V15	GPIO13/TXD2	AA11	GPIO24/PLL_EXT_IN_N
V16	TDO	AA12	F_CLK
V17	GND Core	AA13	CLKP_A
V18	VDD Core	AA14	GPIO17/CTS2_N/SSPOE
V19	TRST_N	AA15	RESET_N
V21	GPIO3	AA16	GPIO22/SFRMIN/TRACEPKT7
V22	GPIO2	AA17	GPIO20/SCLKOUT/TRACEPKT5
W1	D8	AA18	GPIO11/DSR1_N/TRACEPKT3
W2	D9	AA19	GPIO10/DCD1_N/TRACEPKT2
W4	D12	AA20	GPIO8/TXD1/TRACEPKT0
W5	D25	AA21	PIPESTA2
W6	CS_PER2_N	AA22	PIPESTA1

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Pin Number	Pin Name	Pin Number	Pin Name
AB2	D14	AB12	TAP_SEL
AB3	VDD IO	AB13	GND IO
AB4	D27	AB14	GPIO16/DSR2_N/SSPCTLOE/ETMEXTIN1
AB5	D29	AB15	VDD IO
AB6	D31	AB16	TRACECLK
AB7	VDD IO	AB17	GPIO21/SFRMOUT/TRACEPKT6
AB8	CS_PER0_N	AB18	GPIO19/SSPTXD/TRACEPKT4
AB9	RD_N	AB19	VDD IO
AB10	GPIO26	AB20	GPIO9/RXD1/TRACEPKT1
AB11	VDD IO	AB21	TRACESYNC

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1. Pin Functions

1.1 List of Pin Functions

Table 1-1: External Memory Interface Pin Functions

Pin Name	I/O	Function	Alternate Function
A(23:19)	I/O[Note]	External memory address bus (23:19)	CONFIG(4:0)[Note]
A(18:16)	I/O[Note]	External memory address bus (18:16)	BOOT(2:0)[Note]
A(15:0)	O	External memory address bus (15:0)	-
D(31:0)	I/O	External memory data bus (31:0)	-
WR_N	O	Write strobe signal	-
RD_N	O	Read strobe signal	-
CLK_SDRAM	O	Clock to SDRAM	-
CS_SDRAM_N	O	Chip select to SDRAM	-
RAS_SDRAM_N	O	Row address strobe to SDRAM	-
CAS_SDRAM_N	O	Column address strobe to SDRAM	-
WE_SDRAM_N	O	RD/WR signal to SDRAM	-
CS_PER(3:0)_N	O	Chip select to static memories/peripherals	-
BE(3:0)_DQM(3:0)_N	O	Byte enable to static memories/peripherals and SDRAM	-
RDY_PER_N	I	Ready signal from static peripherals	-
DTR_N	O	Direction signal for external driver or scan clock	-
OE_DRIVER_N	O	Enable signal for external driver or scan clock	-

Note: The BOOT(2:0) and CONFIG(4:0) pins are used as inputs and read into the Boot_REG respectively Config_REG system configuration registers during the active RESET phase. After a reset, these pins are available as normal function pins and used as outputs.

Table 1-2: PCI Interface Pin Functions

Pin Name	I/O[Note]	Function	Alternate Function[Note]
AD31	I/O	PCI address/data bit	LBU_CS_R_N
AD(30:29)	I/O	PCI address/data bits	LBU_SEG_(1:0)
AD(28:24)	I/O	PCI address/data bits	LBU_AB(20:16)
AD(23:16)	I/O	PCI address/data bits	LBU_AB(13:6)
AD(15:0)	I/O	PCI address data bits	LBU_DB(15:0)
IDSEL	I	PCI initialization device select	LBU_AB14
CBE3_N	I/O	PCI byte enable	LBU_AB15
CBE2_N	I/O	PCI byte enable	LBU_AB5
CBE1_N	I/O	PCI byte enable	LBU_BE1_N
CBE0_N	I/O	PCI byte enable	LBU_BE0_N
PME_N	I/O	PCI power management	LBU_RDY_N
REQ_N	O	PCI request	LBU_CS_M_N
GNT_N	I	PCI grant	LBU_CFG
CLK_PCI	I	PCI clock	-
RES_PCI_N	I	PCI reset	-
INTA_N	O	PCI INTA_N	LBU_IRQ0_N
INTB_N	O	PCI INTB_N	LBU_IRQ1_N
M66EN	I	PCI clock selection	-
PAR	I/O	PCI parity	LBU_WR_N
SERR_N	I/O	PCI system Error	LBU_POL_RDY
PERR_N	I/O	PCI parity Error	LBU_RD_N
STOP_N	I/O	PCI stop	LBU_AB0
DEVSEL_N	I/O	PCI device select	LBU_AB1
TRDY_N	I/O	PCI target ready	LBU_AB2
IRDY_N	I/O	PCI initiator ready	LBU_AB3
FRAME_N	I/O	PCI cycle frame	LBU_AB4

Note: PCI pins are alternatively used as local bus interface pins; in this table the I/O type is listed for the PCI function.

Table 1-3: Local Bus Interface Pin Functions

Pin Name	I/O[Note]	Function	Alternate Function[Note]
LBU_AB(20:16)	I	LBU address bits	AD(28:24)
LBU_AB15	I	LBU address bit	CBE3_N
LBU_AB14	I	LBU address bit	IDSEL
LBU_AB(13:6)	I	LBU address bits	AD(23:16)
LBU_AB5	I	LBU address bit	CBE2_N
LBU_AB4	I	LBU address bit	FRAME_N
LBU_AB3	I	LBU address bit	IRDY_N
LBU_AB2	I	LBU address bit	TRDY_N
LBU_AB1	I	LBU address bit	DEVSEL_N
LBU_AB0	I	LBU address bit	STOP_N
LBU_DB(15:0)	I/O	LBU data bits	AD(15:0)
LBU_WR_N	I	LBU write control signal	PAR
LBU_RD_N	I	LBU read control signal	PERR_N
LBU_BE(1:0)_N	I	LBU byte enable	CBE(1:0)_N
LBU_SEG_(1:0)	I	LBU page selection signal	AD(30:29)
LBU_IRQ_1_N	O	LBU interrupt request signal	INTB_N
LBU_IRQ_0_N	O	LBU interrupt request signal	INTA_N
LBU_RDY_N	O	LBU ready signal	PME_N
LBU_CS_M_N	I	LBU chip select for ERTEC 400 internal resources	REQ_N
LBU_CS_R_N	I	LBU chip select for page configuration registers	AD31
LBU_CFG	I	LBU RD/WR control selection	GNT_N
LBU_POL_RDY	I	LBU polarity selection for LBU_RDY_N pin	SERR_N

Note: Local bus interface pins are alternatively used as PCI pins; in this table the I/O type is listed for the local bus function.

Table 1-4: RMII Interface Pin Functions

Pin Name[Note]	I/O	Function	Alternate Function[Note]
SMI_MDC	O	SMI clock	SMI_MDC
SMI_MDIO	I/O	SMI input/output	SMI_MDIO
RES_PHY_N	O	Reset PHY	RES_PHY_N
TXD_P0(1:0)	O	Transmit Data Port 0 bits	TXD_P0(1:0)
RXD_P0(1:0)	I	Receive Data Port 0 bits	RXD_P0(1:0)
TX_EN_P0	O	Transmit Enable Port 0	TX_EN_P0
CRS_DV_P0	I	Carrier Sense/Data Valid Port 0	CRS_P0
RX_ER_P0	I	Receive Error Port 0	RX_ER_P0
TXD_P1(1:0)	O	Transmit Data Port 1 bits	TXD_P0(3:2)
RXD_P1(1:0)	I	Receive Data Port 1 bits	RXD_P0(3:2)
TX_EN_P1	O	Transmit Enable Port 1	TX_ERR_P0
CRS_DV_P1	I	Carrier Sense/Data Valid Port 1	RX_DV_P0
RX_ER_P1	I	Receive Error Port 1	COL_P0
TXD_P2(1:0)	O	Transmit Data Port 2 bits	TXD_P1(1:0)
RXD_P2(1:0)	I	Receive Data Port 2 bits	RXD_P1(1:0)
TX_EN_P2	O	Transmit Enable Port 2	TX_EN_P1
CRS_DV_P2	I	Carrier Sense/Data Valid Port 2	CRS_P1
RX_ER_P2	I	Receive Error Port 2	RX_ER_P1
TXD_P3(1:0)	O	Transmit Data Port 3 bits	TXD_P1(3:2)
RXD_P3(1:0)	I	Receive Data Port 3 bits	RXD_P1(3:2)
TX_EN_P3	O	Transmit Enable Port 3	TX_ERR_P1
CRS_DV_P3	I	Carrier Sense/Data Valid Port 3	RX_DV_P1
RX_ER_P3	I	Receive Error Port 3	COL_P1

Note: The alternate functions of RMII pins are MII pins; therefore some pin names are identical for both configurable functions.

Table 1-5: MII Interface Pin Functions

Pin Name[Note]	I/O	Function	Alternate Function[Note]
SMI_MDC	O	Serial management interface clock	SMI_MDC
SMI_MDIO	I/O	Serial management interface data input/output	SMI_MDIO
RES_PHY_N	O	Reset signal to PHYs	RES_PHY_N
TXD_P0(3:2)	O	Transmit data port 0 bits	TXD_P1(1:0)
TXD_P0(1:0)	O	Transmit data port 0 bits	TXD_P0(1:0)
RXD_P0(3:2)	I	Receive data port 0 bits	RXD_P1(1:0)
RXD_P0(1:0)	I	Receive data port 0 bits	RXD_P0(1:0)
TX_EN_P0	O	Transmit enable port 0	TX_EN_P0
CRS_P0	I	Carrier sense port 0	CRS_DV_P0
RX_ER_P0	I	Receive error port 0	RX_ER_P0
TX_ERR_P0	O	Transmit error port 0	TX_EN_P1
RX_DV_P0	I	Receive data valid port 0	CRS_DV_P1
COL_P0	I	Collision port 0	RX_ER_P1
RX_CLK_P0	I	Receive clock port 0	-
TX_CLK_P0	I	Transmit clock port 0	-
TXD_P1(3:2)	O	Transmit data port 1 bits	TXD_P3(1:0)
TXD_P1(1:0)	O	Transmit data port 1 bits	TXD_P2(1:0)
RXD_P1(3:2)	I	Receive data port 1 bits	RXD_P3(1:0)
RXD_P1(1:0)	I	Receive data port 1 bits	RXD_P2(1:0)
TX_EN_P1	O	Transmit enable port 1	TX_EN_P2
CRS_P1	I	Carrier sense port 1	CRS_DV_P2
RX_ER_P1	I	Receive error port 1	RX_ER_P2
TX_ERR_P1	O	Transmit error port 1	TX_EN_P3
RX_DV_P1	I	Receive data valid port 1	CRS_DV_P3
COL_P1	I	Collision port 1	RX_ER_P3
RX_CLK_P1	I	Receive clock port 1	-
TX_CLK_P1	I	Transmit clock port 1	-

Note: The alternate functions of MII pins are RMII pins; therefore some pin names are identical for both configurable functions.

Table 1-6: General Purpose I/O Pin Functions

Pin Name	I/O[Note]	Function	Alternate Function[Note]
GPIO(31:26)	I/O	General purpose I/O signal	-
GPIO25	I/O	General purpose I/O signal	TGEN_OUT1_N
GPIO24	I/O	General purpose I/O signal	PLL_EXT_IN_N
GPIO23	I/O	General purpose I/O signal	SCLKIN, DBGACK
GPIO22	I/O	General purpose I/O signal	SFRMIN, TRACEPKT7
GPIO21	I/O	General purpose I/O signal	SFRMOUT, TRACEPKT6
GPIO20	I/O	General purpose I/O signal	SCLKOUT, TRACEPKT5
GPIO19	I/O	General purpose I/O signal	SSPTXD, TRACEPKT4
GPIO18	I/O	General purpose I/O signal	SSPRXD
GPIO17	I/O	General purpose I/O signal	CTS2_N, SSPOE
GPIO16	I/O	General purpose I/O signal	DSR2_N, SSPCTLOE, ETMEXTIN1
GPIO15	I/O	General purpose I/O signal	DCD2_N, WDOUT0_N
GPIO14	I/O	General purpose I/O signal	RXD2
GPIO13	I/O	General purpose I/O signal	TXD2
GPIO12	I/O	General purpose I/O signal	CTS1_N, ETMEXTOUT
GPIO11	I/O	General purpose I/O signal	DSR1_N, TRACEPKT3
GPIO10	I/O	General purpose I/O signal	DCD1_N, TRACEPKT2
GPIO9	I/O	General purpose I/O signal	RXD1, TRACEPKT1
GPIO8	I/O	General purpose I/O signal	TXD1, TRACEPKT0
GPIO(7:0)	I/O	General purpose I/O signal	-

Note: Function and alternative functions are selected with the GPIO_PORT_MODE_H and GPIO_PORT_MODE_L registers. In this table the I/O types are listed for the GPIO function.

Table 1-7: UART1 and UART2 Pin Functions

Pin Name	I/O[Note]	Function	Alternate Function[Note]
TXD1	O	UART1 transmit data output	GPIO8, TRACEPKT0
RXD1	I	UART1 receive data input	GPIO9, TRACEPKT1
DCD1_N	I	UART1 carrier detection signal	GPIO10, TRACEPKT2
DSR1_N	I	UART1 data set ready signal	GPIO11, TRACEPKT3
CTS1_N	I	UART1 transmit enable signal	GPIO12, ETMEXTOUT
TXD2	O	UART2 transmit data output	GPIO13
RXD2	I	UART2 receive data input	GPIO14
DCD2_N	I	UART2 carrier detection signal	GPIO15, WDOUT0_N
DSR2_N	I	UART2 data set ready signal	GPIO16, SSPCTLOE, ETMEXTIN1
CTS2_N	I	UART2 transmit enable signal	GPIO17, SSPOE

Note: Function and alternative functions are selected with the registers GPIO_PORT_MODE_H and GPIO_PORT_MODE_L. In this table the I/O types are listed for the UART1 and UART2 functions.

Table 1-8: SPI Pin Functions

Pin Name	I/O[Note]	Function	Alternate Function[Note]
SSPRXD	I	SPI receive data input	GPIO18
SSPTXD	O	SPI transmit data output	GPIO19, TRACEPKT4
SCLKOUT	O	SPI clock output	GPIO20, TRACEPKT5
SFRMOUT	O	SPI serial frame input signal	GPIO21, TRACEPKT6
SFRMIN	I	SPI serial frame output signal	GPIO22, TRACEPKT7
SCLKIN	I	SPI clock input	GPIO23, DBGACK
SSPCTLOE	O	SPI clock and serial frame output enable	GPIO16, DSR2_N, ETMEXTIN1
SSPOE	O	SPI output enable	GPIO17, CTS2_N

Note: Function and alternative functions are selected with the GPIO_PORT_MODE_H register. In this table the I/O types are listed for the SPI function.

Table 1-9: MC_PLL Pin Functions

Pin Name	I/O[Note 1]	Function	Alternate Function[Note 1]
PLL_EXT_IN_N	I	MC_PLL input signal	GPIO24
TGEN_OUT1_N	O	MC_PLL output signal[Note 2]	GPIO25

Notes: 1. Function and alternative functions are selected with the GPIO_PORT_MODE_H register. In this table the I/O types are listed for the MC_PLL function.

2. For a PROFINET IRT application, GPIO25 must be configured as TGEN_OUT1_N output pin. A synchronous clock signal is then output at this pin; during certification of a PROFINET IO device with IRT support this signal must be accessible from the outside.

Table 1-10: Clock and Reset Pin Functions

Pin Name	I/O	Function	Alternate Function
TRACECLK	O	ETM trace or scan clock	-
CLKP_A	I	Quartz connection	-
CLKP_B	O	Quartz connection	-
F_CLK	I	F_CLK for F-counter	-
REF_CLK	I	Reference clock	-
RESET_N	I	Hardware reset	-

Table 1-11: JTAG and Debug Interface Pin Functions

Pin Name	I/O[Note]	Function	Alternate Function[Note]
TRST_N	I	JTAG reset signal	-
TCK	I	JTAG clock signal	-
TDI	I	JTAG data input signal	-
TMS	I	JTAG test mode select signal	-
TDO	O	JTAG data output signal	-
DBGREQ	I	Debug request signal	-
DBGACK	O	Debug acknowledge signal	GPIO23/SCLKIN
TAP_SEL	I	TAP controller select signal	-

Note: The DBGACK pin is alternatively used as GPIO or SPI pin; the function is selected with the GPIO_PORT_MODE_H register. In this table the I/O type is listed for the DBGACK function.

Table 1-12: Trace Port Pin Functions

Pin Name	I/O[Note]	Function	Alternate Function[Note]
TRACEPKT7	O	Trace packet bit	GPIO22/SFRMIN
TRACEPKT6	O	Trace packet bit	GPIO21/SFRMOUT
TRACEPKT5	O	Trace packet bit	GPIO20/SCLKOUT
TRACEPKT4	O	Trace packet bit	GPIO19/SSPTXD
TRACEPKT3	O	Trace packet bit	GPIO11/DSR1_N
TRACEPKT2	O	Trace packet bit	GPIO10/DCD1_N
TRACEPKT1	O	Trace packet bit	GPIO9/RXD1
TRACEPKT0	O	Trace packet bit	GPIO8/TXD1
PIPESTA(2:0)	O	CPU pipeline status	-
TRACESYNC	O	Trace sync signal	-
ETMEXTIN1	I	External input to the ETM	GPIO16/DSR2_N/SSPCTLOE
ETMEXTOUT	O	Output signal from the ETM	GPIO12/CTS1_N

Note: Several trace port pins are alternatively used as GPIO, UART or SPI pins; the function is selected with the GPIO_PORT_MODE_H and GPIO_PORT_MODE_L registers. In this table the I/O types are listed for the trace port pin functions.

Table 1-13: Power Supply Pin Functions

Pin Name	Function
VDD Core	Power supply for core, 1.5 V
GND Core	GND for core
VDD IO	Power supply for IO, 3.3 V
GND IO	GND for IO
P5V_PCI	Power supply for PCI, 5V [Note]
AVDD	Analog power supply for PLL, 1.5 V
AGND	Analog GND for PLL
AVDD_PCI	Analog power supply for PLL in PCI I/F, 1.5 V
AGND_PCI	Analog GND for PLL in PCI I/F

Note: In PCI mode the P5V_PCI pins must be connected to the PCI bus supply pins $+V_{IO}$ (name according to PCI specification). In LBU mode the P5V_PCI pins must be connected to VDD IO.

1.2 Pin Characteristics

Table 1-14: Pin Characteristics (1/2)

Pin Name	I/O	Input type	Output type	Internal pull up/down	Drive capability	
					I_{OH}	I_{OL}
A(23:16)	I/O[Note 1]	Schmitt[Note 1]	3.3 V CMOS	-	9 mA	9 mA
A(15:0)	O	-	3.3 V CMOS	-	9 mA	9 mA
D(31:0)	I/O	Schmitt	3.3 V CMOS	50 kΩ pull up	9 mA	9 mA
WR_N	O	-	3.3 V CMOS	-	9 mA	9 mA
RD_N	O	-	3.3 V CMOS	-	9 mA	9 mA
CLK_SDRAM	O	-	3.3 V CMOS	-	9 mA	9 mA
CS_SDRAM_N	O	-	3.3 V CMOS	-	9 mA	9 mA
RAS_SDRAM_N	O	-	3.3 V CMOS	-	9 mA	9 mA
CAS_SDRAM_N	O	-	3.3 V CMOS	-	9 mA	9 mA
WE_SDRAM_N	O	-	3.3 V CMOS	-	9 mA	9 mA
CS_PER(3:0)_N	O	-	3.3 V CMOS	-	6 mA	6 mA
BE(3:0)_DQM(3:0)_N	O	-	3.3 V CMOS	-	9 mA	9 mA
RDY_PER_N	I	Schmitt	-	50 kΩ pull up	-	-
DTR_N	O	-	3.3 V CMOS	-	9 mA	9 mA
OE_DRIVER_N	O	-	3.3 V CMOS	-	9 mA	9 mA
AD(31:0)	I/O	PCI[Note 2]	PCI[Note 2]	-	PCI[Note 2]	
IDSEL	I	PCI[Note 2]	-	-		
CBE(3:0)_N	I/O	PCI[Note 2]	PCI[Note 2]	-		
PME_N	I/O	PCI[Note 2]	PCI[Note 2]	-		
REQ_N	O	-	PCI[Note 2]	-		
GNT_N	I	PCI[Note 2]	-	-		
CLK_PCI	I	PCI[Note 2]	-	-		
RES_PCI_N	I	PCI[Note 2]	-	-		
INTA_N	O	-	PCI[Note 2]	-		
INTB_N	O	-	PCI[Note 2]	-		
M66EN	I	Schmitt	-	-	-	-
PAR	I/O	PCI[Note 2]	PCI[Note 2]	-	PCI[Note 2]	
SERR_N	I/O	PCI[Note 2]	PCI[Note 2]	-		
PERR_N	I/O	PCI[Note 2]	PCI[Note 2]	-		
STOP_N	I/O	PCI[Note 2]	PCI[Note 2]	-		
DEVSEL_N	I/O	PCI[Note 2]	PCI[Note 2]	-		
TRDY_N	I/O	PCI[Note 2]	PCI[Note 2]	-		
IRDY_N	I/O	PCI[Note 2]	PCI[Note 2]	-		
FRAME_N	I/O	PCI[Note 2]	PCI[Note 2]	-		

Notes: 1. The address pins A(23:16) are used as inputs only during the active reset phase.

2. PCI I/Os can be either 3.3 V PCI (if the PCI interface is operated with 3.3 V) or 5 V tolerant PCI (if the PCI interface is configured to 5 V tolerant operation). Please check Tables 2-1 and 2-2 for differences. Drive capability complies to the PCI specification R2.2.

Table 1-14: Pin Characteristics (2/2)

Pin Name	I/O	Input type	Output type	Internal pull up/down	Drive capability	
					I_{OH}	I_{OL}
PIPESTA(2:0)	O	-	3.3 V CMOS	-	9 mA	9 mA
TRACESYNC	O	-	3.3 V CMOS	-	9 mA	9 mA
SMI_MDC	O	-	3.3 V CMOS	-	6 mA	6 mA
SMI_MDIO	I/O	Schmitt	3.3 V CMOS	-	6 mA	6 mA
RES_PHY_N	O	-	3.3 V CMOS	-	6 mA	6 mA
TXD_Pn(1:0)**Note 1**	O	-	3.3 V CMOS	-	6 mA	6 mA
RXD_Pn(1:0)**Note 1**	I	Schmitt	-	50 kΩ pull down	-	-
TX_EN_Pn**Note 1**	O	-	3.3 V CMOS	-	6 mA	6 mA
CRS_DV_Pn**Note 1**	I	Schmitt	-	50 kΩ pull down	-	-
RX_ER_Pn**Note 1**	I	Schmitt	-	50 kΩ pull down	-	-
TXD_Pn(3:0)**Note 2**	O	-	3.3 V CMOS	-	6 mA	6 mA
RXD_Pn(3:0)**Note 2**	I	Schmitt	-	50 kΩ pull down	-	-
TX_EN_Pn**Note 2**	O	-	3.3 V CMOS	-	6 mA	6 mA
CRS_Pn**Note 2**	I	Schmitt	-	50 kΩ pull down	-	-
RX_ER_Pn**Note 2**	I	Schmitt	-	50 kΩ pull down	-	-
TX_ERR_Pn**Note 2**	O	-	3.3 V CMOS	-	6 mA	6 mA
RX_DV_Pn**Note 2**	I	Schmitt	-	50 kΩ pull down	-	-
COL_Pn**Note 2**	I	Schmitt	-	50 kΩ pull down	-	-
RX_CLK_Pn**Note 2**	I	Schmitt	-	50 kΩ pull down	-	-
TX_CLK_Pn**Note 2**	I	Schmitt	-	50 kΩ pull down	-	-
GPIO(31:23)	I/O	Schmitt	3.3 V CMOS	50 kΩ pull up	6 mA	6 mA
GPIO(22:19)	I/O	Schmitt	3.3 V CMOS	50 kΩ pull up	9 mA	9 mA
GPIO(18:12)	I/O	Schmitt	3.3 V CMOS	50 kΩ pull up	6 mA	6 mA
GPIO(11:0)	I/O	Schmitt	3.3 V CMOS	50 kΩ pull up	9 mA	9 mA
TRACECLK	O	-	3.3 V CMOS	-	18 mA	18 mA
CLKP_A	I	Osc. in	-	-	-	-
CLKP_B	O	-	Osc. out	-	6 mA	6 mA
F_CLK	I	3.3 V CMOS	-	-	-	-
REF_CLK	I	3.3 V CMOS	-	-	-	-
RESET_N	I	Schmitt	-	50 kΩ pull up	-	-
TRST_N	I	Schmitt	-	-	-	-
TCK	I	Schmitt	-	50 kΩ pull up	-	-
TDI	I	Schmitt	-	50 kΩ pull up	-	-
TMS	I	Schmitt	-	50 kΩ pull up	-	-
TDO	O	-	3.3 V CMOS	-	6 mA	6 mA
DBGREQ	I	Schmitt	-	50 kΩ pull down	-	-
TAP_SEL	I	Schmitt	-	50 kΩ pull up	-	-

Notes: 1. The number “n” can take the integer values 0 to 3 and refers to the RMII ports.

2. The number “n” can take the integer values 0 and 1 and refers to the MII ports.

Remark: Shared pins are not listed with all possible pin names. Please check Tables 1-1 to 1-13 for possible pin names first, before looking up pin characteristics in Table 1-14.

1.3 Pin Status and Recommended Connections

Table 1-15: Pin Status During Reset and Recommended Connections (1/3)

Pin Name	I/O	Internal pull up/down	I/O during reset	Level during reset	External pull up/down required
A(23:16)	I/O[Note 1]	-	I[Note 1]	-	[Note 1]
A(15:0)	O	-	O	L	-
D(31:0)	I/O	50 kΩ pull up	I	H	-
WR_N	O	-	O	H	-
RD_N	O	-	O	H	-
CLK_SDRAM	O	-	O	L	-
CS_SDRAM_N	O	-	O	H	-
RAS_SDRAM_N	O	-	O	H	-
CAS_SDRAM_N	O	-	O	H	-
WE_SDRAM_N	O	-	O	H	-
CS_PER(3:0)_N	O	-	O	H	-
BE(3:0)_DQM(3:0)_N	O	-	O	H	-
RDY_PER_N	I	50 kΩ pull up	I	H	-
DTR_N	O	-	O	H	-
OE_DRIVER_N	O	-	O	H	-
AD(31:0)	I/O	-	I	-	Pull up[Note 2]
IDSEL	I	-	I	-	Pull up[Note 2]
CBE(3:0)_N	I/O	-	I	-	Pull up[Note 2]
PME_N[Note 3]	I/O	-	I	H	Pull up[Note 4]
REQ_N[Note 3]	O	-	tri-state	-	Pull up[Note 2, 4]
GNT_N[Note 3]	I	-	I	-	Pull up[Note 2, 4]
CLK_PCI[Note 3]	I	-	I	-	Pull down[Note 2, 5]
RES_PCI_N	I	-	I	-	Pull up[Note 2, 4, 5]
INTA_N[Note 3]	O	-	tri-state	H	Pull up[Note 4]
INTB_N[Note 3]	O	-	tri-state	H	Pull up[Note 4]
M66EN[Note 3]	I	-	I	-	Pull down[Note 2, 5]
PAR[Note 3]	I/O	-	I	-	Pull up[Note 2]
SERR_N[Note 3]	I/O	-	I	H	Pull up[Note 2, 4]
PERR_N[Note 3]	I/O	-	I	-	Pull up[Note 2, 4]
STOP_N[Note 3]	I/O	-	I	-	Pull up[Note 2, 4]

Notes: 1. The address pins A(23:16) are used as inputs only during the active reset phase in order to read the devices proper start up configurations. A(23:16) must therefore be equipped with external pull up/down resistors according to the desired start up configuration. Please consult the user's manual for details.

2. These resistors are required, when neither the PCI interface nor the LBU interface are used. In this case ERTEC 400 must be configured to LBU mode (CONFIG2 = 0_b).

3. The reset signal, that affects these pins, is RES_PCI_N.

4. These pull-up resistors are required, when the interface is operated in PCI mode.

5. These resistors are required, when the interface is operated in LBU mode.

Table 1-15: Pin Status During Reset and Recommended Connections (2/3)

Pin Name	I/O	Internal pull up/down	I/O during reset	Level during reset	External pull up/down required
DEVSEL_N[Note 1]	I/O	-	I	-	Pull up[Note 2, 4]
TRDY_N[Note 1]	I/O	-	I	-	Pull up[Note 2, 4]
IRDY_N[Note 1]	I/O	-	I	-	Pull up[Note 2, 4]
FRAME_N[Note 1]	I/O	-	I	-	Pull up[Note 4]
PIPESTA(2:0)	O	-	O	L	-
TRACESYNC	O	-	O	L	-
SMI_MDC	O	-	O	L	-
SMI_MDIO	I/O	-	I	H	Pull up
RES_PHY_N	O	-	O	L	-
TXD_Pn(1:0)[Note 3]	O	-	O	L	-
RXD_Pn(1:0)[Note 3]	I	50 kΩ pull down	I	L	-
TX_EN_Pn[Note 3]	O	-	O	L	-
CRS_DV_Pn[Note 3]	I	50 kΩ pull down	I	L	-
RX_ER_Pn[Note 3]	I	50 kΩ pull down	I	L	-
TXD_Pn(3:0)[Note 5]	O	-	O	L	-
RXD_Pn(3:0)[Note 5]	I	50 kΩ pull down	I	L	-
TX_EN_Pn[Note 5]	O	-	O	L	-
CRS_Pn[Note 5]	I	50 kΩ pull down	I	L	-
RX_ER_Pn[Note 5]	I	50 kΩ pull down	I	L	-
TX_ERR_Pn[Note 5]	O	-	O	L	-
RX_DV_Pn[Note 5]	I	50 kΩ pull down	I	L	-
COL_Pn[Note 5]	I	50 kΩ pull down	I	L	-
RX_CLK_Pn[Note 5]	I	50 kΩ pull down	I	L	-
TX_CLK_Pn[Note 5]	I	50 kΩ pull down	I	L	-
GPIO(31:0)	I/O	50 kΩ pull up	I	H	-
TRACECLK	O	-	O	L	-
CLKP_A	I	-	I	-	-
CLKP_B	O	-	O	-	-
F_CLK	I	-	I	-	-
REF_CLK	I	-	I	-	-
RESET_N	I	50 kΩ pull up	I	L[Note 6]	-

Notes: 1. The reset signal, that affects these pins is RES_PCI_N.

2. These resistors are required, when neither the PCI interface nor the LBU interface are used. In this case ERTEC 400 must be configured to LBU mode (CONFIG2 = 0_b).

3. The number “n” can take the integer values 0 to 3.

4. These pull-up resistors are required, when the interface is operated in PCI mode.

5. The number “n” can take the integer values 0 and 1.

6. RESET_N must be externally driven low in order to reset the device.

Table 1-15: Pin Status During Reset and Recommended Connections (3/3)

Pin Name	I/O	Internal pull up/down	I/O during reset	Level during reset	External pull up/down required
TRST_N	I	-	I	H[Note 1]	Pull up
TCK[Note 2]	I	50 kΩ pull up	I	H	-
TDI[Note 2]	I	50 kΩ pull up	I	H	-
TMS[Note 2]	I	50 kΩ pull up	I	H	-
TDO[Note 2]	O	-	O	L	-
DBGREQ	I	50 kΩ pull down	I	L	-
TAP_SEL	I	50 kΩ pull up	I	H	-

Notes: 1. High level is generated from external pull up resistor and not by internal device circuitry.

2. The reset signal, that affects these pins, is TRST_N.

Remark: Shared pins are not listed with all possible pin names. Please check Tables 1-1 to 1-13 for possible pin names first, before looking up reset characteristics and recommended connections in Table 1-15.

2. Electrical Specifications

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter		Symbol	Ratings	Unit
Supply voltage	1.5 V supply	VDD Core	-0.5 to +2.0	V
	3.3 V supply	VDD IO	-0.5 to +4.6	V
	PLL supply	AVDD, AVDD_PCI	-0.5 to +2.0	V
Input voltage	3.3 V CMOS, V_I < VDD + 0.5 V	V_I	-0.5 to+ 4.6	V
	3.3 V PCI, V_I < VDD + 0.5 V		-0.5 to 5.1	V
	5 V tol. PCI		-0.6 to VDD IO + 2.4	V
Junction temperature		T_J	-40 to +120	°C
Storage temperature		T_{STG}	-65 to +150	°C

Caution: Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Remark: 3.3 V must be applied to the I/O pins only after applying the power supply voltage.

2.2 Operating Conditions

Table 2-2: Recommended Operating Conditions (1/2)

Parameter		Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	1.5 V supply	VDD Core		1.35	1.5	1.65	V
	3.3 V supply	VDD IO		3.0	3.3	3.6	V
	5V supply **Note**	P5V_PCI		4.75	5	5.25	V
	PLL supply	AVDD, AVDD_PCI		1.35	1.5	1.65	V
Ambient temperature		T_A		-40		+85	°C
Output voltage high	3.3 V CMOS	V_{OH}	I_{OH} = 0 mA	VDD IO - 0.1 V			V
			nominal output current	2.4			V
	3.3 V PCI		I_{OH} = -0.5 mA	0.9 x VDD IO			V
	5 V tol. PCI		I_{OH} = -2 mA	2.4			V
Output voltage low	3.3 V CMOS	V_{OL}	I_{OL} = 0 mA			0.1	V
			nominal output current			0.4	V
	3.3 V PCI		I_{OH} = 1.5 mA			0.1 x VDD IO	V
	5 V tol. PCI		I_{OH} = 3 mA			0.55	V
Input voltage high	3.3 V CMOS	V_{IH}		2		VDD IO	V
	3.3 V PCI			0.5 x VDD IO		VDD IO + 0.5 V	V
	5 V tol. PCI			2		P5V_PCI + 0.5 V	V
Input voltage low	3.3 V CMOS	V_{IL}		0		0.8	V
	3.3 V PCI			-0.5		0.3 x VDD IO	V
	5 V tol. PCI			-0.5		0.8	V
Positive trigger voltage	Schmitt input	V_P		1.2		2.4	V
Negative trigger voltage		V_N		0.6		1.8	V
Hysteresis voltage		V_H		0.3		1.5	V
Input rise time	3.3 V CMOS	t_{RI}		0		200	ns
Input fall time		t_{FI}		0		200	ns
Input rise time	Schmitt input	t_{RI}		0		10	ms
Input fall time		t_{FI}		0		10	ms

Note: This condition applies only, if the PCI interface is actually operated at 5 V.

Table 2-2: Recommended Operating Conditions (2/2)

Parameter		Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Pull up resistor (nominal 50 kΩ)				14.2	31.9	80.7	kΩ
Pull down resistor (nominal 50 kΩ)				20.6	44.9	116.4	kΩ
CPU clock frequency[Note 1]		PFC			150		MHz
Oscillator clock frequency[Note 2]		PLL_FC		12.5 - 50 ppm	12.5	12.5 + 50 ppm	MHz
Reference clock frequency[Note 3]		REF_PLL_FC		50 - 50 ppm	50	50 + 50 ppm	MHz
MII transmit/receive clock frequency[Note 4]		PHY_Tx/ Rx_M_FC		2.5		25	MHz
Supply current[Note 5, 6]	1.5 V supply	IDD Core			300	495	mA
	3.3 V supply	IDD IO			80	145	mA
Power consumption[Note 5, 6]	1.5 V supply	PDD Core			450	740	mW
	3.3 V supply	PDD IO			265	470	mW
	total	PDD			715	1210	mW

Notes: 1. The CPU clock is an internal signal. Different CPU core operation frequencies can be selected via hardware settings during reset; possible settings are 50/100/150 MHz.

2. The oscillator clock is present at the CLKP_A and CLKP_B pins.

3. The reference clock must be applied to the REF_CLK pin. If ERTEC 400 is operated in RMII mode, the reference clock is also used for the RMII interface.

4. The MII transmit/receive clock must be applied to the RX_CLK_P(1:0) and TX_CLK_P(1:0) pins, if ERTEC 400 is operated in MII mode. It is not required in RMII mode.

5. Typical values for supply currents and power consumption have been measured under the following conditions:

- Operation of ERTEC 400 on the EB400 evaluation board with 150 MHz core clock frequency
- SDRAM test program and Ethernet traffic running
- No activity on PCI respectively LBU interfaces

6. Maximum values for supply currents and power consumption have been calculated for VDD IO = 3.6 V and VDD Core = 1.65 V at T_A = 85°C.

2.3 Thermal Characteristics

Table 2-3: Thermal Characteristics of Package

Parameter	Symbol	Airflow (m/s)				Unit
		0	0.2	1	2	
Thermal resistance junction to ambient**Note 1**	Θ_{ja}	30	27	23	21	K/W
Thermal resistance junction to top center of the package surface**Note 1**	Ψ_{jt}	0.2	0.3	0.6	0.8	K/W
Thermal resistance top center of the package surface to ambient**Note 1**	Ψ_{ta}	29.8	26.7	22.4	20.2	K/W
Thermal resistance junction to case**Note 2**	Θ_{jc}	5.2	5.2	5.2	5.2	K/W
Maximum case temperature	T_{cmax}	105				°C

Notes: 1. The parameters are valid, if no heat sink is used and a PCB with at least 4 layers and massive ground and power planes.

2. The parameter is valid, if a heat sink is used.

2.4 AC Characteristics

2.4.1 Clock timing

T_A = -40 to +85°C, V_{DDCore} = 1.35 V ~ 1.65 V, V_{DDIO} = 3.0 V ~ 3.6 V

Table 2-4: Clock AC Characteristics (1/2)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Processor clock frequency[Note 1]	PFC		50/100/ 150		MHz
Processor clock period[Note 1]	PTC		20/10/ 6.66		ns
Oscillator clock frequency	PLL_FC	12.5 - 50 ppm	12.5	12.5 + 50 ppm	MHz
Reference clock frequency	REF_PLL_FC	50 - 50 ppm	50	50 + 50 ppm	MHz
PCIClk input frequency	PCI_FC			66.66	MHz
PCIClk input period	PCI_TC	15			ns
PCIClk input high time[Note 2]	PCI_TCH	40		60	%
PCIClk input low time[Note 2]	PCI_TCL	40		60	%
JTAGClk frequency	JTAG_FC			10	MHz
JTAGClk period	JTAG_TC	100			ns
MII transmit clock frequency	PHY_Tx_M_FC	2.5		25	MHz
MII transmit clock period	PHY_Tx_M_TC	40		400	ns
MII transmit clock input high time[Note 2]	PHY_Tx_M_TCH	35			%
MII transmit clock input low time[Note 2]	PHY_Tx_M_TCL	35			%
MII receive clock frequency	PHY_Rx_M_FC	2.5		25	MHz
MII receive clock period	PHY_Rx_M_TC	40		400	ns
MII receive clock input high time[Note 2]	PHY_Rx_M_TCH	35			%
MII receive clock input low time[Note 2]	PHY_Rx_M_TCL	35			%
SPI1_SCLKIN frequency (slave mode)	SPI1_S_FC	0		4.16	MHz
SPI1_SCLKIN low time (slave mode)	SPI1_S_TCL	120			ns
SPI1_SCLKIN high time (slave mode)	SPI1_S_TCH	120			ns
SPI1_SCLKOUT frequency (master mode)	SPI1_M_FC	769×10^{-6}		25	MHz
SPI1_SCLKOUT period (master mode)	SPI1_M_TC	40		1.3×10^{6}	ns
SPI1_SCLKOUT low time (master mode)[Note 2]	SPI1_M_TCL	45		55	%
SPI1_SCLKOUT high time (master mode)[Note 2]	SPI1_M_TCH	45		55	%

Notes: 1. The actually permitted maximum clock frequency respectively minimum clock period is given by the CONFIG(4:3) pin setting during reset and depends additionally on the accuracy of the oscillator clock.

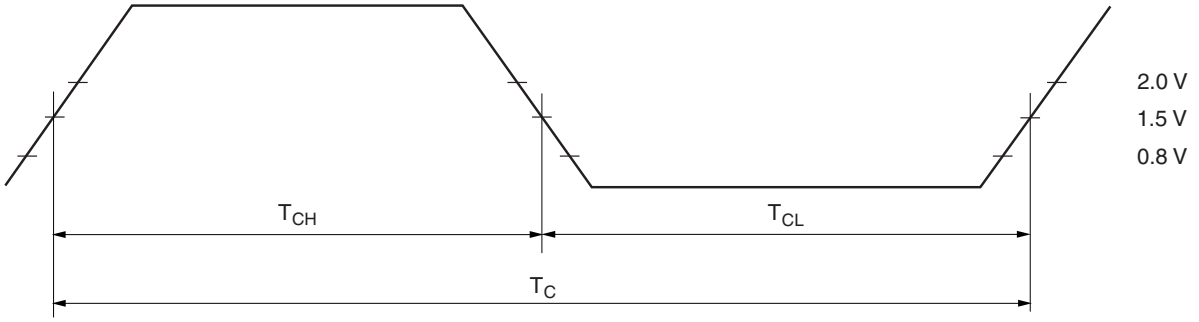
2. High time and low time are specified in per cent of the nominal clock period.

Table 2-4: Clock AC Characteristics (2/2)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
CLK_SDRAM frequency	SDRAM_FC			50	MHz
CLK_SDRAM period	SDRAM_TC	20			ns
CLK_SDRAM clock stability	SDRAM_TCS			+/- 0.2	ns
CLK_SDRAM input high time[Note]	SDRAM_TCH	40		60	%
CLK_SDRAM input low time[Note]	SDRAM_TCL	40		60	%

Note: High time and low time are specified in per cent of the nominal clock period.

Figure 2-1: Clock Waveforms



2.4.2 I/O timing specifications

T_A = -40 to +85°C, V_{DDCore} = 1.35 V ~ 1.65 V, V_{DDIO} = 3.0 V ~ 3.6 V

Table 2-5: I/O Timing Specifications (1/2)

Signal	Input		Output		Unit	Clock	Notes
	Setup time T_{IS} min.	Hold time T_{IH} min.	Valid delay T_{OV} max.	Hold time T_{OH}min.			
D(31:0)	10	0	12.5	2	ns	CLK_SDRAM	6
A(23:0)			11	2	ns	CLK_SDRAM	6
BE(3:0)_DQM_N(3:0)			11	2	ns	CLK_SDRAM	6
CAS_SDRAM_N			11	2	ns	CLK_SDRAM	5
RAS_SDRAM_N			11	2	ns	CLK_SDRAM	5
WE_SDRAM_N			11	2	ns	CLK_SDRAM	5
CS_SDRAM_N			11	2	ns	CLK_SDRAM	5
AD(31:0)	7/3	0	11/6	2/1	ns	PCI_CLK	1, 7
CBE_N(3:0)	7/3	0	11/6	2/1	ns	PCI_CLK	1, 7
PAR	7/3	0	11/6	2/1	ns	PCI_CLK	1, 7
SERR_N	7/3	0	11/6	2/1	ns	PCI_CLK	1, 7
PERR_N	7/3	0	11/6	2/1	ns	PCI_CLK	1, 7
STOP_N	7/3	0	11/6	2/1	ns	PCI_CLK	1, 7
DEVSEL_N	7/3	0	11/6	2/1	ns	PCI_CLK	1, 7
TRDY_N	7/3	0	11/6	2/1	ns	PCI_CLK	1, 7
IRDY_N	7/3	0	11/6	2/1	ns	PCI_CLK	1, 7
FRAME_N	7/3	0	11/6	2/1	ns	PCI_CLK	1, 7
IDSEL	7/3	0	11/6	2/1	ns	PCI_CLK	1, 7
GNT_N	10/5	0			ns	PCI_CLK	1, 7
REQ_N			12/6	2/1	ns	PCI_CLK	1
TRACESYNC			Tc - 3	2	ns	TRACECLK	3, 4
PIPESTA(2:0)			Tc - 3	2	ns	TRACECLK	3, 4
TRACEPKT(7:0)			Tc - 3	2	ns	TRACECLK	3, 4

Notes: 1. Timing parameters are given for 33 MHz and 66 MHz PCI clock frequency (<for 33 MHz> / <for 66 MHz>). The available frequencies are between 0 - 33 MHz, if M66_EN is pulled to VDD and between 33 - 66 MHz, if M66_EN is pulled to GND.

2. Ethernet Signals in MII Mode and in RMII corresponding to the Ethernet mode of the ERTEC 400 (Available are 2 Port-MII or 4 Port-RMII).

3. If the trace interface is operated in half rate mode, Tc corresponds to the distance between a rising and the subsequent falling edge of TRACECLK; if the trace interface is operated in full rate mode, Tc corresponds to a full period of the trace clock TRACECLK.

4. Minimum hold time is measured with 10 pF load and maximum valid delay is measured with 10 pF load.

5. Minimum hold time is measured with 10 pF load and maximum valid delay is measured with 30 pF load.

6. Minimum hold time is measured with 10 pF load and maximum valid delay is measured with 50 pF load.

7. Minimum hold time for 33 MHz PCI is measured at 10 pF and maximum valid delay is measured at 50 pF; minimum hold time for 66 MHz PCI is measured at 10 pF and maximum valid delay is measured at 40 pF load.

Table 2-5: I/O Timing Specifications (2/2)

Signal	Input		Output		Unit	Clock	Notes
	Setup time T_{IS} min.	Hold time T_{IH} min.	Valid delay T_{OV} max.	Hold time T_{OH}min.			
MDIO	10	10	30	10	ns	MDC	6
RXD(3:0)	4	1			ns	RX_CLK	2
RX_DV	4	1			ns	RX_CLK	2
RX_ER	4	1			ns	RX_CLK	2
TXD(3:0)			14	2	ns	TX_CLK	2, 5
TX_EN			14	2	ns	TX_CLK	2, 5
TX_ER			14	2	ns	TX_CLK	2, 5
RXD(1:0)	4	1			ns	REF_CLK	2
CRS_DV	4	1			ns	REF_CLK	2
RX_ER	4	1			ns	REF_CLK	2
TXD(1:0)			13	2	ns	REF_CLK	2, 5
TX_EN			13	2	ns	REF_CLK	2, 5

Notes: 1. Timing parameters are given for 33 MHz and 66 MHz PCI clock frequency (<for 33 MHz> / <for 66 MHz>). The available frequencies are between 0 - 33 MHz, if M66_EN is pulled to VDD and between 33 - 66 MHz, if M66_EN is pulled to GND.

2. Ethernet Signals in MII Mode and in RMII corresponding to the Ethernet mode of the ERTEC 400 (Available are 2 Port-MII or 4 Port-RMII).

3. If the trace interface is operated in half rate mode, Tc corresponds to the distance between a rising and the subsequent falling edge of TRACECLK; if the trace interface is operated in full rate mode, Tc corresponds to a full period of the trace clock TRACECLK.

4. Minimum hold time is measured with 10 pF load and maximum valid delay is measured with 10 pF load.

5. Minimum hold time is measured with 10 pF load and maximum valid delay is measured with 30 pF load.

6. Minimum hold time is measured with 10 pF load and maximum valid delay is measured with 50 pF load.

7. Minimum hold time for 33 MHz PCI is measured at 10 pF and maximum valid delay is measured at 50 pF; minimum hold time for 66 MHz PCI is measured at 10 pF and maximum valid delay is measured at 40 pF load.

Figure 2-2: Input Setup and Hold Waveforms

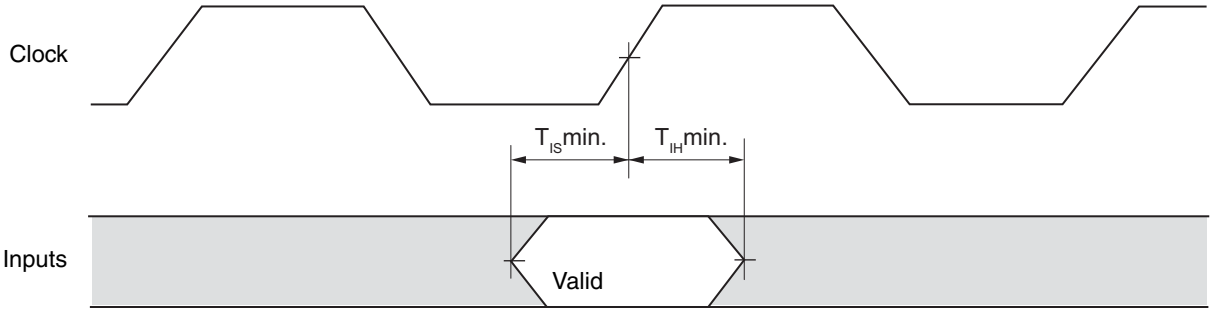
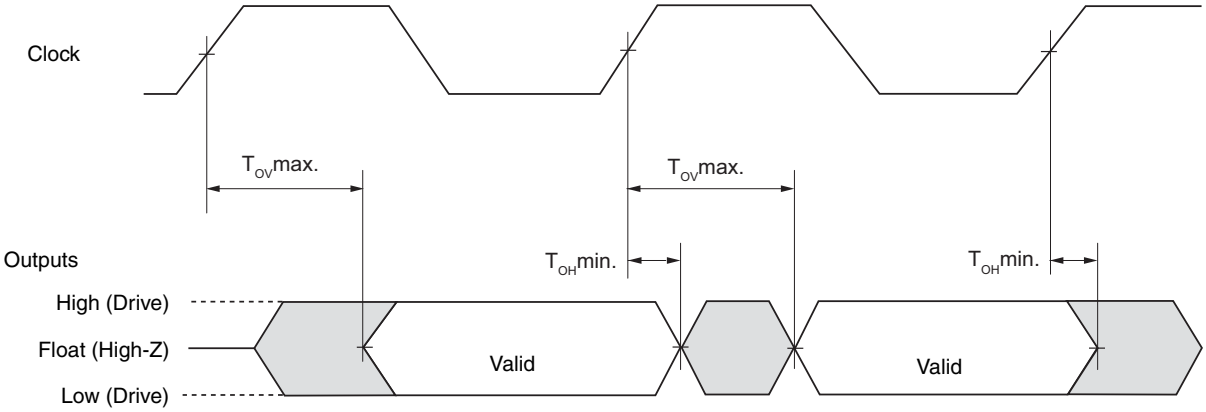


Figure 2-3: Output Delay Waveforms



2.4.3 LBU timing specifications

Remarks: 1. The polarity of the LBU_RDY_N signal can be configured using the LBU_POL_RDY signal. LBU_RDY_N must be pulled to its "ready" level by an external pull-down or pull-up resistor.

LBU_POL_RDY = 0_b	LBU_RDY_N active low	use external pull-down resistor
LBU_POL_RDY = 1_b	LBU_RDY_N active high	use external pull-up resistor

2. The LBU_CFG signal is used to select access control through separate read/write lines or a common read/write line.

LBU_CFG = 0_b	use separate read/write lines LBU_RD_N and LBU_WR_N
LBU_CFG = 1_b	use common read/write line LBU_WR_N

In case of a common read/write line, LBU_WR_N must be high for a read access and low for a write access. The unused LBU_RD_N input must then be pulled to inactive (high) level by an external pull-up resistor.

3. ERTEC 400 responds to a read or write access by first driving LBU_RDY_N to "not ready" level. Then LBU_RDY_N is driven to "ready" level for t_{RAP}. The length of the "not ready" phase of LBU_RDY_N varies strongly on the internal states of ERTEC 400 and the currently ongoing internal communication processes. Therefore no upper limit for the length of the "not ready" period is specified.

4. ERTEC 400 has two LBU chip select inputs; one for access to the page configuration registers (LBU_CS_R_N) and one to access to the ERTEC 400 memory addess space (LBU_CS_M_N). Only one of these chip select signals may be active at a time and it is not allowed to change the chip select during the complete access.

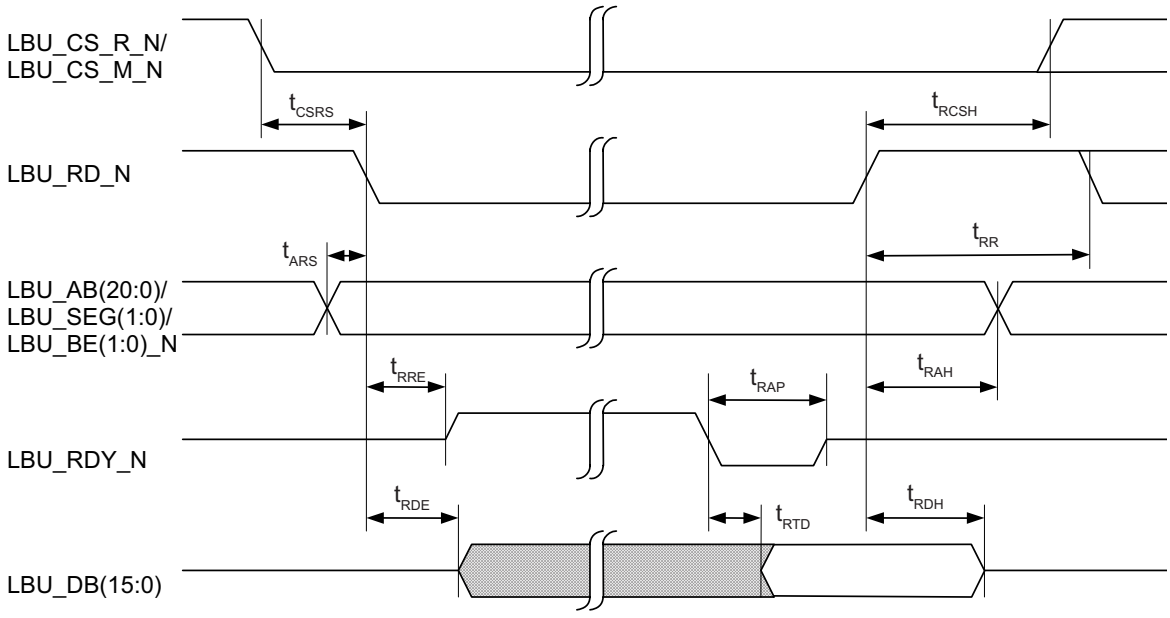
(1) LBU Read from ERTEC 400 with Separate Read/Write line (LBU_RDY_N active low)

T_A = -40 to +85°C, V_{DDCore} = 1.35 V ~ 1.65 V, V_{DDIO} = 3.0 V ~ 3.6 V

Table 2-6: LBU Read from ERTEC 400 with Separate Read/Write line

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Chip select asserted to read pulse asserted delay	t_{CSRS}	-	0	-	ns
Address valid to read pulse asserted setup time	t_{ARS}	-	0	-	ns
Read pulse asserted to ready enabled delay	t_{RRE}	-	5	12	ns
Read pulse asserted to data enable delay	t_{RDE}	-	5	12	ns
Ready active pulse width	t_{RAP}	-	17	23	ns
Ready asserted to data valid delay	t_{RTD}	-	-	5	ns
Read pulse deasserted to chip select deasserted delay	t_{RCSH}	-	0	-	ns
Address valid to read pulse deasserted hold time	t_{RAH}	-	0	-	ns
Data valid/enabled to read pulse deasserted hold time	t_{RDH}	-	0	12	ns
Read recovery time	t_{RR}	-	25	-	ns

Figure 2-4: LBU Read from ERTEC 400 with Separate Read/Write line



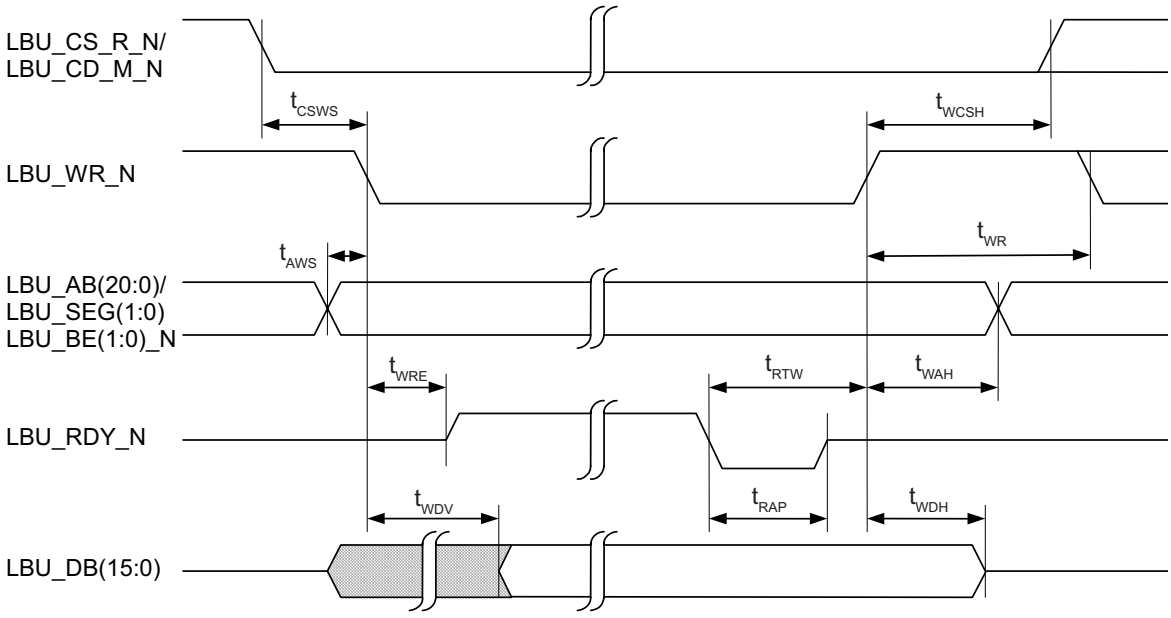
(2) LBU Write to ERTEC 400 with separate Read/Write line (LBU_RDY_N active low)

T_A = -40 to +85°C, V_{DDCore} = 1.35 V ~ 1.65 V, V_{DDIO} = 3.0 V ~ 3.6 V

Table 2-7: LBU Write to ERTEC 400 with Separate Read/Write line

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Chip select asserted to write pulse asserted delay	t_{CSWS}	-	0	-	ns
Address valid to write pulse asserted setup time	t_{AWS}	-	0	-	ns
Write pulse asserted to ready enabled delay	t_{WRE}	-	5	12	ns
Write pulse asserted to data valid delay	t_{WDV}	-	-	40	ns
Ready active pulse width	t_{RAP}	-	17	23	ns
Write pulse deasserted to chip select deasserted delay	t_{WCSH}	-	0	-	ns
Address hold time after write strobe deasserted	t_{WAH}	-	0	-	ns
Ready asserted to write pulse deasserted delay	t_{RTW}	-	0	-	ns
Data hold time after write pulse deasserted	t_{WDH}	-	0	-	ns
Write recovery time	t_{WR}	-	25	-	ns

Figure 2-5: LBU Write to ERTEC 400 with Separate Read/Write line



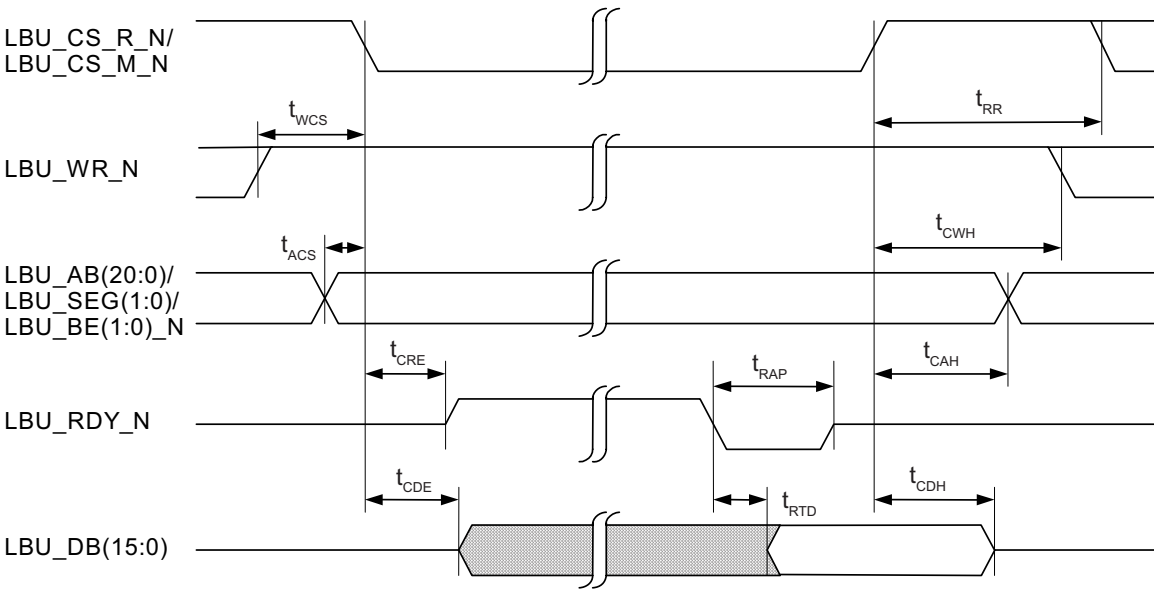
(3) LBU Read from ERTEC 400 with Common Read/Write line (LBU_RDY_N active low)

T_A = -40 to +85°C, V_{DDCore} = 1.35 V ~ 1.65 V, V_{DDIO} = 3.0 V ~ 3.6 V

Table 2-8: LBU Read from ERTEC 400 with Common Read/Write line

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Write signal deasserted to chip select asserted setup time	t_{WCS}	-	2	-	ns
Address valid to chip select asserted setup time	t_{ACS}	-	0	-	ns
Chip select asserted to ready enabled delay	t_{CRE}	-	5	12	ns
Chip select asserted to data enable delay	t_{CDE}	-	5	12	ns
Ready active pulse width	t_{RAP}	-	17	23	ns
Ready asserted to data valid delay	t_{RTD}	-	-	5	ns
Write signal inactive to chip select deasserted hold time	t_{CWH}	-	0	-	ns
Address valid to chip select deasserted hold time	t_{CAH}	-	0	-	ns
Data valid/enabled to chip select deasserted hold time	t_{CDH}	-	0	12	ns
Read recovery time	t_{RR}	-	25	-	ns

***Figure 2-6: LBU Read from ERTEC 400* with Common Read/Write line**



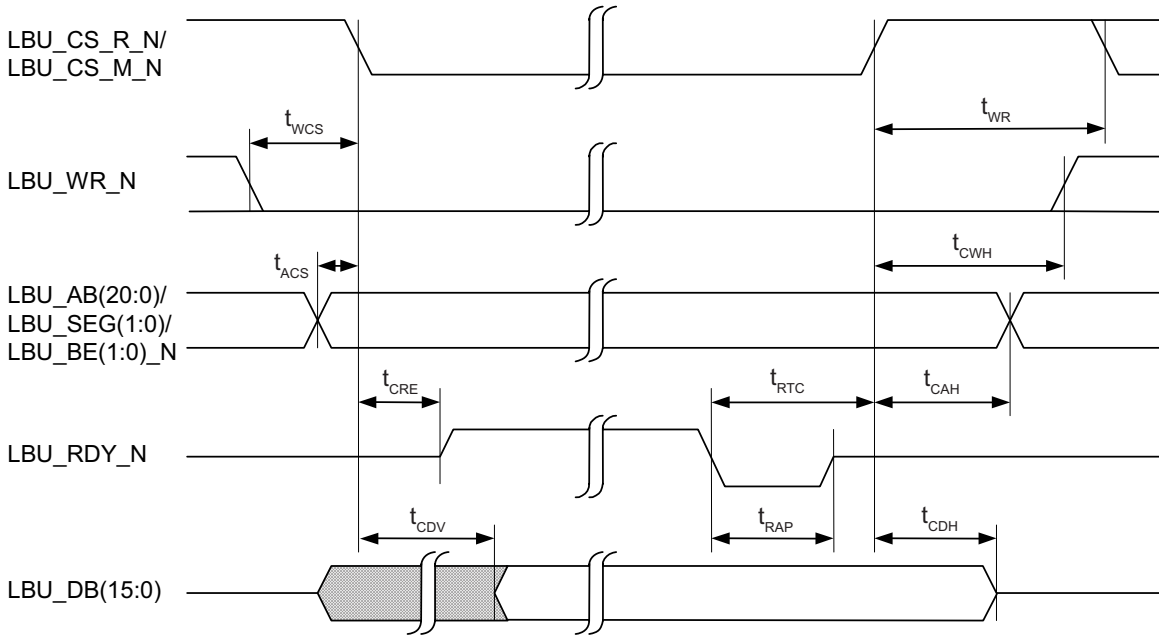
(4) LBU Write to ERTEC 400 with Common Read/Write line (LBU_RDY_N active low)

T_A = -40 to +85°C, V_{DDCore} = 1.35 V ~ 1.65 V, V_{DDIO} = 3.0 V ~ 3.6 V

Table 2-9: LBU Write to ERTEC 400 with Common Read/Write line

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Write signal asserted to chip select setup time	t_{WCS}	-	2	-	ns
Address valid to chip select asserted setup time	t_{ACS}	-	0	-	ns
Chip select asserted to ready enabled delay	t_{CRE}	-	5	12	ns
Chip select asserted to data valid delay	t_{CDV}	-	-	40	ns
Ready active pulse width	t_{RAP}	-	17	23	ns
Write signal deasserted to chip select deasserted hold time	t_{CWH}	-	0	-	ns
Address hold time after chip select deasserted	t_{CAH}	-	0	-	ns
Ready asserted to chip select deasserted delay	t_{RTC}	-	0	-	ns
Data valid/enabled to chip select deasserted hold time	t_{CDH}	-	0	-	ns
Write recovery time	t_{WR}	-	25	-	ns

Figure 2-7: LBU Write to ERTEC 400 with Common Read/Write line



2.4.4 SPI timing specifications

Remarks: 1. Please note, that different serial clock frequency ranges for SPI slave and master modes are given in Table 2-4.

2. Timing diagrams are shown for TI-format only. Other transfer formats can be configured, however the AC-timing parameters (setup/hold times, delays) remain in principle unchanged.

3. Not every external SPI device, that is connected to ERTEC 400, requires usage of all available SPI signals.

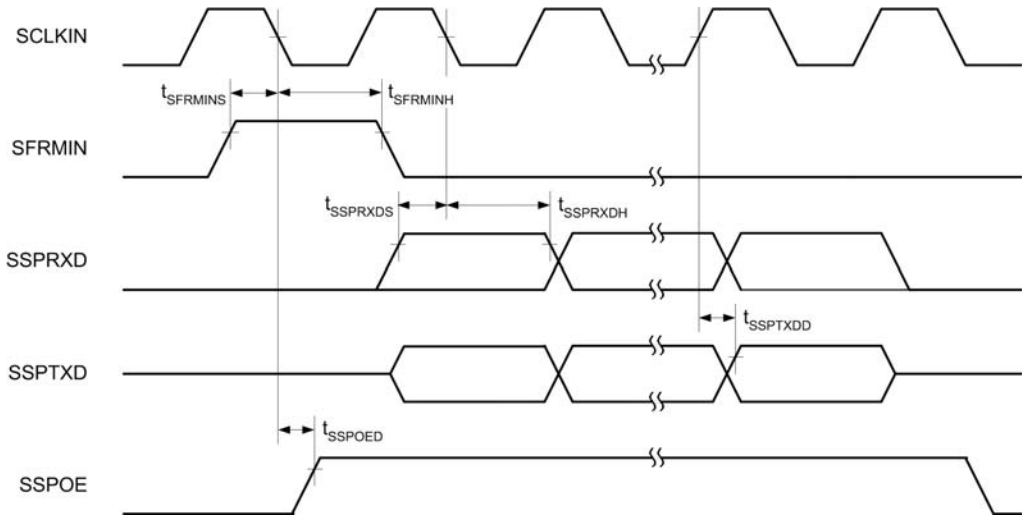
(1) SPI interface configured to slave mode

T_A = -40 to +85°C, V_{DDCore} = 1.35 V ~ 1.65 V, V_{DDIO} = 3.0 V ~ 3.6 V

Table 2-10: SPI Timing Specifications (slave mode)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
SSPRXD setup time	$t_{SSPRXDS}$	-	20	-	ns
SSPRXD hold time	$t_{SSPRXDH}$	-	60	-	ns
SFRMIN setup time	$t_{SFRMINS}$	-	40	-	ns
SFRMIN hold time	$t_{SFRMINH}$	-	20	-	ns
SSPTXD delay	$t_{SSPTXDD}$	-	-	40	ns
SSPOE delay	t_{SSPOED}	-	-	40	ns

Figure 2-8: SPI Timing in Slave Mode (TI-format Example)



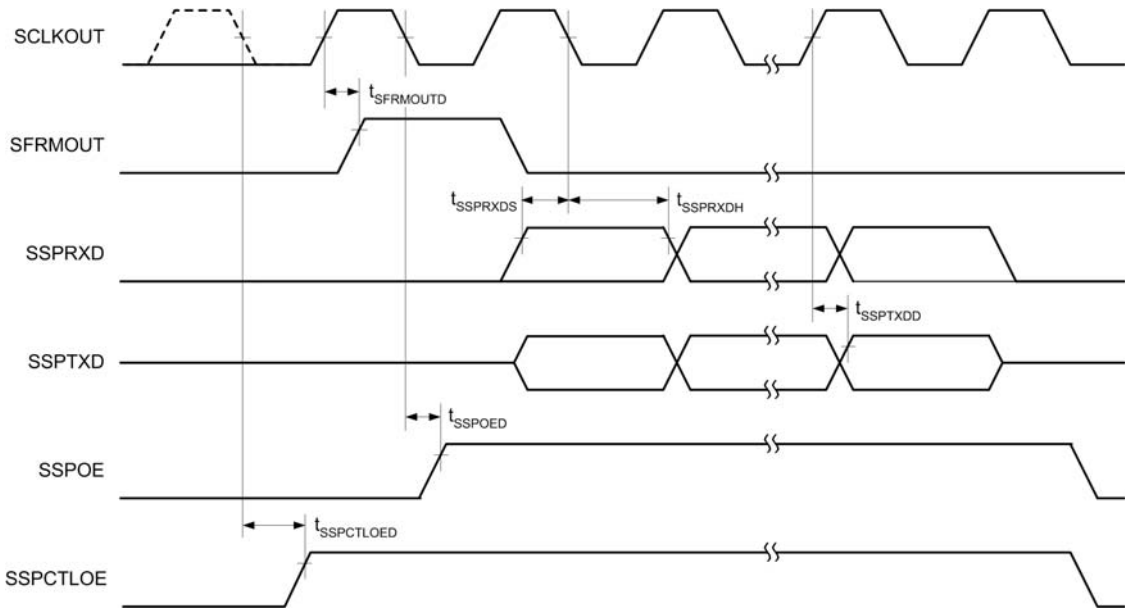
(2) SPI interface configured to master mode

T_A = -40 to +85°C, V_{DDCore} = 1.35 V ~ 1.65 V, V_{DDIO} = 3.0 V ~ 3.6 V

Table 2-11: SPI Timing Specifications (master mode)

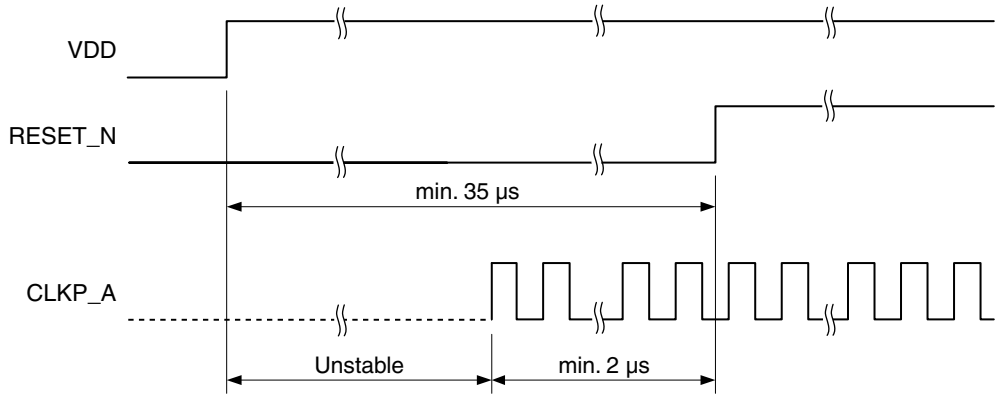
Parameter	Symbol	Condition	MIN.	MAX.	Unit
SSPRXD setup time	$t_{SSPRXDS}$	-	12.4	-	ns
SSPRXD hold time	$t_{SSPRXDH}$	-	0	-	ns
SFRMOUT delay	$t_{SFRMOUTD}$	-	-0.7	0.4	ns
SSPTXD delay	$t_{SSPTXDD}$	-	-0.8	0.4	ns
SSPOE delay	t_{SSPOED}	-	0.2	2.3	ns
SSPCTLOE delay	$t_{SSPCTLOED}$	-	0.1	2.3	ns

Figure 2-9: SPI Timing in Master Mode (TI-format Example)



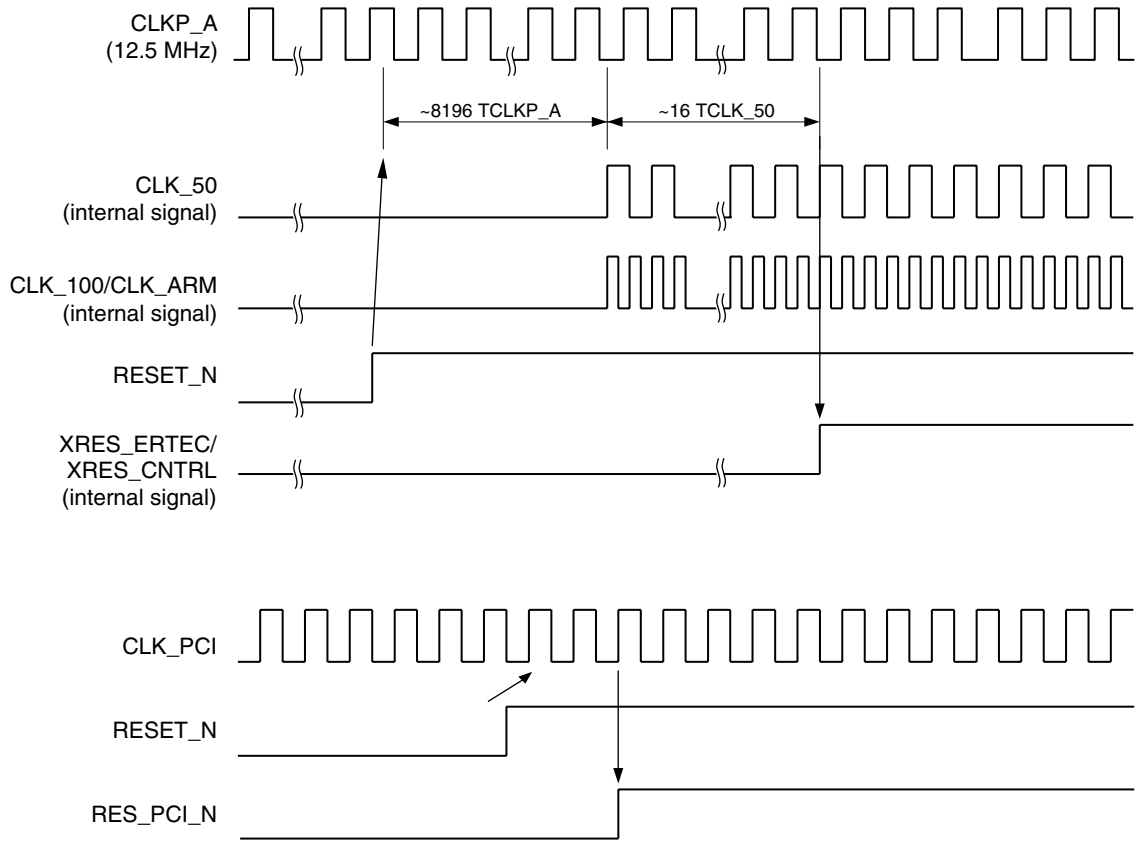
2.4.5 Power-up sequence

Figure 2-10: Power-Up Sequence Timing Diagram



2.4.6 Reset timing

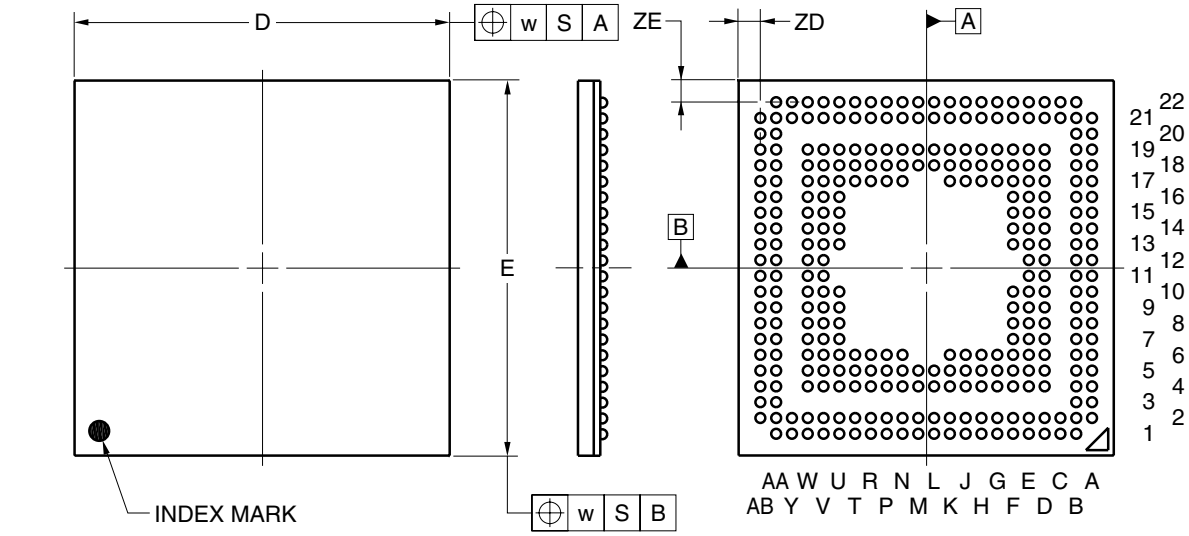
Figure 2-11: Reset Timing Diagram

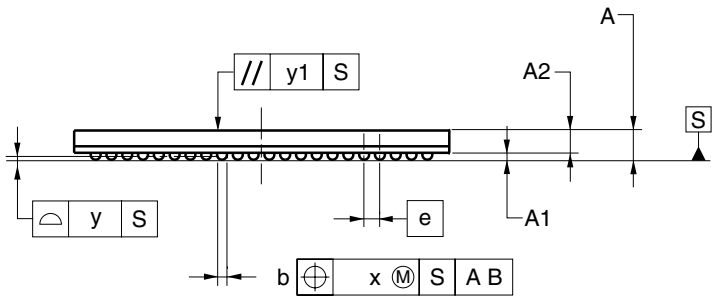


3. Package Drawing

Figure 3-1: Package Drawing

304-PIN PLASTIC FBGA (19x19)





(UNIT:mm)

ITEM	DIMENSIONS
D	19.00 0.10
E	19.00 0.10
w	0.20
e	0.80
A	1.48 0.10
A1	0.35 0.06
A2	1.13
b	0.50 $^{0.05}_{0.10}$
x	0.08
y	0.10
y1	0.20
ZD	1.10
ZE	1.10

P304F1-80-HN2

4. Recommended Soldering Conditions

Solder this product under the following recommended conditions.
For details of the recommended soldering conditions, refer to the information document

Semiconductor Device Mounting Technology Manual (C10535E).

For soldering methods and conditions other than those recommended please consult NEC.

- for μPD800232F1-014-HN2-A (lead-free device)

Table 4-1: Soldering Conditions for Lead-free Device

Soldering Method	Soldering Condition	Symbol of Recommended Soldering Condition
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds max. (220°C min.), Number of times: 3 max., Number of days: 7 **Note**	IR60-107-3

Note: The number of days refers to storage at 25°C, 65% RH MAX after the dry pack has been opened. After that, prebaking is necessary at 125 °C for 10 to 72 hours.

NOTES FOR CMOS DEVICES

① **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN**

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② **HANDLING OF UNUSED INPUT PINS**

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ **PRECAUTION AGAINST ESD**

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ **STATUS BEFORE INITIALIZATION**

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ **INPUT OF SIGNAL DURING POWER OFF STATE**

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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