

Description

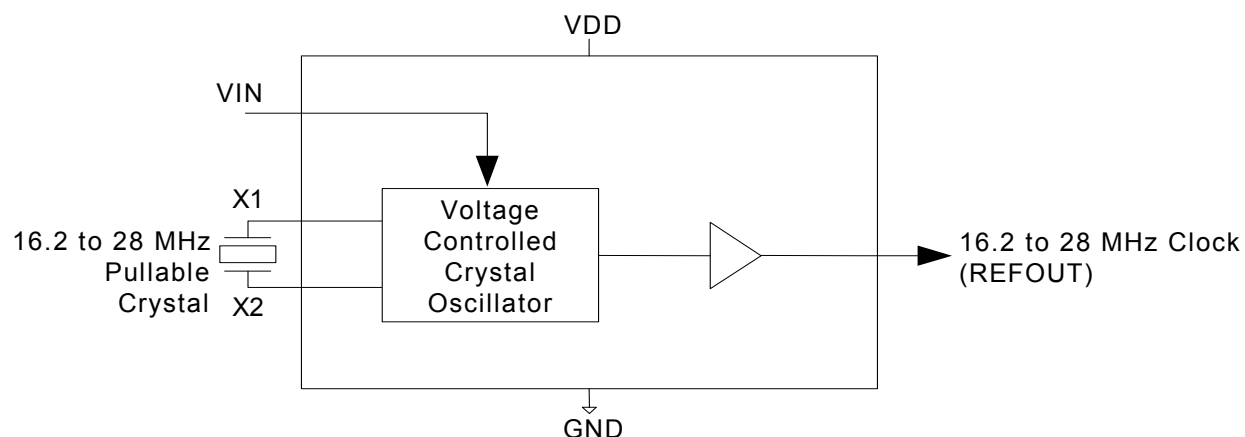
The MK3721 series of devices includes the original MK3721S and the new MK3721D. The MK3721D is a drop-in replacement for the MK3721S device. Compared to the earlier device, the MK3721D offers a wider operating frequency range and improved power supply noise rejection.

The MK3721 is a low cost, low-jitter, high-performance 3.3 volt VCXO designed to replace expensive discrete VCXOs modules. The on-chip Voltage Controlled Crystal Oscillator accepts a 0 to 3.3 V input voltage to cause the output clocks to vary by ± 100 ppm. Using ICS' patented VCXO techniques, the device uses an inexpensive external pullable crystal in the range of 16.2 to 28 MHz to produce a VCXO output clock at that same frequency.

ICS manufactures the largest variety of Set-Top Box and multimedia clock synthesizers for all applications. If more clock outputs are needed, see the MK3732 or MK377x family of parts. Consult ICS to eliminate VCXOs, crystals, and oscillators from your board.

The frequency of the on-chip VCXO is adjusted by an external control voltage input into pin VIN. Because VIN is a high-impedance input, it can be driven directly from an PWM RC integrator circuit. Frequency output increases with VIN voltage input. The usable range of VIN is 0 to 3.3 V.

Block Diagram

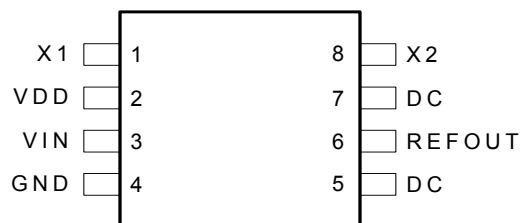


Features

- MK3721D is a drop-in replacement for the earlier MK3721S device
- Packaged in 8-pin SOIC
- Operational frequency range of 16.2 MHz to 28 MHz
- Uses an inexpensive external crystal
- On-chip patented VCXO with pull range of 200 ppm (minimum)
- VCXO tuning voltage of 0 to 3.3 V
- Operating voltage of 3.3 V
- 12 mA output drive capability at TTL levels
- Advanced, low-power, sub-micron CMOS process
- For frequencies between 1 MHz and 8 MHz, use the MK3713D. For higher than 28 MHz, use the MK3732-05.
- Available in a lead-free package

MK3721D is recommended for new designs.

Pin Assignment



MK3721S
MK3721D

8-Pin (150 mil) SOIC

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	XI	Input	Crystal connection. Connect to the external pullable crystal.
2	VDD	Power	Connect to +3.3 V (0.01μf decoupling capacitor recommended).
3	VIN	Input	Voltage input to VCXO. Zero to 3.3 V signal which controls the VCXO frequency.
4	GND	Power	Connect to ground.
5	DC	--	Do not connect to this pin.
6	REFOUT	Output	VCXO CMOS level clock output matches the nominal frequency of the crystal.
7	DC	--	Do not connect anything to this pin.
8	X2	Input	Crystal connection. Connect to a pullable 16.2 to 28 MHz crystal.

External Component Selection

The MK3721 requires a minimum number of external components for proper operation.

Decoupling Capacitors

A decoupling capacitor of 0.01 μ F should be connected between VDD and GND on pins 2 and 4 as close to the MK3721 as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

When the PCB trace between the clock output and the load is over 1 inch, series termination should be used. To series terminate a 50 Ω trace (a commonly used trace impedance), place a 33 Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20 Ω .

Quartz Crystal

The MK3721 VCXO function consists of the external crystal and the integrated VCXO oscillator circuit. To assure the best system performance (frequency pull range) and reliability, a crystal device with the recommended parameters (shown below) must be used, and the layout guidelines discussed in the following section shown must be followed.

The oscillation frequency of a quartz crystal is determined by its “cut” and by the load capacitors connected to it. The MK3721 incorporates on-chip variable load capacitors that “pull” (change) the frequency of the crystal. The crystal specified for use with the MK3721 is designed to have zero frequency error when the total of on-chip + stray capacitance is 14 pF.

Recommended Crystal Parameters:

Initial Accuracy at 25°C	±20 ppm
Temperature Stability	±30 ppm
Aging	±20 ppm
Load Capacitance	14 pF
Shunt Capacitance, C0	7 pF Max
C0/C1 Ratio	250 Max
Equivalent Series Resistance	35 Ω Max

The external crystal must be connected as close to the chip

as possible and should be on the same side of the PCB as the MK3721. There should be no via's between the crystal pins and the X1 and X2 device pins. There should be no signal traces underneath or close to the crystal. See application note MAN05.

Crystal Tuning Load Capacitors

The crystal traces should include pads for small fixed capacitors, one between X1 and ground, and another between X2 and ground. Stuffing of these capacitors on the PCB is optional. The need for these capacitors is determined at system prototype evaluation, and is influenced by the particular crystal used (manufacture and frequency) and by PCB layout. The typical required capacitor value is 1 to 4 pF.

The procedure for determining the value of these capacitors can be found in application note MAN05.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK3721. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70°C
Storage Temperature	-65 to +150°C
Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0	—	+70	°C
Power Supply Voltage (measured in respect to GND)	+3.15		+3.45	V
Reference crystal parameters	Refer to page 3			

DC Electrical Characteristics

VDD=3.3V $\pm$ 5% , Ambient temperature 0 to +70°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.15		3.45	V
Output High Voltage	V _{OH}	I _{OH} = -12 mA	2.4			V
Output Low Voltage	V _{OL}	I _{OL} = 12 mA			0.4	V
Output High Voltage (CMOS Level)	V _{OH}	I _{OH} = -4 mA	VDD-0.4			V
Operating Supply Current	IDD	No load		6		mA
Short Circuit Current	I _{OS}			$\pm$ 50		mA
VIN, VCXO Control Voltage	V _{IA}		0		3.3	V

AC Electrical Characteristics

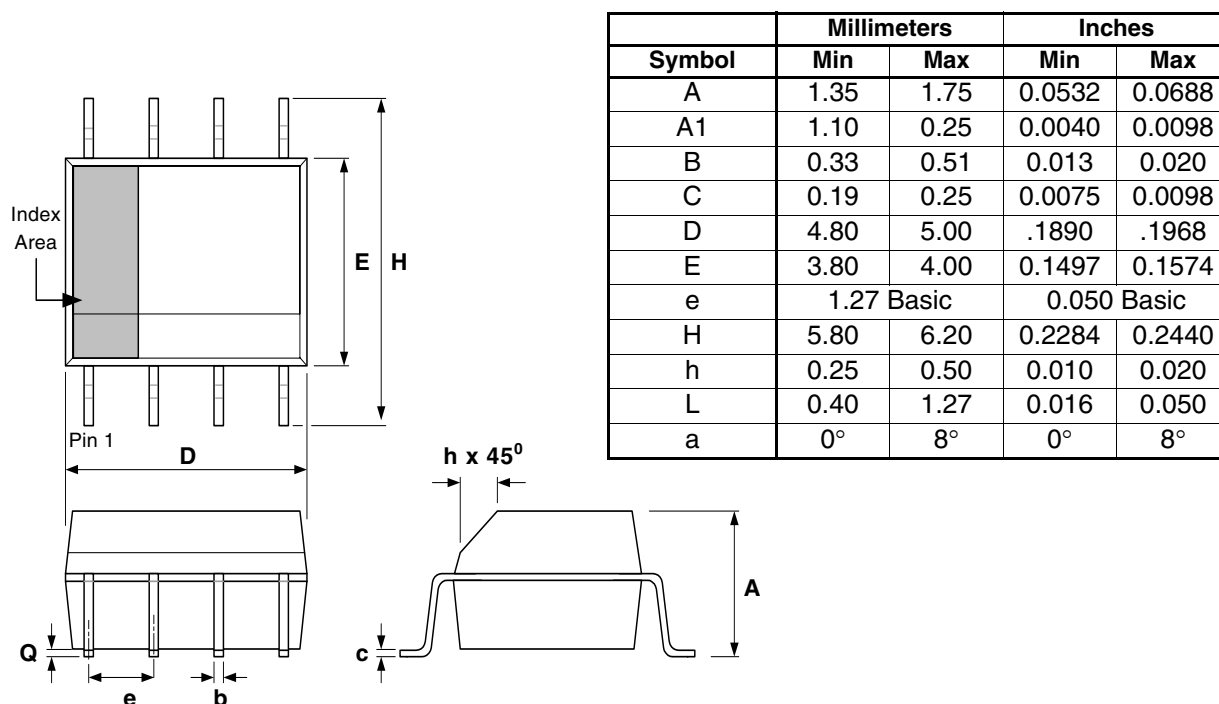
VDD = 3.3V $\pm$ 5%, Ambient Temperature 0 to +70° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Frequency						
MK3721D	F _O		16.2		28	MHz
MK3721S	F _O	24 MHz		24		MHz
Crystal Pullability						
MK3721D	F _P	0V $\leq$ VIN $\leq$ 3.3 V, Note 1	$\pm$ 115			ppm
MK3721S	F _P	0V $\leq$ VIN $\leq$ 3.3 V, Note 1	$\pm$ 100			ppm
VCXO Gain						
MK3721D		VIN = VDD/2 $\pm$ 1 V, Note 1		120		ppm/V
MK3721S		VIN = VDD/2 $\pm$ 1 V, Note 1		140		ppm/V
Output Rise Time	t _{OR}	0.8 to 2.0 V, C _L =15 pF			1.5	ns
Output Fall Time	t _{OF}	2.0 to 0.8 V, C _L =15 pF			1.5	ns
Output Clock Duty Cycle	t _D	Measured at 1.4V, C _L =15 pF	40	50	60	%
Maximum Output Jitter, short term	t _J	C _L =15 pF		110		ps

Note 1: External crystal device must conform with Pullable Crystal Specifications listed on page 3.

Package Outline and Package Dimensions (8-pin SOIC)

Package dimensions are kept current with JEDEC Publication No. 95



Ordering Information

Part / Order Number (Note 1)	Marking	Shipping packaging	Package	Temperature
MK3721D	MK3721D	Tubes	8-pin SOIC	0 to +70° C
MK3721DTR	MK3721D	Tape and Reel	8-pin SOIC	0 to +70° C
MK3721DLF	MK3721DL	Tubes	8-pin SOIC	0 to +70° C
MK3721DLFTR	MK3721DL	Tape and Reel	8-pin SOIC	0 to +70° C
MK3721S	MK3721S	Tubes	8-pin SOIC	0 to +70° C
MK3721STR	MK3721S	Tape and Reel	8-pin SOIC	0 to +70° C

Note 1: MK3721D is recommended for new designs.

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MK3721

LOW COST 16.2 TO 28 MHZ 3.3 VOLT VCXO

VCXO

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