

Description

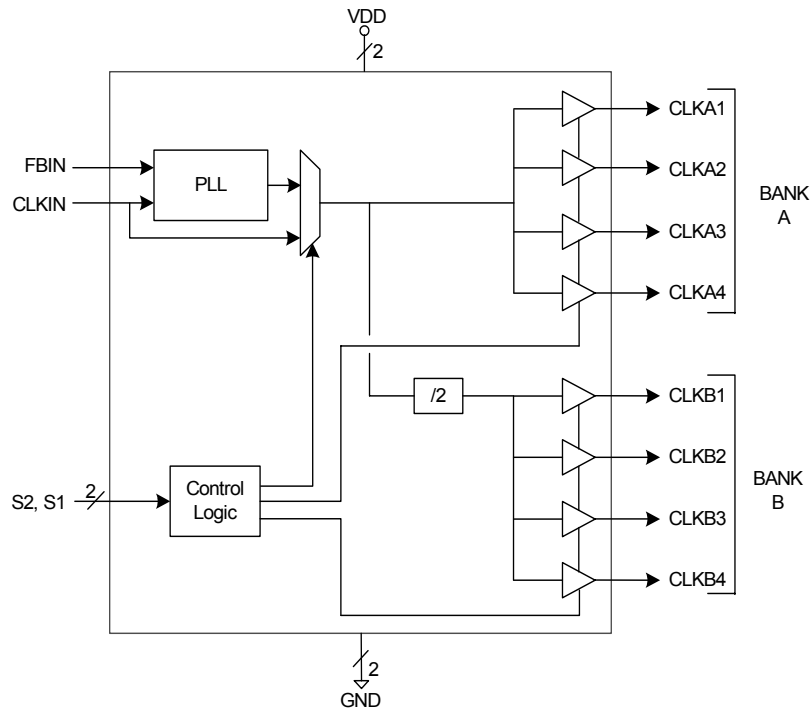
The MK2745-24 is a low-cost, low-jitter, high-performance clock synthesizer for DVD and other MPEG 2-based applications. Using analog Phase-Locked Loop (PLL) techniques, the device accepts a 27 MHz fundamental mode crystal or clock input to produce multiple audio output clocks, a processor clock, and two 27 MHz clocks. The audio clocks are frequency-locked to the 27 MHz using our patented zero ppm error techniques. This allows audio and video to track exactly, thereby eliminating the need for large buffer memory.

IDT manufactures a large variety of DVD, Set-top Box, and multimedia clock synthesizers for all applications. Consult IDT to eliminate crystals and oscillators from your board.

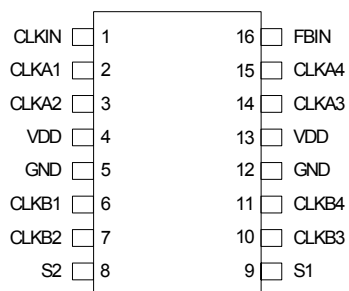
Features

- Packaged in a 16-pin narrow (150 mil) SOIC
- Ideal for AuraVision's notebook DVD solutions
- Patented zero ppm audio clock error for exact audio clock sampling rates, plus 32x and 256x clocks of the sampling frequencies
- Selectable audio sampling frequencies support 32, 44.1, and 96 kHz in most DACs
- 27 MHz fundamental crystal or clock input
- Selectable processor frequencies
- Two clocks of 27 MHz
- Zero ppm in all clocks
- 25 mA output drive capability at TTL levels
- Advanced, low-power, sub-micron CMOS process
- Operating voltage of 3.3 V to 5 V
- See also the MK2712 for NTSC/PAL clocks

Block Diagram



Pin Assignment



16-pin (150 mil) SOIC

Feedback Configuration Table

| Feedback From | CLKA1:A4 | CLKB1:B4 |
|---------------|----------|----------|
| Bank A | CLKIN | CLKIN/2 |
| Bank B | 2XCLKIN | CLKIN |

Output Clock Mode Select Table

| S2 | S1 | Clocks A1:A4 | Clocks B1:B4 | Internet Generation | PLL Status |
|----|----|----------------------------|----------------------------|-----------------------------|------------|
| 0 | 0 | Tri-state (high impedance) | Tri-state (high impedance) | None | On |
| 0 | 1 | Running | Tri-state (high impedance) | PLL | On |
| 1 | 0 | Running | Running | Buffer only (no zero delay) | Off |
| 1 | 1 | Running | Running | PLL | On |

Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|------------|----------|----------|--|
| 1 | CLKIN | Input | Clock input. Connect to input clock source. |
| 2, 3 | CLKA1:A4 | Output | Clock A bank of four outputs. |
| 4 | VDD | Power | Power supply. Connect pin to same voltage as pin 13 (either 3.3 V or 5 V). |
| 5 | GND | Power | Connect to ground. |
| 6, 7 | CLKB1:B4 | Output | Clock B bank of four outputs. These are low skew divide by two of bank A. |
| 8 | S2 | Input | Select input 2. Selects mode for outputs per table above. |
| 9 | S1 | Input | Select input 1. Selects mode for outputs per table above. |
| 10, 11 | CLKB1:B4 | Output | Clock B bank of four outputs. These are low skew divide by two of bank A. |
| 12 | GND | Power | Connect to ground. |
| 13 | VDD | Power | Power supply. Connect pin to same voltage as pin 4 (either 3.3 V or 5 V). |
| 14, 15 | CLKA1:A4 | Output | Clock A bank of four outputs. |
| 16 | FBIN | Input | Feedback input. Determines outputs per table above. |

External Components

The MK2745-24 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.1 μ F should be connected between VDD and GND, as close to the part as possible. A 33 Ω series terminating resistor should be used on each clock output to reduce reflections.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK2745-24. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|--|---------------------|
| Supply Voltage, VDD | 7 V |
| All Inputs and Outputs | -0.5 V to VDD+0.5 V |
| Ambient Operating Temperature (Commercial) | 0 to +70° C |
| Ambient Operating Temperature (Industrial) | -40 to +85° C |
| Storage Temperature | -65 to +150° C |
| Junction Temperature | 125° C |
| Soldering Temperature | 260° C |

Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---|------|------|------|-------|
| Ambient Operating Temperature | 0 | | +70 | °C |
| Power Supply Voltage (measured in respect to GND) | +3.0 | | +5.5 | V |

DC Electrical Characteristics

VDD=3.3 V ±10%, Temp 0 to +70° / -40 to +85° C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|-----------------|--------------------------|-----------|-------|-----------|-------|
| Operating Voltage | VDD | | 3.0 | | 5.5 | V |
| Input High Voltage | V _{IH} | CLKIN pin only | (VDD/2)+1 | VDD/2 | | V |
| Input Low Voltage | V _{IL} | CLKIN pin only | | VDD/2 | (VDD/2)-1 | V |
| Input High Voltage | V _{IH} | | 2 | | | V |
| Input Low Voltage | V _{IL} | | | | 0.8 | V |
| Output High Voltage | V _{OH} | I _{OH} = -18 mA | 2.4 | | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 18 mA | | | 0.4 | V |
| Output High Voltage | V _{OH} | I _{OH} = -5 mA | VDD-0.4 | | | V |
| Operating Supply Current 100 MHz, CLKIN | IDD | No Load S1=S2=1 | | 44 | | mA |
| Short Circuit Current | I _{OS} | Each output | | ± 65 | | mA |
| Input Capacitance | C _{IN} | S1, S1, FBIN | | 7 | | pF |

AC Electrical Characteristics

VDD = 3.3V ±10%, Temp 0 to +70° / -40 to +85° C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---------------------------------------|-----------------|-------------------------------------|------|------|------|-------|
| Input Frequency | | FBIN to CLKA1 S1=S2=1 | 20 | | 160 | MHz |
| Output Frequency | | FBIN to CLKA1 S1=S2=1 | 20 | | 160 | MHz |
| Output Rise Time | t _{OR} | 0.8 to 2.0 V, C _L =30 pF | | | 1.5 | ns |
| Output Fall Time | t _{OF} | 0.8 to 2.0 V, C _L =30 pF | | | 1.5 | ns |
| Output Clock Duty Cycle | | at 1.4V | 40 | 50 | 60 | % |
| Device-to-Device skew, equally loaded | | Rising edges at VDD/2 | | | 700 | ps |
| Output-to-Output skew, equally loaded | | Rising edges at VDD/2 | | | 200 | ps |
| Maximum Absolute Jitter | | | | 300 | | ps |
| Cycle-to-Cycle Jitter | | 30 pF loads 66.67 MHz outputs | | | 400 | ps |
| | | 15 pF loads 66.67 MHz outputs | | | 400 | ps |

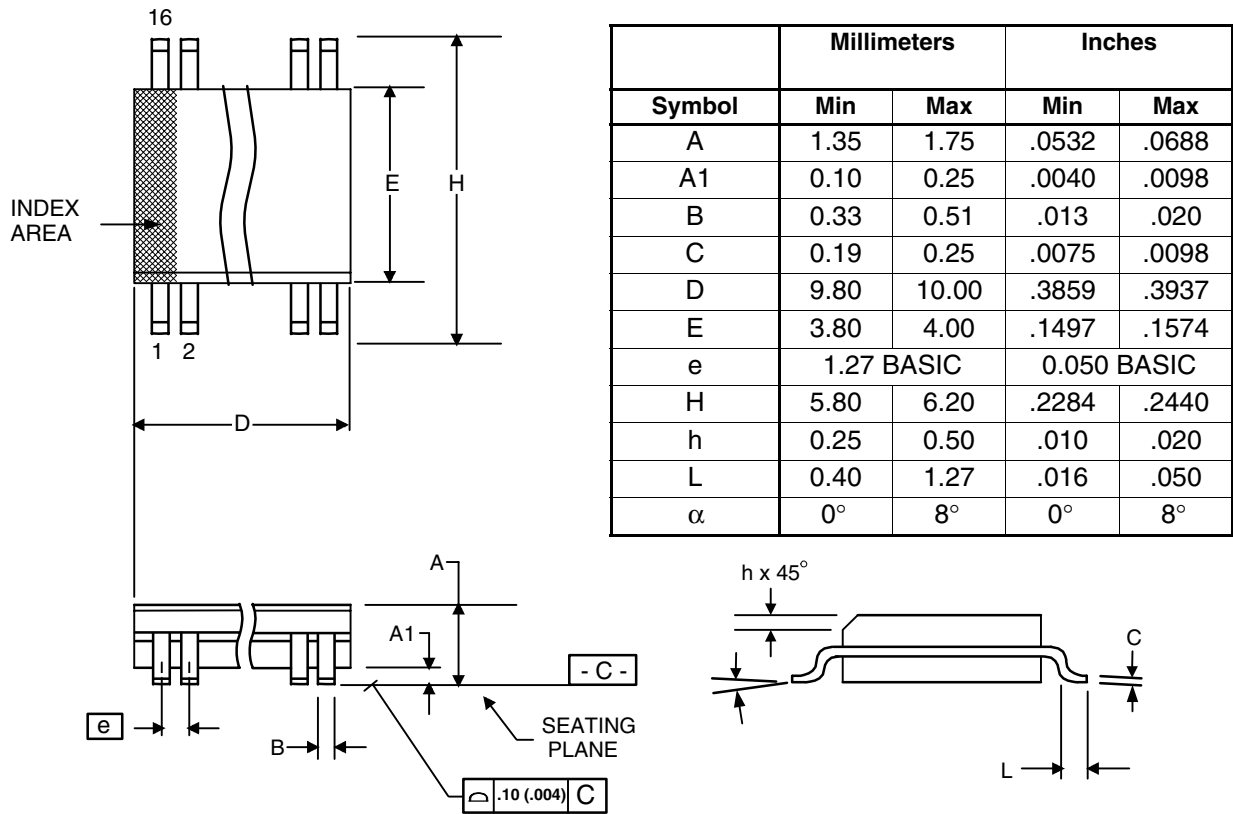
| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|------------|--|------|------|------|-------|
| Skew from Output Bank A to Output Bank B | | All outputs equally loaded | | | 400 | ps |
| Delay CLKIN Rising Edge to FBIN Rising Edge | | Measured at VDD/2 | | | ±250 | ps |
| PLL Lock Time | t_{LOCK} | Stable power supply, valid clocks on CLKIN, FBIN | | | 1 | ms |

Thermal Characteristics

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|---------------|----------------|------|------|------|-------|
| Thermal Resistance Junction to Ambient | θ_{JA} | Still air | | 120 | | °C/W |
| | θ_{JA} | 1 m/s air flow | | 115 | | °C/W |
| | θ_{JA} | 3 m/s air flow | | 105 | | °C/W |
| Thermal Resistance Junction to Case | θ_{JC} | | | 58 | | °C/W |

Package Outline and Package Dimensions (16-pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|------------|--------------------|-------------|---------------|
| MK2745-24SLF | 2745-24SL | Tubes | 16-pin SOIC | 0 to 70° C |
| MK2745-24SLFT | 2745-24SL | Tape and Reel | 16-pin SOIC | 0 to 70° C |
| MK2745-24SILF | 2745-24SIL | Tubes | 16-pin SOIC | -40 to +85° C |
| MK2745-24SILFT | 2745-24SIL | Tape and Reel | 16-pin SOIC | -40 to +85° C |

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