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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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M65677FP

Digital NTSC/PAL Encoder

REJ03F0189-0201

Rev.2.01

Mar 31, 2008

Description

The M65677FP encodes CCIR601 or CCIR656 format Y/Cb/Cr data into analog NTSC and PAL video signals, including Digital Signal Processing functions such as Closed Caption encoding. Overlay OSD, Anti Video Copy Processing^{Note1} e.t.c. It also includes peripheral processing function such as 10 bit DAC e.t.c., so that low cost and compact system can be realized.

Features

- Macrovision's video anti copy process Rev 7.01 supported^{Note1}
- Overlay CGMS signal online 20/283 for 525/60^{Note3}
- Generate CRCC for CGMS Signal
- Overlay WSS signal online 23 for 625/50^{Note4}
- Color adjustment (TINT/color control)
- NTSC, B/G PAL or MPAL Video Outputs
- Component Y/C Video (S-Video) and CVBS or Y/U/V Outputs
- Supporting CCIR601 and CCIR656 format data
- Closed Caption Manager online 21/284 for NTSC
- Generate ODD parity for Closed Caption Manager
- H/V Sync and Composite generating
- Overlay Digital OSD Supporting Y/Cb/Cr 4:4:4
- Over sampling Filter
- 2 ch 10 bit DAC and 3 ch 6 dB Amp^{Note2}
- 3.3 V I/O interface
- I²C Bus Interface for Controls
- Power down mode

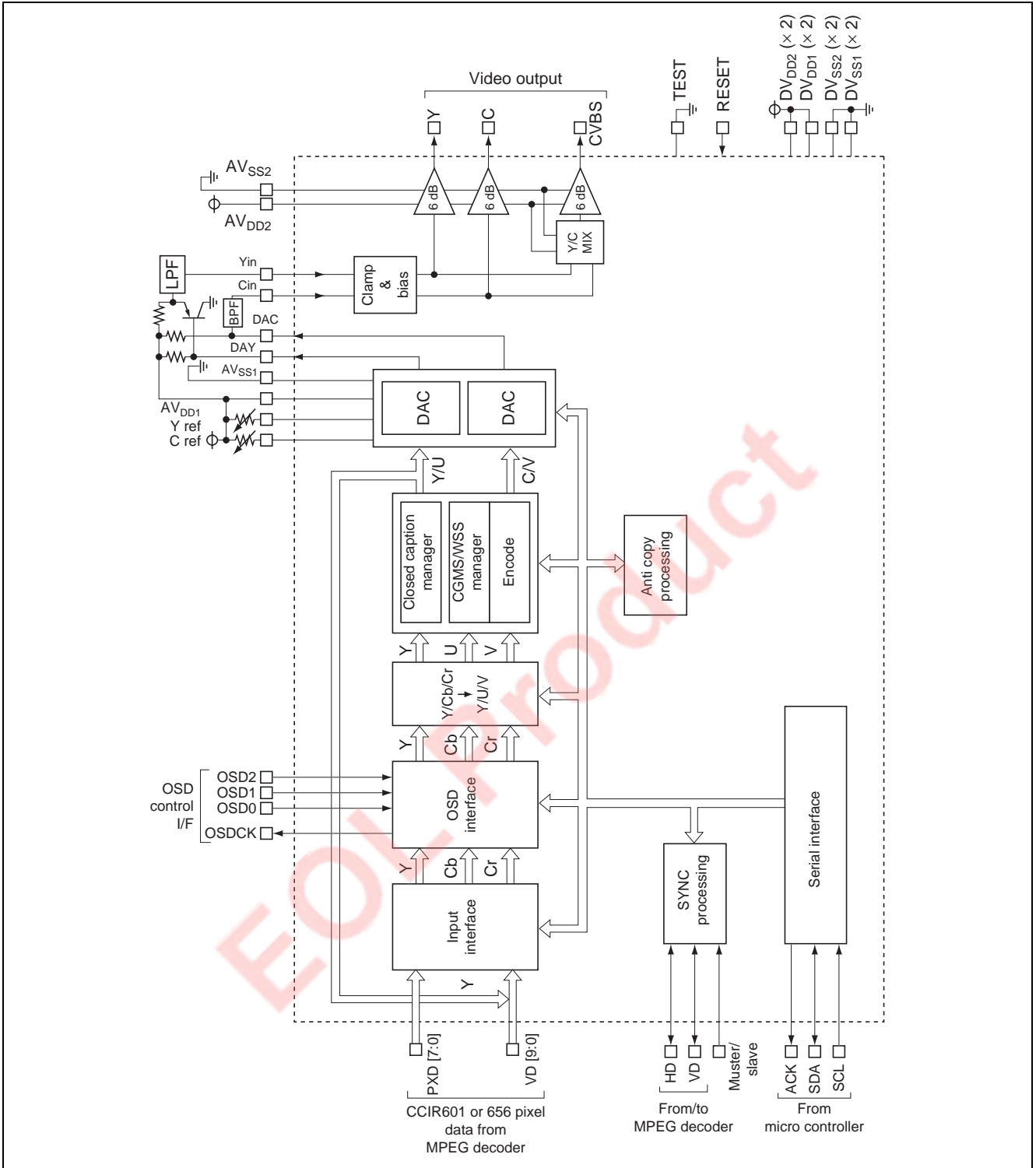
Notes: 1. This device is protected by U.S. patent numbers 4631603, 4577216 and 4819098 and other intellectual property rights. The use of Macrovision Corporation's copy protection technology in the device must be authorized by Macrovision and is intended for home and other limited pay-par-view uses only, unless otherwise authorized in writing by Macrovision. Reverse engineering or disassembly is prohibited.

2. 6 dB Amp max. output is 1.0 Vp-p
3. Copy Generation Management System-A (IEC1880)
4. Wide Screen Signaling (ETS300 294)

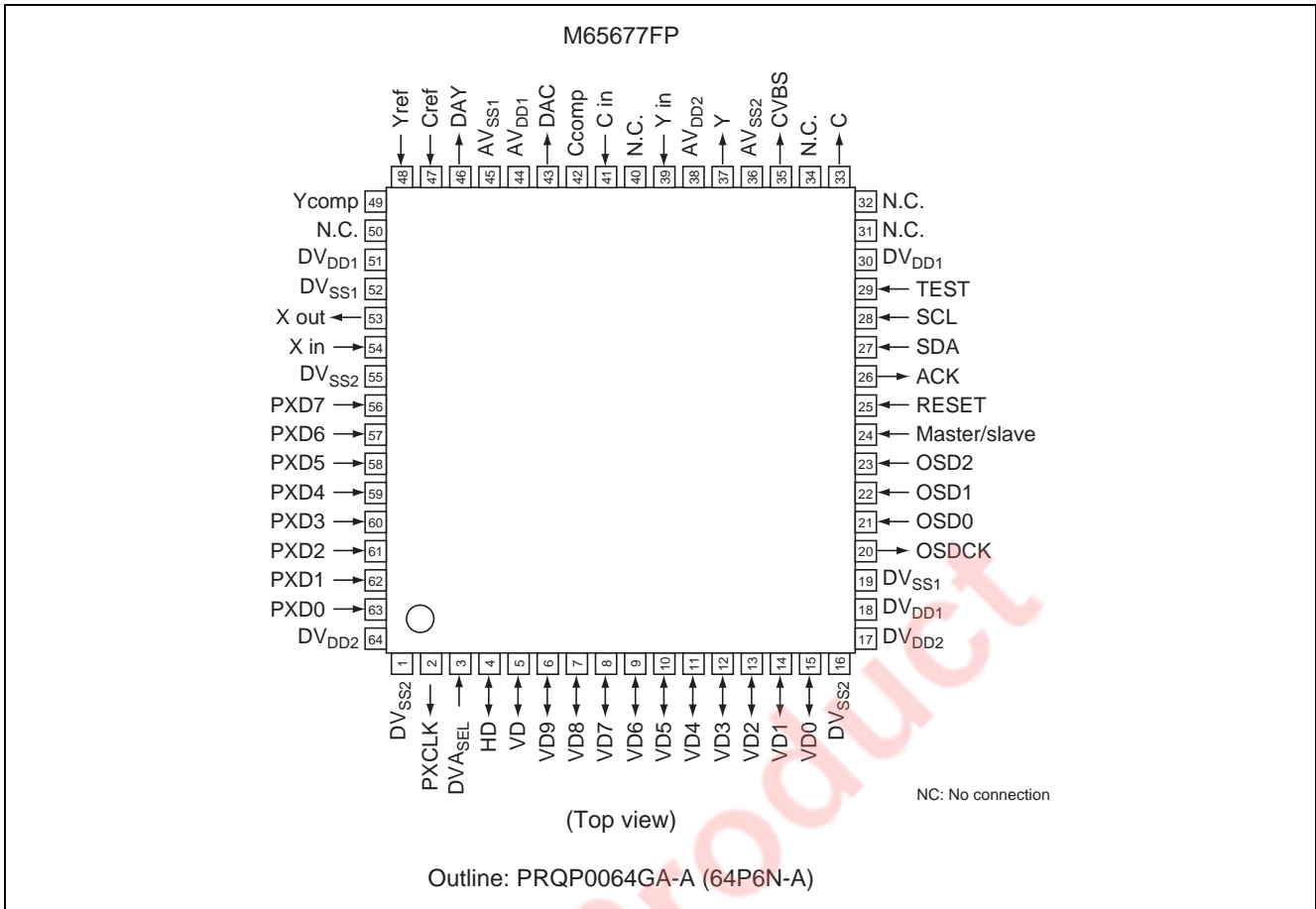
Application

DVB, DVD, Digital CATV, Video CD

Block Diagram



Pin Arrangement



Pin Description

Pin No	Pin Name	Type	Function
1	DV _{SS2}	Supply	Digital ground for the I/O
2	PXCLK	O	Reference clock for input pixel data. The clock frequency is 27.0 MHz
3	DV _A SEL	I	I ² C slave address setting. "Low" is for the address of 40h, "High" is for the address of 42h.
4	HD	I/O	Horizontal sync signal input or output. It is an input and output in the slave and master mode, respectively.
5	VD	I/O	Vertical sync input or output. Or Odd Even signal output. It is an input and output in the slave and master mode, respectively.
6	VD9	I/O	Video data outputs. In the Y/U/V output mode, the output is the 10-bit digital luma signal with a composite sync. VD9 is MSB and VD0 is LSB.
7	VD8		
8	VD7		
9	VD6		
10	VD5		
11	VD4		
12	VD3		
13	VD2		
14	VD1		
15	VD0		
16	DV _{SS2}	Supply	Digital ground for the I/O.
17	DV _{DD2}	Supply	Digital supply for the I/O
18	DV _{DD1}	Supply	Digital supply for the internal logic.
19	DV _{SS1}	Supply	Digital ground for the internal logic.
20	OSDCK	O	The reference clock for an external OSD microcontroller. The frequency is 13.5 MHz or 6.25 MHz, alternated by I ² C bus control.
21	OSD0	I	The color look-up table address input. MSB and LSB are OSD2 and OSD0, respectively.
22	OSD1		
23	OSD2		
24	Master/Slave	I	Synchronizing mode selection. "Low" is for the slave mode. "High" is for the master mode.
25	RESET	I	Initializing reset. "Low" is active.
26	ACK	O	Acknowledge line (Open drain output).
27	SDA	I/O	Serial data line/acknowledge line (Open drain output).
28	SCL	I	Serial clock line.
29	TEST	I	For testing. Is should be grounded during an actual use.
30	DV _{DD1}	Supply	Digital supply for the internal logic.
31	N.C.	—	No connection.
32	N.C.	—	No connection.
33	C	O	The analog chroma output from a 6 dB amplifier. The output amplitude is 1.0 V _{P-P} (Typ), while the input is 0.5 V _{P-P} .
34	N.C.	—	No connection.
35	CVBS	O	The analog composite video signal from a 6 dB amplifier. The output amplitude is 1.24 V _{P-P} (Typ).
36	AV _{SS2}	Supply	Analog ground for 6 dB amplifiers.
37	Y	O	The analog luma output from a 6 dB amplifier. The output amplitude is 1.2 V _{P-P} (Typ), while input is 0.6 V _{P-P} .
38	AV _{SS2}	Supply	Analog supply for 6 dB amplifiers.

Pin Description (cont.)

Pin No	Pin Name	Type	Function
39	Yin	I	The analog luma input from an external LPF. This input has bias circuit. The signal must input via a capacitor.
40	N.C.	—	No connection.
41	Cin	I	The analog chroma input from an external LPF. This input has bias circuit. The signal must input via a capacitor.
42	Ccomp	I	Phase compensation for chroma or V output DAC. It should be connected to the analog ground via a capacitor.
43	DAC	O	Chroma or V signal output. The DAC output should be connected to the analog supply via a load resistor (R_L). The output amplitude is set up by reference resistor (R_{ref}) and R_L .
44	AV _{DD1}	Supply	Analog supply for DACs.
45	AV _{SS1}	Supply	Analog ground for DACs.
46	DAY	O	Luma or U signal output. It should be connected to the analog supply via a load resistor (R_L). The output amplitude is set up by reference resistor (R_{ref}) and R_L .
47	Cref	I	A reference current source for chroma or V signal output DAC. It should be connected to the analog supply via a reference resistor (R_{ref}).
48	Yrel	I	A reference current source for Y or U DAC. It should be connected to the analog supply via a reference resistor (R_{ref}).
49	Ycomp	I	Phase compensation for Y or U DAC. It should be connected to the analog ground via a capacitor.
50	N.C.	—	No connection.
51	DV _{DD1}	Supply	Digital supply for the internal logic.
52	DV _{SS1}	Supply	Digital ground for the internal logic.
53	Xout	O	System clock output. It must be in no connection except for a connection to a X'tal oscillator.
54	Xin	I	System clock input. The clock frequency is only 27.0 MHz.
55	DV _{SS2}	Supply	Digital ground for the I/O.
56	PXD7	I	Pixel data inputs. The acceptable video data are; <ul style="list-style-type: none"> Multiplexed video data (Y/Cb/Cr) including timing reference code of SAV and EAV, defined in CCIR Rec656 Multiplexed video data (Y/Cb/Cr) defined in CCIR Rec601 MSB and LSB are PXD7 and PXD0, respectively.
57	PXD6		
58	PXD5		
59	PXD4		
60	PXD3		
61	PXD2		
62	PXD1		
63	PXD0		
64	DV _{DD2}	Supply	Digital supply for the I/O.

Absolute Maximum Ratings

Item	Symbol	Limits			Unit
		Min	Typ	Max	
Supply voltage	V _{DD}	-0.3	—	4.5	V
Digital input voltage	V _I	-0.3	—	V _{DD} + 0.3	V
Digital output voltage	V _O	-0.3	—	V _{DD} + 0.3	V
Operating temperature	T _a	-20	+25	+75	°C
Storage temperature	T _{stg}	-40	—	+125	°C

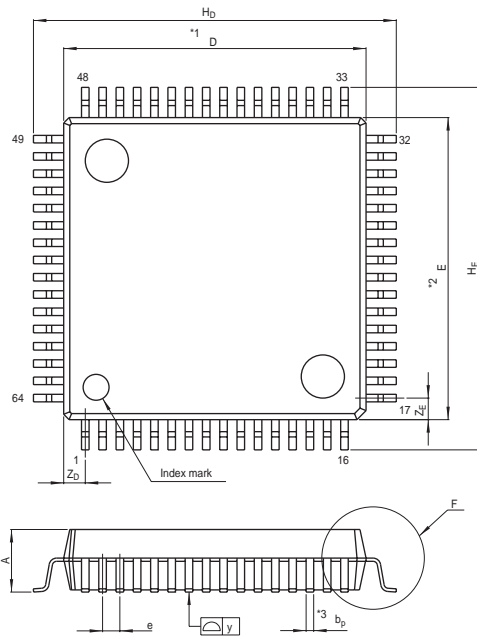
Recommended Operating Condition

($T_a = 25^\circ\text{C}$, $DV_{DD} = AV_{DD} = 3.3\text{ V}$, $DV_{SS} = AV_{SS} = 0\text{ V}$, unless otherwise noted)

Item	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Supply						
Digital supply voltage	DV_{DDX}	3.0	3.3	3.6	V	
Analog supply voltage	AV_{DDX}	3.15	3.3	3.45	V	
Digital current consumption	DI_{DD}	0	—	45	mA	
Analog current consumption	AI_{DD}	0	—	55	mA	
Digital input						
Input voltage	V_{IL}	0	—	0.8	V	$DV_{DD} = 3.0\text{ V}$
	V_{IH}	2.5	—	3.6	V	$DV_{DD} = 3.6\text{ V}$
Input leakage current	I_{IL}/I_{IH}	—	—	15	μA	$DV_{DD} = 3.0\text{ V}$, $V_I = 0\text{ V}$ or $V_I = 3.6\text{ V}$
Input capacitance	C_I	—	7	15	pF	$f = 1\text{ MHz}$, $V_{DD} = 0\text{ V}$
Digital output						
Output voltage	V_{OL}	—	—	0.05	V	$DV_{DD} = 3.3\text{ V}$, $ I_O < 1\text{ A}$
	V_{OH}	3.25	—	—	V	
Output capacitance	C_O	—	7	15	pF	$f = 1\text{ MHz}$, $V_{DD} = 0\text{ V}$
$I^2\text{C}$ Bus						
Output current	I_O	4.0	—	—	mA	$DV_{DD} = 3.0\text{ V}$, $V_{IL} = 0.4\text{ V}$
Output leakage current (off)	I_{OZ}	—	—	15	μA	$DV_{DD} = 3.6\text{ V}$, $V_I = 0\text{ V}$ or $V_I = 3.6\text{ V}$
D/A converter						
Resolution	Res	—	10	—	Bit	
Integral non-linearity error	INL	—	—	2.0	LSB	
Differential non-linearity error	DNL	—	—	1.0	LSB	
Maximum output amplitude	$V_{fS_{MAX}}$	1.5	—	—	V _{p-p}	
6-dB amplifier						
Bias resistor	R_{bias}	7.5	10.0	11.5	k Ω	
Output gain (Y/C)	$G_{V_{YC}}$	5.50	6.00	6.50	dB	
Output Gain (CVBS)	$G_{V_{CV}}$	5.10	6.00	6.85	dB	
Input dynamic range	DR_{in}	0.8	—	—	V _{p-p}	
Output dynamic range	DR_{out}	1.6	—	—	V _{p-p}	
Yin clamp charge current	I_{ych}	-12	-26	-50	μA	
Yin clamp discharge current	I_{yids}	0.26	0.65	1.80	μA	
Yin clamp discharge current	R_{ycl}	20	0.65	70	—	$R_{ycl} = -\frac{I_{ych}}{I_{yids}}$
Yin input clamp voltage	V_{ycl}	0.45	0.50	0.55	V	
Yin output clamp voltage	V_{yocl}	0.40	0.50	0.60	V	
CVBS output clamp voltage	V_{cvcl}	0.30	0.50	0.70	V	
Cin input bias voltage	V_{cin}	0.95	1.00	1.05	V	
C output bias voltage	V_{cob}	0.90	1.00	1.10	V	
Output current	I_{amp}	1.00	—	—	mA	

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP64-14x14-0.80	PRQP0064GA-A	64P6N-A	1.1g



NOTE)
 1. DIMENSIONS **1* AND **2* DO NOT INCLUDE MOLD FLASH.
 2. DIMENSION **3* DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.8	14.0	14.2
E	13.8	14.0	14.2
A ₂	—	2.8	—
H _D	16.5	16.8	17.1
H _E	16.5	16.8	17.1
A	—	—	3.05
A ₁	0	0.1	0.2
b _p	0.3	0.35	0.45
c	0.13	0.15	0.2
θ	0°	—	10°
e	0.65	0.8	0.95
y	—	—	0.10
Z _D	—	1.0	—
Z _E	—	1.0	—
L	0.4	0.6	0.8

EOL Product

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Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.
Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7858/7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2377-3473

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 3518-3399

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510