To our customers,

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Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.



Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

# M37735M4BXXXFP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER



## DESCRIPTION

The M37735M4BXXXFP is a single-chip microcomputer using the 7700 Family core. This single-chip microcomputer has a CPU and a bus interface unit. The CPU is a 16-bit parallel processor that can be an 8-bit parallel processor, and the bus interface unit enhances the memory access efficiency to execute instructions fast. This microcomputer also includes a 32 kHz oscillation circuit, in addition to the ROM, RAM, multiple-function timers, serial I/O, A-D converter, and so on.

## FEATURES

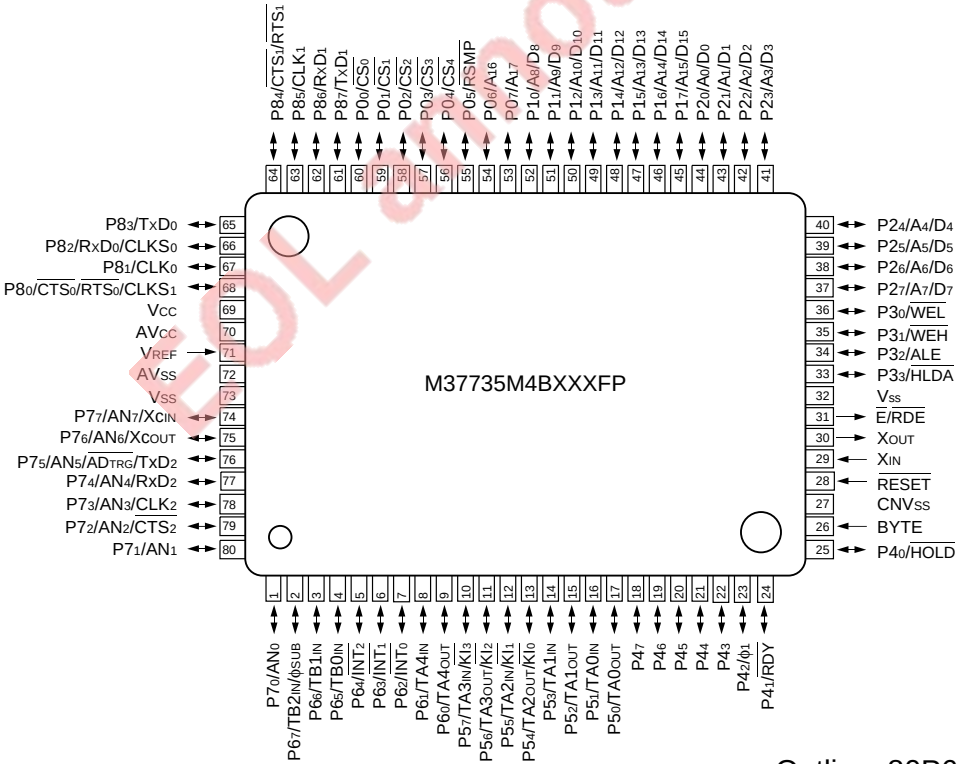
- Number of basic instructions ..... 103
- Memory size ROM ..... 32 Kbytes
  RAM ..... 2048 bytes
- Instruction execution time
  The fastest instruction at 25 MHz frequency ..... 160 ns
- Single power supply ..... 5 V ± 10%
- Low power dissipation (at 25 MHz frequency)
  .....47.5 mW (Typ.)
- Interrupts ..... 19 types, 7 levels
- Multiple-function 16-bit timer ..... 5 + 3
- Serial I/O (UART or clock synchronous) ..... 3
- 10-bit A-D converter ..... 8-channel inputs
- 12-bit watchdog timer
- Programmable input/output
  (ports P0, P1, P2, P3, P4, P5, P6, P7, P8) ..... 68
- Clock generating circuit ..... 2 circuits built-in

## APPLICATION

Control devices for general commercial equipment such as office automation, office equipment, and so on.
Control devices for general industrial equipment such as communication equipment, and so on.

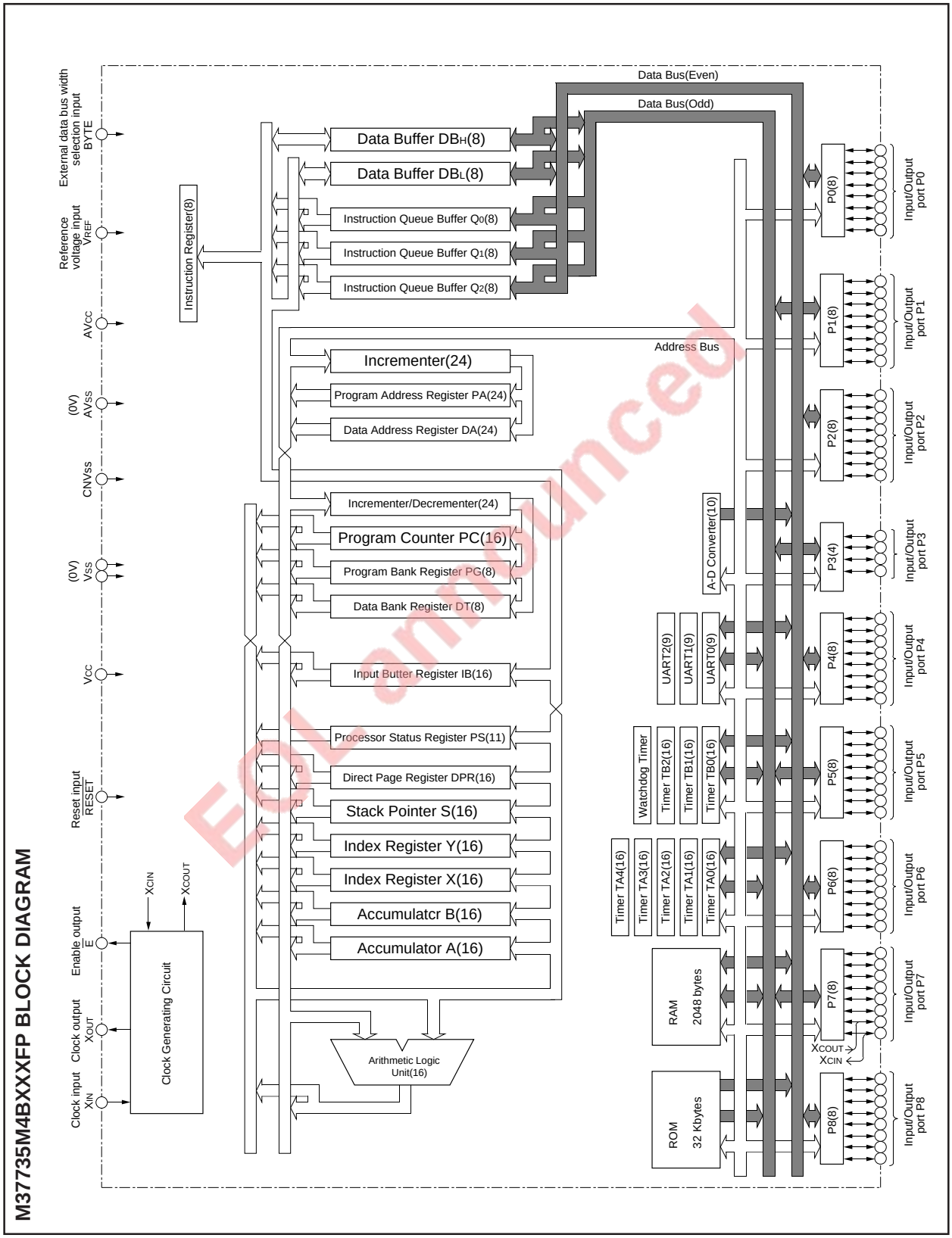


## PIN CONFIGURATION (TOP VIEW)




Outline 80P6N-A

## M37735M4BXXXFP BLOCK DIAGRAM



## FUNCTIONS OF M37735M4BXXXFP

| Parameter | | Functions |
|---|---|---|
| Number of basic instructions | | 103 |
| Instruction execution time | | 160 ns (the fastest instruction at external clock 25 MHz frequency) |
| Memory size | ROM | 32 Kbytes |
| | RAM | 2048 bytes |
| Input/Output ports | P0 – P2, P4 – P8 | 8-bit × 8 |
| | P3 | 4-bit × 1 |
| Multi-function timers | TA0, TA1, TA2, TA3, TA4 | 16-bit × 5 |
| | TB0, TB1, TB2 | 16-bit × 3 |
| Serial I/O | | (UART or clock synchronous serial I/O) × 3 |
| A-D converter | | 10-bit × 1 (8 channels) |
| Watchdog timer | | 12-bit × 1 |
| Interrupts | | 3 external types, 16 internal types<br>Each interrupt can be set to the priority level (0 – 7.) |
| Clock generating circuit | | 2 circuits built-in (externally connected to a ceramic resonator or a quartz-crystal oscillator) |
| Supply voltage | | 5 V ± 10% |
| Power dissipation | | 47.5 mW (at external clock 25 MHz frequency) |
| Input/Output characteristic | Input/Output voltage | 5 V |
| | Output current | 5 mA |
| Memory expansion | | Maximum 1 Mbytes |
| Operating temperature range | | –20 to 85 °C |
| Device structure | | CMOS high-performance silicon gate process |
| Package | | 80-pin plastic molded QFP (80P6N-A) |

## PIN DESCRIPTION

| Pin | Name | Input/Output | Functions |
|---|---|---|---|
| Vcc, Vss | Power source | | Apply 5 V ± 10% to Vcc and 0 V to Vss. |
| CNVss | CNVss input | Input | This pin controls the processor mode. Connect to Vss for the single-chip mode and the memory expansion mode, and to Vcc for the microprocessor mode. |
| $\overline{\text{RESET}}$ | Reset input | Input | When "L" level is applied to this pin, the microcomputer enters the reset state. |
| $X_{IN}$ | Clock input | Input | These are pins of main-clock generating circuit. Connect a ceramic resonator or a quartz-crystal oscillator between $X_{IN}$ and $X_{OUT}$. When an external clock is used, the clock source should be connected to the $X_{IN}$ pin, and the $X_{OUT}$ pin should be left open. |
| $X_{OUT}$ | Clock output | Output | |
| $\overline{E}$ | Enable output | Output | This pin functions as the enable signal output pin which indicates the access status in the internal bus. In the memory expansion mode or the microprocessor mode, this pin functions as the $\overline{\text{RDE}}$ signal output pin. |
| BYTE | External data bus width selection input | Input | In the memory expansion mode or the microprocessor mode, this pin determines whether the external data bus has an 8-bit width or a 16-bit width. The data bus has a 16-bit width when "L" signal is input and an 8-bit width when "H" signal is input. |
| AVcc, AVss | Analog power source input | | Power source input pin for the A-D converter. Externally connect AVcc to Vcc and AVss to Vss. |
| $V_{REF}$ | Reference voltage input | Input | This is reference voltage input pin for the A-D converter. |
| $P0_0$ – $P0_7$ | I/O port P0 | I/O | In the single-chip mode, port P0 becomes an 8-bit I/O port. An I/O direction register is available so that each pin can be programmed for input or output. These ports are in the input mode when reset.<br>In the memory expansion mode or the microprocessor mode, these pins output $\overline{CS_0}$ – $\overline{CS_4}$, $\overline{\text{RSMP}}$ signals, and address ($A_{16}$, $A_{17}$). |
| $P1_0$ – $P1_7$ | I/O port P1 | I/O | In the single-chip mode, these pins have the same functions as port P0. When the BYTE pin is set to "L" in the memory expansion mode or the microprocessor mode and external data bus has a 16-bit width, high-order data ($D_8$ – $D_{15}$) is input/output or an address ($A_8$ – $A_{15}$) is output. When the BYTE pin is "H" and an external data bus has an 8-bit width, only address ($A_8$ – $A_{15}$) is output. |
| $P2_0$ – $P2_7$ | I/O port P2 | I/O | In the single-chip mode, these pins have the same functions as port P0. In the memory expansion mode or the microprocessor mode, low-order data ($D_0$ – $D_7$) is input/output or an address ($A_0$ – $A_7$) is output . |
| $P3_0$ – $P3_3$ | I/O port P3 | I/O | In the single-chip mode, these pins have the same function as port P0. In the memory expansion mode or the microprocessor mode, $\overline{\text{WEL}}$, $\overline{\text{WEH}}$, ALE, and $\overline{\text{HLDA}}$ signals are output. |
| $P4_0$ – $P4_7$ | I/O port P4 | I/O | In the single-chip mode, these pins have the same functions as port P0. In the memory expansion mode or the microprocessor mode, $P4_0$, $P4_1$ and $P4_2$ become $\overline{\text{HOLD}}$ and $\overline{\text{RDY}}$ input pins, and a clock $\phi_1$ output pin, respectively. Functions of the other pins are the same as in the single-chip mode. However, in the memory expansion mode, $P4_2$ can be selected as an I/O port. |
| $P5_0$ – $P5_7$ | I/O port P5 | I/O | In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for timers A0 to A3 and input pins for key input interrupt input ($\overline{KI_0}$ – $\overline{KI_3}$ ). |
| $P6_0$ – $P6_7$ | I/O port P6 | I/O | In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for timer A4, input pins for external interrupt input ($\overline{INT_0}$ – $\overline{INT_2}$) and input pins for timers B0 to B2. $P6_7$ also functions as a sub-clock $\phi_{SUB}$ output pin. |
| $P7_0$ – $P7_7$ | I/O port P7 | I/O | In addition to having the same functions as port P0 in the single-chip mode, these pins function as input pins for A-D converter. $P7_2$ to $P7_5$ also function as I/O pins for UART2. Additionally, $P7_6$ and $P7_7$ have the function as the output pin ($X_{COUT}$) and the input pin ($X_{CIN}$) of the sub-clock (32 kHz) oscillation circuit, respectively. When $P7_6$ and $P7_7$ are used as the $X_{COUT}$ and $X_{CIN}$ pins, connect a resonator or an oscillator between the both. |
| $P8_0$ – $P8_7$ | I/O port P8 | I/O | In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for UART 0 and UART 1. |

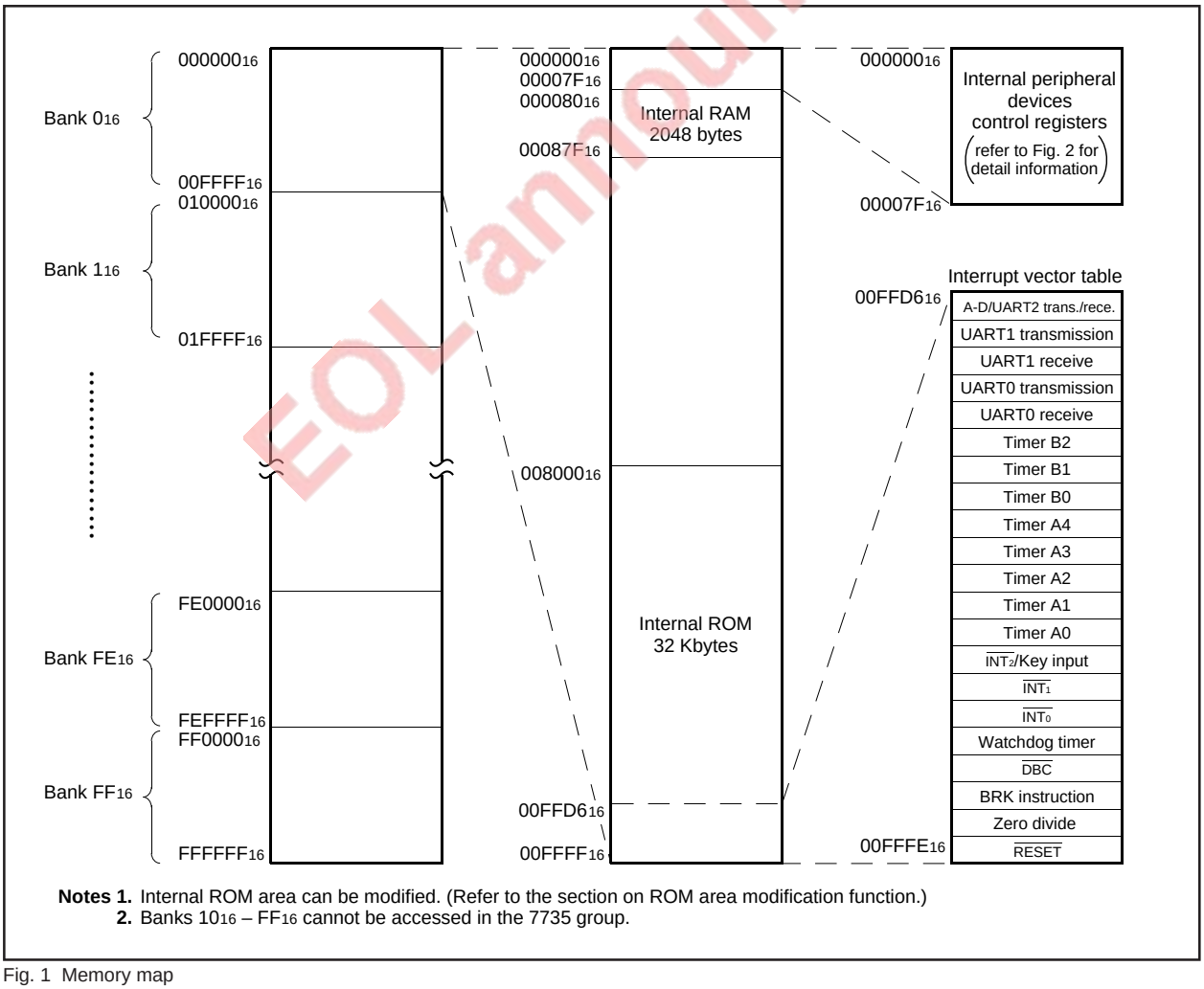
## BASIC FUNCTION BLOCKS

The M37735M4BXXXFP has the same fuanctions as the M37735MHBXXXFP except for the memory allocation and the ROM area modification function.
Refer to the section on the M37735MHBXXXFP.

## MEMORY

The memory map is shown in Figure 1. The address space has a capacity of 16 Mbytes and is allocated to addresses from $0_{16}$ to $FFFFFF_{16}$. The address space is divided by 64-Kbyte unit called bank. The banks are numbered from $0_{16}$ to $FF_{16}$.
However, banks $10_{16}$ – $FF_{16}$ of the 7735 group cannot be accessed. Built-in ROM, RAM and control registers for internal peripheral devices are assigned to bank $0_{16}$.
The 32-Kbyte area from addresses $8000_{16}$ to $FFFF_{16}$ is the built-in ROM. Addresses $FFD6_{16}$ to $FFFF_{16}$ are the RESET and interrupt vector addresses and contain the interrupt vectors. Refer to the section on interrupts for details.
The 2048-byte area allocated to addresses from $80_{16}$ to $87F_{16}$ is the built-in RAM. In addition to storing data, the RAM is used as stack during a subroutine call or interrupts.
Peripheral devices such as I/O ports, A-D converter, serial I/O, timer, and interrupt control registers are allocated to addresses from $0_{16}$ to $7F_{16}$.
Additionally, the internal ROM area can be modified by software. Refer to the section on ROM area modification function for details.
A 256-byte direct page area can be allocated anywhere in bank $0_{16}$ by using the direct page register (DPR). In the direct page addressing mode, the memory in the direct page area can be accessed with two words. Hence program steps can be reduced.






**Notes 1.** Internal ROM area can be modified. (Refer to the section on ROM area modification function.)
**2.** Banks $10_{16}$ – $FF_{16}$ cannot be accessed in the 7735 group.

Fig. 1 Memory map

| Address (Hexadecimal notation) | |
|---|---|
| 000000 | |
| 000001 | |
| 000002 | Port P0 register |
| 000003 | Port P1 register |
| 000004 | Port P0 direction register |
| 000005 | Port P1 direction register |
| 000006 | Port P2 register |
| 000007 | Port P3 register |
| 000008 | Port P2 direction register |
| 000009 | Port P3 direction register |
| 00000A | Port P4 register |
| 00000B | Port P5 register |
| 00000C | Port P4 direction register |
| 00000D | Port P5 direction register |
| 00000E | Port P6 register |
| 00000F | Port P7 register |
| 000010 | Port P6 direction register |
| 000011 | Port P7 direction register |
| 000012 | Port P8 register |
| 000013 | |
| 000014 | Port P8 direction register |
| 000015 | |
| 000016 | |
| 000017 | |
| 000018 | |
| 000019 | |
| 00001A | |
| 00001B | |
| 00001C | Reserved area (Note) |
| 00001D | Reserved area (Note) |
| 00001E | A-D control register 0 |
| 00001F | A-D control register 1 |
| 000020 | A-D register 0 |
| 000021 | |
| 000022 | A-D register 1 |
| 000023 | |
| 000024 | A-D register 2 |
| 000025 | |
| 000026 | A-D register 3 |
| 000027 | |
| 000028 | A-D register 4 |
| 000029 | |
| 00002A | A-D register 5 |
| 00002B | |
| 00002C | A-D register 6 |
| 00002D | |
| 00002E | A-D register 7 |
| 00002F | |
| 000030 | UART 0 transmit/receive mode register |
| 000031 | UART 0 baud rate register (BRG0) |
| 000032 | UART 0 transmission buffer register |
| 000033 | |
| 000034 | UART 0 transmit/receive control register 0 |
| 000035 | UART 0 transmit/receive control register 1 |
| 000036 | UART 0 receive buffer register |
| 000037 | |
| 000038 | UART 1 transmit/receive mode register |
| 000039 | UART 1 baud rate register (BRG1) |
| 00003A | UART 1 transmission buffer register |
| 00003B | |
| 00003C | UART 1 transmit/receive control register 0 |
| 00003D | UART 1 transmit/receive control register 1 |
| 00003E | UART 1 receive buffer register |
| 00003F | |

| Address (Hexadecimal notation) | |
|---|---|
| 000040 | Count start flag |
| 000041 | |
| 000042 | One-shot start flag |
| 000043 | |
| 000044 | Up-down flag |
| 000045 | |
| 000046 | Timer A0 register |
| 000047 | |
| 000048 | Timer A1 register |
| 000049 | |
| 00004A | Timer A2 register |
| 00004B | |
| 00004C | Timer A3 register |
| 00004D | |
| 00004E | Timer A4 register |
| 00004F | |
| 000050 | Timer B0 register |
| 000051 | |
| 000052 | Timer B1 register |
| 000053 | |
| 000054 | Timer B2 register |
| 000055 | |
| 000056 | Timer A0 mode register |
| 000057 | Timer A1 mode register |
| 000058 | Timer A2 mode register |
| 000059 | Timer A3 mode register |
| 00005A | Timer A4 mode register |
| 00005B | Timer B0 mode register |
| 00005C | Timer B1 mode register |
| 00005D | Timer B2 mode register |
| 00005E | Processor mode register 0 |
| 00005F | Processor mode register 1 |
| 000060 | Watchdog timer register |
| 000061 | Watchdog timer frequency selection flag |
| 000062 | Reserved area (Note) |
| 000063 | Memory allocation control register |
| 000064 | UART 2 transmit/receive mode register |
| 000065 | UART 2 baud rate register (BRG2) |
| 000066 | UART 2 transmission buffer register |
| 000067 | |
| 000068 | UART 2 transmit/receive control register 0 |
| 000069 | UART 2 transmit/receive control register 1 |
| 00006A | UART 2 receive buffer register |
| 00006B | |
| 00006C | Oscillation circuit control register 0 |
| 00006D | Port function control register |
| 00006E | Serial transmit control register |
| 00006F | Oscillation circuit control register 1 |
| 000070 | A-D/UART 2 trans./rece. interrupt control register |
| 000071 | UART 0 transmission interrupt control register |
| 000072 | UART 0 receive interrupt control register |
| 000073 | UART 1 transmission interrupt control register |
| 000074 | UART 1 receive interrupt control register |
| 000075 | Timer A0 interrupt control register |
| 000076 | Timer A1 interrupt control register |
| 000077 | Timer A2 interrupt control register |
| 000078 | Timer A3 interrupt control register |
| 000079 | Timer A4 interrupt control register |
| 00007A | Timer B0 interrupt control register |
| 00007B | Timer B1 interrupt control register |
| 00007C | Timer B2 interrupt control register |
| 00007D | $\overline{INT_0}$ interrupt control register |
| 00007E | $\overline{INT_1}$ interrupt control register |
| 00007F | $\overline{INT_2}$/Key input interrupt control register |

**Note.** Do not write to this address.

Fig. 2 Location of internal peripheral devices and interrupt control registers

## ROM AREA MODIFICATION FUNCTION

The internal ROM size and its address area of the M37735M4BXXXFP can be modified by the memory allocation control register's bit 0 shown in Figure 3.

Figure 5 shows the memory allocation in which the internal ROM size and its address area are modified.

Make sure to write data in the memory allocation control register as the flow shown in Figure 4.

This ROM area modification function is valid in memory expansion mode and single-chip mode.

Table 1 shows the relationship between memory allocation selection bits and address corresponding to chip-select signals $\overline{CS_0}$ and $\overline{CS_1}$.

When ordering a mask ROM, Mitsubishi Electric corp. produces the mask ROM using the data within 32 Kbytes (addresses $008000_{16}$ – $00FFFF_{16}$). It is regardless of the selected ROM size (refer to MASK ROM ORDER CONFIRMATION FORM.) Therefore, program "$FF_{16}$" to the addresses out of the selected ROM area in the EPROM which you tender when ordering a mask ROM.

Address $00FFFF_{16}$ of this microcomputer corresponds to the lowest address of the EPROM which you tender.

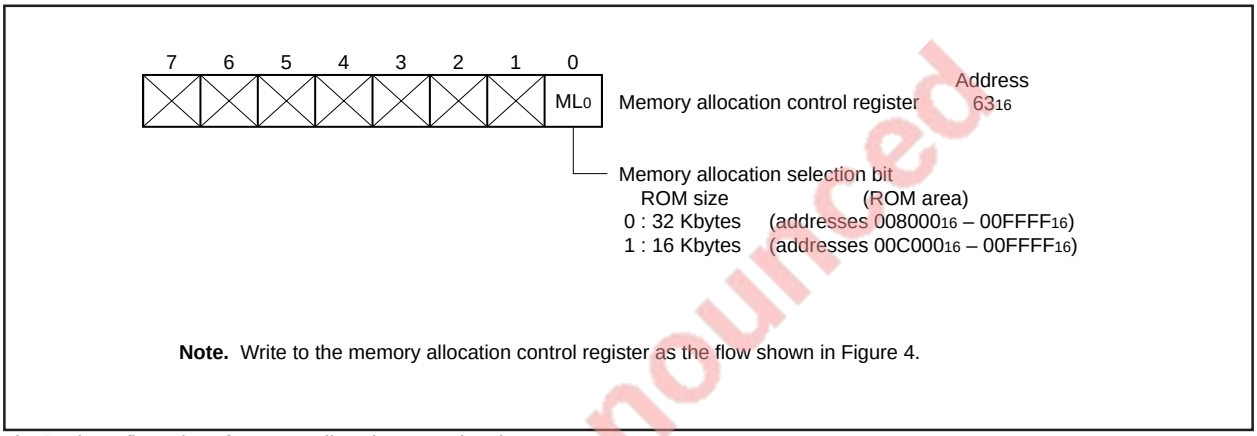



Fig. 3 Bit configuration of memory allocation control register

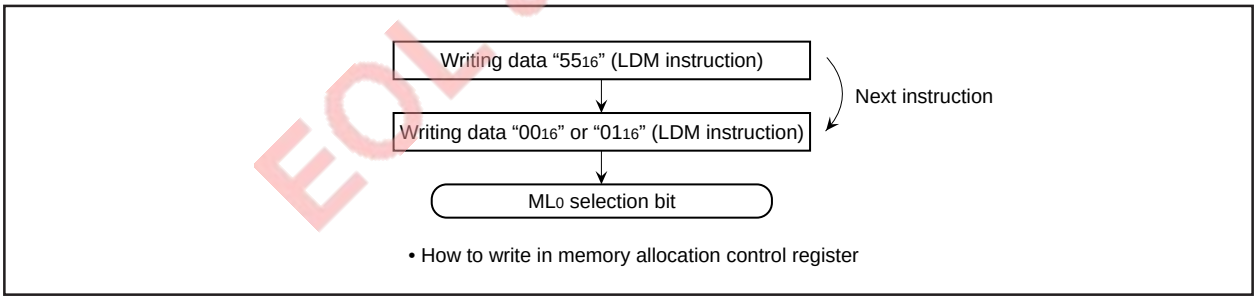



Fig. 4 How to write data in memory allocation control register

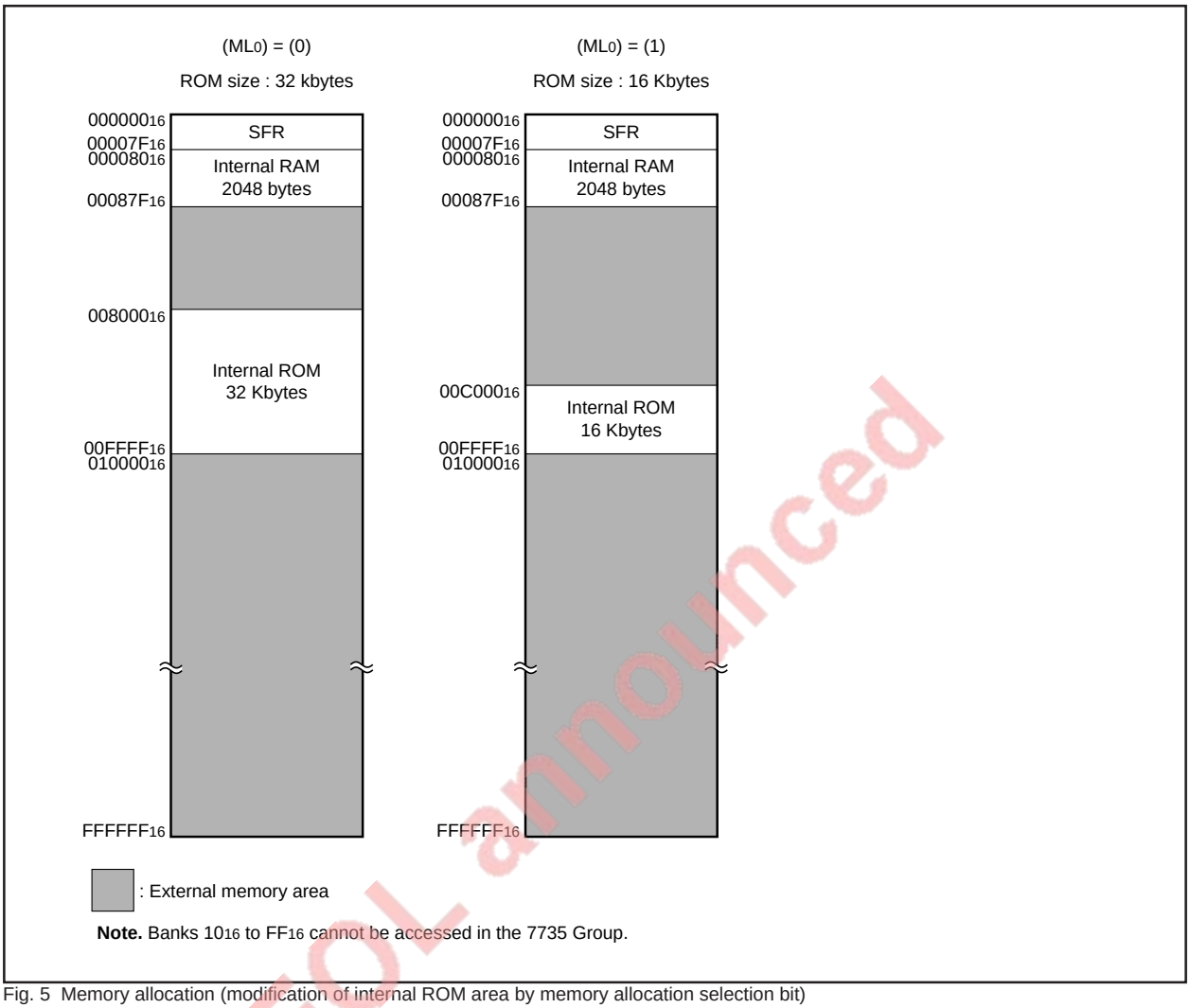



Fig. 5 Memory allocation (modification of internal ROM area by memory allocation selection bit)

Table 1. Relationship between memory allocation selection bits and addresses corresponding to chip-select signals $\overline{CS_0}$ and $\overline{CS_1}$

| Memory allocation select bit $ML_0$ | Internal ROM area | Access address | |
|---|---|---|---|
| | | $\overline{CS_0}$ | $\overline{CS_1}$ |
| 0 | 008000₁₆ – 00FFFF₁₆ | 000880₁₆ – 007FFF₁₆ | 010000₁₆ – 03FFFF₁₆ |
| 1 | 00C000₁₆ – 00FFFF₁₆ | 000880₁₆ – 007FFF₁₆ | 008000₁₆ – 00BFFF₁₆<br>010000₁₆ – 03FFFF₁₆ |

## ADDRESSING MODES

The M37735M4BXXXFP has 28 powerful addressing modes. Refer to the MITSUBISHI SEMICONDUCTORS DATA BOOK SINGLE-CHIP 16-BIT MICROCOMPUTERS for the details of each addressing mode.

## MACHINE INSTRUCTION LIST

The M37735M4BXXXFP has 103 machine instructions. Refer to the MITSUBISHI SEMICONDUCTORS DATA BOOK SINGLE-CHIP 16-BIT MICROCOMPUTERS for details.

## DATA REQUIRED FOR MASK ROM ORDERING

Please send the following data for mask orders.
(1) M37735M4BXXXFP mask ROM order confirmation form
(2) 80P6N mark specification form
(3) ROM data (EPROM 3 sets)

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Vcc | Power source voltage | | –0.3 to +7 | V |
| AVcc | Analog power source voltage | | –0.3 to +7 | V |
| $V_I$ | Input voltage $\overline{RESET}$, CNVss, BYTE | | –0.3 to +12 | V |
| $V_I$ | Input voltage $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_7$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$, $V_{REF}$, $X_{IN}$ | | –0.3 to Vcc + 0.3 | V |
| $V_O$ | Output voltage $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_7$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$, $X_{OUT}$, $\overline{E}$ | | –0.3 to Vcc + 0.3 | V |
| $P_d$ | Power dissipation | Ta = 25 °C | 300 | mW |
| $T_{opr}$ | Operating temperature | | –20 to +85 | °C |
| $T_{stg}$ | Storage temperature | | –40 to +150 | °C |

## RECOMMENDED OPERATING CONDITIONS (Vcc = 5 V ± 10%, Ta = –20 to +85 °C, unless otherwise noted)

| Symbol | Parameter | | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Vcc | Power source voltage | f($X_{IN}$) : Operating | 4.5 | 5.0 | 5.5 | V |
| | | f($X_{IN}$) : Stopped, f($X_{CIN}$) = 32.768 kHz | 2.7 | | 5.5 | |
| AVcc | Analog power source voltage | | | Vcc | | V |
| Vss | Power source voltage | | | 0 | | V |
| AVss | Analog power source voltage | | | 0 | | V |
| $V_{IH}$ | High-level input voltage $P0_0$ – $P0_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_7$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$, $X_{IN}$, $\overline{RESET}$, CNVss, BYTE, $X_{CIN}$ (Note 3) | | 0.8 Vcc | | Vcc | V |
| $V_{IH}$ | High-level input voltage $P1_0$ – $P1_7$, $P2_0$ – $P2_7$ (in single-chip mode) | | 0.8 Vcc | | Vcc | V |
| $V_{IH}$ | High-level input voltage $P1_0$ – $P1_7$, $P2_0$ – $P2_7$ (in memory expansion mode and microprocessor mode) | | 0.5 Vcc | | Vcc | V |
| $V_{IL}$ | Low-level input voltage $P0_0$ – $P0_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_7$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$, $X_{IN}$, $\overline{RESET}$, CNVss, BYTE, $X_{CIN}$ (Note 3) | | 0 | | 0.2Vcc | V |
| $V_{IL}$ | Low-level input voltage $P1_0$ – $P1_7$, $P2_0$ – $P2_7$ (in single-chip mode) | | 0 | | 0.2Vcc | V |
| $V_{IL}$ | Low-level input voltage $P1_0$ – $P1_7$, $P2_0$ – $P2_7$ (in memory expansion mode and microprocessor mode) | | 0 | | 0.16Vcc | V |
| $I_{OH(peak)}$ | High-level peak output current $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_7$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$ | | | | –10 | mA |
| $I_{OH(avg)}$ | High-level average output current $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_7$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$ | | | | –5 | mA |
| $I_{OL(peak)}$ | Low-level peak output current $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_3$, $P5_4$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$ | | | | 10 | mA |
| $I_{OL(peak)}$ | Low-level peak output current $P4_4$ – $P4_7$, $P5_0$ – $P5_3$ | | | | 20 | mA |
| $I_{OL(avg)}$ | Low-level average output current $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_3$, $P5_4$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$ | | | | 5 | mA |
| $I_{OL(avg)}$ | Low-level average output current $P4_4$ – $P4_7$, $P5_0$ – $P5_3$ | | | | 15 | mA |
| f($X_{IN}$) | Main-clock oscillation frequency (Note 4) | | | | 25 | MHz |
| f($X_{CIN}$) | Sub-clock oscillation frequency | | | 32.768 | 50 | kHz |

**Notes 1.** Average output current is the average value of a 100 ms interval.

**2.** The sum of $I_{OL(peak)}$ for ports P0, P1, P2, P3, and P8 must be 80 mA or less,
the sum of $I_{OH(peak)}$ for ports P0, P1, P2, P3, and P8 must be 80 mA or less,
the sum of $I_{OL(peak)}$ for ports P4, P5, P6, and P7 must be 100 mA or less, and
the sum of $I_{OH(peak)}$ for ports P4, P5, P6, and P7 must be 80 mA or less.

**3.** Limits $V_{IH}$ and $V_{IL}$ for $X_{CIN}$ are applied when the sub clock external input selection bit = “1”.

**4.** The maximum value of f($X_{IN}$) = 12.5 MHz when the main clock division selection bit = “1”.

## ELECTRICAL CHARACTERISTICS (Vcc = 5 V, Vss = 0 V, Ta = –20 to 85 °C, f(XIN) = 25 MHz, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{OH}$ | High-level output voltage $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_3$, $P4_0$ – $P4_7$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$ | $I_{OH}$ = –10 mA | 3 | | | V |
| $V_{OH}$ | High-level output voltage $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_3$ | $I_{OH}$ = –400 µA | 4.7 | | | V |
| $V_{OH}$ | High-level output voltage $P3_0$ – $P3_2$ | $I_{OH}$ = –10 mA | 3.1 | | | V |
| | | $I_{CH}$ = –400 µA | 4.8 | | | |
| $V_{OH}$ | High-level output voltage $\overline{E}$ | $I_{OH}$ = –10 mA | 3.4 | | | V |
| | | $I_{OH}$ = –400 µA | 4.8 | | | |
| $V_{OL}$ | Low-level output voltage $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_3$, $P4_0$ – $P4_3$, $P5_4$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_5$, $P8_0$ – $P8_7$ | $I_{OL}$ = 10 mA | | | 2 | V |
| $V_{OL}$ | Low-level output voltage $P4_4$ – $P4_7$, $P5_0$ – $P5_3$ | $I_{OL}$ = 20 mA | | | 2 | V |
| $V_{OL}$ | Low-level output voltage $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_3$ | $I_{OL}$ = 2 mA | | | 0.45 | V |
| $V_{OL}$ | Low-level output voltage $P3_0$ – $P3_2$ | $I_{OL}$ = 10 mA | | | 1.9 | V |
| | | $I_{OL}$ = 2 mA | | | 0.43 | |
| $V_{OL}$ | Low-level output voltage $\overline{E}$ | $I_{OL}$ = 10 mA | | | 1.6 | V |
| | | $I_{OL}$ = 2 mA | | | 0.4 | |
| $V_{T+} – V_{T–}$ | Hysteresis $\overline{HOLD}$, $\overline{RDY}$, TA0IN – TA4IN, TB0IN – TB2IN, $\overline{INT0}$ – $\overline{INT2}$, $\overline{ADTRG}$, $\overline{CTS0}$, $\overline{CTS1}$, $\overline{CTS2}$, CLK0, CLK1, CLK2, $\overline{KI0}$ – $\overline{KI3}$ | | 0.4 | | 1 | V |
| $V_{T+} – V_{T–}$ | Hysteresis $\overline{RESET}$ | | 0.2 | | 0.5 | V |
| $V_{T+} – V_{T–}$ | Hysteresis XIN | | 0.1 | | 0.4 | V |
| $V_{T+} – V_{T–}$ | Hysteresis XCIN (When external clock is input) | | 0.1 | | 0.4 | V |
| $I_{IH}$ | High-level input current $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_7$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$, XIN, $\overline{RESET}$, CNVss, BYTE | $V_I$ = 5 V | | | 5 | µA |
| $I_{IL}$ | Low-level input current $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_7$, $P5_0$ – $P5_3$, $P6_0$, $P6_1$, $P6_5$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$, XIN, $\overline{RESET}$, CNVss, BYTE | $V_I$ = 0 V | | | –5 | µA |
| $I_{IL}$ | Low-level input current $P5_4$ – $P5_7$, $P6_2$ – $P6_4$ | $V_I$ = 0 V, without a pull-up transistor | | | –5 | µA |
| | | $V_I$ = 0 V, with a pull-up transistor | –0.25 | –0.5 | –1.0 | mA |
| $V_{RAM}$ | RAM hold voltage | When clock is stopped. | 2 | | | V |

## ELECTRICAL CHARACTERISTICS ($V_{CC}$ = 5 V, $V_{SS}$ = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $I_{CC}$ | Power source current | In single-chip mode, output pins are open, and other pins are $V_{SS}$. | $V_{CC}$ = 5 V, $f(X_{IN})$ = 25 MHz (square waveform), $f(f_2)$ = 12.5 MHz, $f(X_{CIN})$ = 32.768 kHz, in operating (Note 1) | | 9.5 | 19 | mA |
| | | | $V_{CC}$ = 5 V, $f(X_{IN})$ = 25 MHz (square waveform), ($f(f_2)$ = 1.5625 MHz), $f(X_{CIN})$ = Stopped, in operating (Note 1) | | 1.3 | 2.6 | mA |
| | | | $V_{CC}$ = 5V, $f(X_{IN})$ = 25 MHz (square waveform), $f(X_{CIN})$ = 32.768 kHz, when a WIT instruction is executed (Note 2) | | 10 | 20 | μA |
| | | | $V_{CC}$ = 5 V, $f(X_{IN})$ : Stopped, $f(X_{CIN})$ : 32.768 kHz, in operating (Note 3) | | 50 | 100 | μA |
| | | | $V_{CC}$ = 5 V, $f(X_{IN})$ : Stopped, $f(X_{CIN})$ : 32.768 kHz, when a WIT instruction is executed (Note 4) | | 5 | 10 | μA |
| | | | Ta = 25 °C, when clock is stopped | | | 1 | μA |
| | | | Ta = 85 °C, when clock is stopped | | | 20 | μA |

**Notes 1.** This applies when the main clock external input selection bit = "1", the main clock division selection bit = "0", and the signal output stop bit = "1".
**2.** This applies when the main clock external input selection bit = "1" and the system clock stop bit at wait state = "1".
**3.** This applies when CPU and the clock timer are operating with the sub clock (32.768 kHz) selected as the system clock.
**4.** This applies when the $X_{COUT}$ drivability selection bit = "0" and the system clock stop bit at wait state = "1".

## A–D CONVERTER CHARACTERISTICS

($V_{CC}$ = $AV_{CC}$ = 5 V, $V_{SS}$ = $AV_{SS}$ = 0 V, Ta = –20 to 85 °C, $f(X_{IN})$ = 25 MHz (Note), unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| — | Resolution | $V_{REF}$ = $V_{CC}$ | | | 10 | Bits |
| — | Absolute accuracy | $V_{REF}$ = $V_{CC}$ | | | ± 3 | LSB |
| $R_{LADDER}$ | Ladder resistance | $V_{REF}$ = $V_{CC}$ | 10 | | 25 | kΩ |
| $t_{CONV}$ | Conversion time | | 9.44 | | | μs |
| $V_{REF}$ | Reference voltage | | 2 | | $V_{CC}$ | V |
| $V_{IA}$ | Analog input voltage | | 0 | | $V_{REF}$ | V |

**Note.** This applies when the main clock division selection bit = "0" and $f(f_2)$ = 12.5 MHz.

## TIMING REQUIREMENTS ($V_{CC}$ = 5 V ± 10%, $V_{SS}$ = 0 V, Ta = –20 to 85 °C, f($X_{IN}$) = 25 MHz, unless otherwise noted (Note))

**Notes 1.** This applies when the main clock division selection bit = "0" and f($f_2$) = 12.5 MHz.

**2.** Input signal's rise/fall time must be 100 ns or less, unless otherwise noted.

### External clock input

| Symbol | Parameter | Limits | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_c$ | External clock input cycle time (Note 3) | 40 | | ns |
| $t_{w(H)}$ | External clock input high-level pulse width (Note 4) | 15 | | ns |
| $t_{w(L)}$ | External clock input low-level pulse width (Note 4) | 15 | | ns |
| $t_r$ | External clock rise time | | 8 | ns |
| $t_f$ | External clock fall time | | 8 | ns |

**Notes 3.** When the main clock division selection bit = "1", the minimum value of tc = 80 ns.

**4.** When the main clock division selection bit = "1", values of $t_{w(H)}$ / tc and $t_{w(L)}$ / tc must be set to values from 0.45 through 0.55.

### Single-chip mode

| Symbol | Parameter | Limits | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{su(P0D–E)}$ | Port P0 input setup time | 60 | | ns |
| $t_{su(P1D–E)}$ | Port P1 input setup time | 60 | | ns |
| $t_{su(P2D-E)}$ | Port P2 input setup time | 60 | | ns |
| $t_{su(P3D–E)}$ | Port P3 input setup time | 60 | | ns |
| $t_{su(P4D–E)}$ | Port P4 input setup time | 60 | | ns |
| $t_{su(P5D–E)}$ | Port P5 input setup time | 60 | | ns |
| $t_{su(P6D–E)}$ | Port P6 input setup time | 60 | | ns |
| $t_{su(P7D–E)}$ | Port P7 input setup time | 60 | | ns |
| $t_{su(P8D–E)}$ | Port P8 input setup time | 60 | | ns |
| $t_{h(E–P0D)}$ | Port P0 input hold time | 0 | | ns |
| $t_{h(E–P1D)}$ | Port P1 input hold time | 0 | | ns |
| $t_{h(E–P2D)}$ | Port P2 input hold time | 0 | | ns |
| $t_{h(E–P3D)}$ | Port P3 input hold time | 0 | | ns |
| $t_{h(E–P4D)}$ | Port P4 input hold time | 0 | | ns |
| $t_{h(E–P5D)}$ | Port P5 input hold time | 0 | | ns |
| $t_{h(E–P6D)}$ | Port P6 input hold time | 0 | | ns |
| $t_{h(E–P7D)}$ | Port P7 input hold time | 0 | | ns |
| $t_{h(E–P8D)}$ | Port P8 input hold time | 0 | | ns |

### Memory expansion mode and microprocessor mode

| Symbol | Parameter | Limits | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{su(D–RDE)}$ | Data input setup time | 32 | | ns |
| $t_{su(RDY–\phi1)}$ | $\overline{RDY}$ input setup time | 55 | | ns |
| $t_{su(HOLD–\phi1)}$ | $\overline{HOLD}$ input setup time | 55 | | ns |
| $t_{h(RDE–D)}$ | Data input hold time | 0 | | ns |
| $t_{h(\phi1–RDY)}$ | $\overline{RDY}$ input hold time | 0 | | ns |
| $t_{h(\phi1–HOLD)}$ | $\overline{HOLD}$ input hold time | 0 | | ns |

### Timer A input (Count input in event counter mode)

| Symbol | parameter | Limits | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN input cycle time | 80 | | ns |
| $t_{w(TAH)}$ | TAiIN input high-level pulse width | 40 | | ns |
| $t_{w(TAL)}$ | TAiIN input low-level pulse width | 40 | | ns |

### Timer A input (Gating input in timer mode)

| Symbol | parameter | Limits | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN input cycle time (Note) | 320 | | ns |
| $t_{w(TAH)}$ | TAiIN input high-level pulse width (Note) | 160 | | ns |
| $t_{w(TAL)}$ | TAiIN input low-level pulse width (Note) | 160 | | ns |

**Note.** Limits change depending on f(XIN). Refer to “DATA FORMULAS”.

### Timer A input (External trigger input in one-shot pulse mode)

| Symbol | parameter | Limits | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN input cycle time (Note) | 320 | | ns |
| $t_{w(TAH)}$ | TAiIN input high-level pulse width | 80 | | ns |
| $t_{w(TAL)}$ | TAiIN input low-level pulse width | 80 | | ns |

**Note.** Limits change depending on f(XIN). Refer to “DATA FORMULAS”.

### Timer A input (External trigger input in pulse width modulation mode)

| Symbol | parameter | Limits | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{w(TAH)}$ | TAiIN input high-level pulse width | 80 | | ns |
| $t_{w(TAL)}$ | TAiIN input low-level pulse width | 80 | | ns |

### Timer A input (Up-down input in event counter mode)

| Symbol | parameter | Limits | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(UP)}$ | TAiOUT input cycle time | 2000 | | ns |
| $t_{w(UPH)}$ | TAiOUT input high-level pulse width | 1000 | | ns |
| $t_{w(UPL)}$ | TAiOUT input low-level pulse width | 1000 | | ns |
| $t_{su(UP-TIN)}$ | TAiOUT input setup time | 400 | | ns |
| $t_{h(TIN-UP)}$ | TAiOUT input hold time | 400 | | ns |

### Timer A input (Two-phase pulse input in event counter mode)

| Symbol | parameter | Limits | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAjIN input cycle time | 800 | | ns |
| $t_{su(TAjIN-TAjOUT)}$ | TAjIN input setup time | 200 | | ns |
| $t_{su(TAjOUT-TAjIN)}$ | TAjOUT input setup time | 200 | | ns |

### Timer B input (Count input in event counter mode)

| Symbol | Parameter | Limits | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN input cycle time (one edge count) | 80 | | ns |
| $t_{w(TBH)}$ | TBiIN input high-level pulse width (one edge count) | 40 | | ns |
| $t_{w(TBL)}$ | TBiIN input low-level pulse width (one edge count) | 40 | | ns |
| $t_{c(TB)}$ | TBiIN input cycle time (both edges count) | 160 | | ns |
| $t_{w(TBH)}$ | TBiIN input high-level pulse width (both edges count) | 80 | | ns |
| $t_{w(TBL)}$ | TBiIN input low-level pulse width (both edges count) | 80 | | ns |

### Timer B input (Pulse period measurement mode)

| Symbol | Parameter | Limits | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN input cycle time (Note) | 320 | | ns |
| $t_{w(TBH)}$ | TBiIN input high-level pulse width (Note) | 160 | | ns |
| $t_{w(TBL)}$ | TBiIN input low-level pulse width (Note) | 160 | | ns |

**Note.** Limits change depending on f(XIN). Refer to “DATA FORMULAS”.

### Timer B input (Pulse width measurement mode)

| Symbol | Parameter | Limits | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN input cycle time (Note) | 320 | | ns |
| $t_{w(TBH)}$ | TBiIN input high-level pulse width (Note) | 160 | | ns |
| $t_{w(TBL)}$ | TBiIN input low-level pulse width (Note) | 160 | | ns |

**Note.** Limits change depending on f(XIN). Refer to “DATA FORMULAS”.

### A-D trigger input

| Symbol | Parameter | Limits | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(AD)}$ | $\overline{\text{ADTRG}}$ input cycle time (minimum allowable trigger) | 1000 | | ns |
| $t_{w(ADL)}$ | $\overline{\text{ADTRG}}$ input low-level pulse width | 125 | | ns |

### Serial I/O

| Symbol | Parameter | Limits | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi input cycle time | 200 | | ns |
| $t_{w(CKH)}$ | CLKi input high-level pulse width | 100 | | ns |
| $t_{w(CKL)}$ | CLKi input low-level pulse width | 100 | | ns |
| $t_{d(C-Q)}$ | TxDi output delay time | | 80 | ns |
| $t_{h(C-Q)}$ | TxDi hold time | 0 | | ns |
| $t_{su(D-C)}$ | RxDi input setup time | 30 | | ns |
| $t_{h(C-D)}$ | RxDi input hold time | 90 | | ns |

### External interrupt $\overline{\text{INT}}$i input, key input interrupt $\overline{\text{KI}}$i input

| Symbol | Parameter | Limits | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{w(INH)}$ | $\overline{\text{INT}}$i input high-level pulse width | 250 | | ns |
| $t_{w(INL)}$ | $\overline{\text{INT}}$i input low-level pulse width | 250 | | ns |
| $t_{w(KIL)}$ | $\overline{\text{KI}}$i input low-level pulse width | 250 | | ns |

## DATA FORMULAS

### Timer A input (Gating input in timer mode)

| Symbol | Parameter | Limits | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN input cycle time | $\frac{8 \times 10^9}{2 \cdot f(f_2)}$ | | ns |
| $t_{w(TAH)}$ | TAiIN input high-level pulse width | $\frac{4 \times 10^9}{2 \cdot f(f_2)}$ | | ns |
| $t_{w(TAL)}$ | TAiIN input low-level pulse width | $\frac{4 \times 10^9}{2 \cdot f(f_2)}$ | | ns |

### Timer A input (External trigger input in one-shot pulse mode)

| Symbol | Parameter | Limits | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN input cycle time | $\frac{8 \times 10^9}{2 \cdot f(f_2)}$ | | ns |

### Timer B input (In pulse period measurement mode or pulse width measurement mode)

| Symbol | Parameter | Limits | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN input cycle time | $\frac{8 \times 10^9}{2 \cdot f(f_2)}$ | | ns |
| $t_{w(TBH)}$ | TBiIN input high-level pulse width | $\frac{4 \times 10^9}{2 \cdot f(f_2)}$ | | ns |
| $t_{w(TBL)}$ | TBiIN input low-level pulse width | $\frac{4 \times 10^9}{2 \cdot f(f_2)}$ | | ns |

**Note.** $f(f_2)$ represents the clock $f_2$ frequency.
For the relation to the main clock and sub clock, refer to Table 10 in data sheet “M37735MHBXXXFP”.

## SWITCHING CHARACTERISTICS ($V_{CC}$ = 5 V ± 10%, $V_{SS}$ = 0 V, Ta = –20 to 85°C, f($X_{IN}$) = 25 MHz (Note), unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| $t_{d(E-P0Q)}$ | Port P0 data output delay time | Fig. 6 | | 80 | ns |
| $t_{d(E-P1Q)}$ | Port P1 data output delay time | | | 80 | ns |
| $t_{d(E-P2Q)}$ | Port P2 data output delay time | | | 80 | ns |
| $t_{d(E-P3Q)}$ | Port P3 data output delay time | | | 80 | ns |
| $t_{d(E-P4Q)}$ | Port P4 data output delay time | | | 80 | ns |
| $t_{d(E-P5Q)}$ | Port P5 data output delay time | | | 80 | ns |
| $t_{d(E-P6Q)}$ | Port P6 data output delay time | | | 80 | ns |
| $t_{d(E-P7Q)}$ | Port P7 data output delay time | | | 80 | ns |
| $t_{d(E-P8Q)}$ | Port P8 data output delay time | | | 80 | ns |

**Note.** This applies when the main clock division selection bit = “0” and f($f_2$) = 12.5 MHz.

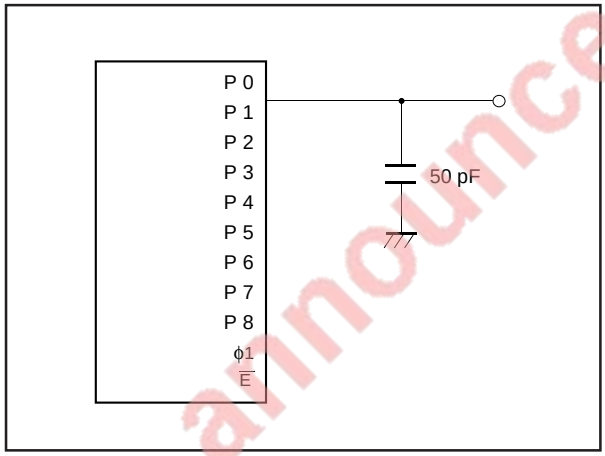



Fig. 6 Measuring circuit for ports P0 – P8 and $\phi_1$

## Memory expansion mode and microprocessor mode

($V_{CC}$ = 5 V ± 10%, $V_{SS}$ = 0 V, Ta = 25 °C, f($X_{IN}$) = 25 MHz (Note 1), unless otherwise noted)

| Symbol | Parameter | (Note 2) Wait mode | Test conditions | Limits Min. | Limits Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(CS-WE)}$ $t_{d(CS-RDE)}$ | Chip-select output delay time | No wait<br>Wait 1 | Fig. 6 | 12 | | ns |
| | | Wait 0 | | 87 | | ns |
| $t_{h(WE-CS)}$ $t_{h(RDE-CS)}$ | Chip-select hold time | | | 4 | | ns |
| $t_{d(An-WE)}$ $t_{d(An-RDE)}$ | Address output delay time | No wait<br>Wait 1 | | 12 | | ns |
| | | Wait 0 | | 87 | | ns |
| $t_{d(A-WE)}$ $t_{d(A-RDE)}$ | Address output delay time | No wait<br>Wait 1 | | 12 | | ns |
| | | Wait 0 | | 75 | | ns |
| $t_{h(WE-An)}$ $t_{h(RDE-An)}$ | Address hold time | | | 18 | | ns |
| $t_{w(ALE)}$ | ALE pulse width | No wait<br>Wait 1 | | 22 | | ns |
| | | Wait 0 | | 57 | | ns |
| $t_{su(A-ALE)}$ | Address output set up time | No wait<br>Wait 1 | | 5 | | ns |
| | | Wait 0 | | 45 | | ns |
| $t_{h(ALE-A)}$ | Address hold time | No wait<br>Wait 1 | | 9 | | ns |
| | | Wait 0 | | 15 | | ns |
| $t_{d(ALE-WE)}$ $t_{d(ALE-RDE)}$ | ALE output delay time | No wait<br>Wait 1 | | 4 | | ns |
| | | Wait 0 | | 10 | | ns |
| $t_{d(WE-DQ)}$ | Data output delay time | | | | 45 | ns |
| $t_{h(WE-DQ)}$ | Data hold delay time | | | 18 | | ns |
| $t_{w(WE)}$ | $\overline{WEL}$/$\overline{WEH}$ pulse width | No wait | | 50 | | ns |
| | | Wait 1<br>Wait 0 | | 130 | | ns |
| $t_{pxz(RDE-DZ)}$ | Floating start delay time | | | | 5 | ns |
| $t_{pzx(RDE-DZ)}$ | Floating release delay time | | | 20 | | ns |
| $t_{w(RDE)}$ | $\overline{RDE}$ pulse width | No wait | | 48 | | ns |
| | | Wait 1<br>Wait 0 | | 128 | | ns |
| $t_{d(RSMP-WE)}$ $t_{d(RSMP-RDE)}$ | $\overline{RSMP}$ output delay time | | | 10 | | ns |
| $t_{h(\phi1-RSMP)}$ | $\overline{RSMP}$ hold time | | | 0 | | ns |
| $t_{d(WE-\phi1)}$ $t_{d(RDE-\phi1)}$ | $\phi_1$ output delay time | | | 0 | 18 | ns |
| $t_{d(\phi1-HLDA)}$ | $\overline{HLDA}$ output delay time | | | | 50 | ns |

**Notes 1.** This applies when the main clock division selection bit = “0” and f($f_2$) = 12.5 MHz.

**2.** No wait : Wait bit = “1”.
Wait 1 : The external memory area is accessed with wait bit = “0” and wait selection bit = “1”.
Wait 0 : The external memory area is accessed with wait bit = “0” and wait selection bit = “0”.

## Memory expansion mode and microprocessor mode

### Bus timing data formulas ($V_{CC}$ = 5 V ± 10%, $V_{SS}$ = 0 V, Ta = –20 to 85 °C, f($X_{IN}$) = 25 MHz (Max., Note1), unless otherwise noted)

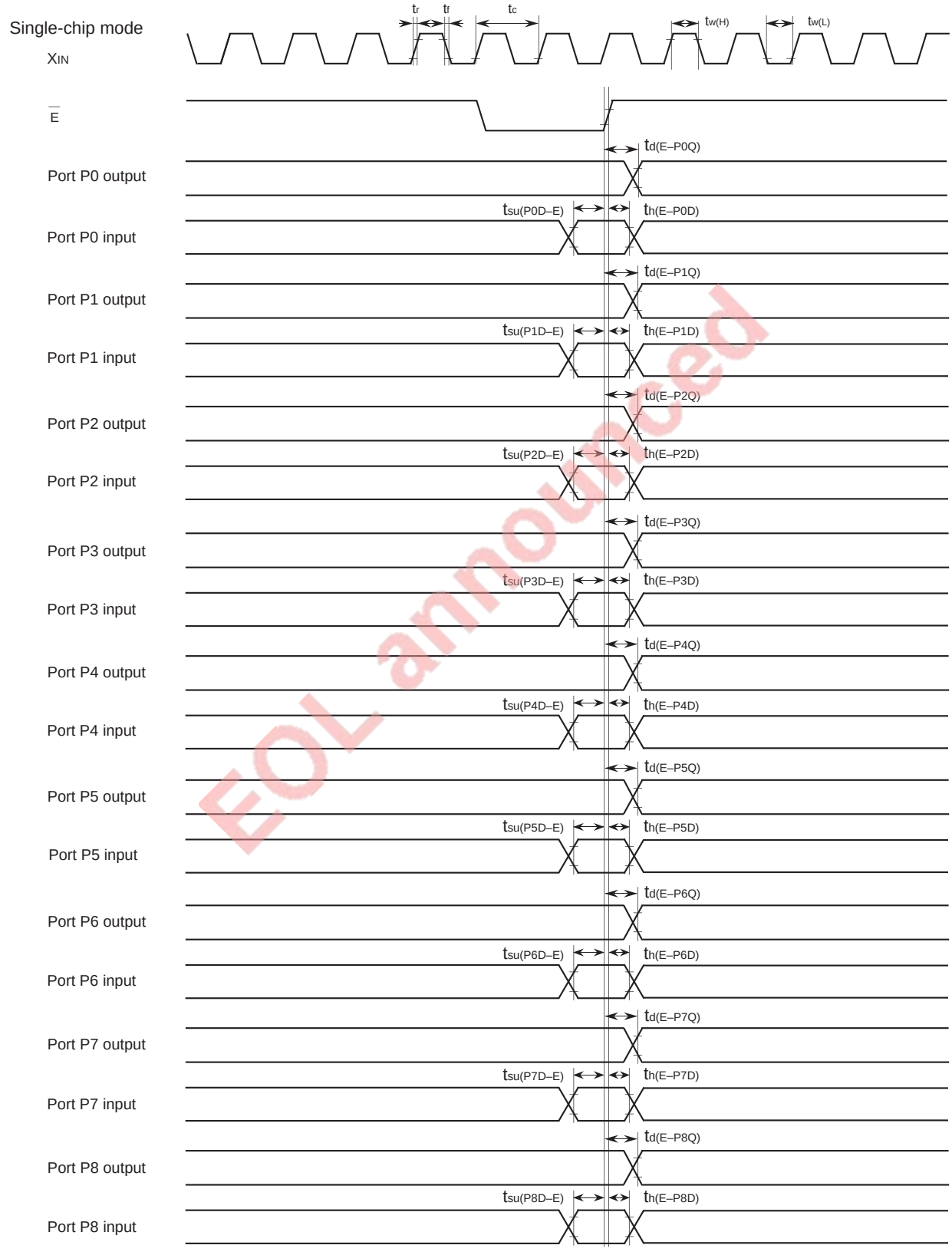
| Symbol | Parameter | Wait mode | Limits Min. | Limits Max. | Unit |
|---|---|---|---|---|---|
| $t_{d(CS–WE)}$ $t_{d(CS–RDE)}$ | Chip-select output delay time | No wait Wait 1 | $\frac{1 \times 10^9}{2 \cdot f(f_2)} - 28$ | | ns |
| | | Wait 0 | $\frac{3 \times 10^9}{2 \cdot f(f_2)} - 33$ | | ns |
| $t_{h(WE–CS)}$ $t_{h(RDE–CS)}$ | Chip-select hold time | | 4 | | ns |
| $t_{d(An–WE)}$ $t_{d(An–RDE)}$ | Address output delay time | No wait Wait 1 | $\frac{1 \times 10^9}{2 \cdot f(f_2)} - 28$ | | ns |
| | | Wait 0 | $\frac{3 \times 10^9}{2 \cdot f(f_2)} - 33$ | | ns |
| $t_{d(A–WE)}$ $t_{d(A–RDE)}$ | Address output delay time | No wait Wait 1 | $\frac{1 \times 10^9}{2 \cdot f(f_2)} - 28$ | | ns |
| | | Wait 0 | $\frac{3 \times 10^9}{2 \cdot f(f_2)} - 45$ | | ns |
| $t_{h(WE–An)}$ $t_{h(RDE–An)}$ | Address hold time | | $\frac{1 \times 10^9}{2 \cdot f(f_2)} - 22$ | | ns |
| $t_{w(ALE)}$ | ALE pulse width | No wait Wait 1 | $\frac{1 \times 10^9}{2 \cdot f(f_2)} - 18$ | | ns |
| | | Wait 0 | $\frac{2 \times 10^9}{2 \cdot f(f_2)} - 23$ | | ns |
| $t_{su(A–ALE)}$ | Address output set up time | No wait Wait 1 | $\frac{1 \times 10^9}{2 \cdot f(f_2)} - 35$ | | ns |
| | | Wait 0 | $\frac{2 \times 10^9}{2 \cdot f(f_2)} - 35$ | | ns |
| $t_{h(ALE–A)}$ | Address hold time | No wait Wait 1 | 9 | | ns |
| | | Wait 0 | $\frac{1 \times 10^9}{2 \cdot f(f_2)} - 25$ | | ns |
| $t_{d(ALE–WE)}$ $t_{d(ALE–RDE)}$ | ALE output delay time | No wait Wait 1 | 4 | | ns |
| | | Wait 0 | $\frac{1 \times 10^9}{2 \cdot f(f_2)} - 30$ | | ns |
| $t_{d(WE–DQ)}$ | Data output delay time | | | 45 | ns |
| $t_{h(WE–DQ)}$ | Data hold time | | $\frac{1 \times 10^9}{2 \cdot f(f_2)} - 22$ | | ns |
| $t_{w(WE)}$ | $\overline{WEL}$/$\overline{WEH}$ pulse width | No wait | $\frac{2 \times 10^9}{2 \cdot f(f_2)} - 30$ | | ns |
| | | Wait 1 Wait 0 | $\frac{4 \times 10^9}{2 \cdot f(f_2)} - 30$ | | ns |
| $t_{pxz(RDE–DZ)}$ | Floating start delay time | | | 5 | ns |
| $t_{pzx(RDE–DZ)}$ | Floating release delay time | | $\frac{1 \times 10^9}{2 \cdot f(f_2)} - 20$ | | ns |
| $t_{w(RDE)}$ | $\overline{RDE}$ pulse width | No wait | $\frac{2 \times 10^9}{2 \cdot f(f_2)} - 32$ | | ns |
| | | Wait 1 Wait 0 | $\frac{4 \times 10^9}{2 \cdot f(f_2)} - 32$ | | ns |
| $t_{d(RSMP–WE)}$ $t_{d(RSMP–RDE)}$ | $\overline{RSMP}$ output delay time | | $\frac{1 \times 10^9}{2 \cdot f(f_2)} - 30$ | | ns |
| $t_{h(\phi1–RSMP)}$ | $\overline{RSMP}$ hold time | | 0 | | ns |
| $t_{d(WE–\phi1)}$ $t_{d(RDE–\phi1)}$ | $\phi_1$ output delay time | | 0 | 18 | ns |

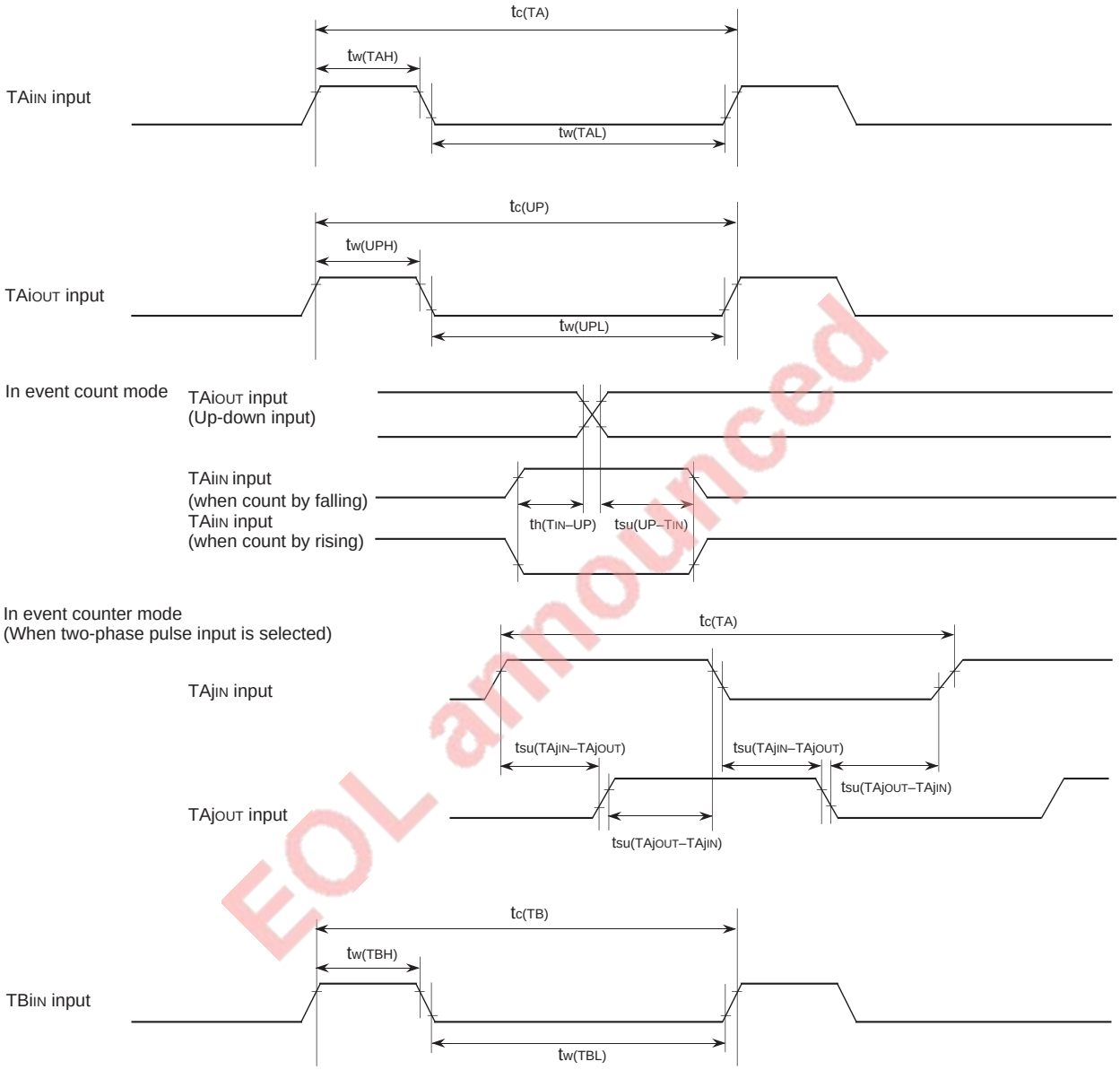
**Notes 1.** This applies when the main-clock division selection bit = “0”.

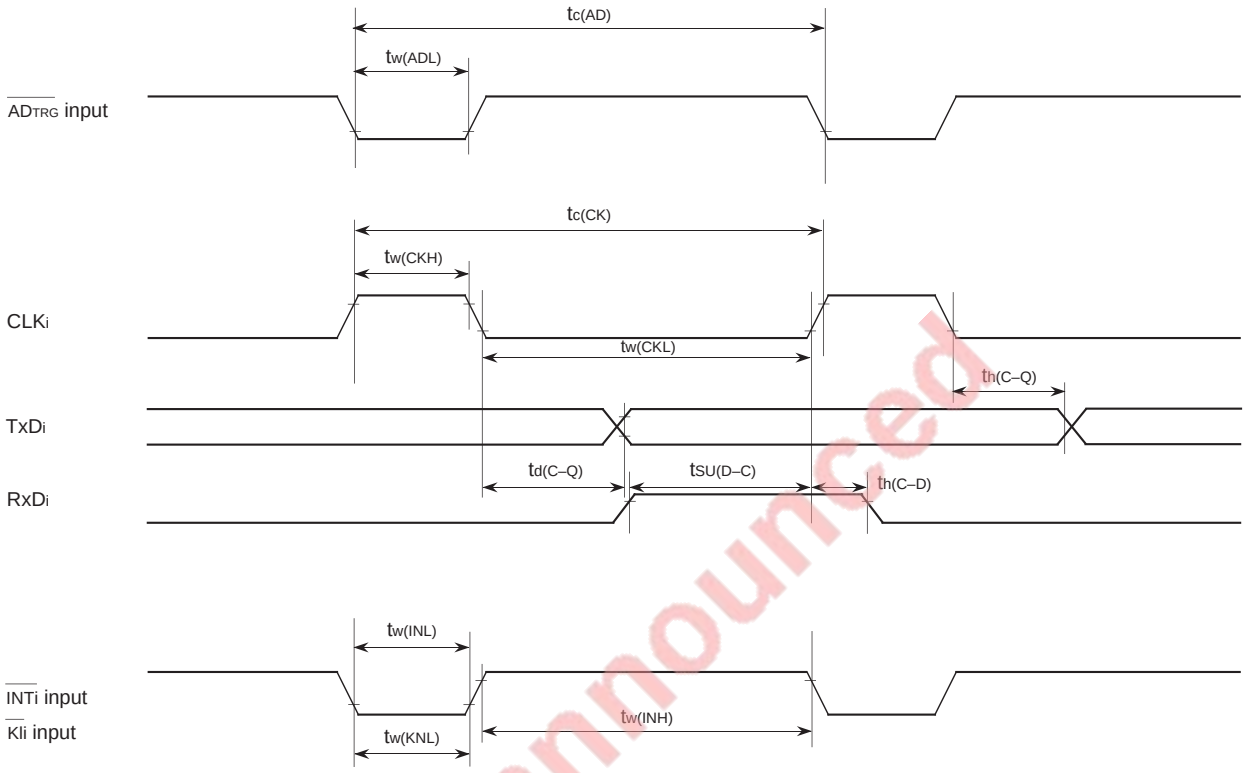
**2.** f($f_2$) represents the clock $f_2$ frequency.
For the relation to the main clock and sub clock, refer to Table 10 in data sheet “M37735MHBXXXFP”.

## TIMING DIAGRAM

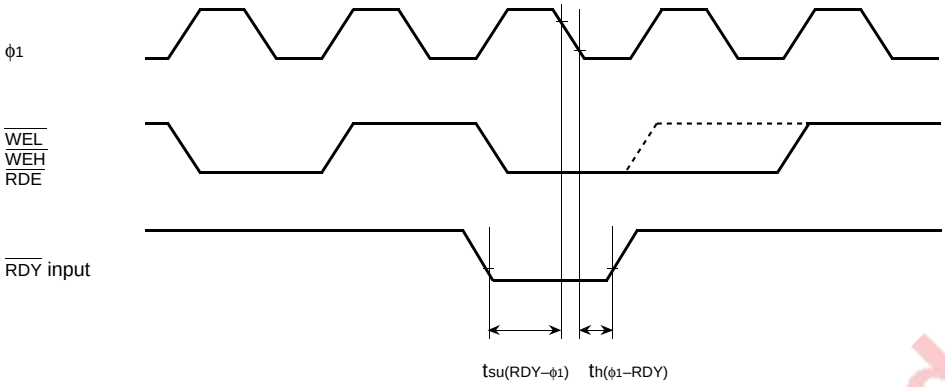
Single-chip mode



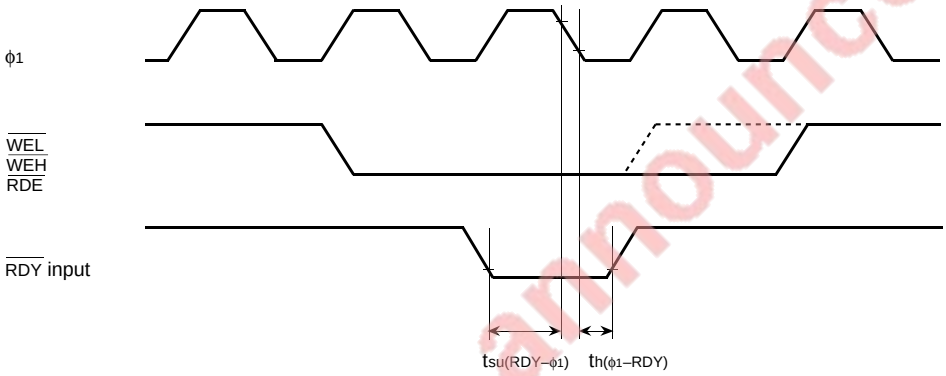




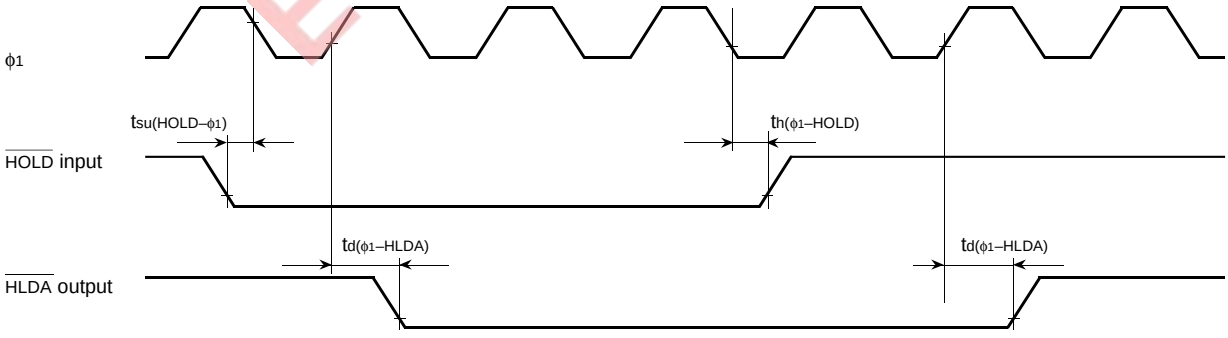
Memory expansion mode and microprocessor mode
(When wait bit = "1")




( When wait bit = "0")

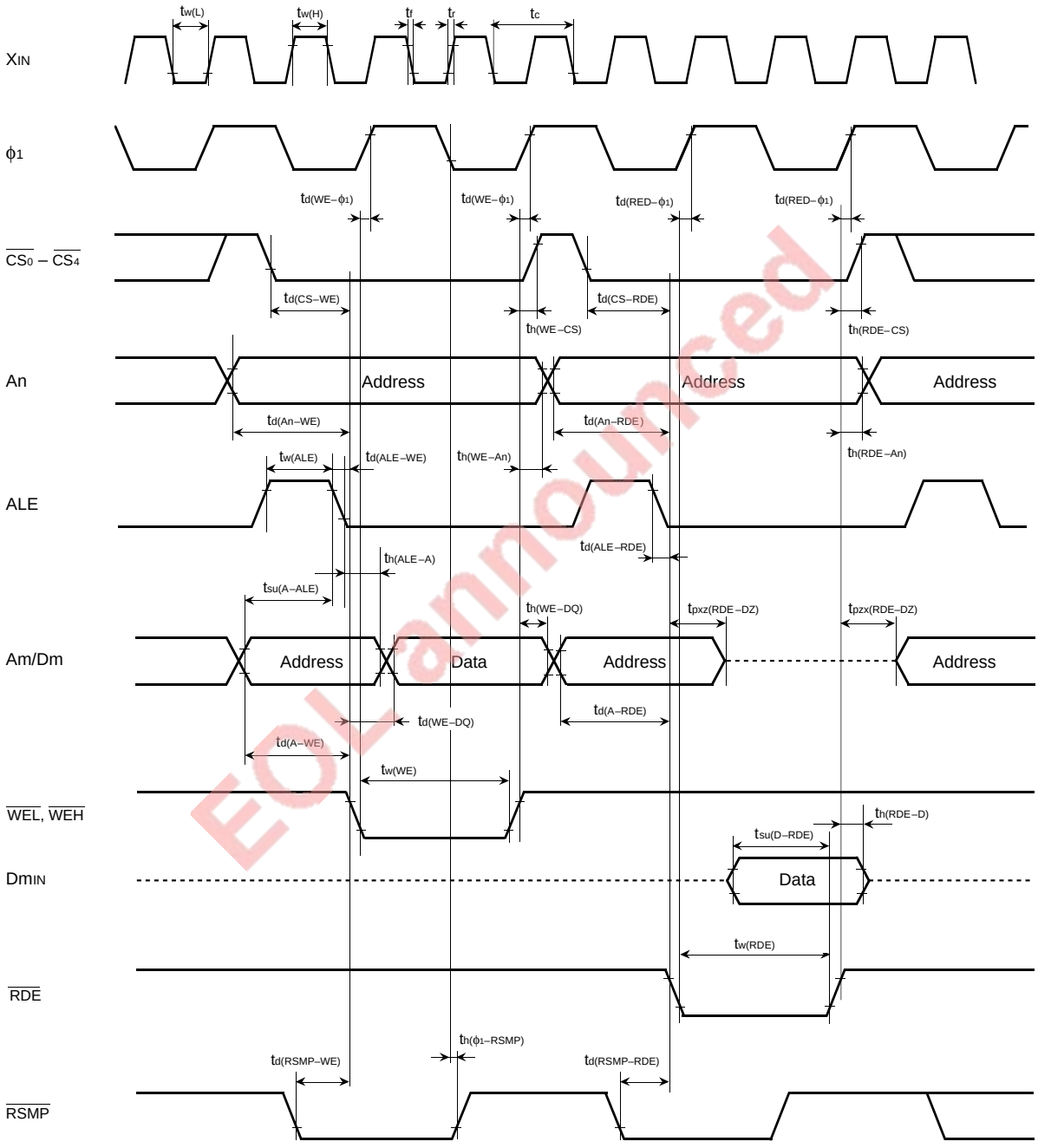



(When wait bit = "1" or "0" in common)



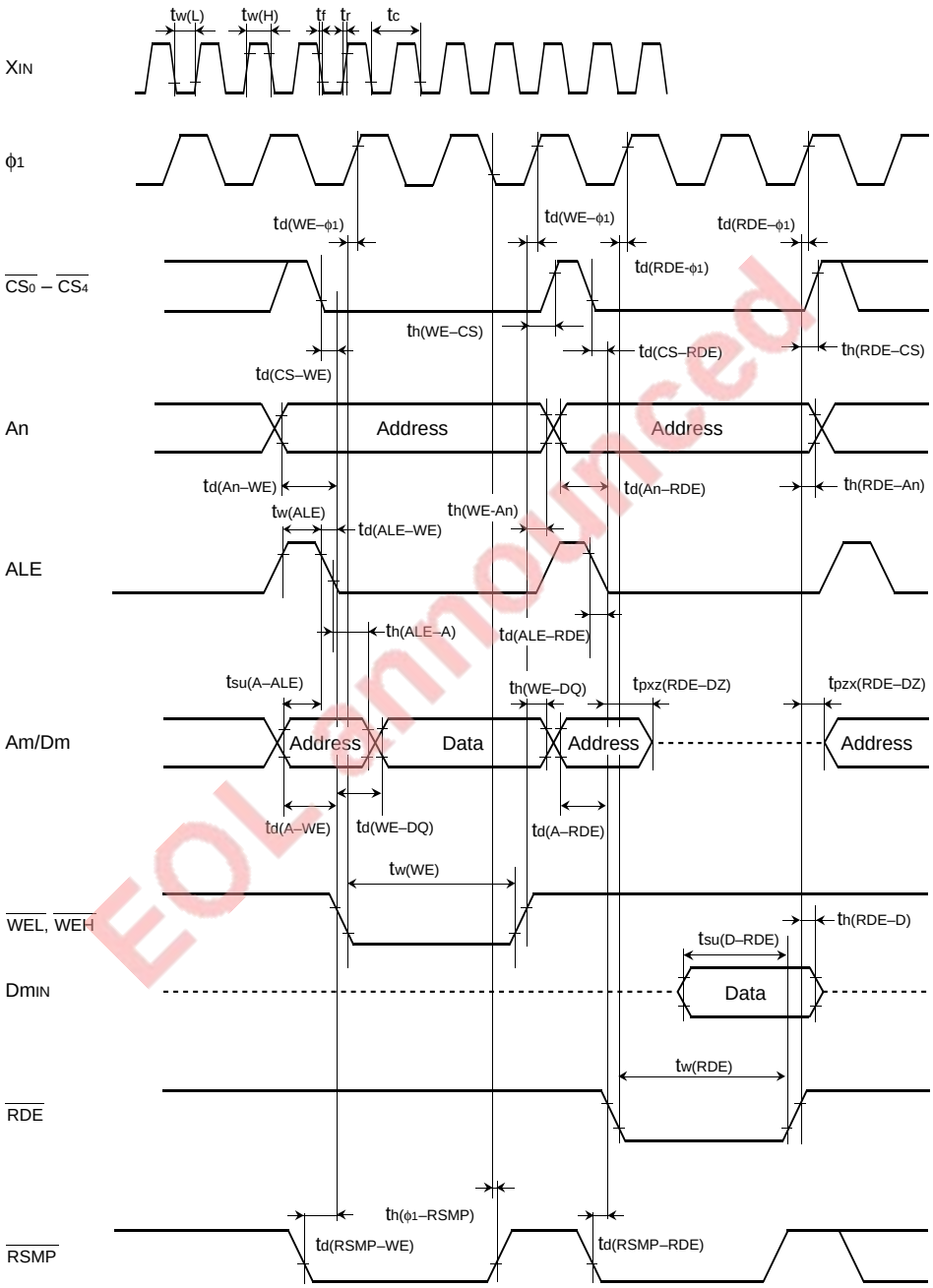

Test conditions
- $V_{CC}$ = 5 V ± 10%
- Input timing voltage : $V_{IL}$ = 1.0 V, $V_{IH}$ = 4.0 V
- Output timing voltage : $V_{OL}$ = 0.8 V, $V_{OH}$ = 2.0 V

Memory expansion mode and microprocessor mode
(No wait : When wait bit = "1")



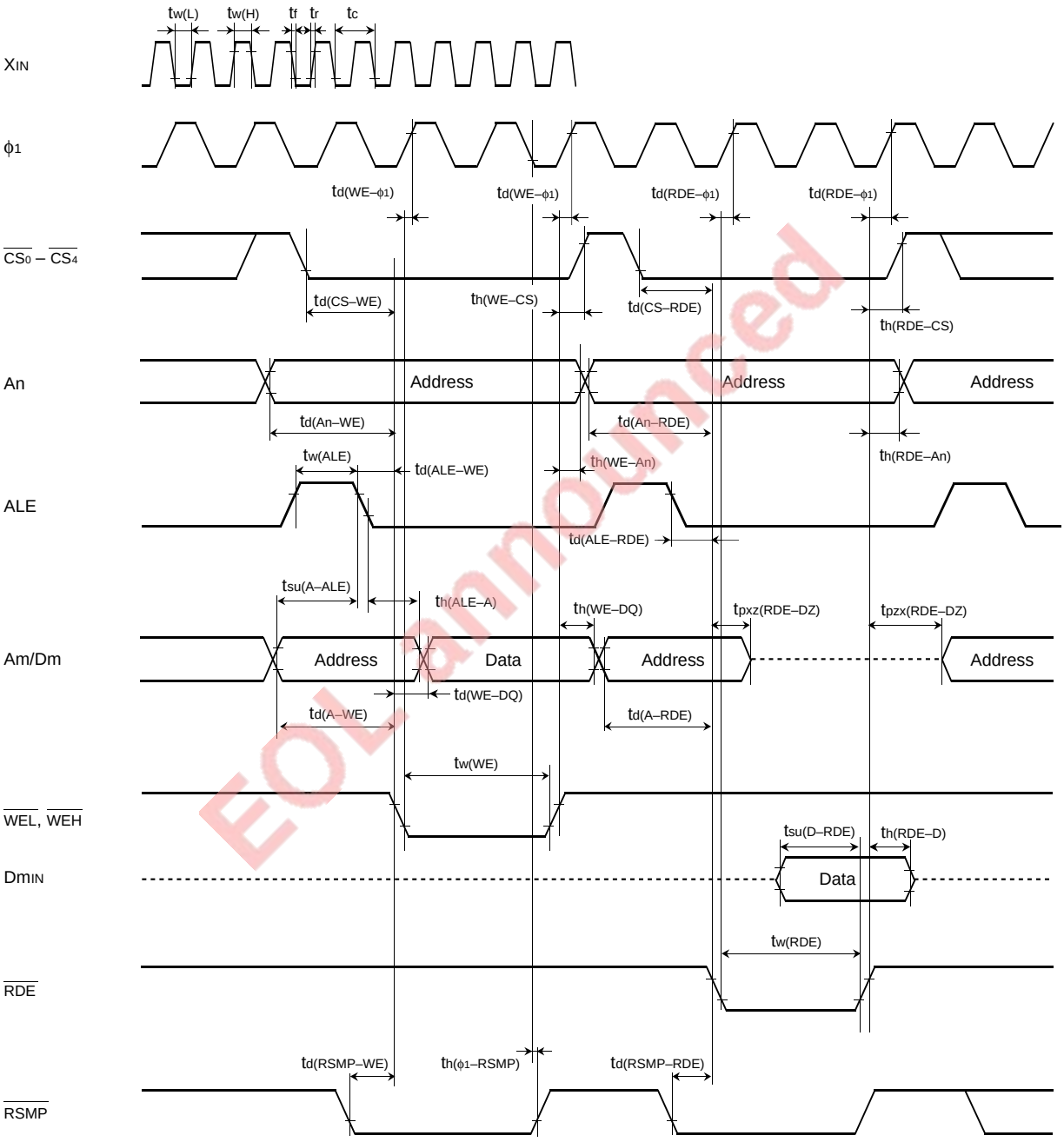

Test condition
- Vcc = 5 V ± 10%
- Output timing voltage : $V_{IL}$ = 0.8 V, $V_{IH}$ = 2.0 V
- Data input $Dm_{IN}$ : $V_{IL}$ = 0.8 V, $V_{IH}$ = 2.5 V

Memory expansion mode and microprocessor mode
(Wait 1 : The external area is accessed when wait bit = “0” and wait selection bit = “1”.)




Test condition
- Vcc = 5 V ± 10%
- Output timing voltage : VOL = 0.8 V, VOH = 2.0 V
- Data input DmIN : VIL = 0.8 V, VIH = 2.5 V

Memory expansion mode and microprocessor mode
(Wait 0 : The external memory area is accessed when wait bit = “0” and wait selection bit = “0”.)





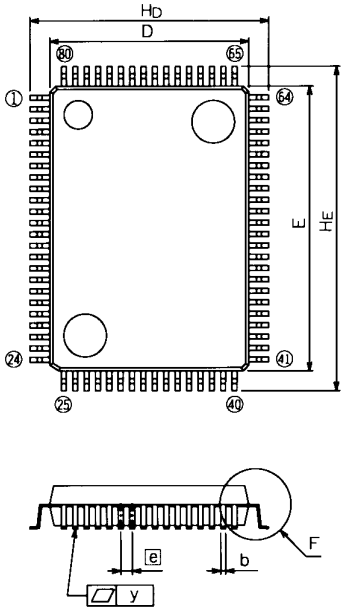

Test conditions
- Vcc = 5 V ± 10%
- Output timing voltage : VOL = 0.8 V, VOH = 2.0 V
- Data input DmIN : VIL = 0.8 V, VIH = 2.5 V

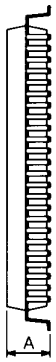
## PACKAGE OUTLINE

80P6N−A — Plastic 80pin 14×20mm body QFP

| EIAJ Package Code | JEDEC Code | Weight(g) | Lead Material |
|---|---|---|---|
| QFP80-P-1420-0.80 | – | 1.58 | Alloy 42 |

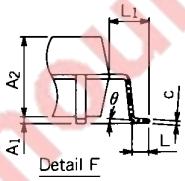
Scale :

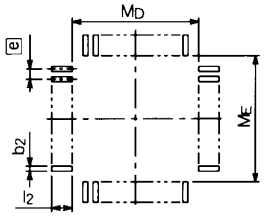









Recommended Mount Pad

| Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| A | – | – | 3.05 |
| $A_1$ | 0 | 0.1 | 0.2 |
| $A_2$ | – | 2.8 | – |
| b | 0.3 | 0.35 | 0.45 |
| c | 0.13 | 0.15 | 0.2 |
| D | 13.8 | 14.0 | 14.2 |
| E | 19.8 | 20.0 | 20.2 |
| e | – | 0.8 | – |
| $H_D$ | 16.5 | 16.8 | 17.1 |
| $H_E$ | 22.5 | 22.8 | 23.1 |
| L | 0.4 | 0.6 | 0.8 |
| $L_1$ | – | 1.4 | – |
| y | – | – | 0.1 |
| θ | 0° | – | 10° |
| $b_2$ | – | 0.5 | – |
| $l_2$ | 1.3 | – | – |
| $M_D$ | – | 14.6 | – |
| $M_E$ | – | 20.6 | – |

GZZ–SH00–78B<84A0>

| Mask ROM number | |
|---|---|

# 7700 FAMILY MASK ROM ORDER CONFIRMATION FORM
# SINGLE-CHIP 16-BIT MICROCOMPUTER
# M37735M4BXXXFP
# MITSUBISHI ELECTRIC

| Receipt | Date: | |
|---|---|---|
| | Section head signature | Supervisor signature |
| | | |

Note : Please fill in all items marked ※

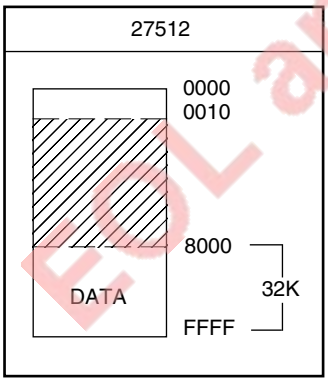
| ※ | | | | | | |
|---|---|---|---|---|---|---|
| Customer | Company name | TEL ( ) | Issuance signatures | Responsible officer | Supervisor |
| | Date issued | Date: | | | |

※1. Confirmation

Specify the name of the product being ordered.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based on this data.
We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data.
Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM areas [ ][ ][ ][ ] (hexadecimal notation)

EPROM Type :




(1) Set "FF16" in the shaded area.
(2) Address 016 to 1016 are the area for storing the data on model designation and options.This area must be written with the data shown below.
Details for option data are given next in the section describing the STP instruction option.
Address and data are written in hexadecimal notation.

| | Address | | Address | | Address |
|---|---|---|---|---|---|
| 4D | 0 | 42 | 8 | Option data | 10 |
| 33 | 1 | FF | 9 | | |
| 37 | 2 | FF | A | | |
| 37 | 3 | FF | B | | |
| 33 | 4 | FF | C | | |
| 35 | 5 | FF | D | | |
| 4D | 6 | FF | E | | |
| 34 | 7 | FF | F | | |

※2. STP instruction option

One of the following sets of data should be written to the option data address (1016) of the EPROM you have ordered.
Check @ in the appropriate box.

☐ STP instruction enable 0116 Address 1016
☐ STP instruction disable 0016 Address 1016

※3. Mark specification

Mark specification must be submitted using the correct form for the type of package being ordered fill out the appropriate 80P6N Mark Specification Form (for M37735M4BXXXFP) and attach to the Mask ROM Order Confirmation Form.

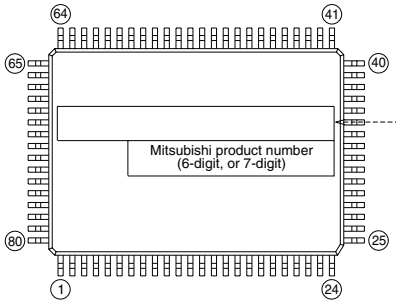
※4. Comments

# 80P6N (80-PIN QFP) MARK SPECIFICATION FORM

Mitsubishi IC catalog name

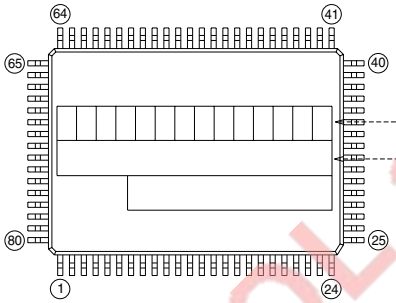
Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark




Mitsubishi IC catalog name

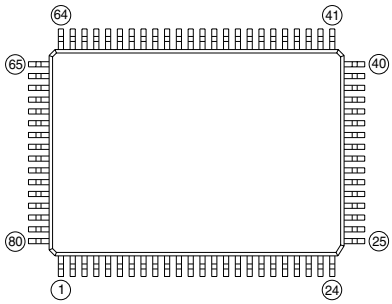
B. Customer's Parts Number + Mitsubishi IC Catalog Name




Customer's Parts Number
Note : The fonts and size of characters are standard Mitsubishi type.
Mitsubishi IC catalog name
Notes 1 : The mark field should be written right aligned.
2 : The fonts and size of characters are standard Mitsubishi type.
3 : Customer's parts number can be up to 14 alphanumeric characters for capital letters, hyphens, commas, periods and so on.



C. Special Mark Required




Notes1 : If special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated technically as close as possible.
Mitsubishi product number (6-digit, or 7-digit) and Mask ROM number (3-digit) are always marked for sorting the products.
2 : If special character fonts (e,g., customer's trade mark logo) must be used in Special Mark, check the box below.
For the new special character fonts, a clean font original (ideally logo drawing) must be submitted.

Special character fonts required

☐

MITSUBISHI MICROCOMPUTERS

# M37735M4BXXXFP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER



Renesas Technology Corp.
Nippon Bldg.,6-2,Otemachi 2-chome,Chiyoda-ku,Tokyo,100-0004 Japan


H-LF481-A KI-9703 Printed in Japan (ROD) II
New publication, effective Mar. 1997.
Specifications subject to change without notice.

RENESAS
Renesas Technology Corp.

| REVISION DESCRIPTION LIST | M37735M4BXXXFP DATA SHEET |
|---|---|

| Rev. No. | Revision Description | Rev. date |
|---|---|---|
| 1.0 | First Edition | 970604 |
| 1.01 | The following are added:<br>•MASK ROM ORDER CONFIRMATION FORM<br>•MARK SPECIFICATION FORM | 980526 |