

To our customers,

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

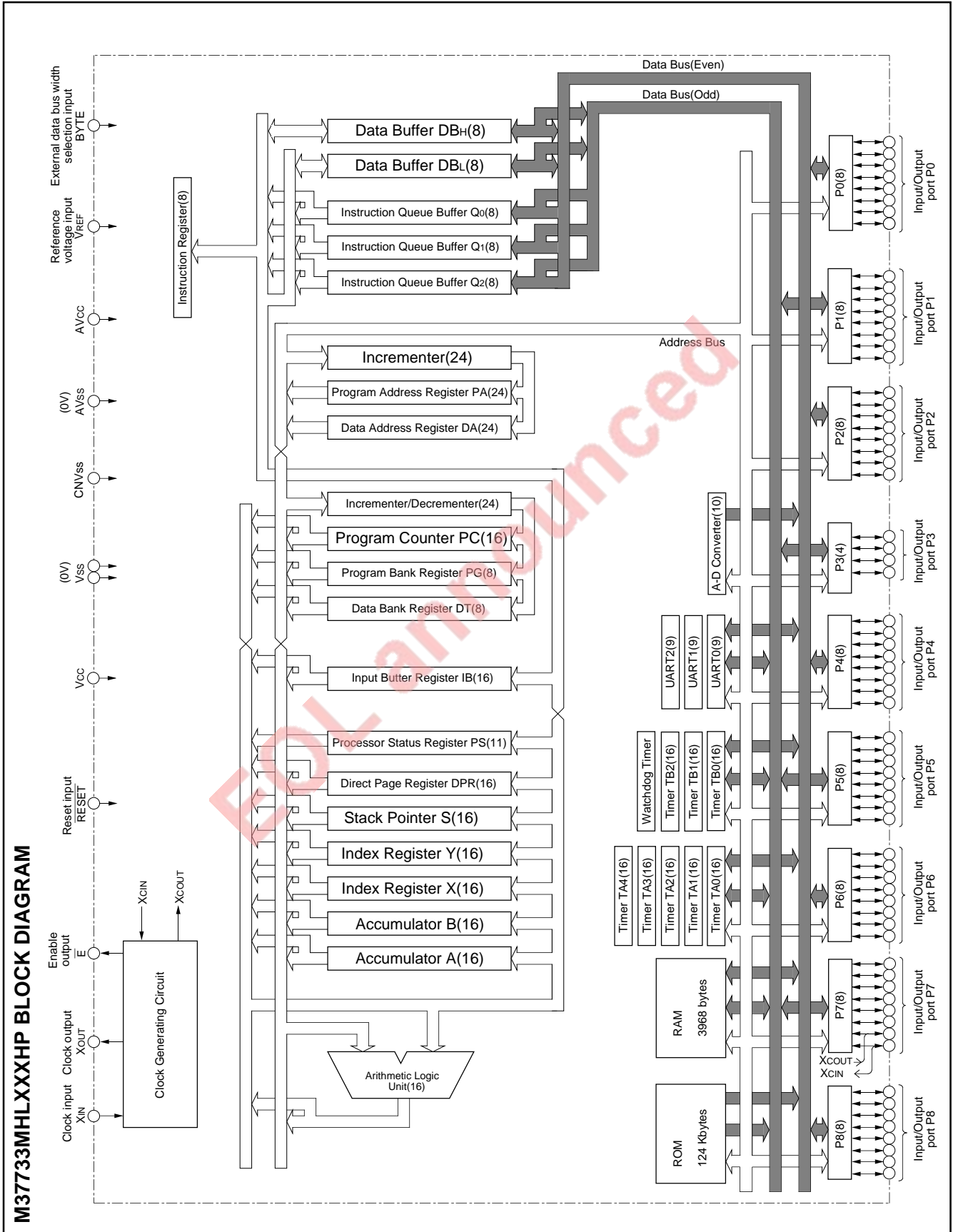
Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

MITSUBISHI MICROCOMPUTERS
M37733MHLXXXHP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER



FUNCTIONS OF M37733MHLXXXHP

Parameter		Functions
Number of basic instructions		103
Instruction execution time		333 ns (the fastest instruction at external clock 12 MHz frequency)
Memory size	ROM	124 Kbytes
	RAM	3968 bytes
Input/Output ports	P0 – P2, P4 – P8	8-bit X 8
	P3	4-bit X 1
Multi-function timers	TA0, TA1, TA2, TA3, TA4	16-bit X 5
	TB0, TB1, TB2	16-bit X 3
Serial I/O		(UART or clock synchronous serial I/O) X 3
A-D converter		10-bit X 1 (8 channels)
Watchdog timer		12-bit X 1
Interrupts		3 external types, 16 internal types Each interrupt can be set to the priority level (0 – 7.)
Clock generating circuit		2 circuits built-in (externally connected to a ceramic resonator or a quartz-crystal oscillator)
Supply voltage		2.7 – 5.5 V
Power dissipation		9 mW (at 3 V supply voltage, external clock 12 MHz frequency) 22.5 mW (at 5 V supply voltage, external clock 12 MHz frequency)
Input/Output characteristic	Input/Output voltage	5 V
	Output current	5 mA
Memory expansion		Maximum 16 Mbytes
Operating temperature range		–40 to 85 °C
Device structure		CMOS high-performance silicon gate process
Package		80-pin plastic molded fine-pitch QFP (80P6D-A;0.5 mm lead pitch)

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PIN DESCRIPTION

Pin	Name	Input/Output	Functions
Vcc, Vss	Power source		Apply 2.7 – 5.5 V to Vcc and 0 V to Vss.
CNVss	CNVss input	Input	This pin controls the processor mode. Connect to Vss for the single-chip mode and the memory expansion mode, and to Vcc for the microprocessor mode.
RESET	Reset input	Input	When "L" level is applied to this pin, the microcomputer enters the reset state.
XIN	Clock input	Input	These are pins of main-clock generating circuit. Connect a ceramic resonator or a quartz-crystal oscillator between XIN and XOUT. When an external clock is used, the clock source should be connected to the XIN pin, and the XOUT pin should be left open.
XOUT	Clock output	Output	
E	Enable output	Output	This pin functions as the enable signal output pin which indicates the access status in the internal bus. When output level of E signal is "L", data/instruction read or data write is performed.
BYTE	External data bus width selection input	Input	In the memory expansion mode or the microprocessor mode, this pin determines whether the external data bus has an 8-bit width or a 16-bit width. The data bus has a 16-bit width when "L" signal is input and an 8-bit width when "H" signal is input.
AVcc, AVss	Analog power source input		Power source input pin for the A-D converter. Externally connect AVcc to Vcc and AVss to Vss.
VREF	Reference voltage input	Input	This is reference voltage input pin for the A-D converter.
P00 – P07	I/O port P0	I/O	In the single-chip mode, port P0 becomes an 8-bit I/O port. An I/O direction register is available so that each pin can be programmed for input or output. These ports are in the input mode when reset. In the memory expansion mode or the microprocessor mode, these pins output address (A0 – A7).
P10 – P17	I/O port P1	I/O	In the single-chip mode, these pins have the same functions as port P0. When the BYTE pin is set to "L" in the memory expansion mode or the microprocessor mode and external data bus has a 16-bit width, high-order data (D8 – D15) is input/output or an address (A8 – A15) is output. When the BYTE pin is "H" and an external data bus has an 8-bit width, only address (A8 – A15) is output.
P20 – P27	I/O port P2	I/O	In the single-chip mode, these pins have the same functions as port P0. In the memory expansion mode or the microprocessor mode, low-order data (D0 – D7) is input/output or an address (A16 – A23) is output.
P30 – P33	I/O port P3	I/O	In the single-chip mode, these pins have the same function as port P0. In the memory expansion mode or the microprocessor mode, R/W, BHE, ALE, and HLDA signals are output.
P40 – P47	I/O port P4	I/O	In the single-chip mode, these pins have the same functions as port P0. In the memory expansion mode or the microprocessor mode, P40, P41, and P42 become HOLD and RDY input pins, and a clock ϕ_1 output pin, respectively. Functions of the other pins are the same as in the single-chip mode. However, in the memory expansion mode, P42 can be selected as an I/O port.
P50 – P57	I/O port P5	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for timers A0 to A3 and input pins for key input interrupt input ($\overline{KI}_0 - \overline{KI}_3$).
P60 – P67	I/O port P6	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for timer A4, input pins for external interrupt input ($\overline{INT}_0 - \overline{INT}_2$) and input pins for timers B0 to B2. P67 also functions as sub-clock ϕ_{SUB} output pin.
P70 – P77	I/O port P7	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins function as input pins for A-D converter. P72 to P75 also function as I/O pins for UART2. Additionally, P76 and P77 have the function as the output pin (Xcout) and the input pin (Xcin) of the sub-clock (32 kHz) oscillation circuit, respectively. When P76 and P77 are used as the Xcout and Xcin pins, connect a resonator or an oscillator between the both.
P80 – P87	I/O port P8	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for UART 0 and UART 1.

BASIC FUNCTION BLOCKS

The M37733MHLXXXHP has the same functions as the M37733MHBXXXFP except for the package and the reset circuit. Refer to the section on the M37733MHBXXXFP.

RESET CIRCUIT

The microcomputer is released from the reset state when the RESET pin is returned to "H" level after holding it at "L" level with the power source voltage at 2.7 – 5.5 V. Program execution starts at the address formed by setting address A₂₃ – A₁₆ to 001₆, A₁₅ – A₈ to the contents of address FFFF₁₆, and A₇ – A₀ to the contents of address FFFE₁₆. Figure 3 shows an example of a reset circuit. When the stabilized clock is input from the external to the main-clock oscillation circuit, the reset input voltage must be 0.55 V or less when the power source voltage reaches 2.7 V. When a resonator/oscillator is connected to the main-clock oscillation circuit, change the reset input voltage from "L" to "H" after the main-clock oscillation is fully stabilized.

The status of the internal registers during reset is the same as the M37733MHBXXXFP's.

ADDRESSING MODES

The M37733MHLXXXHP has 28 powerful addressing modes. Refer to the "7700 Family Software Manual" for the details.

MACHINE INSTRUCTION LIST

The M37733MHLXXXHP has 103 machine instructions. Refer to the "7700 Family Software Manual" for the details.

DATA REQUIRED FOR MASK ROM ORDERING

Please send the following data for mask orders.

- (1) M37733MHLXXXHP mask ROM order confirmation form
- (2) 80P6D, 80P6Q mark specification form
- (3) ROM data (EPROM 3 sets)

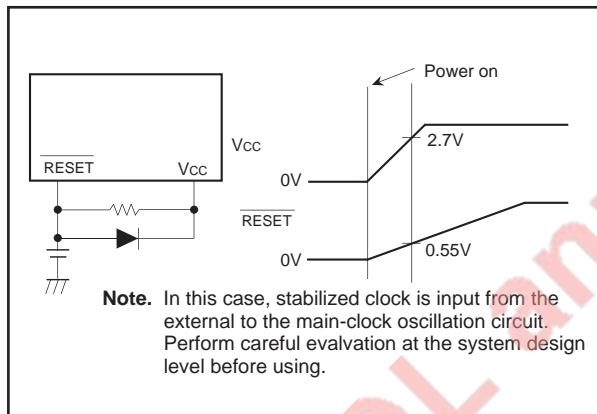


Fig. 1 Example of a reset circuit

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{cc}	Power source voltage		-0.3 to +7	V
AV _{cc}	Analog power source voltage		-0.3 to +7	V
V _i	Input voltage RESET, CNV _{ss} , BYTE		-0.3 to +12	V
V _i	Input voltage P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, V _{REF} , X _{IN}		-0.3 to V _{cc} + 0.3	V
V _o	Output voltage P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, X _{OUT} , E		-0.3 to V _{cc} + 0.3	V
P _d	Power dissipation	T _a = 25 °C	200	mW
T _{opr}	Operating temperature		-40 to +85	°C
T _{stg}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (V_{cc} = 5 V ± 10%, T_a = -40 to +85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit	
		Min.	Typ.	Max.		
V _{cc}	Power source voltage	f(X _{IN}) : Operating	2.7		5.5	V
		f(X _{IN}) : Stopped, f(X _{CIN}) = 32.768 kHz	2.7		5.5	
AV _{cc}	Analog power source voltage		V _{cc}		V	
V _{ss}	Power source voltage		0		V	
AV _{ss}	Analog power source voltage		0		V	
V _{IH}	High-level input voltage P00 – P07, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, X _{IN} , RESET, CNV _{ss} , BYTE, X _{CIN} (Note 3)	0.8 V _{cc}		V _{cc}	V	
V _{IH}	High-level input voltage P10 – P17, P20 – P27 (in single-chip mode)	0.8 V _{cc}		V _{cc}	V	
V _{IH}	High-level input voltage P10 – P17, P20 – P27 (in memory expansion mode and microprocessor mode)	0.5 V _{cc}		V _{cc}	V	
V _{IL}	Low-level input voltage P00 – P07, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, X _{IN} , RESET, CNV _{ss} , BYTE, X _{CIN} (Note 3)	0		0.2V _{cc}	V	
V _{IL}	Low-level input voltage P10 – P17, P20 – P27 (in single-chip mode)	0		0.2V _{cc}	V	
V _{IL}	Low-level input voltage P10 – P17, P20 – P27 (in memory expansion mode and microprocessor mode)	0		0.16V _{cc}	V	
I _{OH(peak)}	High-level peak output current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87			-10	mA	
I _{OH(avg)}	High-level average output current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87			-5	mA	
I _{OL(peak)}	Low-level peak output current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P43, P54 – P57, P60 – P67, P70 – P77, P80 – P87			10	mA	
I _{OL(peak)}	Low-level peak output current P44 – P47, P50 – P53			16	mA	
I _{OL(avg)}	Low-level average output current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P43, P54 – P57, P60 – P67, P70 – P77, P80 – P87			5	mA	
I _{OL(avg)}	Low-level average output current P44 – P47, P50 – P53			12	mA	
f(X _{IN})	Main-clock oscillation frequency (Note 4)			12	MHz	
f(X _{CIN})	Sub-clock oscillation frequency		32.768	50	kHz	

- Notes**
1. Average output current is the average value of a 100 ms interval.
 2. The sum of I_{OL(peak)} for ports P0, P1, P2, P3, and P8 must be 80 mA or less, the sum of I_{OH(peak)} for ports P0, P1, P2, P3, and P8 must be 80 mA or less, the sum of I_{OL(peak)} for ports P4, P5, P6, and P7 must be 100 mA or less, and the sum of I_{OH(peak)} for ports P4, P5, P6, and P7 must be 80 mA or less.
 3. Limits V_{IH} and V_{IL} for X_{CIN} are applied when the sub clock external input selection bit = "1".
 4. The maximum value of f(X_{IN}) = 6 MHz when the main clock division selection bit = "1".

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -40\text{ to }+85\text{ }^\circ\text{C}$, $f(X_{IN}) = 12\text{ MHz}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min.	Typ.	Max.		
V _{OH}	High-level output voltage P00 – P07, P10 – P17, P20 – P27, P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87	V _{CC} = 5 V, I _{OH} = –10 mA	3			V	
		V _{CC} = 3 V, I _{OH} = –1 mA	2.5				
V _{OH}	High-level output voltage P00 – P07, P10 – P17, P20 – P27, P33	V _{CC} = 5 V, I _{OH} = –400 μ A	4.7			V	
V _{OH}	High-level output voltage P30 – P32	V _{CC} = 5 V, I _{OH} = –10 mA	3.1			V	
		V _{CC} = 5 V, I _{OH} = –400 μ A	4.8				
		V _{CC} = 3 V, I _{OH} = –1 mA	2.6				
V _{OH}	High-level output voltage \bar{E}	V _{CC} = 5 V, I _{OH} = –10 mA	3.4			V	
		V _{CC} = 5 V, I _{OH} = –400 μ A	4.8				
		V _{CC} = 3 V, I _{OH} = –1 mA	2.6				
V _{OL}	Low-level output voltage P00 – P07, P10 – P17, P20 – P27, P33, P40 – P43, P54 – P57, P60 – P67, P70 – P77, P80 – P87	V _{CC} = 5 V, I _{OL} = 10 mA			2	V	
		V _{CC} = 3 V, I _{OL} = 1 mA			0.5		
V _{OL}	Low-level output voltage P44 – P47, P50 – P53	V _{CC} = 5 V, I _{OL} = 16 mA			1.8	V	
		V _{CC} = 3 V, I _{OL} = 10 mA			1.5		
V _{OL}	Low-level output voltage P00 – P07, P10 – P17, P20 – P27, P33	V _{CC} = 5 V, I _{OL} = 2 mA			0.45	V	
V _{OL}	Low-level output voltage P30 – P32	V _{CC} = 5 V, I _{OL} = 10 mA			1.9	V	
		V _{CC} = 5 V, I _{OL} = 2 mA			0.43		
		V _{CC} = 3 V, I _{OL} = 1 mA			0.4		
V _{OL}	Low-level output voltage \bar{E}	V _{CC} = 5 V, I _{OL} = 10 mA			1.6	V	
		V _{CC} = 5 V, I _{OL} = 2 mA			0.4		
		V _{CC} = 3 V, I _{OL} = 1 mA			0.4		
V _{T+} – V _{T–}	Hysteresis $\overline{\text{HOLD}}$, $\overline{\text{RDY}}$, TA0IN – TA4IN, TB0IN – TB2IN, INT0 – INT2, ADTRG, $\overline{\text{CTS0}}$, $\overline{\text{CTS1}}$, $\overline{\text{CTS2}}$, CLK0, CLK1, CLK2, $\overline{\text{K10}}$ – $\overline{\text{K13}}$	V _{CC} = 5 V	0.4		1	V	
		V _{CC} = 3 V	0.1		0.7		
V _{T+} – V _{T–}	Hysteresis $\overline{\text{RESET}}$	V _{CC} = 5 V	0.2		0.5	V	
		V _{CC} = 3 V	0.1		0.4		
V _{T+} – V _{T–}	Hysteresis X _{IN}	V _{CC} = 5 V	0.1		0.4	V	
		V _{CC} = 3 V	0.06		0.26		
V _{T+} – V _{T–}	Hysteresis X _{CIN} (When external clock is input)	V _{CC} = 5 V	0.1		0.4	V	
		V _{CC} = 3 V	0.06		0.26		
I _{IH}	High-level input current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, X _{IN} , $\overline{\text{RESET}}$, CNV _{SS} , BYTE	V _{CC} = 5 V, V _I = 5 V			5	μ A	
		V _{CC} = 3 V, V _I = 3 V			4		
I _{IL}	Low-level input current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P53, P60, P61, P65 – P67, P70 – P77, P80 – P87, X _{IN} , $\overline{\text{RESET}}$, CNV _{SS} , BYTE	V _{CC} = 5 V, V _I = 0 V			–5	μ A	
		V _{CC} = 3 V, V _I = 0 V			–4		
I _{IL}	Low-level input current P54 – P57, P62 – P64	V _I = 0 V, without a pull-up transistor	V _{CC} = 5 V			–5	μ A
			V _{CC} = 3 V			–4	
		V _I = 0 V, with a pull-up transistor	V _{CC} = 5 V	–0.25	–0.5	–1.0	mA
			V _{CC} = 3 V	–0.08	–0.18	–0.35	
V _{RAM}	RAM hold voltage	When clock is stopped.	2			V	

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -40\text{ to }+85\text{ }^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit		
			Min.	Typ.	Max.			
I _{CC}	Power source current	When single-chip mode, output pins are open, and other pins are V _{SS} .	V _{CC} = 5 V, f(X _{IN}) = 12 MHz (square waveform), f(f ₂) = 6 MHz, f(X _{CIN}) = 32.768 kHz, in operating (Note 1)		4.5	9	mA	
			V _{CC} = 3 V, f(X _{IN}) = 12 MHz (square waveform), f(f ₂) = 6 MHz, f(X _{CIN}) = 32.768 kHz, in operating (Note 1)		3	6	mA	
			V _{CC} = 3 V, f(X _{IN}) = 12 MHz (square waveform), f(f ₂) = 0.75 MHz, f(X _{CIN}) : Stopped, in operating		0.4	0.8	mA	
			V _{CC} = 3 V, f(X _{IN}) = 12 MHz (square waveform), f(X _{CIN}) = 32.768 kHz, when a WIT instruction is executed (Note 2)		6	12	μA	
			V _{CC} = 3 V, f(X _{IN}) : Stopped, f(X _{CIN}) = 32.768 kHz, in operating (Note 3)		30	60	μA	
			V _{CC} = 3 V, f(X _{IN}) : Stopped, f(X _{CIN}) = 32.768 kHz, when a WIT instruction is executed (Note 4)		3	6	μA	
			T _a = 25 °C, when clock is stopped				1	μA
			T _a = 85 °C, when clock is stopped				20	μA

- Notes 1.** This applies when the main clock external input selection bit = "1", the main clock division selection bit = "0", and the signal output stop bit = "1".
- 2.** This applies when the main clock external input selection bit = "1" and the system clock stop bit at wait state = "1".
- 3.** This applies when CPU and the clock timer are operating with the sub clock (32.768 kHz) selected as the system clock.
- 4.** This applies when the X_{COUT} drivability selection bit = "0" and the system clock stop bit at wait state = "1".

A–D CONVERTER CHARACTERISTICS

($V_{CC} = AV_{CC} = 5\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -40\text{ to }+85\text{ }^\circ\text{C}$, $f(X_{IN}) = 12\text{ MHz}$, unless otherwise noted (Note))

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution	V _{REF} = V _{CC}			10	Bits
—	Absolute accuracy	V _{REF} = V _{CC}			± 3	LSB
RLADDER	Ladder resistance	V _{REF} = V _{CC}	10		25	kΩ
t _{CONV}	Conversion time		19.6			μs
V _{REF}	Reference voltage		2.7		V _{CC}	V
V _{IA}	Analog input voltage		0		V _{REF}	V

Note. This applies when the main clock division selection bit = "0" and f(f₂) = 6 MHz.

TIMING REQUIREMENTS ($V_{CC} = 2.7 - 5.5$ V, $V_{SS} = 0$ V, $T_a = -40$ to $+85$ °C, $f(X_{IN}) = 12$ MHz, unless otherwise noted (Note 1))

Notes 1. This applies when the main clock division selection bit = "0" and $f(f_2) = 6$ MHz.

2. Input signal's rise/fall time must be 100 ns or less, unless otherwise noted.

External clock input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_c	External clock input cycle time (Note 1)	83		ns
$t_{w(H)}$	External clock input high-level pulse width (Note 2)	33		ns
$t_{w(L)}$	External clock input low-level pulse width (Note 2)	33		ns
t_r	External clock rise time		15	ns
t_f	External clock fall time		15	ns

Notes 1. When the main clock division selection bit = "1", the minimum value of $t_c = 166$ ns.

2. When the main clock division selection bit = "1", values of $t_{w(H)} / t_c$ and $t_{w(L)} / t_c$ must be set to values from 0.45 through 0.55.

Single-chip mode

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su}(P0D-E)$	Port P0 input setup time	200		ns
$t_{su}(P1D-E)$	Port P1 input setup time	200		ns
$t_{su}(P2D-E)$	Port P2 input setup time	200		ns
$t_{su}(P3D-E)$	Port P3 input setup time	200		ns
$t_{su}(P4D-E)$	Port P4 input setup time	200		ns
$t_{su}(P5D-E)$	Port P5 input setup time	200		ns
$t_{su}(P6D-E)$	Port P6 input setup time	200		ns
$t_{su}(P7D-E)$	Port P7 input setup time	200		ns
$t_{su}(P8D-E)$	Port P8 input setup time	200		ns
$t_{h(E-P0D)}$	Port P0 input hold time	0		ns
$t_{h(E-P1D)}$	Port P1 input hold time	0		ns
$t_{h(E-P2D)}$	Port P2 input hold time	0		ns
$t_{h(E-P3D)}$	Port P3 input hold time	0		ns
$t_{h(E-P4D)}$	Port P4 input hold time	0		ns
$t_{h(E-P5D)}$	Port P5 input hold time	0		ns
$t_{h(E-P6D)}$	Port P6 input hold time	0		ns
$t_{h(E-P7D)}$	Port P7 input hold time	0		ns
$t_{h(E-P8D)}$	Port P8 input hold time	0		ns

Memory expansion mode and microprocessor mode

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su}(D-E)$	Data input setup time	50		ns
$t_{su}(RDY-\phi 1)$	RDY input setup time	80		ns
$t_{su}(HOLD-\phi 1)$	HOLD input setup time	80		ns
$t_{h(E-D)}$	Data input hold time	0		ns
$t_{h}(\phi 1-RDY)$	RDY input hold time	0		ns
$t_{h}(\phi 1-HOLD)$	HOLD input hold time	0		ns

Timer A input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiN input cycle time	250		ns
$t_{w(TAH)}$	TAiN input high-level pulse width	125		ns
$t_{w(TAL)}$	TAiN input low-level pulse width	125		ns

Timer A input (Gating input in timer mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiN input cycle time (Note)	666		ns
$t_{w(TAH)}$	TAiN input high-level pulse width (Note)	333		ns
$t_{w(TAL)}$	TAiN input low-level pulse width (Note)	333		ns

Note. Limits change depending on $f(X_{IN})$. Refer to "DATA FORMULAS".

Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiN input cycle time (Note)	666		ns
$t_{w(TAH)}$	TAiN input high-level pulse width	166		ns
$t_{w(TAL)}$	TAiN input low-level pulse width	166		ns

Note. Limits change depending on $f(X_{IN})$. Refer to "DATA FORMULAS".

Timer A input (External trigger input in pulse width modulation mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiN input high-level pulse width	166		ns
$t_{w(TAL)}$	TAiN input low-level pulse width	166		ns

Timer A input (Up-down input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT input cycle time	3333		ns
$t_{w(UPH)}$	TAiOUT input high-level pulse width	1666		ns
$t_{w(UPL)}$	TAiOUT input low-level pulse width	1666		ns
$t_{su(UP-T_{IN})}$	TAiOUT input setup time	666		ns
$t_{h(T_{IN}-UP)}$	TAiOUT input hold time	666		ns

Timer A input (Two-phase pulse input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAjIN input cycle time	2000		ns
$t_{su(TAjIN-TAjOUT)}$	TAjIN input setup time	500		ns
$t_{su(TAjOUT-TAjIN)}$	TAjOUT input setup time	500		ns

Timer B input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (one edge count)	250		ns
$t_{w(TBH)}$	TBiIN input high-level pulse width (one edge count)	125		ns
$t_{w(TBL)}$	TBiIN input low-level pulse width (one edge count)	125		ns
$t_{c(TB)}$	TBiIN input cycle time (both edges count)	500		ns
$t_{w(TBH)}$	TBiIN input high-level pulse width (both edges count)	250		ns
$t_{w(TBL)}$	TBiIN input low-level pulse width (both edges count)	250		ns

Timer B input (Pulse period measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (Note)	666		ns
$t_{w(TBH)}$	TBiIN input high-level pulse width (Note)	333		ns
$t_{w(TBL)}$	TBiIN input low-level pulse width (Note)	333		ns

Note. Limits change depending on $f(X_{IN})$. Refer to "DATA FORMULAS".

Timer B input (Pulse width measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (Note)	666		ns
$t_{w(TBH)}$	TBiIN input high-level pulse width (Note)	333		ns
$t_{w(TBL)}$	TBiIN input low-level pulse width (Note)	333		ns

Note. Limits change depending on $f(X_{IN})$. Refer to "DATA FORMULAS".

A-D trigger input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(AD)}$	ADTRG input cycle time (minimum allowable trigger)	1333		ns
$t_{w(ADL)}$	ADTRG input low-level pulse width	166		ns

Serial I/O

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	333		ns
$t_{w(CKH)}$	CLKi input high-level pulse width	166		ns
$t_{w(CKL)}$	CLKi input low-level pulse width	166		ns
$t_{d(C-Q)}$	TxDi output delay time		100	ns
$t_{h(C-Q)}$	TxDi hold time	0		ns
$t_{su(D-C)}$	RxDi input setup time	65		ns
$t_{h(C-D)}$	RxDi input hold time	75		ns

External interrupt \overline{INT}_i input, key input interrupt \overline{KI}_i input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{w(INH)}$	\overline{INT}_i input high-level pulse width	250		ns
$t_{w(INL)}$	\overline{INT}_i input low-level pulse width	250		ns
$t_{w(KIL)}$	\overline{KI}_i input low-level pulse width	250		ns

DATA FORMULAS

Timer A input (Gating input in timer mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIn input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TAH)}$	TAiIn input high-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TAL)}$	TAiIn input low-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns

Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIn input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns

Timer B input (In pulse period measurement mode or pulse width measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIn input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TBH)}$	TBiIn input high-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TBL)}$	TBiIn input low-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns

Note. $f(f_2)$ represents the clock f_2 frequency.

For the relation to the main clock and sub clock, refer to Table 9 in data sheet "M37733MHBXXXFP".

EOL announced

SWITCHING CHARACTERISTICS

($V_{CC} = 2.7 - 5.5 V$, $V_{SS} = 0 V$, $T_a = -40$ to $+85^\circ C$, $f(XIN) = 12 MHz$, unless otherwise noted (Note))

Single-chip mode

Symbol	Parameter	Test conditions	Limits		Unit
			Min.	Max.	
$t_{d(E-P0Q)}$	Port P0 data output delay time	Fig. 2		300	ns
$t_{d(E-P1Q)}$	Port P1 data output delay time			300	ns
$t_{d(E-P2Q)}$	Port P2 data output delay time			300	ns
$t_{d(E-P3Q)}$	Port P3 data output delay time			300	ns
$t_{d(E-P4Q)}$	Port P4 data output delay time			300	ns
$t_{d(E-P5Q)}$	Port P5 data output delay time			300	ns
$t_{d(E-P6Q)}$	Port P6 data output delay time			300	ns
$t_{d(E-P7Q)}$	Port P7 data output delay time			300	ns
$t_{d(E-P8Q)}$	Port P8 data output delay time			300	ns

Note. This applies when the main clock division selection bit = "0" and $f(f_2) = 6 MHz$.

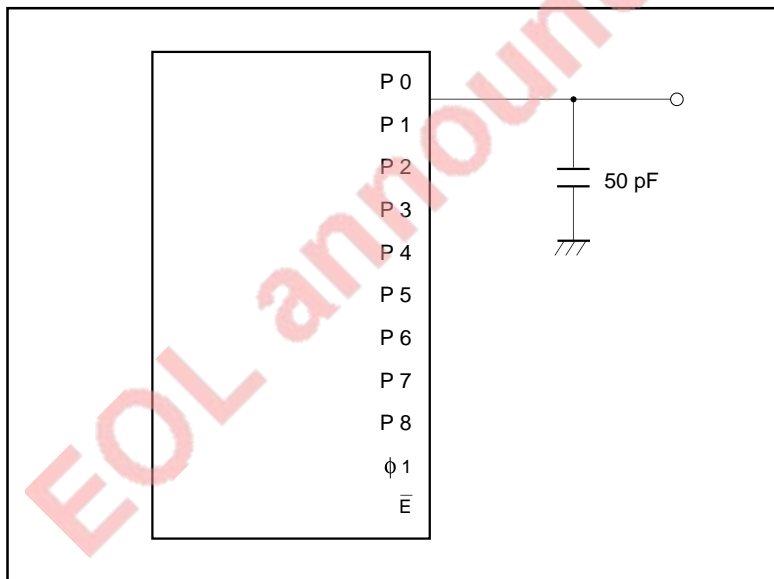


Fig. 2 Measuring circuit for ports P0 – P8 and phi 1

Memory expansion mode and microprocessor mode

(V_{CC} = 2.7 – 5.5 V, V_{SS} = 0 V, T_a = –40 to +85°C, f(XIN) = 12 MHz (Note 1), unless otherwise noted)

Symbol	Parameter	(Note 2) Wait mode	Test conditions	Limits		Unit
				Min.	Max.	
td(An–E)	Address output delay time	No wait	Fig. 2	20		ns
		Wait 1				
		Wait 0		182		ns
td(A–E)	Address output delay time	No wait		20		ns
		Wait 1				
		Wait 0		162		ns
th(E–An)	Address hold time			40		ns
tw(ALE)	ALE pulse width	No wait		40		ns
		Wait 1				
		Wait 0		123		ns
tsu(A–ALE)	Address output set up time	No wait		10		ns
		Wait 1				
		Wait 0		93		ns
th(ALE–A)	Address hold time	No wait		9		ns
		Wait 1				
		Wait 0	40		ns	
td(ALE–E)	ALE output delay time	No wait	4		ns	
		Wait 1				
		Wait 0	40		ns	
td(E–DQ)	Data output delay time			90	ns	
th(E–DQ)	Data hold time		40		ns	
tw(EL)	E pulse width	No wait	131		ns	
		Wait 1				
		Wait 0	298		ns	
tpxz(E–DZ)	Floating start delay time			10	ns	
tpzx(E–DZ)	Floating release delay time		53		ns	
td(BHE–E)	BHE output delay time	No wait	20		ns	
		Wait 1				
		Wait 0	182		ns	
td(R/W–E)	R/W output delay time	No wait	20		ns	
		Wait 1				
		Wait 0	182		ns	
th(E–BHE)	BHE hold time		33		ns	
th(E–R/W)	R/W hold time		33		ns	
td(E–φ 1)	φ 1 output delay time		0	30	ns	
td(φ 1–HLDA)	HLDA output delay time			120	ns	

Notes 1. This applies when the main clock division selection bit = “0” and f(f₂) = 6 MHz.

2. No wait : Wait bit = “1”.

Wait 1 : The external memory area is accessed with wait bit = “0” and wait selection bit = “1”.

Wait 0 : The external memory area is accessed with wait bit = “0” and wait selection bit = “0”.

Memory expansion mode and microprocessor mode

Bus timing data formulas ($V_{CC} = 2.7 - 5.5 \text{ V}$, $V_{SS} = 0 \text{ V}$, $T_a = -40 \text{ to } +85 \text{ }^\circ\text{C}$, $f(XIN) = 12 \text{ MHz (Max., Note)}$, unless otherwise noted)

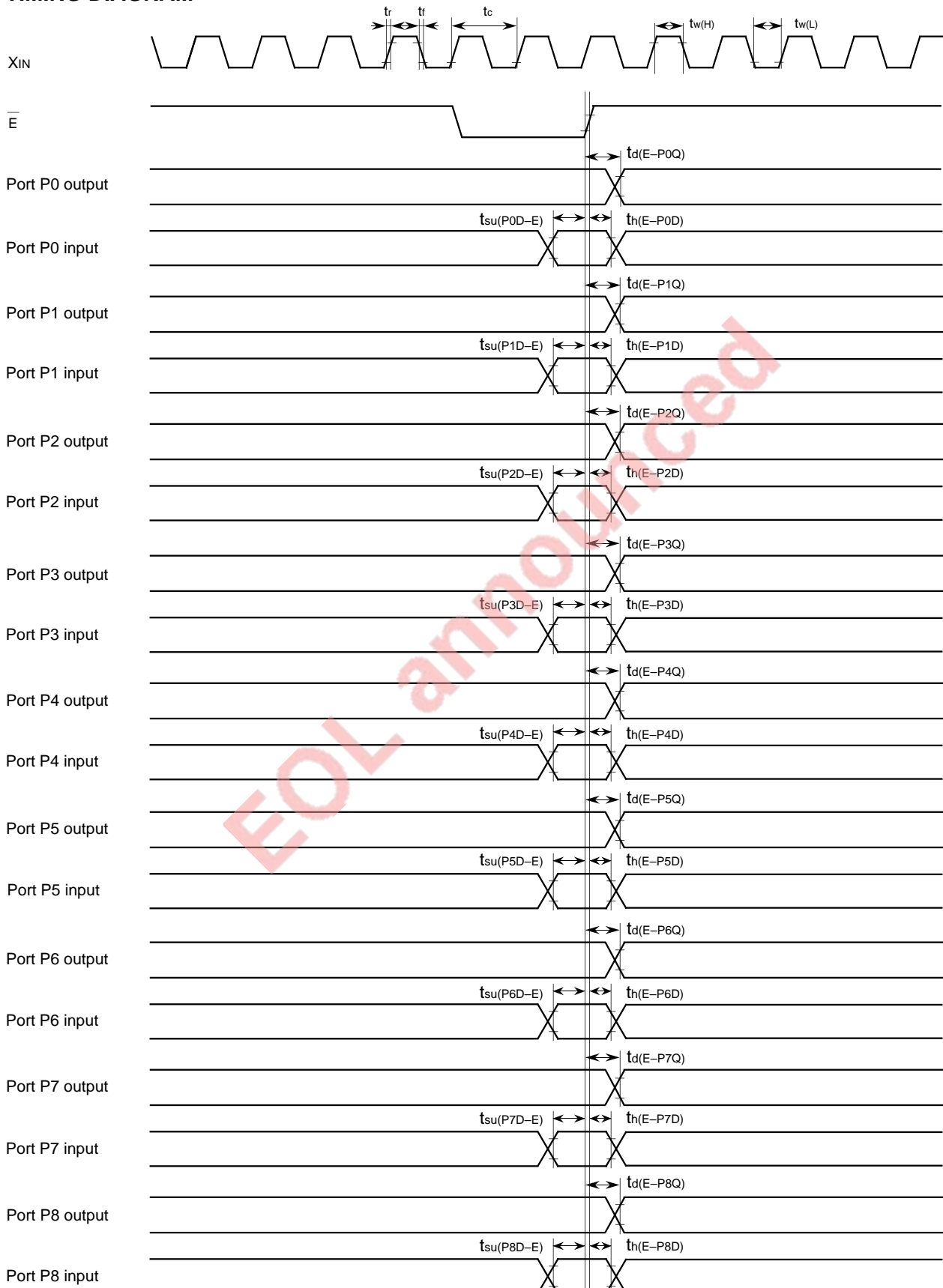
Symbol	Parameter	Wait mode	Limits		Unit
			Min.	Max.	
td(An-E)	Address output delay time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 63	ns
		Wait 1	$\frac{3 \times 10^9}{2 \cdot f(f_2)}$	- 68	
		Wait 0	$\frac{3 \times 10^9}{2 \cdot f(f_2)}$	- 68	
td(A-E)	Address output delay time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 63	ns
		Wait 1	$\frac{3 \times 10^9}{2 \cdot f(f_2)}$	- 88	
		Wait 0	$\frac{3 \times 10^9}{2 \cdot f(f_2)}$	- 88	
th(E-An)	Address hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 43	ns
tw(ALE)	ALE pulse width	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 43	ns
		Wait 1	$\frac{2 \times 10^9}{2 \cdot f(f_2)}$	- 43	
		Wait 0	$\frac{2 \times 10^9}{2 \cdot f(f_2)}$	- 43	
tsu(A-ALE)	Address output set up time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 73	ns
		Wait 1	$\frac{2 \times 10^9}{2 \cdot f(f_2)}$	- 73	
		Wait 0	$\frac{2 \times 10^9}{2 \cdot f(f_2)}$	- 73	
th(ALE-A)	Address hold time	No wait	9		ns
		Wait 1	$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 43	
		Wait 0	$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 43	
td(ALE-E)	ALE output delay time	No wait	4		ns
		Wait 1	$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 43	
		Wait 0	$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 43	
td(E-DQ)	Data output delay time			90	ns
th(E-DQ)	Data hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 43	ns
tw(EL)	\bar{E} pulse width	No wait	$\frac{2 \times 10^9}{2 \cdot f(f_2)}$	- 35	ns
		Wait 1	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$	- 35	
		Wait 0	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$	- 35	
tpxz(E-DZ)	Floating start delay time			10	ns
tpzx(E-DZ)	Floating release delay time		$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 30	ns
td(BHE-E)	\overline{BHE} output delay time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 63	ns
		Wait 1	$\frac{3 \times 10^9}{2 \cdot f(f_2)}$	- 68	
		Wait 0	$\frac{3 \times 10^9}{2 \cdot f(f_2)}$	- 68	
td(R/W-E)	R/\overline{W} output delay time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 63	ns
		Wait 1	$\frac{3 \times 10^9}{2 \cdot f(f_2)}$	- 68	
		Wait 0	$\frac{3 \times 10^9}{2 \cdot f(f_2)}$	- 68	
th(E-BHE)	\overline{BHE} hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 50	ns
th(E-R/W)	R/\overline{W} hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 50	ns
td(E-φ 1)	φ 1 output delay time		0	30	ns

Notes 1. This applies when the main-clock division selection bit = "0".

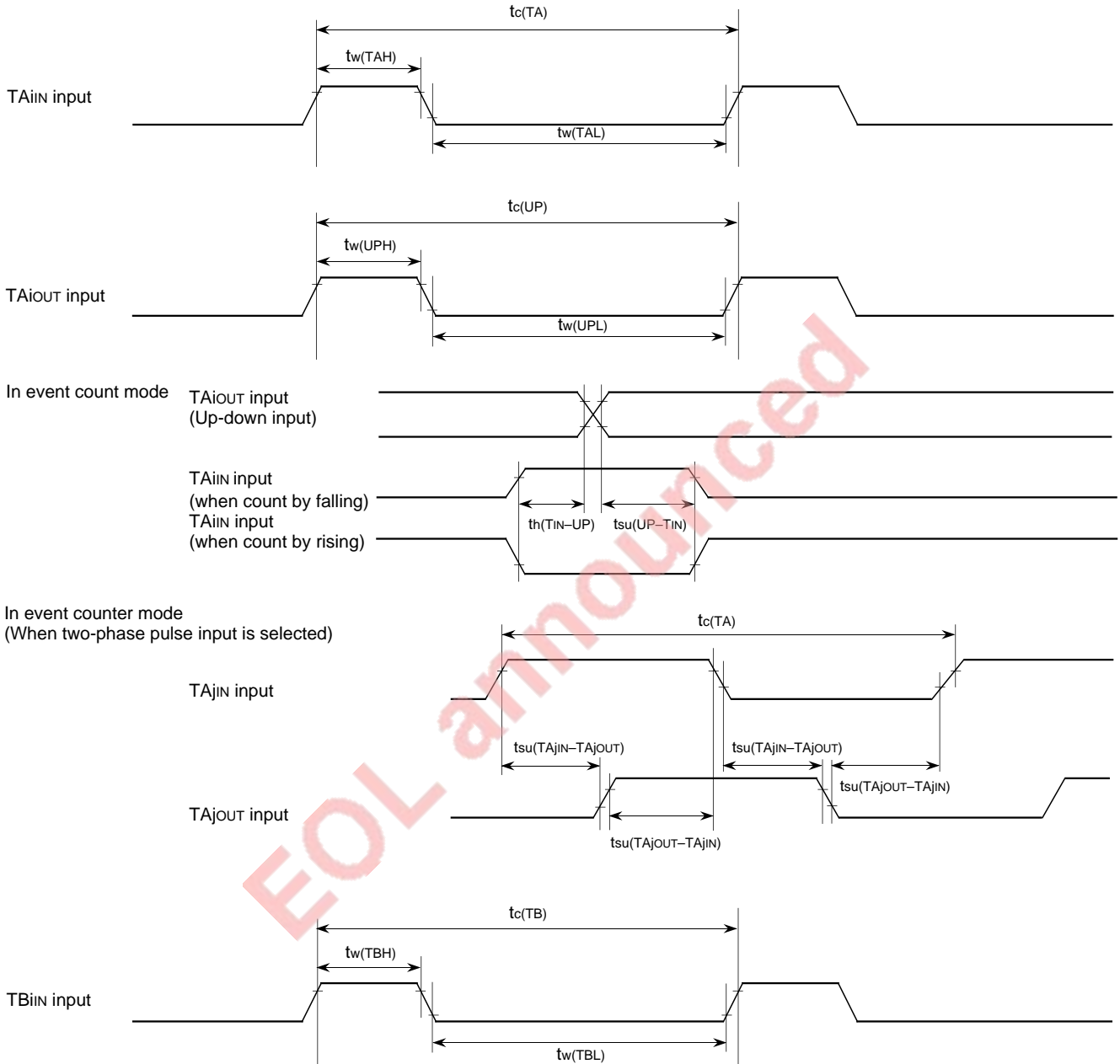
2. $f(f_2)$ represents the clock f_2 frequency.

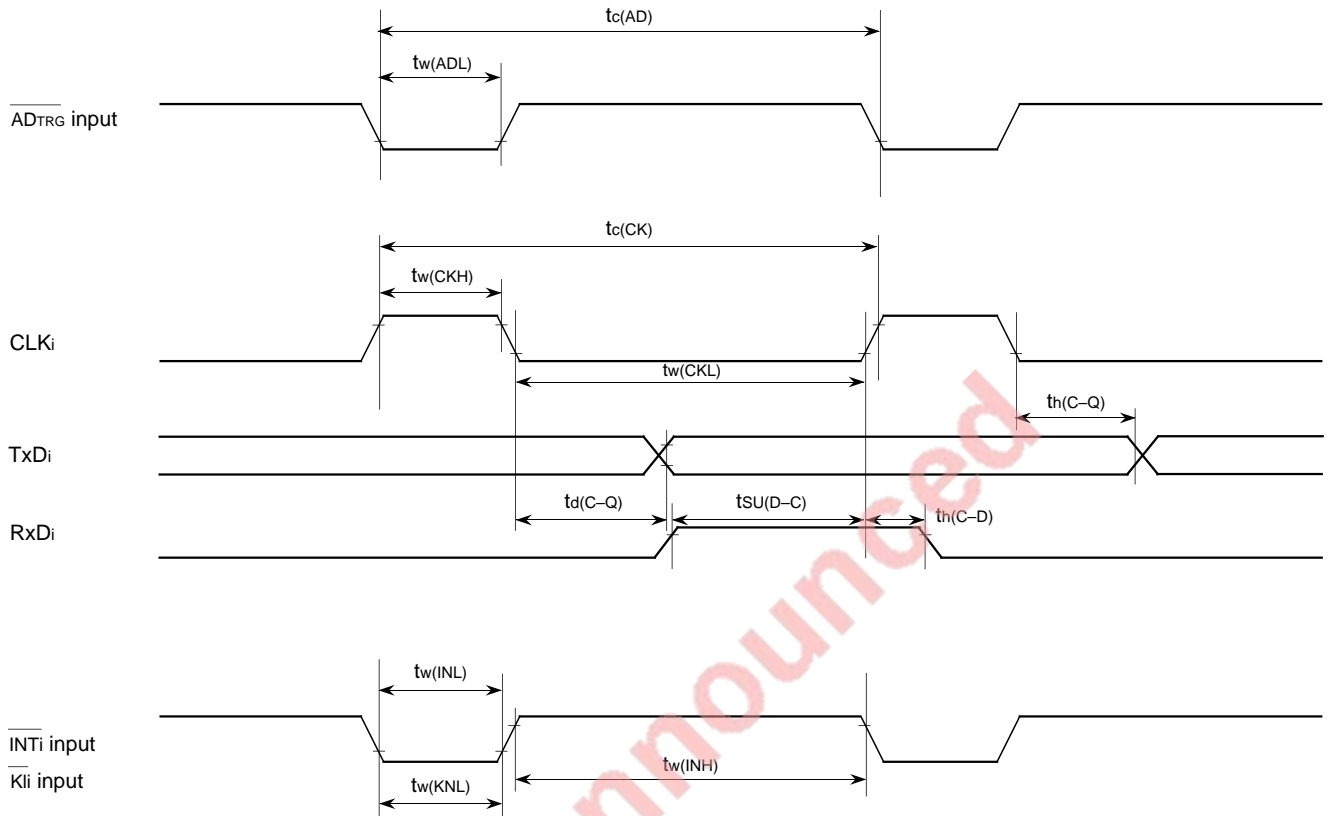
For the relation to the main clock and sub clock, refer to Table 9 in data sheet "M37733MHBXXXFP".

TIMING DIAGRAM



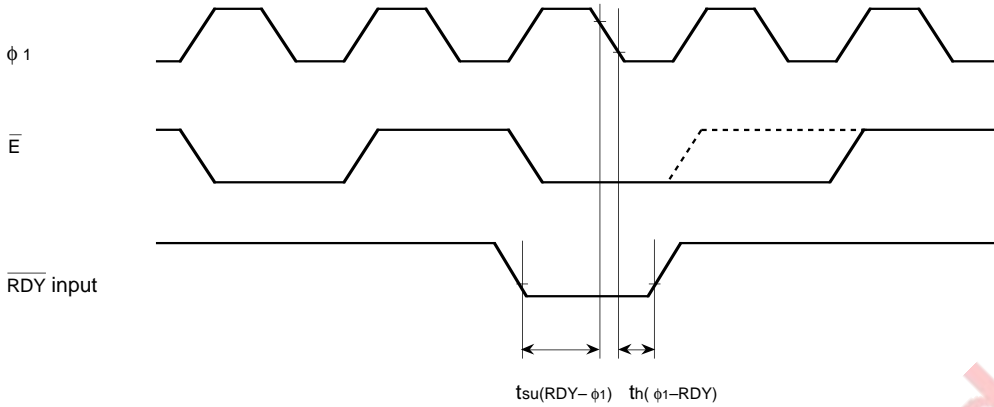
EOL announced



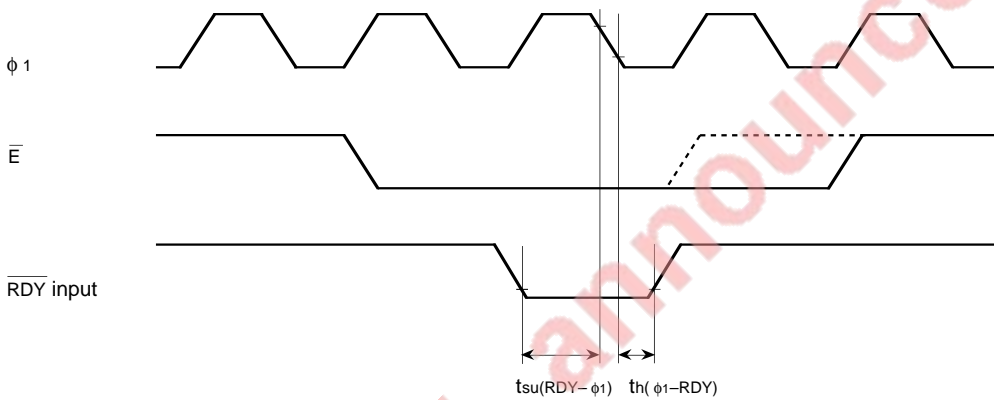


EOL announced

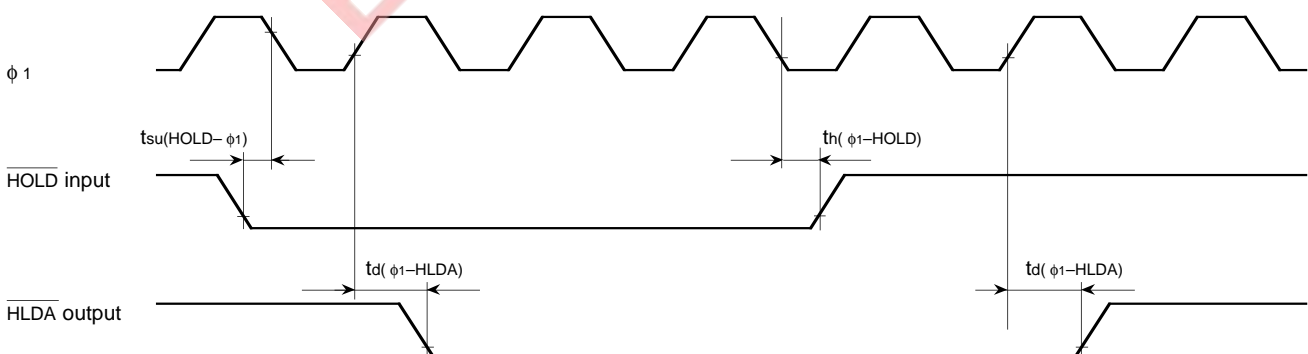
Memory expansion mode and microprocessor mode
 (When wait bit = "1")



(When wait bit = "0")



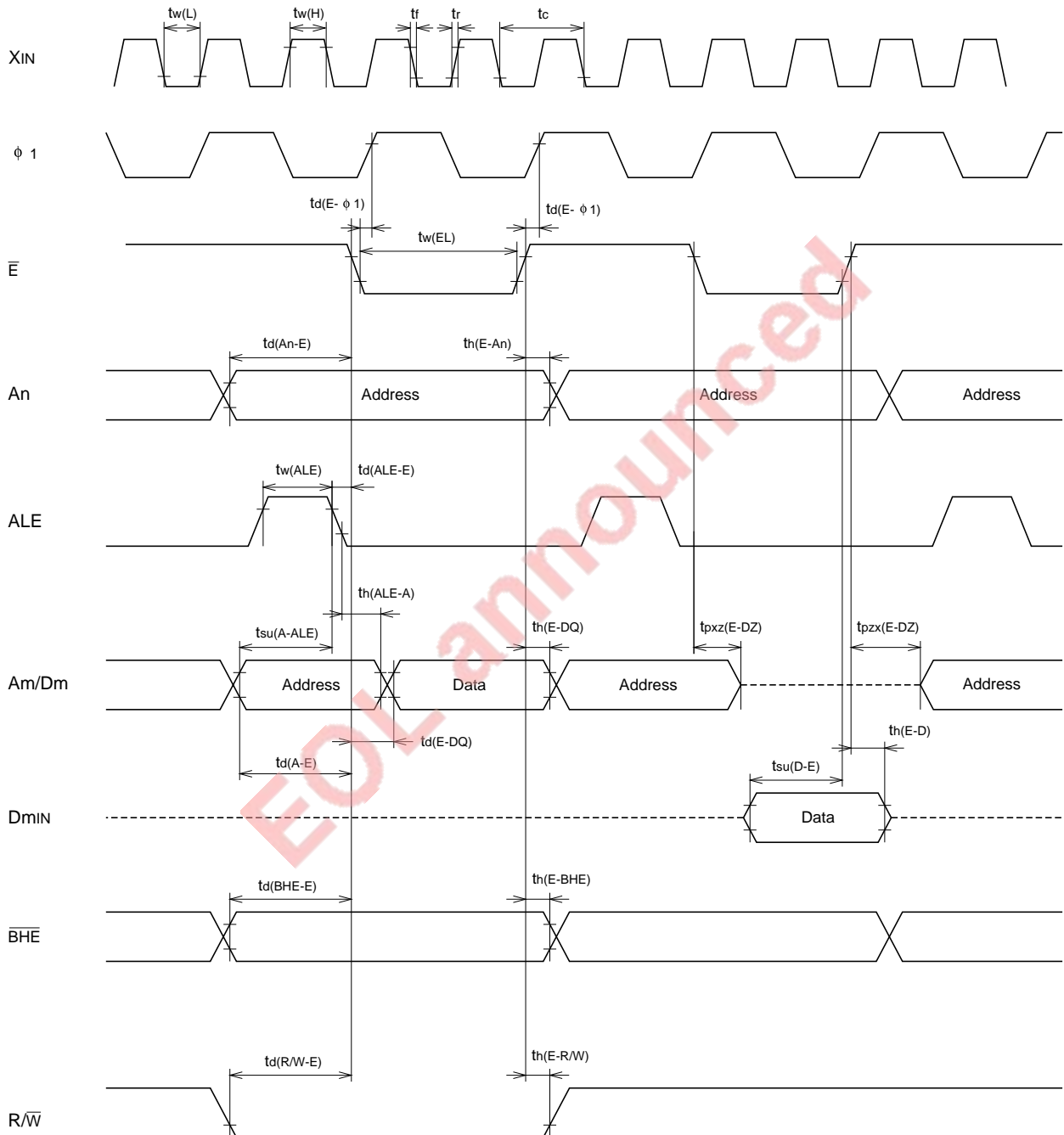
(When wait bit = "1" or "0" in common)



Test conditions

- $V_{CC} = 2.7 - 5.5 \text{ V}$
- Input timing voltage : $V_{IL} = 0.2 V_{CC}$, $V_{IH} = 0.8 V_{CC}$
- Output timing voltage : $V_{OL} = 0.8 \text{ V}$, $V_{OH} = 2.0 \text{ V}$

Memory expansion mode and microprocessor mode
 (No wait : When wait bit = "1")

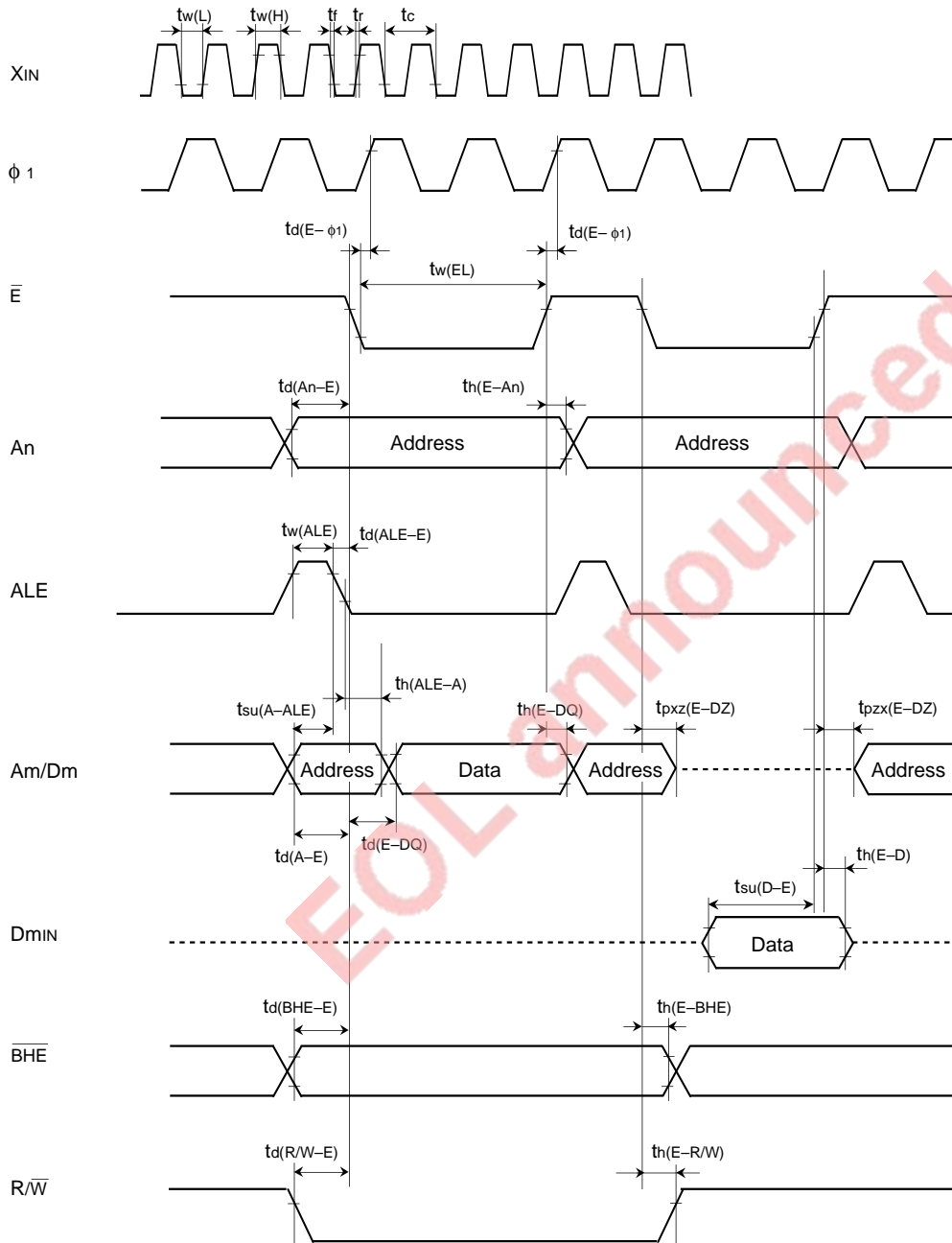


Test condition

- $V_{CC} = 2.7 - 5.5 V$
- Output timing voltage : $V_{OL} = 0.8 V, V_{OH} = 2.0 V$
- Data input D_{min} : $V_{IL} = 0.16 V_{CC}, V_{IH} = 0.5 V_{CC}$

Memory expansion mode and microprocessor mode

(Wait 1 : The external area is accessed when wait bit = "0" and wait selection bit = "1".)

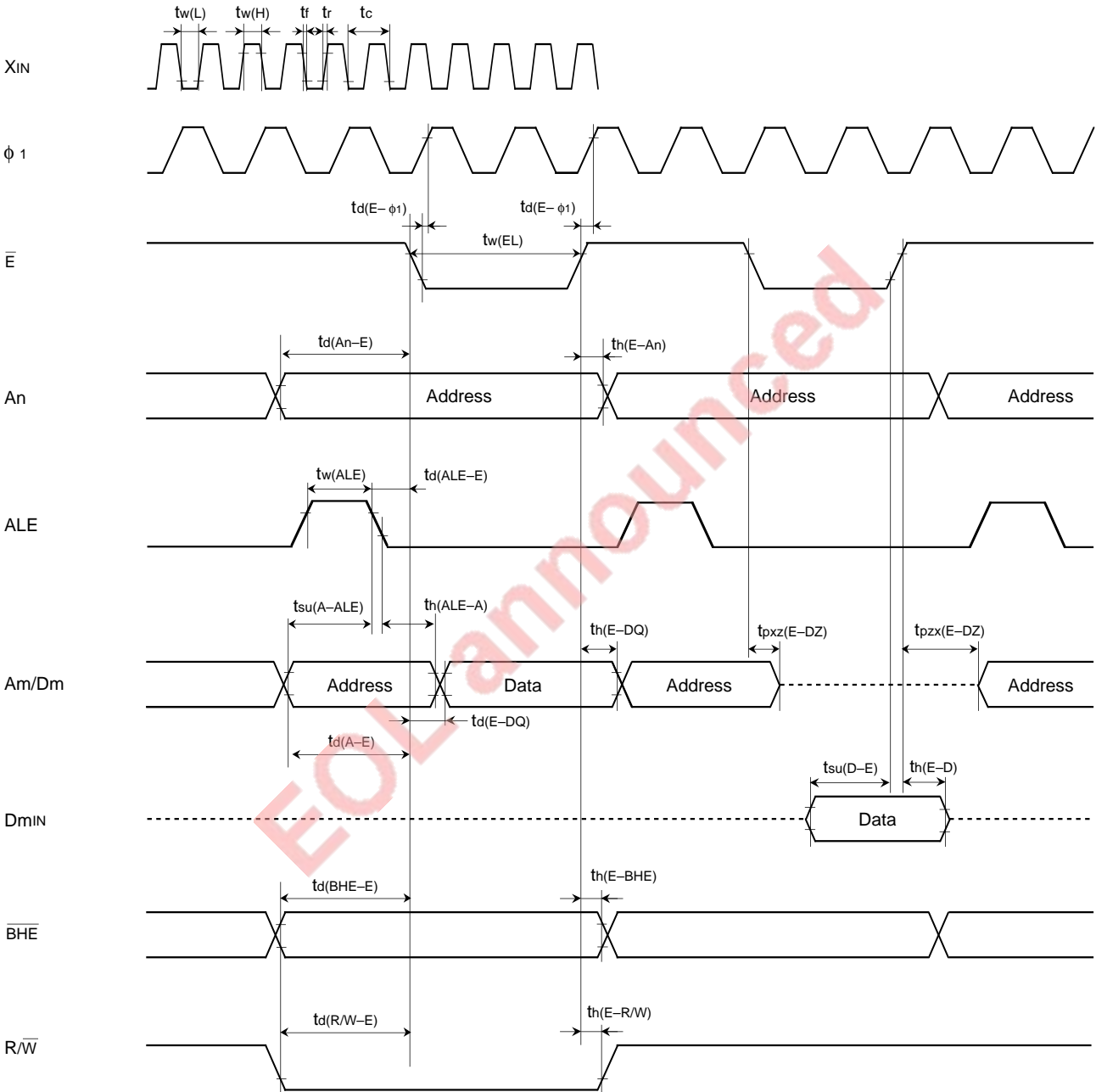


Test condition

- $V_{CC} = 2.7 - 5.5 V$
- Output timing voltage : $V_{OL} = 0.8 V$, $V_{OH} = 2.0 V$
- Data input D_{min} : $V_{IL} = 0.16 V_{CC}$, $V_{IH} = 0.5 V_{CC}$

Memory expansion mode and microprocessor mode

(Wait 0 : The external memory area is accessed when wait bit = "0" and wait selection bit = "0".)



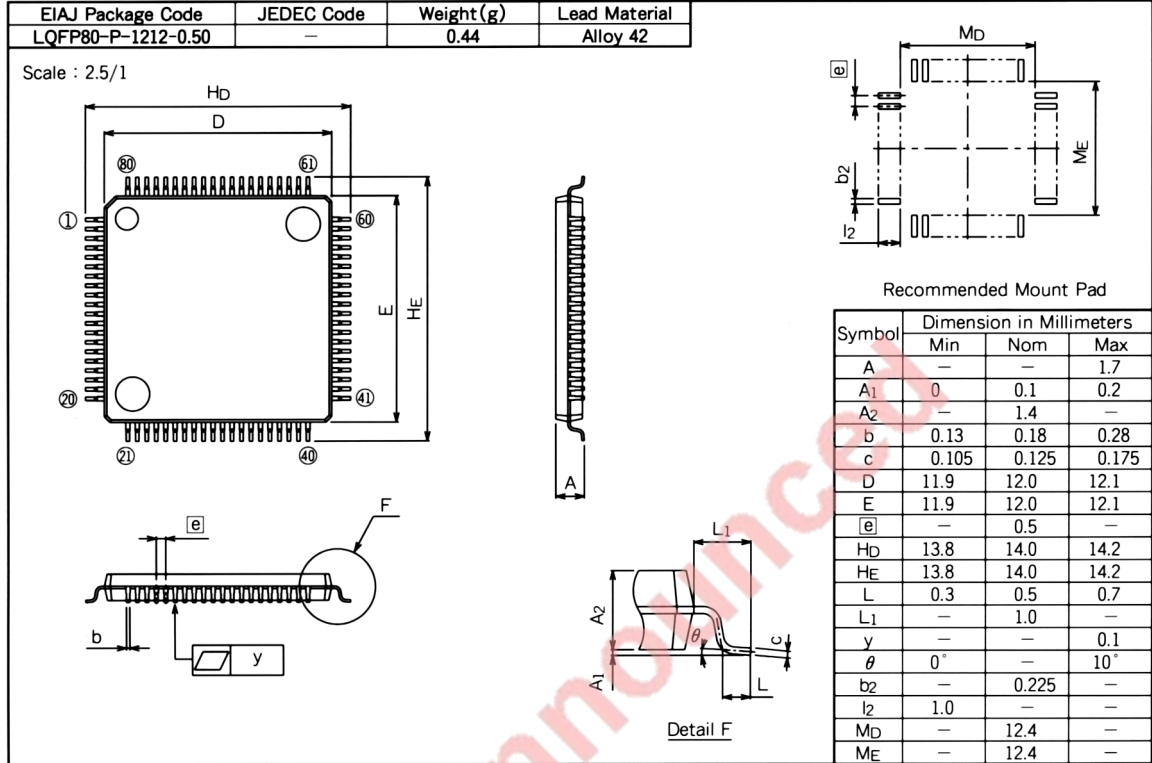
Test conditions

- $V_{CC} = 2.7 - 5.5$ V
- Output timing voltage : $V_{OL} = 0.8$ V, $V_{OH} = 2.0$ V
- Data input D_{min} : $V_{IL} = 0.16$ V_{CC} , $V_{IH} = 0.5$ V_{CC}

PACKAGE OUTLINE

80P6D-A

Plastic 80pin 12x12mm body LQFP



EOL announcement

GZZ-SH00-44B<68A0>

7700 FAMILY MASK ROM ORDER CONFIRMATION FORM
SINGLE-CHIP 16-BIT MICROCOMPUTER
M37733MHLXXXHP
MITSUBISHI ELECTRIC

Mask ROM number	
-----------------	--

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked ※

※	Customer	Company name	TEL ()	Issuance signatures	Responsible officer	Supervisor
		Date issued	Date:			

※1. Confirmation

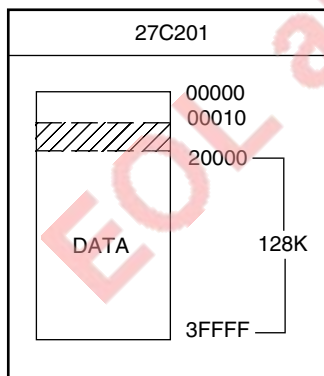
Specify the name of the product being ordered.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based on this data.
We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data.
Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM areas

--	--	--	--

 (hexadecimal notation)

EPROM Type :



- (1) Set "FF₁₆" in the shaded area.
- (2) Address 0₁₆ to 10₁₆ are the area for storing the data on model designation and options. This area must be written with the data shown below.
Details for option data are given next in the section describing the STP instruction option.
Address and data are written in hexadecimal notation.

Address	Address	Address
4D 0	4C 8	Option data 10
33 1	FF 9	
37 2	FF A	
37 3	FF B	
33 4	FF C	
33 5	FF D	
4D 6	FF E	
48 7	FF F	

※2. STP instruction option

One of the following sets of data should be written to the option data address (10₁₆) of the EPROM you have ordered.
Check @ in the appropriate box.

- STP instruction enable Address 10₁₆
 STP instruction disable Address 10₁₆

※3. Mark specification

Mark specification must be submitted using the correct form for the type of package being ordered fill out the appropriate 80P6D Mark Specification Form (for M37733MHLXXXHP) and attach to the Mask ROM Order Confirmation Form.

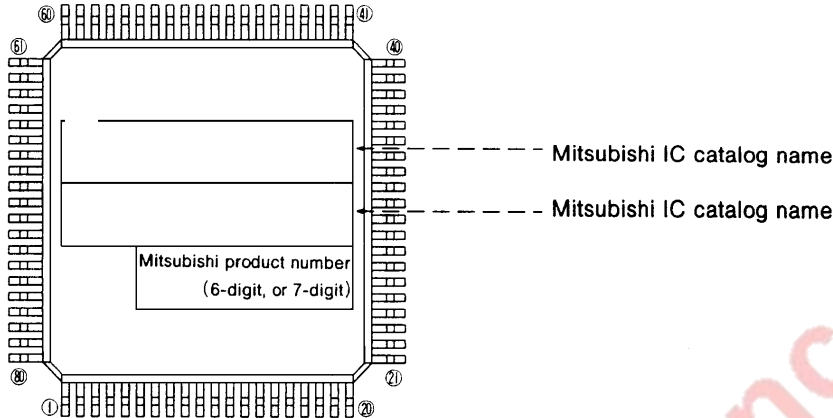
※4. Comments

80P6S (80-PIN QFP) MARK SPECIFICATION FORM
80P6D (80-PIN Fine-pitch QFP)

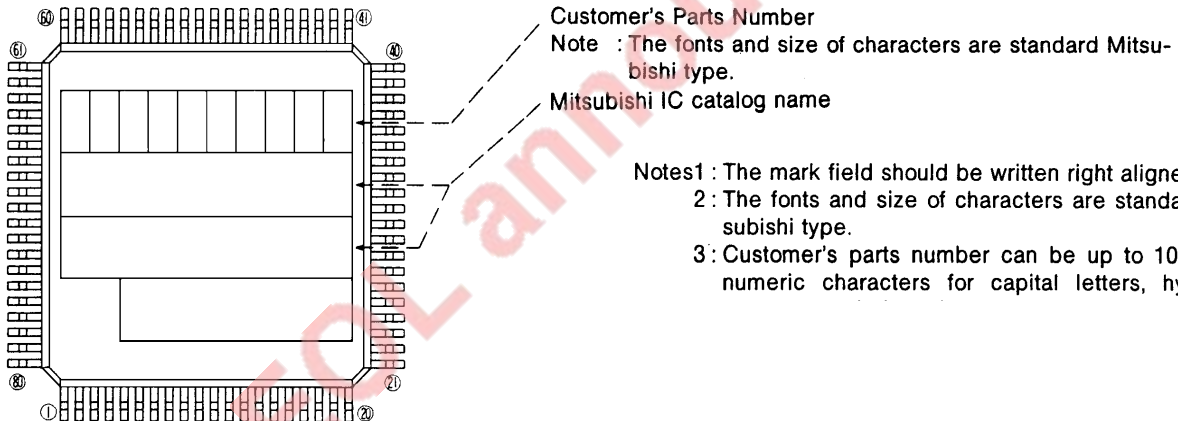
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark

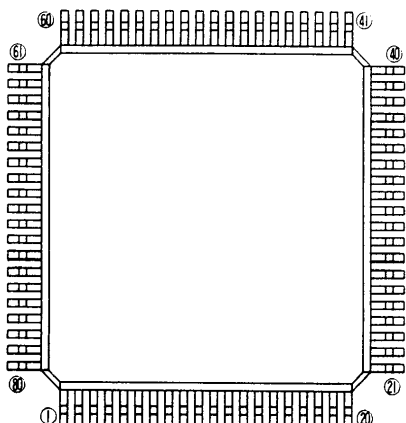


B. Customer's Parts Number + Mitsubishi IC Catalog Name



- Notes1 : The mark field should be written right aligned.
 2 : The fonts and size of characters are standard Mitsubishi type.
 3 : Customer's parts number can be up to 10 alphanumeric characters for capital letters, hyphens,

C. Special Mark Required



- Notes1 : If special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated technically as close as possible. Mitsubishi product number (6-digit, or 7-digit) and Mask ROM number (3-digit) are always marked for sorting the products.
 2 : If special character fonts (e.g., customer's trade mark logo) must be used in Special Mark, check the box below.
 For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special character fonts required

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

MITSUBISHI MICROCOMPUTERS
M37733MHLXXXHP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

EOL announced

Renesas Technology Corp.

Nippon Bldg.,6-2,Otemachi 2-chome,Chiyoda-ku,Tokyo,100-0004 Japan

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REVISION DESCRIPTION LIST

M37733MHLXXXHP Datasheet

Rev. No.	Revision Description		Rev. date																				
1.00	First Edition		970414																				
1.01	The following are added: <ul style="list-style-type: none"> • MASK ROM ORDER CONFIRMATION FORM • MARK SPECIFICATION FORM 		980421																				
2.00	The following are revised:		980731																				
	Page	Previous Version	Revised Version																				
	P1 PIN CONFIGURATION (TOP VIEW)	Outline 80P6D-A	Outline 80P6D-A, 80P6Q-A																				
	P5 Right column Line 2	The M37733MHLXXXHP has 28 powerful addressing modes. Refer to the SINGLE-CHIP 16-BIT MICROCOMPUTERS DATA BOOK for the details of each addressing mode. MACHINE INSTRUCTION LIST The M37733MHLXXXHP has 103 machine instructions. Refer to the SINGLE-CHIP 16-BIT MICROCOMPUTERS DATA BOOK for details.	The M37733MHLXXXHP has 28 powerful addressing modes. Refer to the "7700 Family Software Manual" for the details. MACHINE INSTRUCTION LIST The M37733MHLXXXHP has 103 machine instructions. Refer to the "7700 Family Software Manual" for the details.																				
	Line 10	(2) 80P6D mark specification form	(2) 80P6D, 80P6Q mark specification form																				
	P6 RECOMMENDED OPERATING CONDITIONS	Previous Version <table border="1"> <thead> <tr> <th rowspan="2">Symbol</th> <th rowspan="2">Parameter</th> <th colspan="3">Limits</th> <th rowspan="2">Unit</th> </tr> <tr> <th>Min.</th> <th>Typ.</th> <th>Max.</th> </tr> </thead> <tbody> <tr> <td rowspan="2">Vcc</td> <td rowspan="2">Power source voltage</td> <td>f(XIN) : Operating</td> <td>4.5</td> <td>5.0</td> <td>5.5</td> <td rowspan="2">V</td> </tr> <tr> <td>f(XIN) : Stopped, f(XCIN) = 32.768 kHz</td> <td>2.7</td> <td></td> <td>5.5</td> </tr> </tbody> </table>		Symbol	Parameter	Limits			Unit	Min.	Typ.	Max.	Vcc	Power source voltage	f(XIN) : Operating	4.5	5.0	5.5	V	f(XIN) : Stopped, f(XCIN) = 32.768 kHz	2.7		5.5
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