iW3700

High Performance Digital Integrated PFC and Flyback Controller for LED Driver Applications

The iW3700 is a high performance combination AC/DC controller specifically designed for high performance dimmable solid-state lighting LED driver applications. The device integrates both power factor correction (PFC) and LED current and voltage regulation stages in a single SOIC-14 package to enable a high integration level and overall system optimization. With full digital control inside, the iW3700 delivers best-in-class PF, total harmonic distortion (THD), current and voltage regulation, dimming resolution and dimming range. With Renesas' patented ***PrimAccurate*™** technology, the iW3700 eliminates the complicated regulation and dimming circuit on the secondary side.

The iW3700's unique dual-mode, dual dimming pin interface significantly simplifies the application design. The end-user can field-program the maximum LED current through one dimming pin by analog voltage level, an adjustable resistor or PWM duty cycle. The second dimming port can be used for 3-in-1 dimming: analog level, PWM duty cycle or resistor dimming. Internally, the iW3700 processes the dimming inputs and regulates the output current percentage = DIM1 % x DIM2%.

A dedicated light-off mode in the iW3700 turns off the LED while keeping itself powered when the dimming signal input is less than the light off threshold. This is achieved by regulating the output voltage at a low constant voltage (CV) target which is lower than the LED load light-on threshold. In light-off mode, the iW3700 continually monitors the dimming inputs. If the dimming signal input becomes higher than the light-on threshold, the iW3700 immediately wakes up and resumes LED current regulation.

The PFC stage in the iW3700 has very fast dynamic load response on top of the good PF/THD/harmonic performance. This enables the use of a lower voltage rated, lower capacitance value, high-voltage DC bus electrolytic capacitor, which greatly helps the power density and BOM cost.

Features

- Input AC voltage range: 85 ~ 305V
- Support up to 150W
- CV/CC mode with seamless transition
- Optional Constant Power (CP) limit
- Dimming range: 0.0625% ~ 100%
- Highest dimming resolution: 0.0625%
- CC line and load regulation < ±3%
- CV line and load regulation < ±3%
- Over temperature current de-rating with NTC and/or internal sensor
- 3-in-1 dimming on both dimming ports
- Auto dimming signal types detection
- PF > 0.9, THD < 20% at 277V/50Hz, 50% load
- Meets IEC61000-3-2 harmonic requirement
- "Follower" DC bus level of PFC for good efficiency
- Supports 450V_{DC} bus capacitor up to 280V_{AC} input with up to 2.5W/µF energy density
- Rich protection features:
  - Output over voltage (OVP)
  - Output short circuit (OSP)
  - Over current protection (OCP)
  - V_{VIN} over/under voltage
  - V_{BUS} over/under voltage
  - PFC over load protection
  - Over temperature protection (OTP)

Applications

- Two-stage AC/DC dimmable LED lighting drivers
- Two-stage AC/DC LED light strip drivers

Contents

1. Overview

1.1 Block Diagram

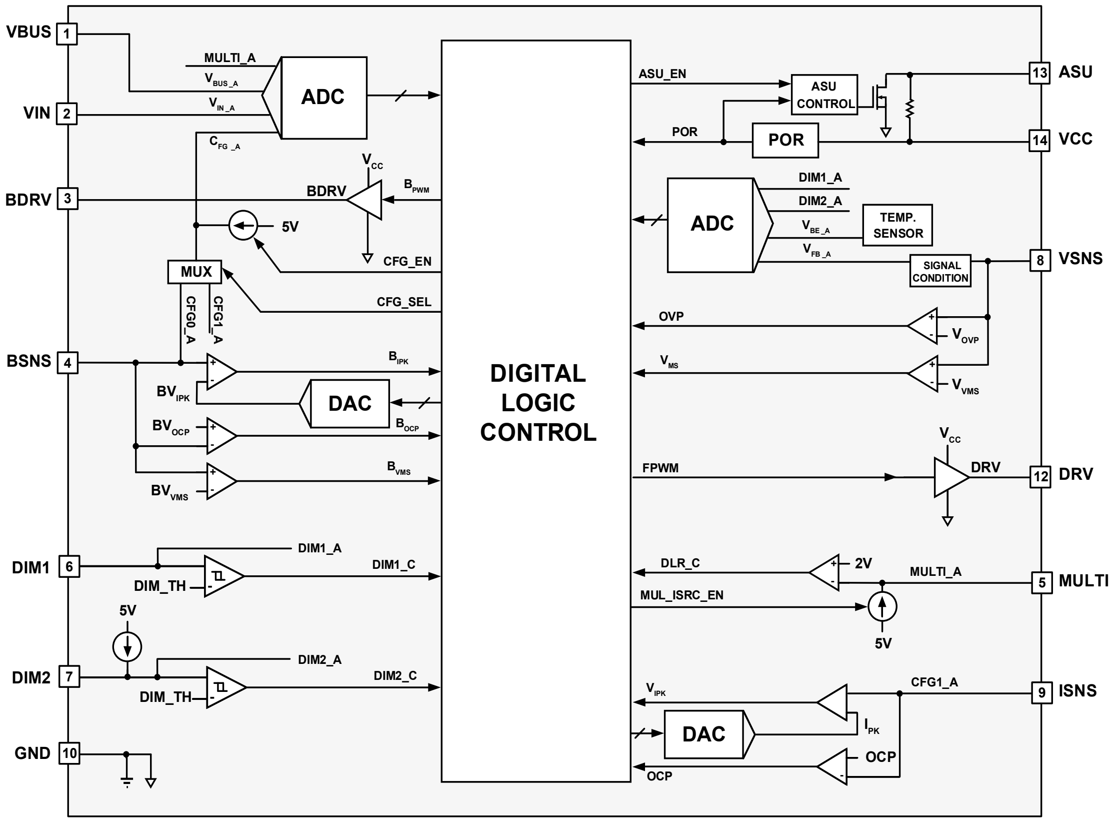


Figure 1. iW3700 Functional Block Diagram

1.2 Typical Application

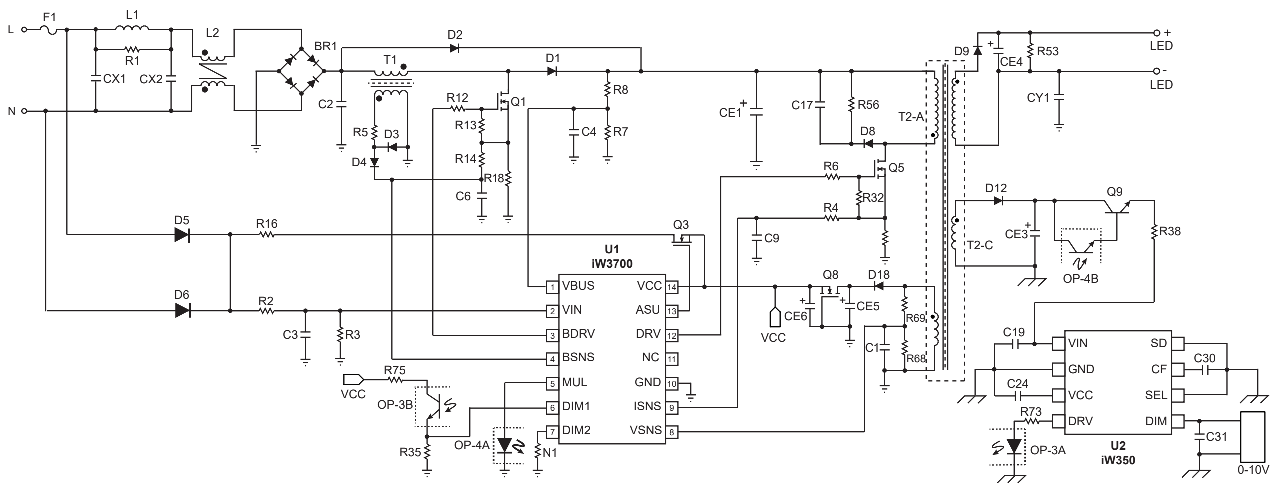


Figure 2. Typical Application for 2-Stage 0-10V Dimmable Driver with iW350

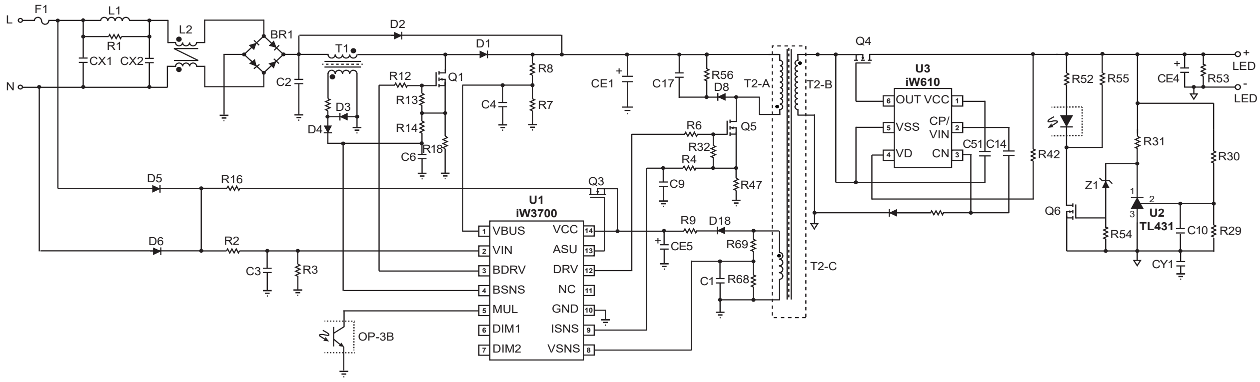


Figure 3. Typical Application for 2-Stage LED Light Stripe Driver with TL431 and iW610

2. Pin Information

2.1 Pin Assignments

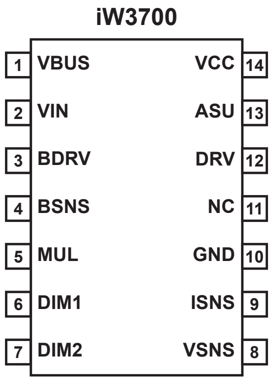


Figure 4. Top View

2.2 Pin Description

Pin Number	Pin Name	Type	Description
1	VBUS	Analog in	PFC output DC bus sensing
2	VIN	Analog in	AC line voltage sensing
3	BDRV	Analog out	PFC boost power MOSFET driver
4	BSNS	Analog in	PFC boost current and inductor sensing
5	MUL	Analog I/O	Multi-function pin depending on configuration
6	DIM1	Analog in	Dimming 1 input pin
7	DIM2	Analog in	Dimming 2 input pin
8	VSNS	Analog in	Flyback output voltage and transformer sensing
9	ISNS	Analog in	Flyback current sensing
10	GND	Ground	Ground reference
11	NC	Not connect	Not connected
12	DRV	Analog out	Flyback power MOSFET driver
13	ASU	Analog out	Active startup control
14	VCC	Power	IC power

3. Specifications

3.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Symbol	Minimum	Maximum	Unit
Continuous DC Supply Current at VCC pin	I_{VCC}		20	mA
VCC pin	V_{VCC}	-0.3	20	V
VBUS pin	V_{VBUS}	-0.3	5.5	V
VIN pin	V_{VIN}	-0.3	5.5	V
BDRV pin	V_{BDRV}	-0.3	20	V
BSNS pin	V_{BSNS}	-0.3	5.5	V
MUL pin	V_{MUL}	-0.3	5.5	V
DIM1, DIM2 pin	V_{DIM}	-0.3	5.2	V
VSNS pin	V_{VSNS}	-0.8	5.5	V
ISNS pin	V_{ISNS}	-0.3	5.5	V
DRV pin	V_{DRV}	-0.3	20	V
ASU pin	V_{ASU}	-0.3	20	V
Maximum Junction Temperature	T_{JMAX}	-40	150	°C
Maximum Storage Temperature Range	T_{STG}	-65	150	°C
ESD Rating		**Value**		**Unit**
Human Body Model (Tested per JS-001-2017)		±2		kV
Latch-Up (Tested per JESD78E; Class 2, Level A)		±100		mA

3.2 Thermal Specifications

Thermal Resistance (Typical)	θ_{JA} (°C/W) [1]
14-Led SOIC Package	45

3.3 Electrical Specifications

V_{VCC} = 18V, T_A = 25°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VBUS pin						
VBUS startup voltage low limit (Note 1)	$V_{VBUS\_ST(MIN)}$			0.708		V
VBUS startup voltage high limit (Note 1)	$V_{VBUS\_ST(MAX)}$			0.762		V
VBUS OVP voltage (Note 1)	V_{VBUS_OVP}			3.042		V
VBUS UVP voltage (Note 1)	V_{VBUS_UVP}			0.531		V
VIN Pin						
VIN brown out voltage (Note 1)	V_{VIN_BROUT}	Peak of AC		0.708		V
VIN turn off voltage (Note 1)	V_{VIN_OFF}	Continuous for 10ms		0.27		V
VIN startup voltage low limit (Note 1)	$V_{VIN\_ST(MIN)}$	Peak of AC		0.762		V
VIN startup voltage high limit (Note 1)	$V_{VIN\_ST(MAX)}$	Peak of AC		2.958		V
VIN OVP voltage (Note 1)	V_{VIN_OVP}	Peak of AC		2.718		V
VIN OVP recovery voltage (Note 1)	$V_{VIN\_OVP\_REC}$	Peak of AC		2.688		V
BDRV pin						
Driver high level (Note 1)	$V_{BDRV(HIGH)}$			V_{VCC}-0.2		V
Driver low level (Note 1)	$V_{BDRV(LOW)}$			0.2		V
Driver source impedance	B_{DRV_ISRC}	CL = 470pF		30	45	Ω
Driver sink impedance	B_{DRV_ISINK}	CL = 470pF		8	16	Ω
BSNS pin						
Boost I_{PK} regulation high limit (Note 1)	$B_{VIPK(MAX)}$			1.022		V
Boost I_{PK} regulation low limit (Note 1)	$B_{VIPK(MIN)}$			0.02		V
Boost OCP threshold	B_{OCP}	T_A = 25°C, pos edge	1.74	1.8	1.84	V
Configuration 0 current	I_{CFG_0}		459	500	534	µA
MUL pin						
MUL current source drive current	I_{MUL}		183	200	214	µA
MUL DLR comparator threshold	V_{DLR_C}	T_A = 25°C, neg edge	1.94	2	2.06	V
NTC minimum startup voltage (Note 1)	$NTC_{\_ST(MIN)}$			0.344		V
NTC de-rating start voltage (Note 1)	$NTC_{\_DERATING(ST)}$			0.625		V
NTC thermal shutdown voltage (Note 1)	$NTC_{\_OTP}$			0.296		V
DIM1, DIM2 pin						
Analog DIM 0% threshold (Note 1)	$V_{DIM\_ANA(MIN)}$			0.337		V
Analog DIM 100% threshold (Note 1)	$V_{DIM\_ANA(MAX)}$			2.73		V
PWM DIM high level threshold	$V_{DIM\_L\_TO\_H}$		2.44	2.5	2.56	V
PWM DIM low level threshold	$V_{DIM\_H\_TO\_L}$		1.45	1.5	1.55	V
Light off DIM % threshold (Note 1)	$L_{\_OFF\_TH}$			0.0625		%
Light on DIM % threshold (Note 1)	$L_{\_ON\_TH}$			0.3125		%
DIM2 current source	I_{DIM2}		92	100	107	µA

3.3 Electrical Specifications (Continued)

V_{VCC} = 18V, T_A = 25°C, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VSNS pin						
VSNS CV regulation target (Note 1)	V_{SNS_CV}			2.688		V
VSNS light-off regulation target (Note 1)	V_{SNS_LO}	-00 and -30 Options		0.44		V
		-20 and -21 Options		0.672		V
VSNS short threshold (Note 1)	V_{OSP}			0.282		V
V_{OVP} threshold	V_{OVP}		3.11	3.2	3.25	V
ISNS pin						
ISNS regulation high limit (Note 1)	$V_{ISNS(MAX)}$			1.022		V
ISNS regulation low limit (Note 1)	$V_{ISNS(MIN)}$			0.08		V
OCP threshold	$V_{ISNS(OCP)}$	T_A = 25°C, pos edge	1.73	1.8	1.84	V
DRV pin						
Driver high level (Note 1)	$V_{DRV(HIGH)}$			V_{VCC}-0.2		V
Driver low level (Note 1)	$V_{DRV(LOW)}$			0.2		V
Driver source impedance	$DRV_{\_ISRC}$	CL = 470pF		30	47	Ω
Driver sink impedance	$DRV_{\_ISINK}$	CL = 470pF		8	15	Ω
VCC pin						
Startup voltage	$V_{VCC(ST)}$		15.9	17	18.1	V
Under voltage lock out	$V_{VCC(UVLO)}$		7.9	8.8	9.7	V
VCC high voltage threshold	$V_{VCC(HIGH)}$		15.9	16.5	17	V
VCC low voltage threshold	$V_{VCC(LOW)}$		8.9	9.3	9.5	V
Leakage current before POR	$I_{VCC(LK)}$	V_{VCC} = 15V, before POR		30	59	µA
Quiescent current after POR	I_{VCCQ}	Without driver switching		2.5	4.3	mA
Temperature Sensor						
Over temperature threshold (Note 1)	T_{OTP}			150		°C
Max startup Temperature (Note 1)	$T_{ST(MAX)}$			120		°C

1. These parameters are not 100% tested. They are guaranteed by design.

4. Typical Performance Graphs

T_A = 25°C, unless otherwise specified.

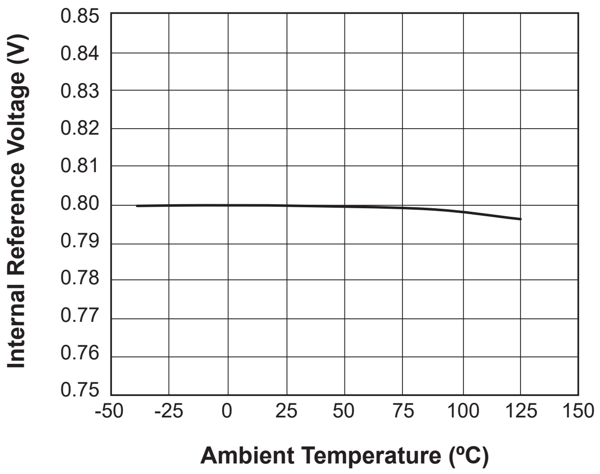


Figure 5. Internal Reference Voltage vs. Ambient Temperature

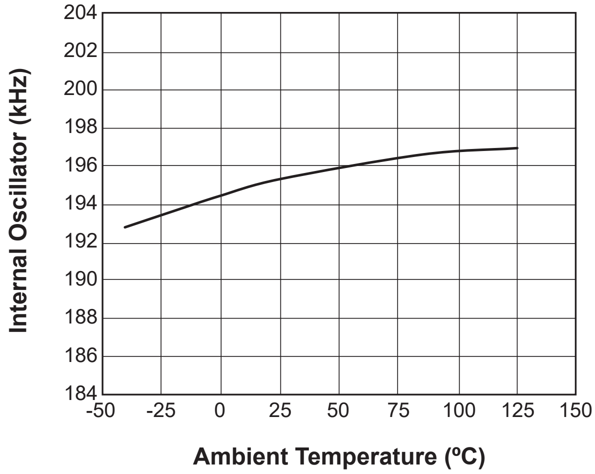


Figure 6. Internal Clock Frequency vs. Ambient Temperature

5. Application Information

The PFC boost stage of the iW3700 operates in critical discontinuous conduction mode (CDCM) at heavy load and discontinuous mode (DCM) at medium to light load. The flyback stage of the iW3700 also operates in CDCM at high dimming or heavy load and DCM at low dimming or medium to light load. The boost stage and flyback stage operate independently except both stop at same time during fault conditions.

The iW3700 monitors the DIM1 and DIM2 signals and delivers the output current (I_{OUT}) percentage accordingly in real time. If the duty received is lower than $L_{\_OFF\_TH}$ the iW3700 will go into light-off mode and keeps the output voltage (V_{OUT}) below the LED forward voltage while sustaining V_{VCC} by the auxiliary winding of the flyback.

5.1 Pin Detail

Pin 1 – VBUS

VBUS pin is the feedback sensing pin of the PFC boost output for V_{VBUS} voltage regulation. With standard scaling ratio, V_{VBUS} is regulated at 1.23*AC RMS voltage plus 75V. The maximum V_{VBUS} voltage is 420V while the minimum V_{VBUS} voltage is 250V. The VBUS pin is recommended to connect with a resistor divider of standard scaling ratio of 151.

Pin 2 – VIN

VIN pin is the sensing pin of the AC line voltage. VIN is used for both PFC function and AC voltage qualification. The VIN pin should be connected to the line voltage before the bridge rectifier to see the true AC voltage. It is also recommended to connect to the input voltage with a resistor divider of standard scaling ratio of 151.

Pin 3 – BDRV

BDRV pin is the power MOSFET gate drive pin of the boost PFC stage. The BDRV pin connects to the power MOSFET gate with either of the commonly used fast turn-off circuits, whether a diode of PNP transistor.

Pin 4 – BSNS

BSNS pin has three functions. The first function is the peak current regulation of the boost PFC MOSFET. During PFC MOSFET turn on, the BSNS voltage linearly ramps up until the target peak current is reached. The iW3700 then turns off the PFC MOSFET. The second function is sensing the PFC inductor reset and subsequent resonant “valley” used for CDCM and DCM for quasi-resonant switching. The third function is the configuration of the boost PFC turn on/off load percentage threshold in CV mode with R14 in Figure 2.

Table 5.1 BSNS Configuration

CFG Setting	Recommend Resistance	PFC Turn On/Off load % in CV
1	0.75kΩ	16% / 12%
2	1.5kΩ	21% / 17%
3	2.5kΩ	31% / 27%
4	3.6kΩ	PFC always on

Pin 5 – MUL

MUL is the multi-function pin. Depending on the I_{SNS} configuration (see ISNS pin for details), it performs different functions.

- NTC de-rating function: connect a 100kΩ NTC thermistor for over temperature de-rating. (See section 5.8 for details)
- iW350 control function: connect to the LED side of an optocoupler to control the power supply of the iW350 interface chip (see Figure 2). If the iW3700 is at no load (LED open) condition, the power supply of the iW350 is cut off to reduce power loss and minimize the cross-regulation and prevent V_{OUT} losing regulation, as the iW350 is powered by another auxiliary winding of the flyback transformer.
- The TL431 feedback function: connect to the collector side of an optocoupler to receive the feedback signal from TL431 circuit for CV mode dynamic load response (DLR) enhancement (see Figure 3). At no

load condition, when a heavy load is suddenly applied, the iW3700 is not able to detect the V_{OUT} drop due to primary side sensing (PSR) limitation. The TL431 circuit, which sits on V_{OUT} side, sends out a signal to notify the iW3700 of the load change so it can respond accordingly.

Pin 6, 7 – DIM1 and DIM2
DIM1 and DIM2 pins are used to set the output current percentage of the iW3700. The current output % = DIM1% x DIM2%. For example, if received PWM duty signal is 50% on both DIM pins, the output current % is 50% * 50% = 25%.

Both DIM1 and DIM2 can accept the PWM duty signal or analog voltage level signal. For the PWM duty signal, it is required to be either 3.3V or 5V logic level with the frequency within 150Hz to 4kHz for optimized performance. For analog level signal, 0-$V_{DIM\_ANA(MIN)}$ maps to 0% output; $V_{DIM\_ANA(MAX)}$ or above maps to 100% output; $V_{DIM\_ANA(MIN)}$ to $V_{DIM\_ANA(MAX)}$ maps linearly from 0-100% dimming %.

DIM2 pin internally has an accurate 100µA current source for resistor current-set or dimming application. DIM2 voltage is equal to 100µA multiplied by the external resistance.

The iW3700 has comprehensive logic to automatically determine whether it is PWM duty signal type or analog level signal type at startup if the PWM duty signal is within the spec mentioned above.

Pin 8 – VSNS
VSNS pin is used for indirect V_{OUT} sensing by the auxiliary winding, as well as flyback transformer reset and subsequent resonant "valley" sensing. With Rensas' patented ***PrimAccurate*** technology, the iW3700 is able to sense V_{OUT} accurately across input and load condition. The transformer reset and valley information is used for CDCM and DCM quasi-resonant operation.

Pin 9 – ISNS
ISNS pin has two functions. The first is for flyback MOSFET current sensing. When the flyback MOSFET is on, the voltage on ISNS pin ramps up linearly. When the target peak current is reached, the iW3700 will turn off the flyback MOSFET. The second function is for configuration of the MUL pin function with R4 in Figure 2.

Table 5.2 ISNS Configuration

CFG Setting	Recommend Resistance	MUL Function
1	0.75kΩ	NTC I_{OUT} De-rating
2	1.5kΩ	iW350 Control
3	2.5kΩ	TL431 Feedback
4	3.6kΩ	Not Used

Pin 10 – Ground
Ground reference.

Pin 11 – NC
Not connected.

Pin 12 – DRV
DRV pin is the power MOSFET gate drive pin of the flyback stage. DRV pin connects to the power MOSFET gate with either of the commonly used fast turn-off circuits, whether a diode or PNP transistor.

Pin 13 – ASU
ASU is the active startup pin for fast power-on when AC is connected. ASU pin should connect to the gate of a high voltage depletion MOSFET (DFET) to achieve the fast startup function. The source of the DFET connects to the VCC pin via a resistor or a diode. The drain of the DFET should connect to AC voltage via startup resistors.

Pin 14 – VCC
VCC pin is the power source of the iW3700. For most of the LED driver applications which require supporting a wide V_{OUT} range, which causes a wide auxiliary winding voltage range, an external LDO is required to keep V_{VCC} voltage below 16V. To make sure V_{VCC} does not drop below UVLO during startup process, a 47µF or bigger V_{VCC} capacitor is required. A 0.1µF ceramic de-coupling cap is also required to be placed close to VCC pin.

5.2 Operational Cycle and States

Before POR, the ASU pin is connected to VCC pin internally. As a result, the external high voltage depletion mode FET (DFET) (Q3 in Figure 2) is in "on" state with its gate and source at equal voltage. When AC is applied, the V_{VCC} is charged by the DFET via the AC line voltage. When V_{VCC} reaches POR voltage, the iW3700 enables and pulls the ASU pin to ground. As a result the DFET $V_{GS} = -V_{VCC}$ and is turned off and V_{VCC} stops being charged from AC line by DFET.

After POR, the iW3700 enters the qualification state. The qualification state checks:

1. Whether the peak of AC voltage is within $V_{VIN\_ST(MAX)}$ and $V_{VIN\_ST(MIN)}$
2. Whether the V_{VBUS} voltage is within $V_{VBUS\_ST(MAX)}$ and $V_{VBUS\_ST(MIN)}$
3. Whether the Internal temperature sensor is below $T_{ST(MAX)}$
4. Whether the NTC voltage is above $T_{NTC\_ST(MIN)}$ if NTC function is selected

For the V_{VIN} check, the iW3700 needs to wait 12ms to ensure the peak of AC voltage appears for detection. If the qualification passes, the iW3700 enters startup state. If the qualification fails, the iW3700 waits until V_{VCC} drops to UVLO and reaches another POR for a new qualification cycle.

During startup state, the flyback stage uses a fixed frequency, fixed peak current (I_{PK}) switching scheme to raise the output voltage until VSNS pin can reliably detect V_{OUT} and valley. There are five sub-states within the startup state, each sub-state increases I_{PK} and/or increases the switching frequency to delivery more energy. At any moment if VSNS > V_{OSP} for a few PWM switching cycles, the iW3700 exits startup state and enters CC or light-off state depending on DIM1 and DIM2 condition.

In the CC state, the iW3700 outputs well-regulated output current percentage (I_{OUT}%) based on the signal received at DIM1 and DIM2 pins across supported AC input range and V_{OUT} range. However, if at any time the output voltage equals or exceeds the CV voltage reference due to load condition, the iW3700 transitions to CV state to keep output voltage regulated. In CV state, the actual I_{OUT}% is lower than the command from DIM1 and DIM2 pins. If the output voltage drops below the CV reference with I_{OUT}% dictated by DIM1 and DIM2, the iW3700 goes back to CC state and regulates the I_{OUT}% based on DIM1 and DIM2 again. PFC is always on in CC state regardless of I_{OUT}% while PFC is turned off when I_{OUT}% is below a certain threshold in CV state based on configuration.

If at any time, the DIM1 or/and DIM2 pin detects a light-off dimming command input, the iW3700 enters light-off mode. In the light-off mode, the iW3700 regulates V_{OUT} at V_{SNS_LO} to keep the IC powered while keeping V_{OUT} < LED forward voltage to avoid lighting up. If at any time, DIM1 and DIM2 detects a duty greater than L_{ON_TH}, the iW3700 enters CC state again. PFC is turned off in light-off state for lower power consumption.

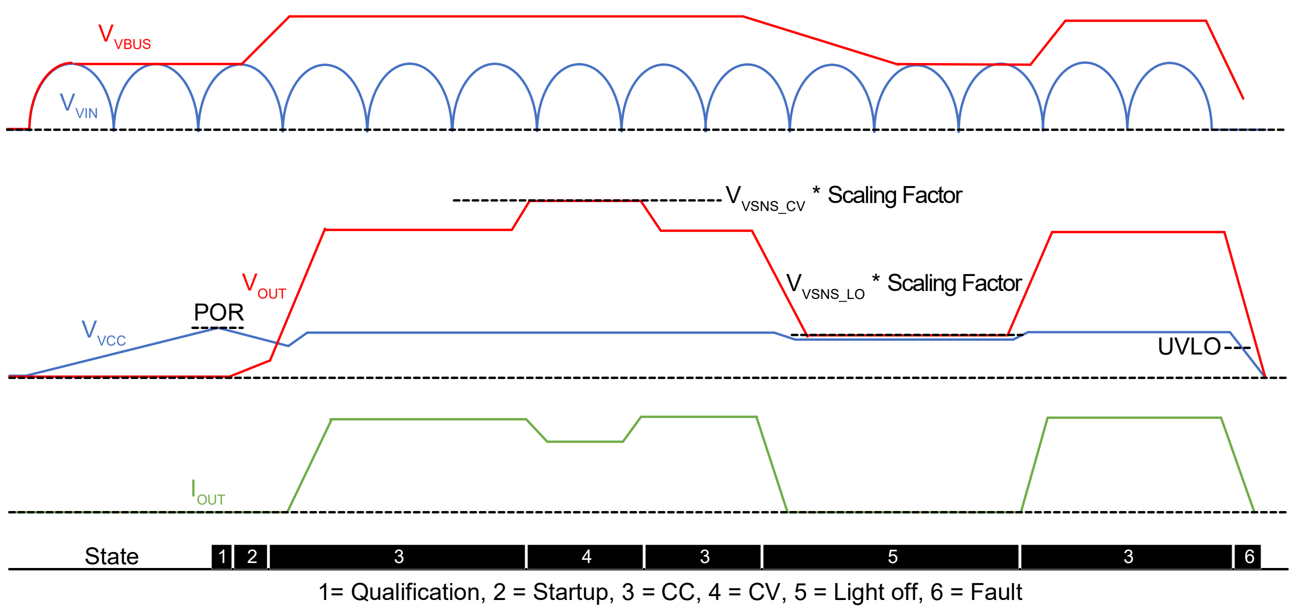


Figure 7. Operation Cycle of the iW3700

When the AC input, output, external component value or thermal condition does not meet the operating criteria, the iW3700 enters the fault state. Once in fault state, the iW3700 resets itself. Depending on the fault type, the iW3700 restarts and enter qualification state again immediately if the fault is not critical such as V_{VIN} brown out. If the fault is critical such as OVP, OSP, the iW3700 enters wait state, enabling Smart Hiccup mode, which extends the time interval between startup attempts. When the wait state expires, the iW3700 enters qualification state for a new startup attempt. Detailed information can be found in section 5.7.

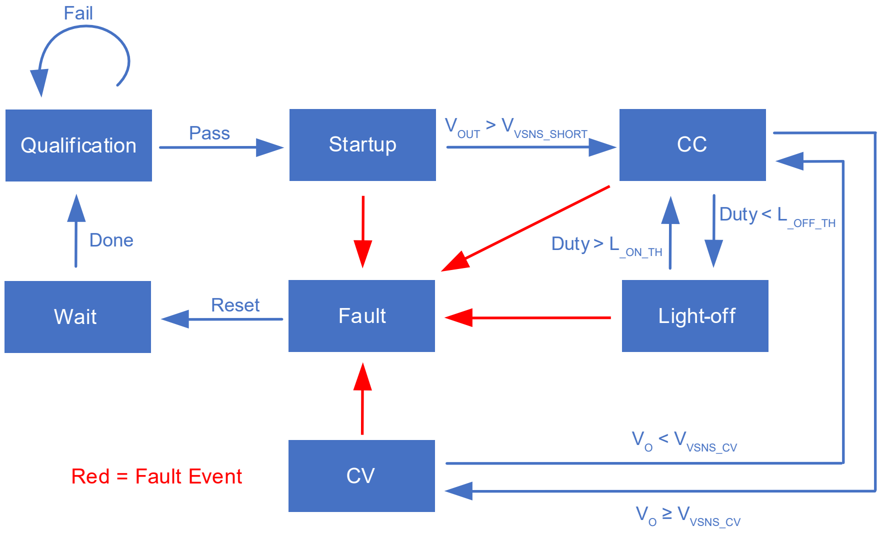


Figure 8. Main States of iW3700 Operation

5.3 Dimming Signal Processing

The iW3700 can accept both PWM signal and analog voltage level signal as command to control the I_{OUT} %. At startup, the iW3700 detects which signal type it is and responds accordingly. By default, the iW3700 assumes the dimming signal input is an analog level until it sees consistent PWM style switching.

The specification and mapping of accepted analog level signal and PWM duty signal are described in detail in section 5.1, in the DIM pins detailed information. The I_{OUT} % = DIM1% x DIM2% then rounded to the closest 0.0625% step.

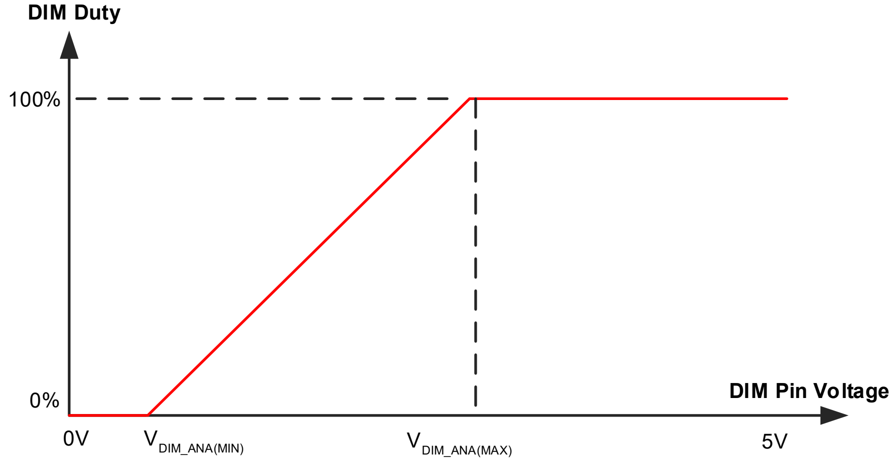


Figure 9. Analog Level Signal vs. DIM% Mapping

For the special case of 100% duty or 0% duty of PWM signal, both are essentially an “analog voltage level”. Therefore, PWM = 1 voltage level must > 3.3V * 95% = 3.13V and PWM = 0 voltage level must < 3.3V * 5% = 165mV. This definition is compatible with analog voltage level signal’s 100% and 0% respectively.

A hysteresis of signal detection is built-in for noise immunity so that the I_{OUT}% does not change due to the noise on DIM1 and DIM2 pin. DIM1 pin has a hysteresis of ±0.1% duty for PWM dimming signal and ±0.5% level (±12mV) for analog dimming signal; DIM2 pin has a hysteresis of ±0.05% duty for PWM dimming signal and ±0.5% level (±12mV) for analog dimming signal.

5.4 LED Current Regulation

The iW3700 regulates the output current indirectly from primary side using Renesas' patented ***PrimAccurate*** technology. For the Flyback converter working in DCM or CDCM, the equation for I_{OUT} is:

$$I_{OUT} = 0.5 \times N_{PS} \times \frac{V_{IPK}}{R_S} \times \frac{T_R}{T_P} \times \eta \qquad (5.1)$$

In which N_{PS} is the turns ratio between primary and secondary winding, R_S is the current sense resistor value, V_{IPK} is the voltage drop on R_S proportional to primary-side peak current which can be detected on the ISNS pin. T_R is the flyback transformer reset time, T_P is the period of the PWM switching frequency and η is the flyback efficiency.

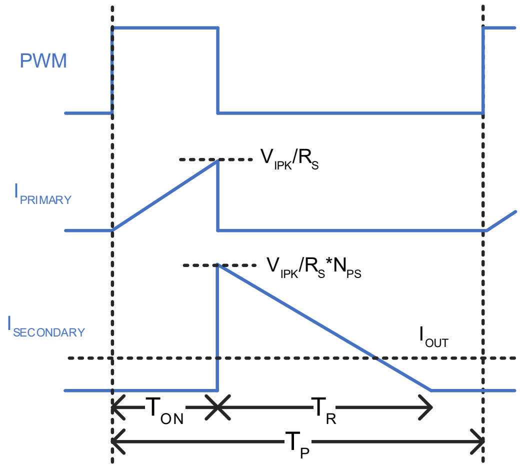


Figure 10. Primary-Side Current Estimation

Equation 5.1 can be re-arranged to solve for V_{IPK} and its relationship to I_{OUT} regulation if other variables are know, which is implemented in the iW3700

$$V_{IPK} = 2 \times I_{OUT} \times \frac{R_S}{N_{PS}} \times \frac{\frac{T_P}{T_R}}{\eta} \qquad (5.2)$$

In which N_{PS}, R_S and η are fixed to a specific application design. T_P is internally pre-defined in the iW3700 based on I_{OUT}% to optimize for efficiency at different loading. To accommodate wide V_{VBUS} and wide V_{OUT} ranges which result in wide operating range, the iW3700 does not regulate the absolute T_P. Instead, it regulates the relative T_P = k * (T_{ON} + T_R). Figure 11 shows the targeted k curve of T_P vs. I_{OUT}%. For EMI and efficiency purpose, the actual T_P ends at the next "valley" of the resonance after the T_P target is achieved, also known as quasi-resonant switching when I_{OUT}% > 15%.

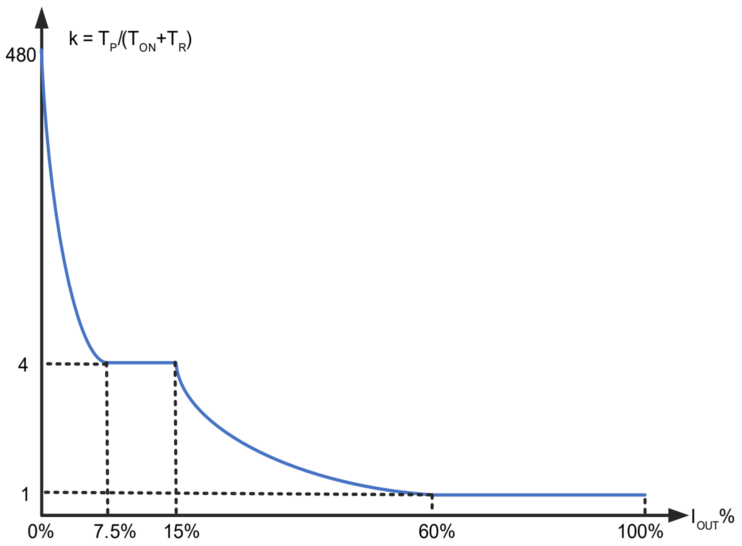


Figure 11. Targeted k Curve of T_P vs. I_{OUT}%

It is worth noting that in the equation 5.2, N_{PS}, efficiency and R_S can be normalized out when converting V_{IPK} vs. absolute I_{OUT} into V_{IPK} vs. I_{OUT}%. However, T_R, T_P are related to real-time V_{VBUS}, V_{OUT} as well as L_M/R_S ratio of the application. As a result, the V_{IPK} vs. I_{OUT}% curve is adaptive to V_{VBUS}, V_{OUT} and L_M/R_S.

5.5 Constant Voltage Regulation and Constant Power Limit

In case of LED-open or too many LEDs connected to the output, the iW3700 enters CV mode and regulates the output voltage proportional to V_{SNS_CV}. This avoids the over-voltage under LED-open or too many LED conditions. The I_{OUT}% in CV mode is determined by the common proportional-integration (PI) feedback loop. The feedback loop gets V_{OUT} information from the VSNS pin, internally named as V_{FB}. V_{VSNS} is sampled at a fixed time before the V_{VSNS} signal falling edge to minimize the impact from the secondary-side current variation. The V_{FB} is held until next sampling time.

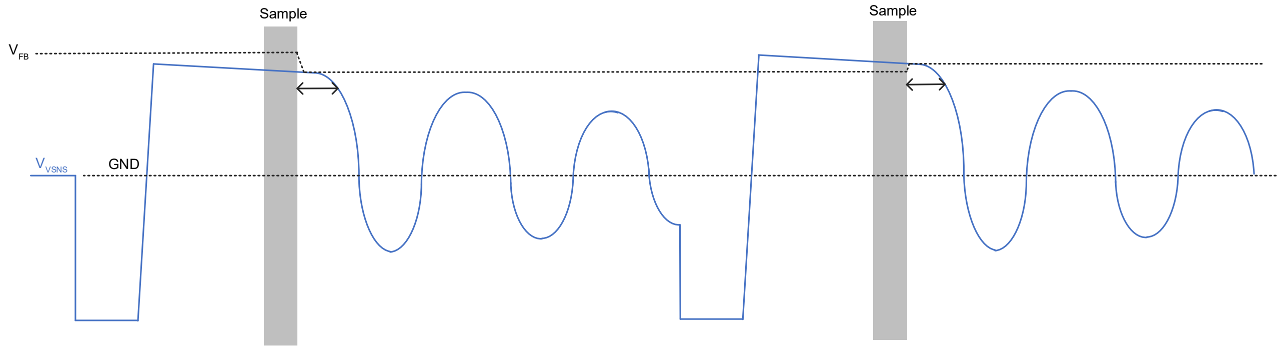


Figure 12. V_{OUT} Sensing from the Primary Side

The V_{FB} signal is compared with V_{VSNS_CV}, generating an error signal and determines I_{OUT}% to keep $V_{FB} = V_{VSNS\_CV}$. In case the feedback loop gives I_{OUT}% higher than dimming duty from DIM1 and DIM2 pin, the iW3700 goes back to CC mode and I_{OUT}% is determined by dimming duty again.

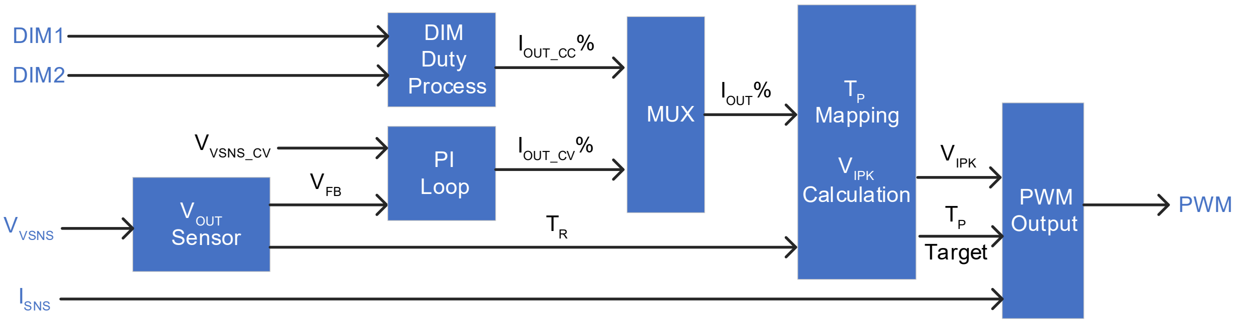


Figure 13. Output Control Flow

Based on the V_{OUT} and I_{OUT} regulation profile of the iW3700, it can tell that the maximum power output point is when V_{OUT} is equal to CV reference, which is proportional to V_{VSNS_CV} and with I_{OUT} = 100%. In some applications, it is desired to keep the output power constant and not keep increasing when V_{OUT} is higher than a defined % of CV reference. In the iW3700-3X, a constant power (CP) limit is imposed to achieve such target. The CP entry point is a percentage of CV reference, which is determined by the last digit of the part number. For example, iW3700-30 enters the CP point at 90% of CV reference.

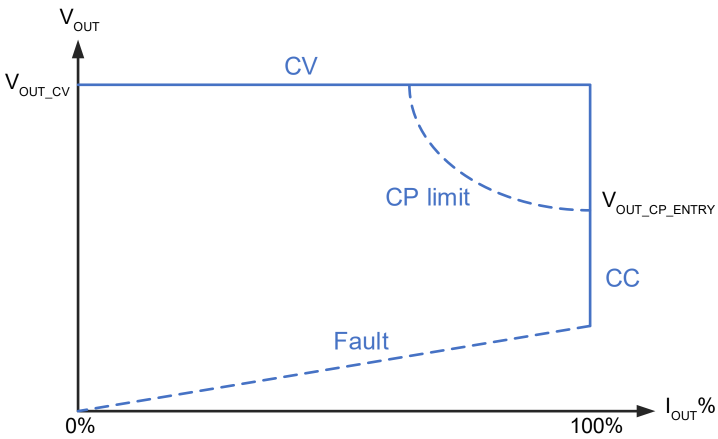


Figure 14. V_{OUT}, I_{OUT} Regulation Profile and CP Limit

5.6 Boost PFC Stage

The boost stage of the iW3700 serves as the integrated PFC function to help iW3700 applications to meet PF, THD and individual harmonic requirements. The output of the boost is the input of the flyback. A bus capacitor (CE1 in Figure 2) is used for energy buffering. The boost stage is relatively independent from the flyback stage with its own feedback loop and operation modes.

The boost PFC is on when the iW3700 is in startup, CC and CV mode (when load is higher than certain %, see configuration for details); The boost PFC is off when the iW3700 is in qualification, light-off, fault and CV mode (when load is lower).

To achieve overall optimized efficiency of both stages, the V_{VBUS} regulation target (V_{VBUS_REF}) is a function of the AC voltage with min and max clamping. Figure 15 shows the relationship between V_{VBUS} and V_{VIN} (see section 5.1 for details).

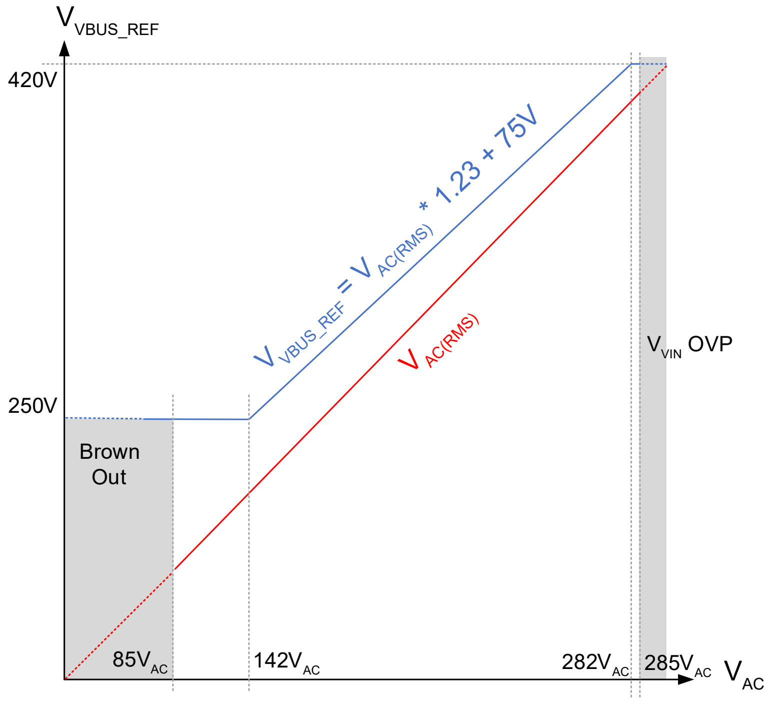


Figure 15. V_{VBUS_REF} vs. V_{AC} (RMS)

5.6.1 PFC Sensing

There are three sensing pins related to the boost operation: VIN, VBUS and BSNS. The VIN pin is used for shaping the AC current and achieving the PFC function. The VBUS pin is used to sense the bus voltage for closed loop control. The BSNS pin is a used to sense both PFC MOSFET peak current (I_{PK}) as well as PFC inductor reset and resonance valley after reset to achieve CDCM and DCM with quasi-resonant switching.

During PFC MOS on time, the auxiliary winding of the PFC inductor is reverse biased. As a result, the auxiliary winding signal is blocked by the diode (D1 in Figure 16). At the same time, I_{PK} linearly ramps up and the BSNS pin can detect the voltage drop on R_{S_BOOST}, which is proportional to I_{PK} via CFG resistor (R1 in Figure 16) for peak current control.

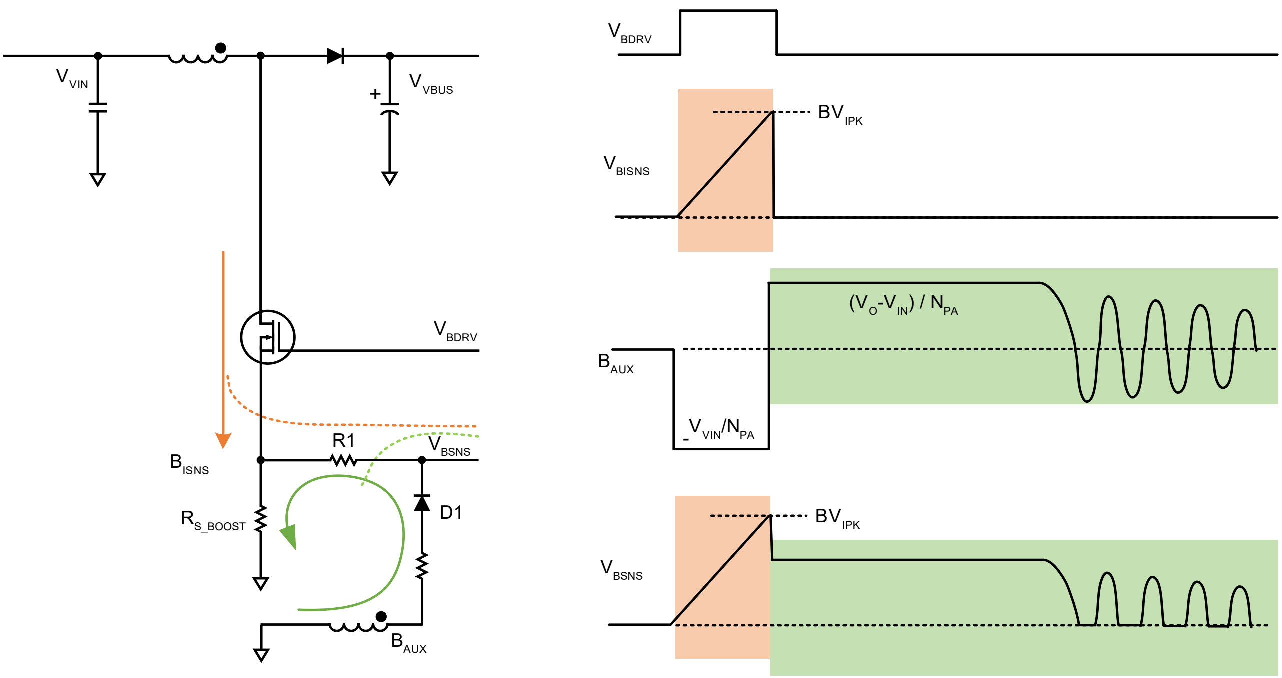


Figure 16. Time Multiplex Sensing of BSNS pin

During PFC MOS off time, the voltage-drop on R_{S_BOOST} is 0 as the MOSFET is off. The auxiliary winding of the PFC inductor is forward biased. As a result, the voltage on BSNS pin is approximately the scaled version of boost auxiliary winding which carries the boost inductor reset and resonance valley information.

Based on the detected B_{SNS} signal, valley mode switching can be achieved to optimize the efficiency and EMI for Boost PFC stage.

Boost PFC stage will enter the burst mode for the lightest load and no-load conditions. In this mode the boost PFC is turned on and off based on power balancing to keep V_{VBUS} voltage regulated.

Step 1: When the PFC feedback loop gives a power % that is lower than 1.5%, the PFC is turned off.

Step 2: After PFC is off, the V_{VBUS} voltage will drop due to loading from flyback.

Step 3: When V_{VBUS} drops below V_{VBUS_REF}, the feedback loop will ramp up the power %.

Step 4: When power % is higher than 1.6%, the PFC starts operating again and boost up V_{VBUS}.

Step 5: As V_{VBUS} rises above V_{VBUS_REF}, the feedback loop will reduce power % and goes back to step 1.

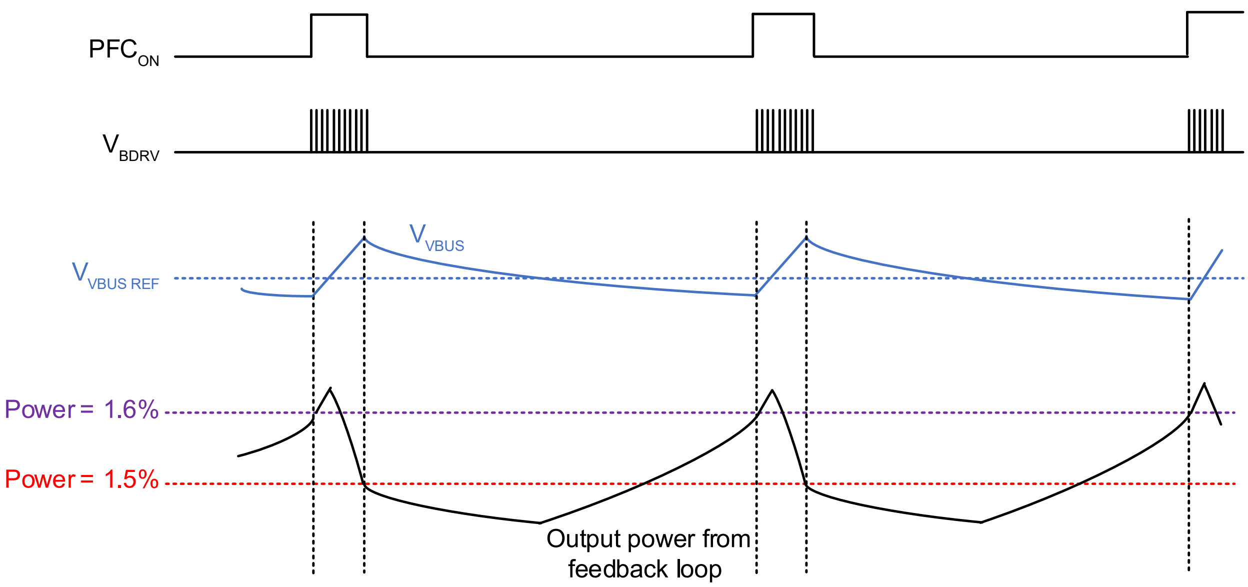


Figure 17. Burst Mode of PFC

5.6.2 PFC Peak Current Regulation

To achieve good PF, the AC current must be proportional to the AC voltage sinusoidal shape waveform. In a DCM or CDCM boost converter, the input AC current equation is:

$$I_{AC} = 0.5 \times \frac{V_{IPK}}{R_{S\ BOOST}} \times \frac{(T_{ON} + T_R)}{T_P} \qquad (5.3)$$

To make it proportional to AC line voltage, I_{AC} should proportional to V_{VIN}

$$I_{AC} = k \times V_{VIN} = 0.5 \times \frac{V_{IPK}}{R_{S\ BOOST}} \times \frac{(T_{ON} + T_R)}{T_P} \qquad (5.4)$$

In which k is a constant for a given AC RMS voltage and given output power % operating point. Combine all fixed values into k and makes it another constant k1:

$$V_{IPK} = \frac{T_P}{(T_{ON} + T_R)} \times k1 \times V_{VIN} \qquad (5.5)$$

In equation 5.5, T_P is determined by the iW3700 as described in 5.6.4, V_{VIN}, T_{ON} and T_R can be measured by VIN pin, BDRV and BSNS pins. As a result, V_{IPK} of the boost at a given AC RMS voltage and given output power % can be derived.

5.6.3 PFC Dynamic Load Handling

The feedback loop for any PFC controller is inherently slow due to PFC function. It is normally designed to have bandwidth from 1Hz ~ 10Hz for stable operation. Therefore, non-linear handling is necessary to help the V_{VBUS} regulation during fast dynamic load transient.

In the case of light load to heavy load step, V_{VBUS} will dip. When the iW3700 detects the V_{VBUS} voltage is lower than $V_{DLR\_HI\_ENTER}$, the boost immediately increases the output to 100% of the power to stop the V_{VBUS} from dropping. As a result, the V_{VBUS} rises and once it reaches $V_{DLR\_HI\_EXIT}$, the boost is back to output the power % based on feedback loop again. During 100% power period, feedback loop continues to function as normal while its command is not being used.

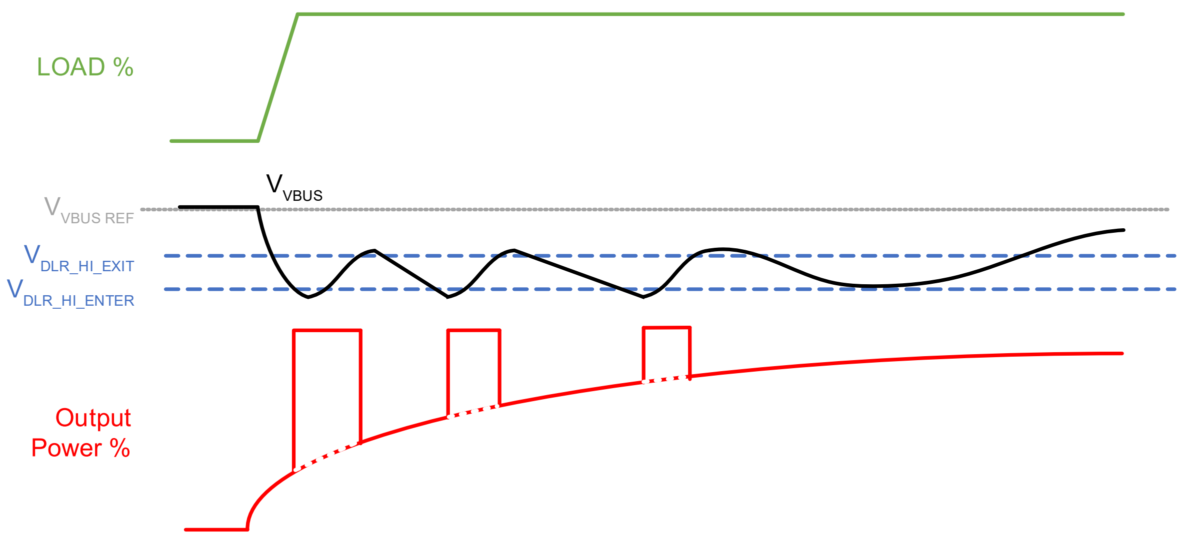


Figure 18. DLR Handling Light Load to Heavy Load

In the case of heavy load to light load jump, V_{VBUS} will overshoot. When the iW3700 detects the V_{VBUS} voltage higher than $V_{DLR\_LOW\_ENTER}$, the boost immediately reduces the output to 0% of the power to stop the V_{VBUS} from rising. As a result, the V_{VBUS} drops and once it reaches $V_{DLR\_LOW\_EXIT}$, the boost will be back to output the power % based on feedback loop again. During 0% power period, feedback loop continues functions as normal while its output is not being used.

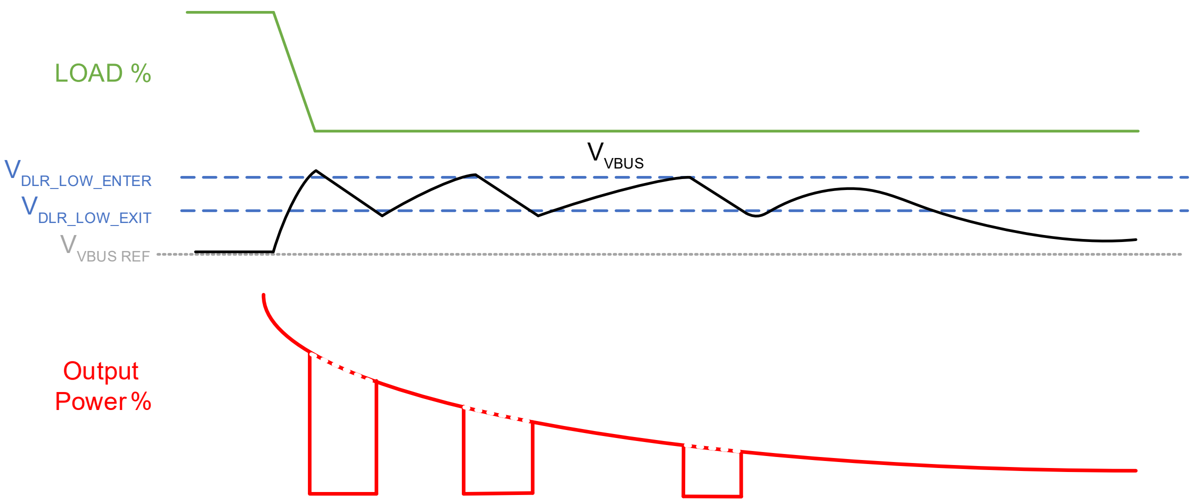


Figure 19. DLR Handling Heavy Load to Light Load

5.6.4 PFC DC Input EMI Dithering

In the case of DC input, V_{VIN} is flat. As a result, the peak current (I_{PK}) of the boost and switching period (T_P) are constants in steady state. This may cause a high tone at the harmonics frequency of switching frequency on EMI spectrum which is undesired. To spread out the tone, a dithering of boost B_{VIPK} is enabled when DC input is detected.

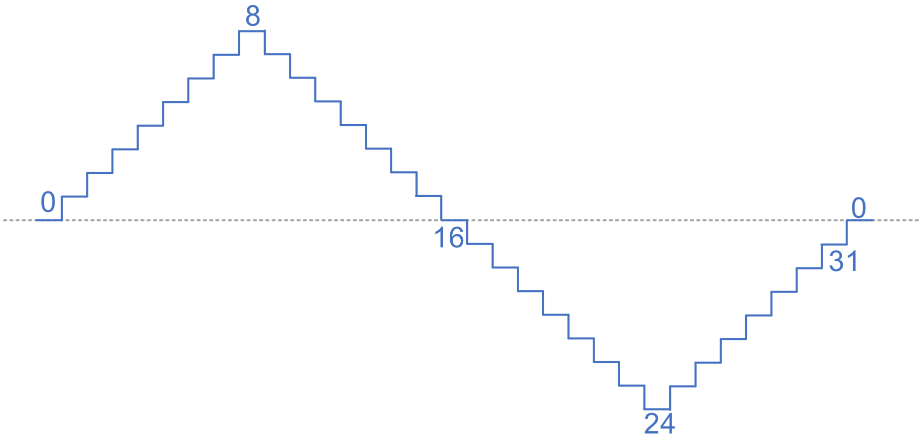


Figure 20. V_{IPK} of Boost Dithering Under DC Input

The dithering is implemented in a cycle of 32 boost switching cycles. From switching cycle 1 to 8, the B_{VIPK} of boost increases 1/64 of its value each cycle. From switching cycle 9 to 24, the B_{VIPK} of the boost decreases 1/64 of its value each cycle. From switching cycle 24 to 32, the B_{VIPK} of the boost increases 1/64 of its value each cycle again to complete one dithering cycle. The average output power keeps unchanged comparing to no dithering.

5.7 Application Design Guidance

5.7.1 Flyback ISNS Pin Parameters

The current sense resistor R_S (R47 in Figure 2) of the flyback stage can be calculated by:

$$R_S = \frac{300mV}{\frac{I_{OUT}}{N_{PS}}} \times flyback\_\eta \qquad (5.6)$$

In which the N_{PS} is the turns ratio between primary winding and secondary winding. Flyback_η is the efficiency of the flyback stage. The RC filter of ISNS pin (R4 and C9 of Figure 2) should be adjusted so that I_{OUT} at highest V_{AC} input is about same as the lowest V_{AC} input. R4 value is already determined by configuration so C9 should be adjusted accordingly.

5.7.2 Flyback VSNS Pin Parameters

The VSNS pin resistor divider can be calculated by:

$$V_{VSNS\_CV} = \frac{V_{OUT\_CV}}{N_{SA}} \times \frac{R_{VSNS\_BOT}}{(R_{VSNS\_BOT} + R_{VSNS\_UPPER})} \qquad (5.7)$$

In which V_{OUT_CV} is the target CV regulation point. N_{SA} is the turns ratio between the secondary winding and auxiliary winding. R_{VSNS_BOT} is the bottom resistor of VSNS pin (R68 in Figure 2) and R_{VSNS_UPPER} is the upper resistor of VSNS pin (R69 in Figure 2).

It is recommended to set R68 between 1.5kΩ to 2kΩ and calculate R69 accordingly. It is also recommended to parallel a 10pF cap with R69 (C1 in Figure 2) for very high frequency noise filtering.

5.7.3 Flyback Transformer Design

The flyback transformer design should start with turns ratios. First step is to set N_{PS} with desired CV reference (V_{OUT_CV}) of the application. It is common to set N_{PS} * V_{OUT_CV} ≥ 70V and ≤ 140V for best performance in an offline DCM flyback converter. The second step is N_{SA}. It is recommended to set N_{SA} * 50V = V_{OUT_CV} if the application is designed for CC focused applications (Figure 2). Or N_{SA}*15V = V_{OUT_CV} if the application is designed for CV focused applications (Figure 3).

Next up is to determine L_M of the transformer. For the iW3700, it is recommended to set L_M/R_S ≥ 1000u and ≤ 1600u. The higher L_M/R_S results in lower switching frequency and lower switching loss. However, it also results in a higher number of turns in the transformer thus higher DCR of the windings and higher conduction loss.

To calculate the actual number of turns, it is needed to pick a specific transformer core that fits the application power level. The bigger core that sacrifices physical size will have higher A_E (effective cross section area) and results in a smaller number of turns and better efficiency. The number of primary turns can be determined by:

$$Turns = I_{PK} \times \frac{L_M}{(B_{MAX} \times A_E)} \quad (5.8)$$

In which $I_{PK} = V_{ISNS(MAX)} / R_S$, B_{MAX} is the max flux density of the core according to core material type.

5.7.4 Boost BSNS Pin Parameters

The current sense resistor R_{S_BOOST} (R18 in Figure 2) for boost stage can be calculated by:

$$R_{S\_BOOST} = \frac{27}{(V_{OUT\_CV} \times I_{OUT} \times 120\%)} \quad (5.9)$$

Or for iW3700-3X with CP limit on the flyback:

$$R_{S\_BOOST} = \frac{27}{(V_{OUT\_CP\_ENTRY} \times I_{OUT} \times 120\%)} \quad (5.10)$$

In which 120% is the margin factor so that full power of boost stage is 1.2 times of full power of flyback stage to make sure the boost can deliver enough energy to power the flyback at any condition. Next up the CFG resistor (R14 in Figure 2) is determined by configuration. The C_{BSNS} filter cap (C6 in Figure 2) should be set so that R14 * C6 is around 50ns. For the auxiliary winding pull-up resistor (R5 in Figure 2), it should be set by

$$110mV \leq \frac{14}{N_{PA\_BOOST}} \times \frac{R14}{(R5 + R14)} \quad (5.11)$$

In which N_{PA_BOOST} is the primary-to-auxiliary turns ratio of the boost inductor.

5.7.5 Boost Inductor Design

The boost inductor turns ratio is recommended to set between 9 to 11 for all applications. The L_{M_BOOST} of the boost inductor in the iW3700 is recommended to set so that L_{M_BOOST} / R_{S_BOOST} ≥ 1000u and ≤ 2000u. The higher L_{M_BOOST} / R_{S_BOOST} results in lower switching frequency and lower switching loss. However, it also results in higher number of turns thus higher DCR in the windings and higher conduction loss.

To calculate the actual number of turns, it is needed to pick a specific inductor core that fits the application power level. The bigger core that sacrifice physical size will have higher A_{E_BOOST} (effectively cross section area) and results in lower number of turns and better efficiency. The number of primary turns can be determined by:

$$Turns_{BOOST} = I_{PK\_BOOST} \times \frac{L_{M\_BOOST}}{(B_{MAX} \times A_{E\_BOOST})} \quad (5.12)$$

In which $I_{PK} = B_{VIPK(MAX)} / R_{S\_BOOST}$, B_{MAX} is the max flux density of the core according to core material type.

5.7.6 iW350 Enable Control

The iW350 enable control is activated by configuration on ISNS pin. The internal 200µA current source can drive the optocoupler LED side directly without the need for a current limit resistor as shown in Figure 2.

On the output side, a 60V NPN bipolar with beta > 20 should be used with the optocoupler output to build a Darlington connection in order to amplify the gain. This is because the current-transfer-ratio (CTR) of the opto is normally around 1 and not enough to power the iW350 when the iW3700 is driving the optocoupler with 200µA.

5.7.7 TL431 Feedback Control

The TL431 feedback is activated by configuration on ISNS pin. To achieve best performance and avoid false triggering of a DLR event, it is recommended to set the resistor divider on the TL431 input to be:

$$2.495V = V_{OUT\_CV} \times 96\% \times \frac{R_{BOT}}{(R_{TOP} + R_{BOT})} \quad (5.13)$$

In which R_{TOP} is the pull up resistor (R30 in Figure 3) and R_{BOT} is the pull-down resistor (R29 in Figure 3). A filter cap of 10pF is recommended to parallel with R29. If the V_{OUT_CV} is > 25V, a zener diode must be added (Z1 in Figure 3) in series with the DRV pin of the TL431 to make sure $V_{OUT\_CV} – V_{ZENER}$ < 25V.

5.7.8 Application Layout Consideration

For application layout design, it is important to separate both boost and flyback power loops with IC sensing loop. As a combo controller, the ground return point of the sensing resistors of boost stage (R_{S_BOOST}) and that of the flyback stage (R_S) must be at the same point, which should be the ground node of the V_{VBUS} bulk capacitor (CE1 in Figure 2). Figure 21 below illustrates the recommended layout concept.

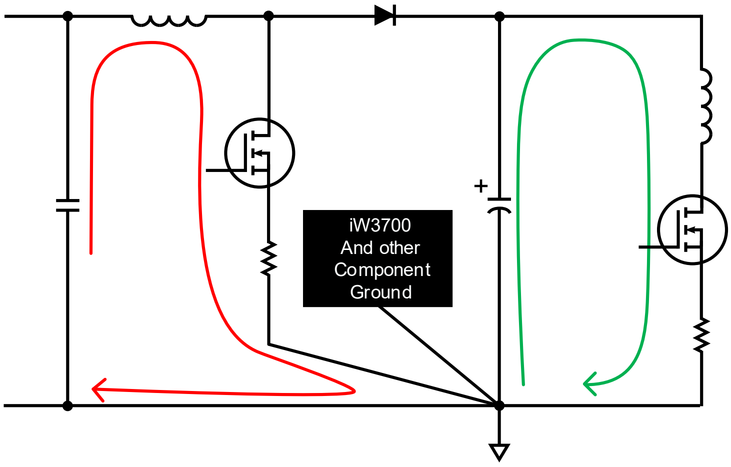


Figure 21. Layout Consideration of the iW3700

5.8 Protections, Limits and De-Rating

A comprehensive list of fault protections is built-in to the iW3700 to protect the system from damage during different kinds of abnormal conditions. Besides the protection, de-rating and limit functions are also included in the iW3700 for safe operation.

5.8.1 Output Over Voltage Protection (OVP)

If at any time the V_{VSNS} platform voltage exceeds the V_{OVP} for 8 consecutive switching cycles, OVP triggers.

Once triggered, the iW3700 stops both boost and flyback stages switching. An extended startup delay of 1 to 2 seconds is imposed for OVP. During the wait period, C_{VCC} is charged by the active startup circuit to $V_{VCC(HIGH)}$. The ASU circuit is disabled at this threshold and C_{VCC} discharges to $V_{VCC(LOW)}$ due to the internal IC current consumption on the VCC pin. This process repeats for several cycles before the wait time expires and next startup attempt.

5.8.2 Output Short Protection (OSP)

If at any time the V_{VSNS} platform voltage is not above V_{OSP} for 500µs consecutively, or the iW3700 is stuck in the startup state for more than 180 switching cycles, the OSP triggers.

Once triggered, the iW3700 stops both boost and flyback stages switching. An extended startup delay of 1 to 2 seconds is imposed for OSP. During the wait period, C_{VCC} is charged by the active startup circuit to $V_{VCC(HIGH)}$. The ASU circuit is disabled at this threshold and C_{VCC} discharges to $V_{VCC(LOW)}$ due to the internal IC current consumption on the VCC pin. This process repeats for several cycles before the wait time expires and next startup attempt.

5.8.3 V_{BUS} Over Voltage Protection (V_{VBUS} OVP)

If at any time the V_{VBUS} voltage is above V_{VBUS_OVP} for 150µs consecutively, V_{VBUS} OVP triggers.

Once triggered, the iW3700 will stop both boost and flyback stages switching. An extended startup delay of 1 to 2 seconds is imposed for V_{VBUS} OVP. During the wait period, C_{VCC} is charged by the active startup circuit to $V_{VCC(HIGH)}$. The ASU circuit is disabled at this threshold and C_{VCC} discharges to $V_{VCC(LOW)}$ due to the internal IC current consumption on the VCC pin. This process repeats for several cycles before the wait time expires and next startup attempt.

5.8.4 V_{BUS} Under Voltage Protection (V_{VBUS} UVP)

If at any time the V_{VBUS} voltage is below V_{VBUS_UVP} for 150µs consecutively, V_{VBUS} UVP triggers.

Once triggered, the iW3700 stops both boost and flyback stages switching. The extended startup delay is not imposed for V_{VBUS} UVP. The iW3700 does qualification as new startup attempt every ASU charging cycle after V_{VCC} is charged to V_{VCC_HI}.

5.8.5 AC Brown Out Protection (V_{VIN} UVP)

If at any time the V_{VIN} peak voltage is below V_{VIN_BROUT} for consecutive 3 AC half cycles, or the V_{VIN} voltage is below V_{VIN_OFF} for 10ms consecutively, V_{VIN} UVP will trigger.

Once triggered, the iW3700 will stop both boost and flyback stages switching. The extended startup delay is not imposed for V_{VIN} UVP. The iW3700 does qualification as new startup attempt every ASU charging cycle after V_{VCC} is charged to V_{VCC_HI}.

5.8.6 AC Over Voltage Protection (V_{VIN} OVP)

If at any time the V_{VIN} peak voltage is above V_{VIN_OVP} for consecutive 8 AC half cycles, V_{VIN} OVP triggers.

Once triggered, the iW3700 stops only the boost and the flyback keeps operating as normal. As a result, the power factor will be low during V_{VIN} OVP. When V_{VIN} peak voltage is below $V_{VIN\_OVP\_REC}$ for 3 consecutive AC half cycles, the V_{VIN} OVP is removed, and the boost converter operates again. V_{VIN} OVP is disabled in iW3700-01.

5.8.7 PFC Over Load Protection (PFC OLP)

When boost stage is on, if the V_{VBUS} voltage cannot reach V_{VBUS_REF} within 2 seconds, PFC OLP triggers.

Once triggered, the iW3700 stops both boost and flyback stages switching. An extended startup delay of 1 to 2 seconds is imposed for PFC OLP. During the wait period, C_{VCC} is charged by the active startup circuit to $V_{VCC(HIGH)}$. The ASU circuit is disabled at this threshold and C_{VCC} discharges to $V_{VCC(LOW)}$ due to the internal IC current consumption on the VCC pin. This process repeats for several cycles before the wait time expires and next startup attempt.

5.8.8 Over Temperature Protection (OTP)

If at any time the internal temperature sensor reaches T_{OTP}, or MUL pin voltage is below V_{NTC_OTP} if NTC function is selected by configuration, OTP will trigger.

Once triggered, the iW3700 will stop both boost and flyback stages switching. An extended startup delay of 1 to 2 seconds is imposed for OTP. During the wait period, C_{VCC} is charged by the active startup circuit to $V_{VCC(HIGH)}$. The ASU circuit is disabled at this threshold and C_{VCC} discharges to $V_{VCC(LOW)}$ due to the internal IC current consumption on the VCC pin. This process repeats for several cycles before the wait time expires and next startup attempt.

5.8.9 Over Temperature De-rating

The over temperature de-rating is designed in the iW3700 to reduce the output power mildly when mild over temperature condition occurs. In this way, the system can be protected during mild over temperature condition without interruption of light output. Figure 22 shows the I_{OUT}% vs the internal temperature sensor temperature.

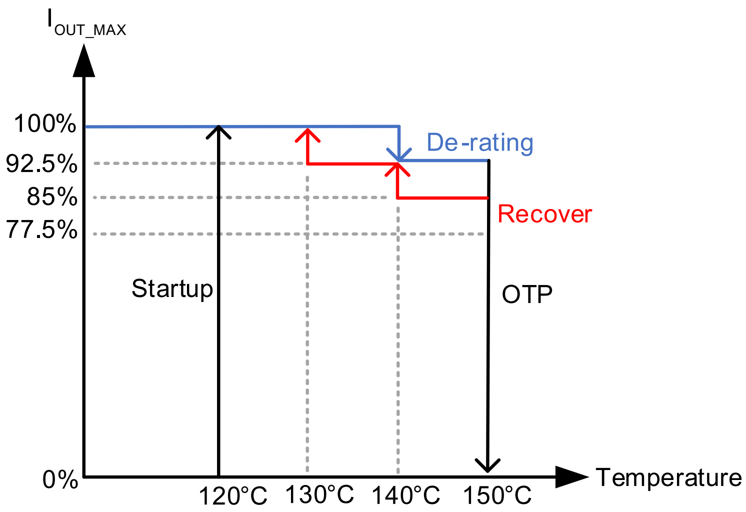


Figure 22. Internal Temperature Sensor Based I_{OUT} De-rating Profile

If the NTC function is selected by configuration, the NTC voltage is sensed by the MUL pin and achieves NTC de-rating function. Figure 23 shows the I_{OUT}% vs. NTC votlage

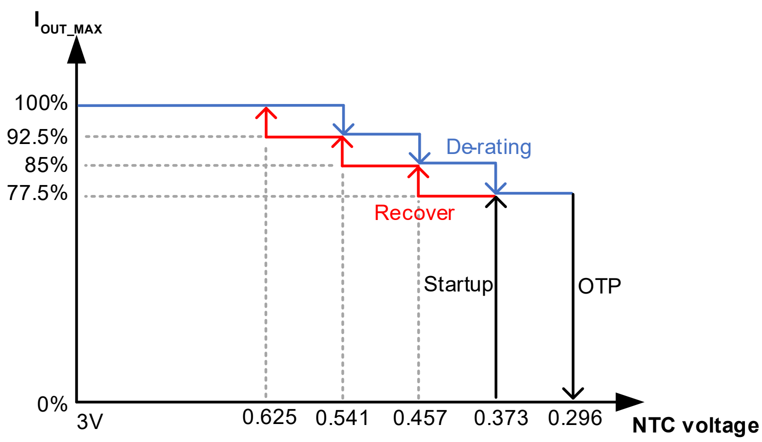


Figure 23. NTC Based I_{OUT} De-rating Profile

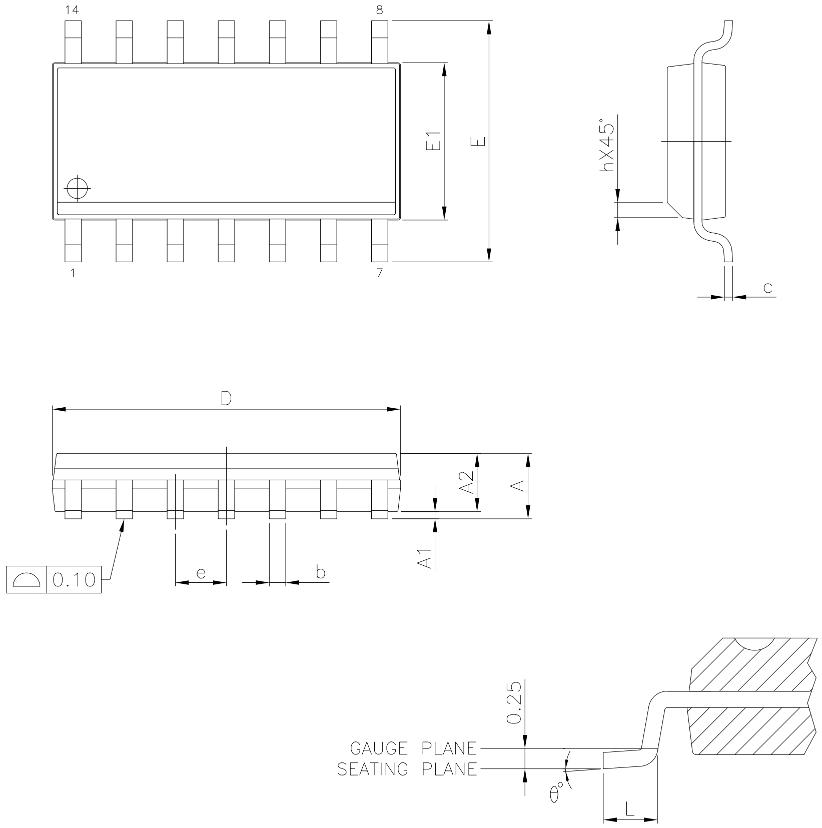
Internal temperature sensor de-rating and NTC de-rating can work concurrently. The iW3700 outputs the lower I_{OUT}% from two de-ratings.

5.8.10 Cycle-by-cycle Peak Current Limit (PCL)

The iW3700 limits the peak current in both boost and flyback stage. When the DRV pin is high, if the ISNS pin reaches OCP, the DRV pin immediately turns off the flyback MOSFET. When the BDRV pin is high, if the BSNS pin reaches the BOCP, the BDRV pin immediately turns off the boost MOSFET.

6. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.



SYMBOLS	MIN.	MAX.
A	1.35	1.75
A1	0.10	0.25
A2	1.25	1.50
b	0.33	0.51
c	0.19	0.25
D	8.55	8.75
E	5.80	6.20
E1	3.80	4.00
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.50
θ°	0	8

UNIT : mm

NOTES:
1.JEDEC OUTLINE : MS-012 AB
2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm. PER SIDE.
3.DIMENSIONS "E1" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE.

Figure 24. 14-Lead SOIC Package

7. Ordering Information

Part Number	Description	Package	Description
iW3700-00	CC focused, DIM ports enabled	SOIC-14	Tape & Reel[1]
iW3700-01	CC focused, DIM ports enabled, VIN OVP disabled	SOIC-14	Tape & Reel[1]
iW3700-20	CV focused, DIM ports disabled	SOIC-14	Tape & Reel[1]
iW3700-21	CV focused, DIM ports disabled, x-capacitor discharge disabled	SOIC-14	Tape & Reel[1]
iW3700-30	CC focused, DIM ports enabled, with $V_{OUT\_CP\_ENTRY}$ = 90%	SOIC-14	Tape & Reel[1]

1. Tape & Reel packing quantity is 2,500/reel. Minimum packing quantity is 2,500.

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