ISL97698

High Efficiency 2-Channel White LED Driver for Smartphone Backlighting

FN8417
Rev.1.00
Sep 7, 2017

The ISL97698 is a highly integrated 2-channel LED driver for white LED (WLED) backlit TFT-LCD panels. The device is composed of a synchronous boost converter and two low-side current sinks that are capable of driving an output voltage up to 23.5V and 25mA LED current, per string. The ISL97698 operates from an input supply of 2.5V to 5.5V.

The driver features Dynamic Headroom Control that monitors the highest LED forward voltage string to determine the requested boost output voltage. With a controlled low 70mV headroom voltage and low 0.35mA IC supply current, the device provides very high efficiency.

The ISL97698 offers 8-bit linear or 11-bit logarithmic controlled analog output current, with dimming control from a PWM, SWIRE, or I^2C interface. Internally, the PWM duty cycle, SWIRE, and I^2C digital inputs are converted to a DC LED current. This analog dimming scheme provides high efficiency and eliminates audible noise and PWM dimming related EMI concerns. The ISL97698 also features Content Adaptive Backlight Control (CABC), which uses the product of the PWM and SWIRE, or PWM and I^2C, or SWIRE and I^2C inputs to determine the LED string current. The I^2C interface is also used for configuration settings and fault detection. The ISL97698 incorporates various protections including: open circuit, short circuit, and thermal shutdown.

The device is offered in a 1.39mmx1.69mm, 3x4 array WLCSP package. It is specified for operation across the -40°C to +85°C ambient temperature range.

Related Literature

- For a full list of related documents, visit our website
  - ISL97698 product page

Features

- High efficiency operation:
  - Up to 91% with 2P4S configuration
  - Up to 90% with 2P6S configuration
- Extremely low supply current (0.35mA)
- Dynamic headroom control
  - Very low headroom voltage (70mV)
- 20mm^2 total solution PCB area
  - Only three external components required
- Analog dimming control by PWM, SWIRE, or I^2C
- 8-bit linear or 11-bit logarithmic analog output current control
- Content Adaptive Backlight Control (CABC)
- Input voltage from 2.5V to 5.5V
- 23.5V maximum output voltage
- Drives 50µA to 25mA LED strings
- Open circuit and short circuit fault protection
- 12 bump, 0.4mm pitch chip scale package

Applications

- WLED backlit LCD displays for smartphones, digital cameras, GPS, etc.

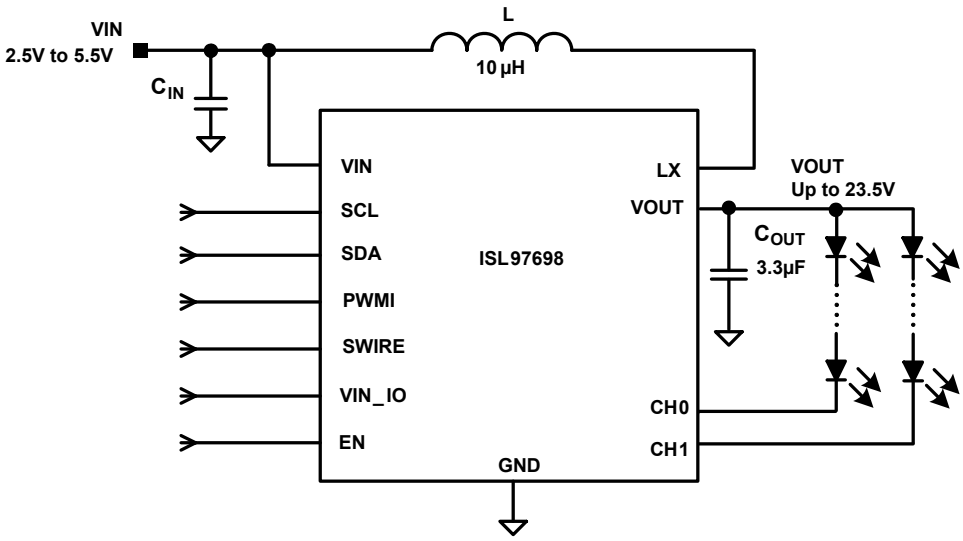
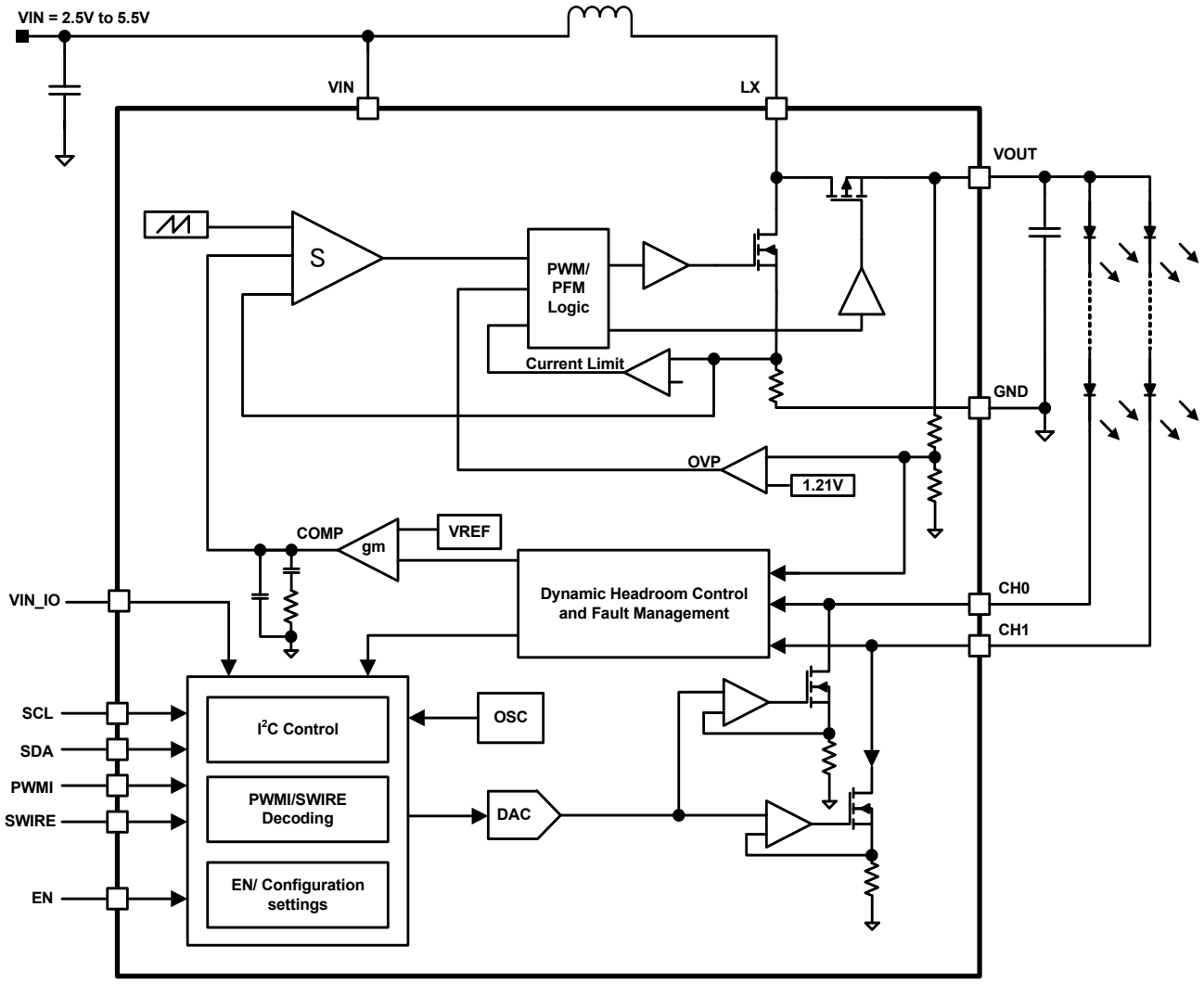


FIGURE 1. ISL97698 TYPICAL APPLICATION CIRCUIT: TFT-LCD BACKLIGHT

Block Diagram



Ordering Information

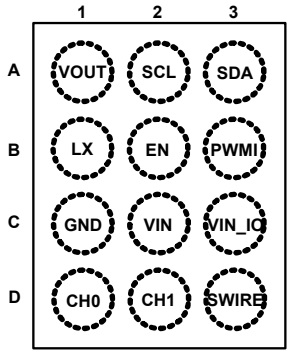
PART NUMBER Notes (1, 2, 3)	PART MARKING	TEMP RANGE (°C)	TAPE AND REEL (UNITS)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ISL97698IIZ-T	7698	-40 to +85	6k	3x4 array, 0.4mm pitch CSP	W3x4.12A

NOTES:

1. Refer to TB347 for details on reel specifications.
2. These Intersil Pb-free WLCSP and BGA packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu - e1 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free WLCSP and BGA packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the product information page for ISL97698. For more information on MSL, see TB363.

Pin Configuration

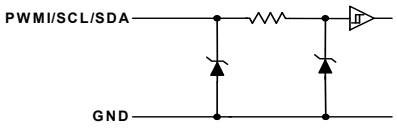
ISL97698
(3x4 ARRAY, 0.4mm PITCH CSP)
TOP VIEW



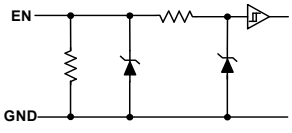
Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
A1	VOUT	Boost Output Voltage. This is also the output voltage sense connection for over voltage sensing.
A2	SCL	Serial Clock Connection for I^2C Interface (high impedance input). Circuit 1 shows its equivalent circuit.
A3	SDA	Serial Data Connection for I^2C Interface (high impedance input, open-drain output). Circuit 1 shows its equivalent circuit.
B1	LX	Drain Connection for Boost Converter's Internal N-Channel MOSFET and P-Channel MOSFET.
B2	EN	IC Enable pin, active high. Circuit 2 shows its equivalent circuit.
B3	PWMI	PWM Input for Dimming Control. Do not leave this pin floating. Circuit 1 shows its equivalent circuit.
C1	GND	Ground
C2	VIN	Input Supply Voltage. Bypass VIN to GND with a ceramic capacitor. Circuit 3 shows its equivalent circuit.
C3	VIN_IO	Digital Interface Supply Voltage for PWMI/SWIRE inputs. Circuit 4 shows its equivalent circuit.
D1	CH0	Channel 0 Current Sink and Monitoring. Tie this pin to GND if channel is not used.
D2	CH1	Channel 1 Current Sink and Monitoring. Tie this pin to GND if channel is not used.
D3	SWIRE	SWIRE Input for Dimming Control. Do not leave this pin floating. Circuit 5 shows its equivalent circuit.

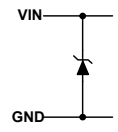
Equivalent Circuit



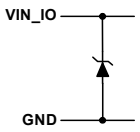
Circuit 1



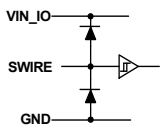
Circuit 2



Circuit 3



Circuit 4



Circuit 5

Absolute Maximum Ratings

VOUT, LX (to GND) . . . . . -0.3V to 24.5V
VIN, VIN_IO, SCL, SDA, PWMI, SWIRE, EN (to GND) . . . . . -0.3V to 6V
CH0, CH1 (to GND) . . . . . -0.3V to 6V
Maximum Average Current Into LX Pin 1.1A
ESD Rating
Human Body Model (Tested per JESD22-A114) 2kV
Latch Up (Tested per JESD78: Class II, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
12 Bump, 0.4mm Pitch CSP (Notes 4, 5)	90	60

Maximum Continuous Junction Temperature . . . . . +125°C
Storage Temperature . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Input Voltage (VIN) . . . . . 2.5V to 5.5V
Digital Interface Supply Voltage (VIN_IO) . . . . . 1.8V to 5.5V
Output Voltage (VOUT) . . . . . Up to 23.5V
Output Current per Channel (CH0, CH1) . . . . . Up to 25mA
Ambient Temperature Range . . . . . -40°C to +85°C
CH0/CH1 Voltage . . . . . 0V to 5.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. See TB379
5. For θ_{JC}, the “case temp” location is taken at the package top center.

Electrical Specifications

$V_{IN} = V_{IN\_IO} = EN = 3.7V$, T_A = +25°C unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
GENERAL						
VIN	Input Supply Voltage		**2.5**		**5.5**	V
VIN_IO	Digital Interface Supply Voltage				**5.5**	V
I_{VIN}	VIN Supply Current	LX not switching (Overdrive VOUT)		0.35		mA
$I_{SHUTDOWN}$	VIN Shutdown Supply Current	EN = 0V		1	**3**	µA
VIN_{UVLO}	VIN Undervoltage Lockout	VIN rising	**2.2**	2.3	**2.4**	V
		Hysteresis		150		mV
VIN_IO_{UVLO}	VIN_IO Undervoltage Lockout Threshold	VIN_IO rising	**1.4**	1.5	**1.6**	V
		Hysteresis		70		mV
BOOST REGULATOR						
T_{SS}	Soft-Start Time	If soft-start goes through all 8 steps and Boost FET current reaches the limit		7		ms
I_{LX}	Boost FET Current Limit		**0.9**	1.1	**1.3**	A
I_{PFM}	Peak FET Current in PFM Mode	When ABS not active (04h<4> = 0)	**250**	296	**350**	mA
$r_{DS(ON)N}$	Boost Low-Side Switch ON-Resistance			300		mΩ
$r_{DS(ON)P}$	Boost High-Side Switch ON-Resistance			470		mΩ
D_{MAX}	Boost Maximum Duty Cycle	f_{SW} = 850kHz	**92**			%
D_{MIN}	Boost Minimum Duty Cycle	f_{SW} = 850kHz			**15**	%
f_{SW}	Boost Switching Frequency	Default frequency setting (04h<3:0> = Ah)	**765**	850	**935**	kHz
$I_{LX\_LEAKAGE}$	LX Leakage Current	LX = 23.5V			**10**	µA
REFERENCE						
I_{MATCH}	Channel-to-Channel DC Current Matching	I_{LED} = 1mA to 25mA	**-2.5**		**+2.5**	%
I_{ACC}	Current Accuracy	I_{LED} = 1mA to 25mA	**-3**		**+3**	%

Electrical Specifications $V_{IN} = V_{IN\_IO} = EN = 3.7V$, $T_A = +25°C$ unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
I_{STEP}	Percent Current Change between Successive Setting Steps	Linear, spec is percentage of current at 100% dimming level		0.4		%
		Logarithmic, spec is percentage of current change between steps		0.3		%
FAULT DETECTION						
V_{SC}	Channel Short Circuit Threshold		**4**	4.5	**5.75**	V
T_{OTP}	Over Temperature Threshold	Temperature Rising		135		°C
V_{OVP}	Overvoltage Threshold			25		V
CHANNEL CURRENT SINKS						
$V_{HEADROOM}$	Current Sink Headroom at CHx Pin of Channel with Higher Forward Voltage (Dominant Channel)	I_{LED} = 25mA		70 (Note 9)		mV
$V_{HEADROOM\_RANGE}$	Dominant Channel Current Sink Headroom Range at CHx Pin	I_{LED} = 25mA		11		mV
LOGIC INPUTS						
V_{IL}	Logic Inputs Low Voltage	SWIRE, PWMI			**0.15 * VIN_IO**	V
		EN, SCL, SDA			**0.4**	V
V_{IH}	Logic Inputs High Voltage	SWIRE, PWMI	**0.78 * VIN_IO**			V
		EN, SCL, SDA	**1.1**			V
I_{LEAK}	Input Leakage	SCL = SDA = PWMI = SWIRE = 5V			**300**	ns
R_{EN}	Internal Pull-Down Resistance	EN		2		MΩ
I^2C INTERFACE						
t_{EN_I2C}	Minimum Time Between EN High and I^2C Enabled			0.1		ms
f_{SCL}	SCL Clock Frequency				**400**	kHz
PWM Interface						
f_{PWMI}	PWM Input Frequency Range	(Note 7)	0.1		10	kHz
R_{DPWM}	PWM Dimming Output Resolution	(Note 7)			8	bit
SWIRE Interface						
R_{SWIRE}	SWIRE Dimming Output Resolution (Note 8)	(Note 7)	5		11	bit

NOTES:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C. Temperature limits are established by characterization and are not production tested.
7. Compliance to limits is assured by characterization and design.
8. 5-bit and 11-bit are specs for logarithmic dimming. For linear dimming, the SWIRE dimming output resolution is 8-bit.
9. Varies within range specified by $V_{HEADROOM\_RANGE}$.

Typical Performance Curves

T_A = +25°C, VIN = VIN_IO = EN = 3.7V, L = TDK VLF302510MT-10uH, C_{OUT} = 3.3µF/25V, f_{SW} = 850kHz, I_{LED} = 25mA/string, 2P6S Configuration, default register settings, unless otherwise noted.

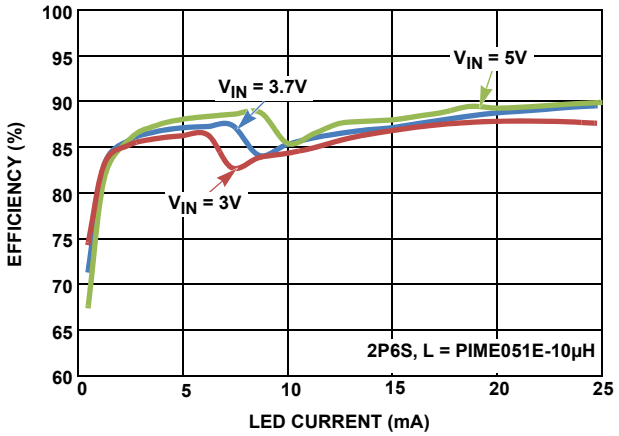


FIGURE 2. BOOST EFFICIENCY vs LED CURRENT (2P6S)

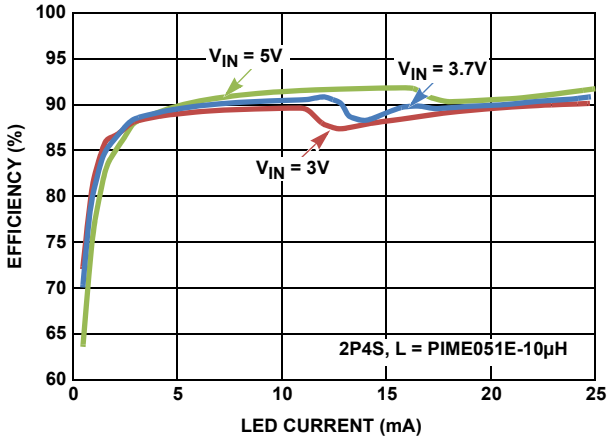


FIGURE 3. BOOST EFFICIENCY vs LED CURRENT (2P4S)

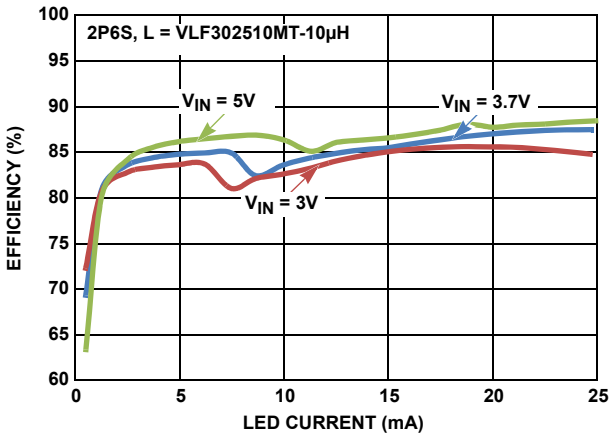


FIGURE 4. BOOST EFFICIENCY vs LED CURRENT (2P6S)

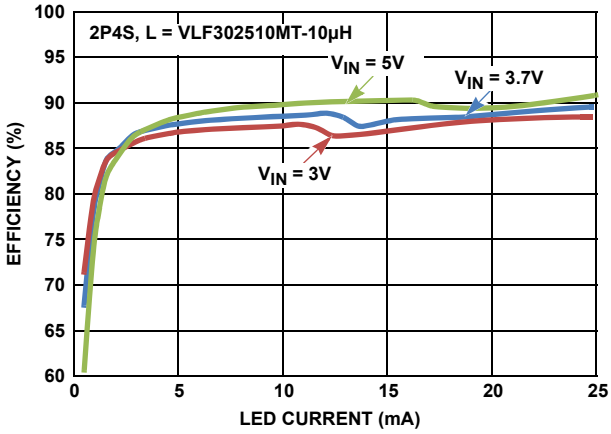


FIGURE 5. BOOST EFFICIENCY vs LED CURRENT (2P4S)

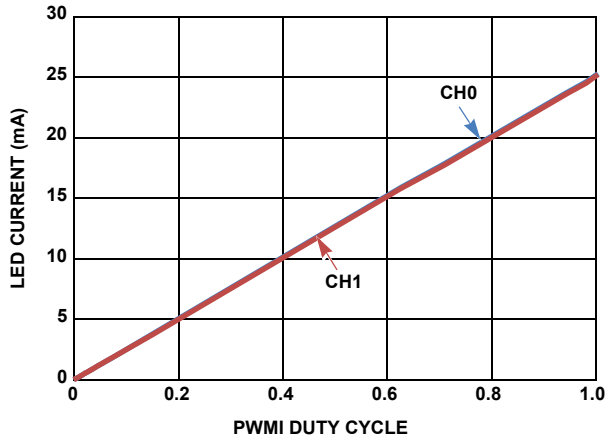


FIGURE 6. DIMMING ACCURACY (8-BIT LINEAR MODE)

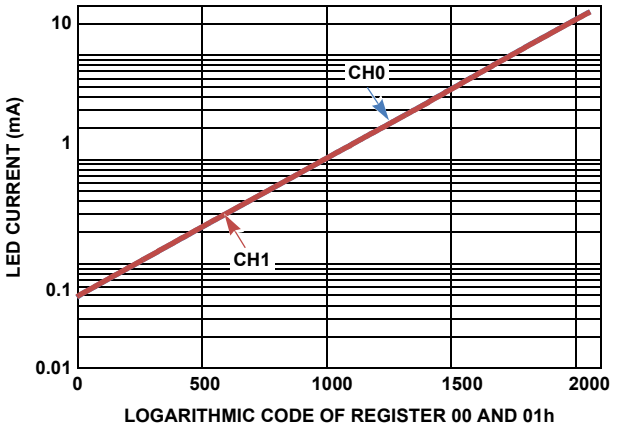


FIGURE 7. DIMMING Accuracy (11-BIT LOGARITHMIC MODE)

Typical Performance Curves

T_A = +25°C, VIN = VIN_IO = EN = 3.7V, L = TDK VLF302510MT-10uH, C_{OUT} = 3.3µF/25V, f_{SW} = 850kHz, I_{LED} = 25mA/string, 2P6S Configuration, default register settings, unless otherwise noted. **(Continued)**

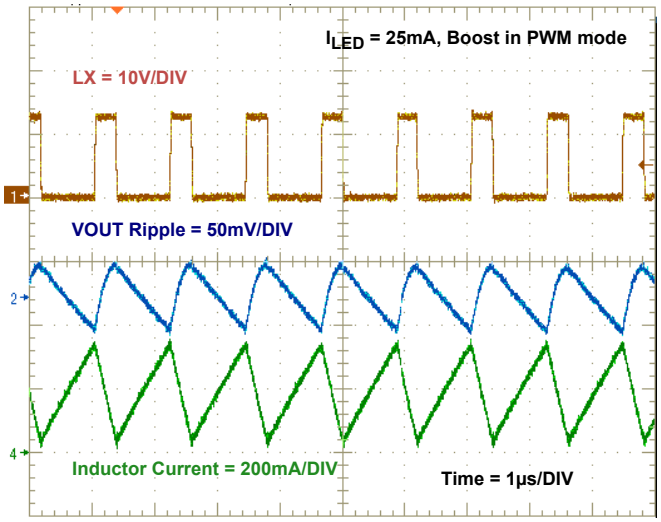


FIGURE 8. BOOST INDUCTOR CURRENT and VOUT RIPPLE in PWM MODE)

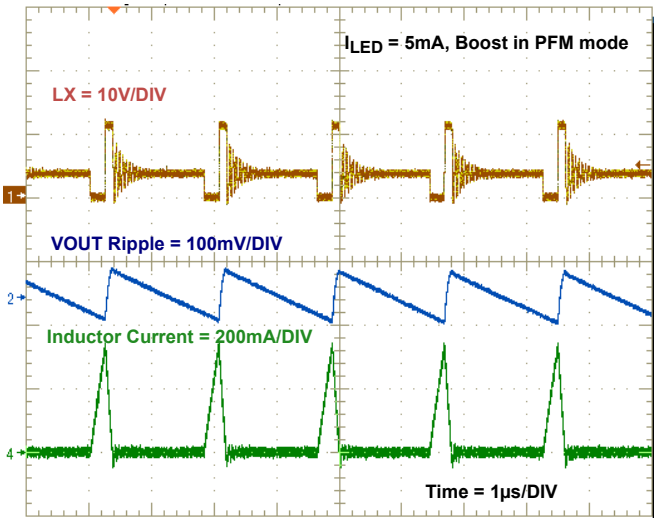


FIGURE 9. BOOST INDUCTOR CURRENT and VOUT RIPPLE in PFM MODE

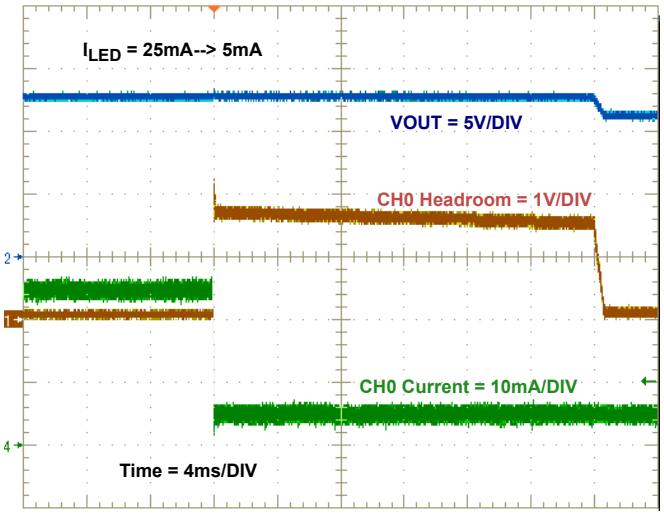


FIGURE 10. TRANSIENT RESPONSE (LED CURRENT CHANGES from 25mA to 5mA)

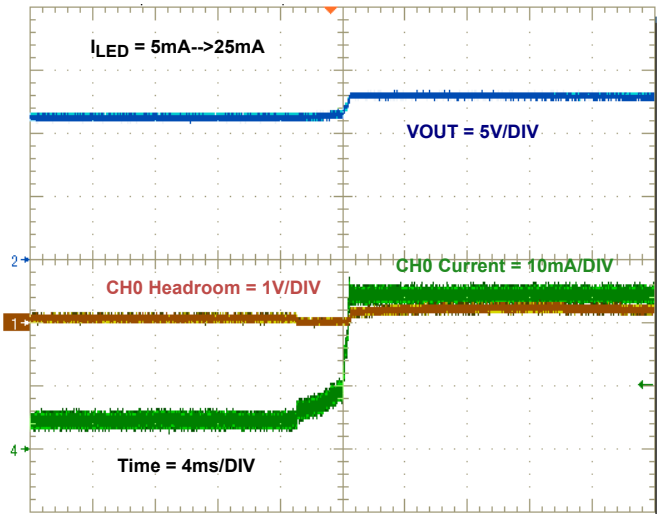


FIGURE 11. TRANSIENT RESPONSE (LED CURRENT CHANGES from 5mA to 25mA)

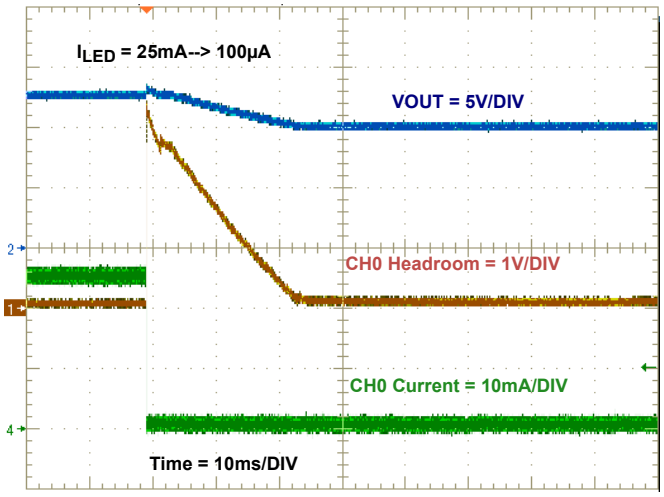


FIGURE 12. TRANSIENT RESPONSE (LED CURRENT CHANGES from 25mA to 100µA)

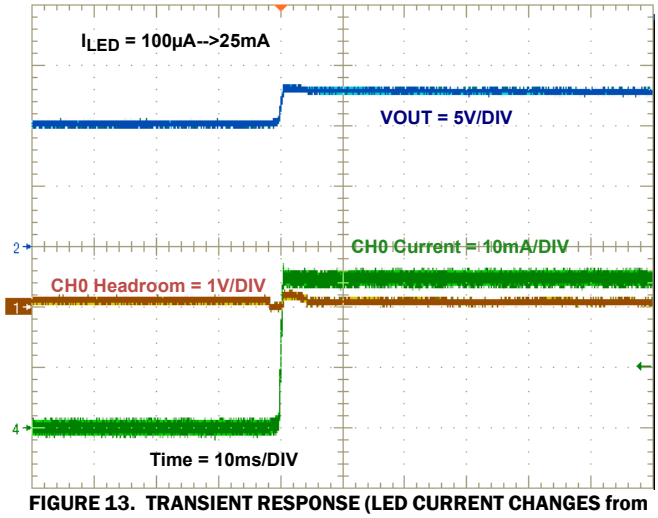


FIGURE 13. TRANSIENT RESPONSE (LED CURRENT CHANGES from 100µA to 25mA)

Typical Performance Curves

T_A = +25°C, VIN = VIN_IO = EN = 3.7V, L = TDK VLF302510MT-10uH, C_{OUT} = 3.3µF/25V, f_{SW} = 850kHz, I_{LED} = 25mA/string, 2P6S Configuration, default register settings, unless otherwise noted. **(Continued)**

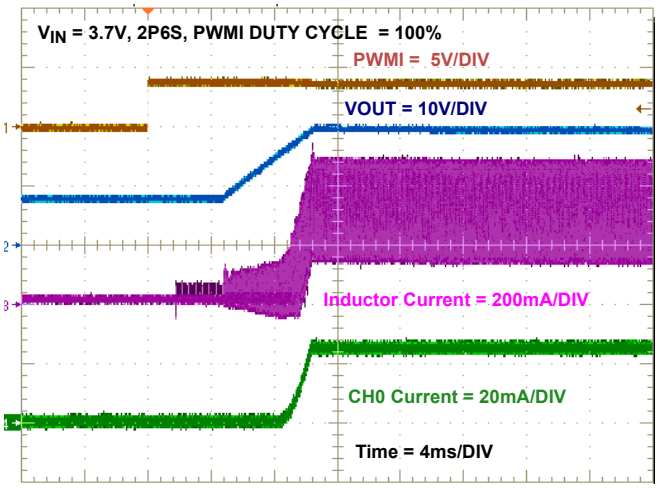


FIGURE 14. START-UP WAVEFORMS (100% BRIGHTNESS)

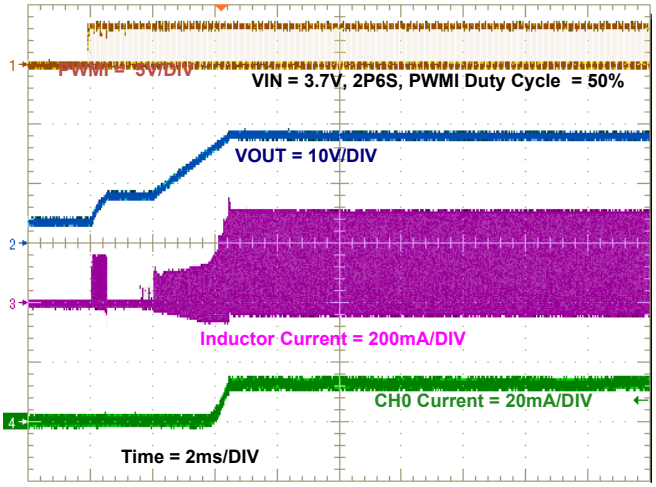


FIGURE 15. START-UP WAVEFORMS (50% BRIGHTNESS)

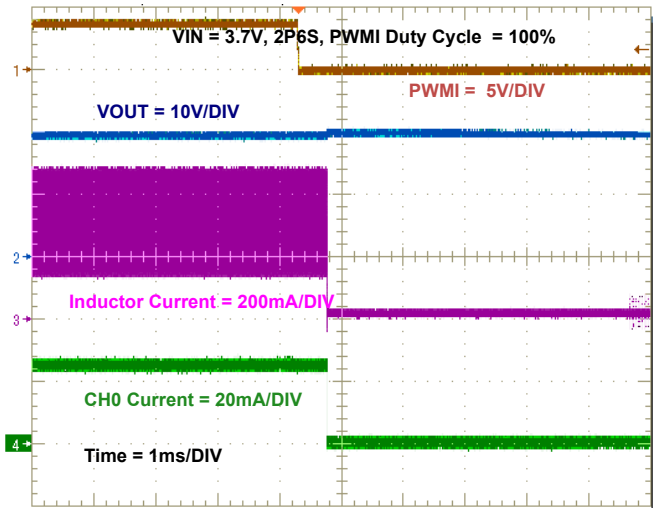


FIGURE 16. SHUTDOWN WAVEFORMS (100% BRIGHTNESS)

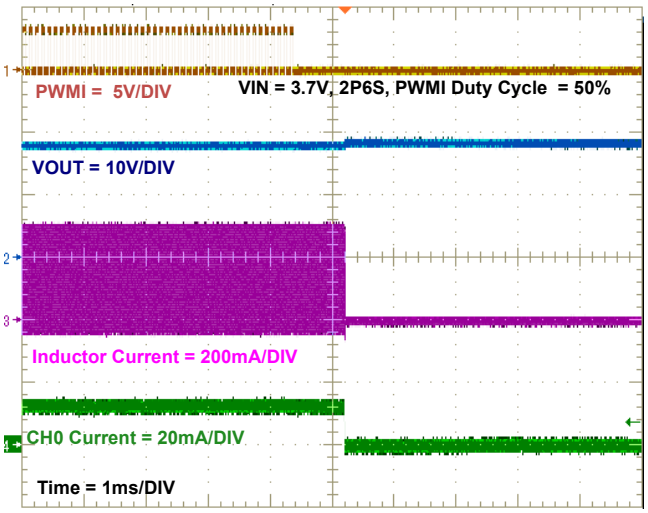


FIGURE 17. SHUTDOWN WAVEFORMS (50% BRIGHTNESS)

Application Information

I²C Digital Interface

The ISL97698 uses a standard I²C interface bus for communication. The two-wire interface links one or more Masters and uniquely addressable Slave devices. The Master generates clock signals and is responsible for initiating data transfers. The serial clock is on the SCL line and the serial data (bi-directional) is on the SDA line. The ISL97698 supports clock rates up to 400kHz (Fast-Mode), and is backwards compatible with standard 100kHz clock rates (Standard-mode).

The SDA and SCL lines must be HIGH when the bus is free (not in use). An external pull-up resistor (typically 2.2kΩ to 4.7kΩ) or current-source is required for SDA and SCL.

The ISL97698 meets standard I²C timing specifications. See Figure 18 and Table 1, which show the standard timing definitions and specifications for I²C communication.

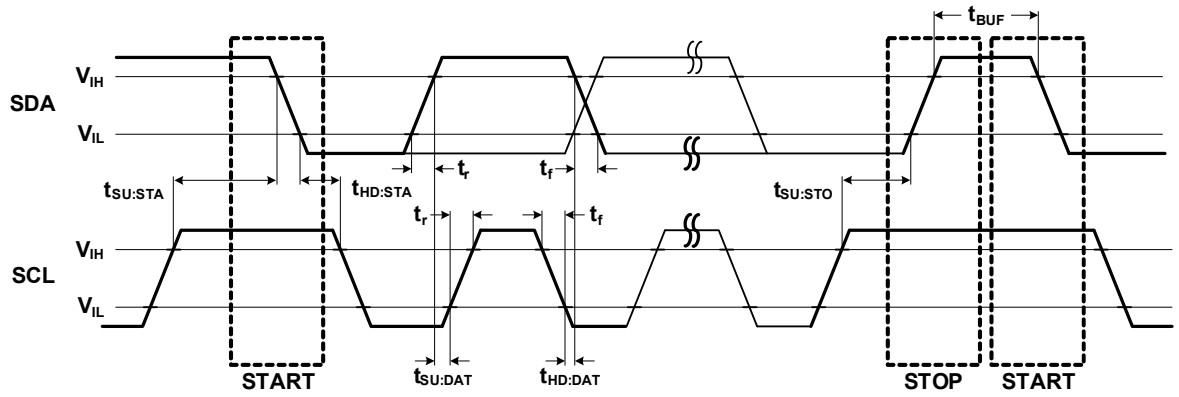


FIGURE 18. I²C TIMING DEFINITIONS

TABLE 1. I²C TIMING CHARACTERISTICS

PARAMETER	SYMBOL	FAST-MODE		STANDARD-MODE		UNIT
		MIN	MAX	MIN	MAX	
SCL Clock Frequency	f_{SCL}	0	400	0	100	kHz
Set-up Time for a START Condition	$t_{SU:STA}$	0.6	-	4.7	-	µs
Hold Time for a START Condition	$t_{HD:STA}$	0.6	-	4.0	-	µs
Set-up Time for a STOP Condition	$t_{SU:STO}$	0.6	-	4.0	-	µs
Bus Free Time between a STOP and START Condition	t_{BUF}	1.3	-	4.7	-	µs
Data Set-up Time	$t_{SU:DAT}$	100	-	250	-	ns
Data Hold Time	$t_{HD:DAT}$	0	-	0	-	µs
Rise Time of SDA and SCL (Note 10)	t_r	$20+0.1C_b$	300	-	1000	ns
Fall Time of SDA and SCL (Note 10)	t_f	$20+0.1C_b$	300	-	300	ns
Capacitive load on each bus line (SDA/SCL)	C_b		400	-	400	pF

NOTE:

10. C_b = total capacitance of one bus line in pF.

START AND STOP CONDITION

All I^2C communication begins with a START condition indicating the beginning of a transaction, and ends with a STOP condition signaling the end of the transaction.

A START condition is signified by a HIGH-to-LOW transition on the serial data line (SDA) while the serial clock line (SCL) is HIGH. A STOP condition is signified by a LOW-to-HIGH transition on the SDA line while SCL is HIGH. See timing specifications in Table 1.

The Master always initiates START and STOP conditions. After a START condition, the bus is considered "busy." After a STOP condition, the bus is considered "free". The ISL97698 also supports repeated STARTs, where the bus will remain busy for continued transaction(s).

DATA VALIDITY

The data on the SDA line must be stable (clearly defined as HIGH or LOW) during the HIGH period of the clock signal. The state of the SDA line can only change when the SCL line is LOW (except to create a START or STOP condition). See timing specifications in Table 1.

The voltage levels used to indicate a logical '0' (LOW) and logical '1' (HIGH) are determined by the V_{IL} and V_{IH} thresholds, respectively, see the "Electrical Specifications" Table on page 4.

BYTE FORMAT

Every byte transferred on SDA must be 8 bits in length. After every byte of data sent by the transmitter there must be an Acknowledge bit (from the receiver) to signify that the previous 8 bits were transferred successfully. Data is always transferred on SDA with the most significant bit (MSB) first. See "Acknowledge (ACK)".

ACKNOWLEDGE (ACK)

Each 8-bit data transfer is followed by an Acknowledge (ACK) bit from the receiver. The Acknowledge bit signifies that the previous 8 bits of data was transferred successfully (master-slave or slave-master).

When the Master sends data to the Slave (e.g., during a WRITE transaction), after the 8^{th} bit of a data byte is transmitted, the Master tri-states the SDA line during the 9^{th} clock. The Slave device acknowledges that it received all 8 bits by pulling down the SDA line, generating an ACK bit.

When the Master receives data from the Slave (e.g. during a data READ transaction), after the 8^{th} bit is transmitted, the Slave tri-states the SDA line during the 9^{th} clock. The Master acknowledges that it received all 8 bits by pulling down the SDA line, generating an ACK bit.

NOT ACKNOWLEDGE (NACK)

A Not Acknowledge (NACK) is generated when the receiver does not pull-down the SDA line during the acknowledge clock (that is, the SDA line remains HIGH during the 9^{th} clock). This indicates to the Master that it can generate a STOP condition to end the transaction and free the bus.

A NACK can be generated for various reasons. For example:

- After an I^2C device address is transmitted, there is NO receiver with that address on the bus to respond.
- The receiver is busy performing an internal operation (reset, recall, etc), and cannot respond.
- The Master (acting as a receiver) needs to indicate the end of a transfer with the Slave (acting as a transmitter).

DEVICE ADDRESS AND R/$\overline{W}$ BIT

Data transfers follow the format shown in Figure 20 and Figure 21. After a valid START condition, the first byte sent in a transaction contains the 7-bit Device (Slave) Address plus a direction (R/$\overline{W}$) bit. The Device Address identifies which device (of up to 127 devices on the I^2C bus) the Master wishes to communicate with.

After a START condition, the ISL97698 monitors the first 8 bits (Device Address Byte) and checks for its 7-bit Device Address in the MSBs. If it recognizes the correct Device Address it will ACK, and becomes ready for further communication. If it does not see its Device Address, it will sit idle until another START condition is issued on the bus.

To access the ISL97698, the 7-bit Device Address is 27h (0100111x), located in MSB bits <b_7:b_1>. The eighth bit of the Device Address byte (LSB bit <b_0>) indicates the direction of transfer, READ or WRITE (R/$\overline{W}$). A "0" indicates a WRITE operation - the Master will transmit data to the ISL97698 (receiver). A "1" indicates a Read operation - the Master will receive data from the ISL97698 (transmitter). See Figure 19.

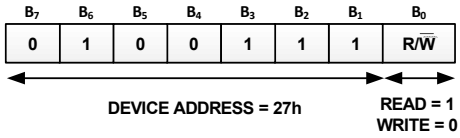


FIGURE 19. DEVICE ADDRESS BYTE FORMAT

Write Operation

A WRITE sequence requires an I²C START condition, followed by a valid Device Address Byte with the R/$\overline{W}$ bit set to '0', a valid Register Address Byte, a Data Byte, and a STOP condition. After each valid byte is sent, the ISL97698 (slave) responds with an ACK. When the Write transaction is completed, the Master should generate a STOP condition. For sent data to be latched by the ISL97698, the STOP condition should occur after a full byte (8-bits) is sent and ACK. If a STOP is generated in the middle of a byte transaction, the data will be ignored. See Figure 20 for the ISL97698 I²C Write protocol.

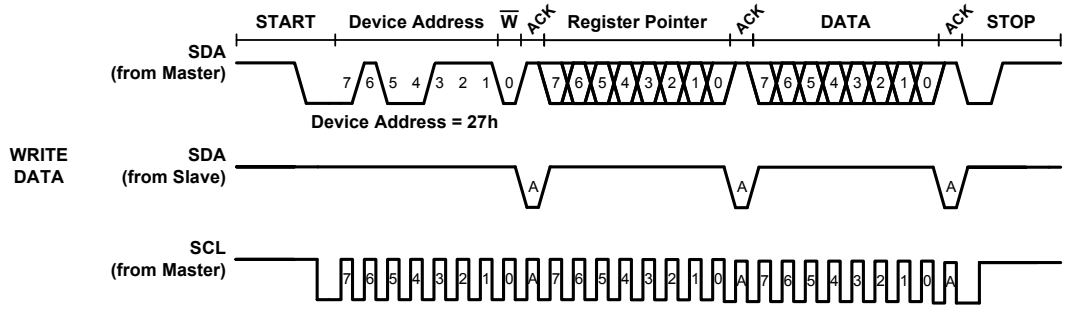


FIGURE 20. I²C WRITE TIMING DIAGRAM

Read Operation

A READ sequence requires the Master to first write to the ISL97698 to indicate the Register Address/pointer to read from. Send a START condition, followed by a valid Device Address Byte with the R/$\overline{W}$ set to '0', and then a valid Register Address Byte. Then the Master generates either a Repeat START condition, or a STOP condition followed by a new START condition, and a valid Device Address Byte with the R/$\overline{W}$ bit set to '1'. Then the ISL97698 is ready to send data to the Master from the requested Register Address.

The ISL97698 sends out the Data Byte by asserting control of the SDA pin while the Master generates clock pulses on the SCL pin. When transmission of the desired data is complete, the Master generates a NACK condition followed by a STOP condition, and this completes the I²C Read sequence. See Figure 21 for the ISL97698 I²C Read protocol.

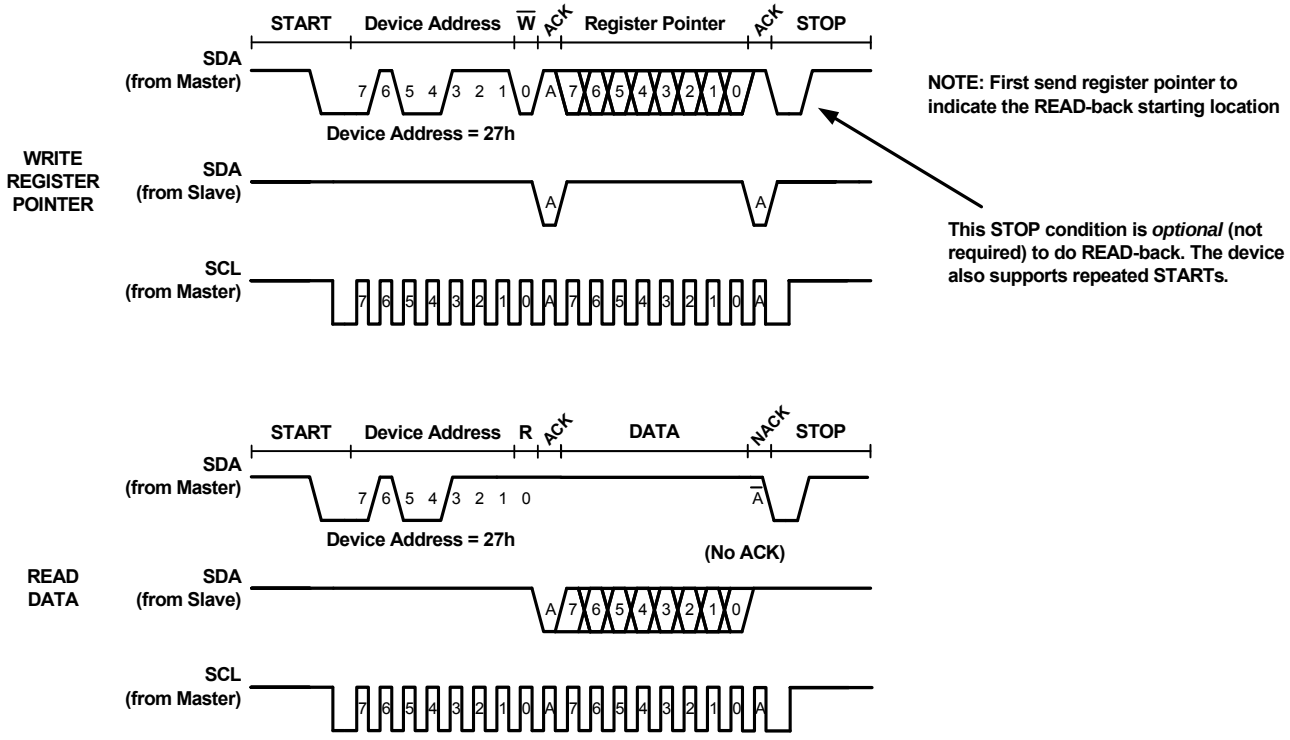


FIGURE 21. I²C READ TIMING DIAGRAM

Register Descriptions and Addresses

Table 2 contains the detailed register map, with descriptions and addresses for ISL97698 registers. Each volatile register is one byte (8-bit) in size. When writing data to adjust register settings using I^2C, the data is latched-in after the 8th bit (LSB) is received.

The ISL97698 has default register settings that are always applied at IC power-ON or after a reset. In Table 2, the default register settings are indicated with **BOLD** face text.

Reserved registers should only be written with the bit value indicated in the Register Map. Also, Register Addresses (pointers) not indicated in the Register Map are reserved and should not be written to.

Note, to clear/reset all the volatile registers to the default values, power cycle VIN.

TABLE 2. REGISTER MAP

Register (Note 11)	R/W	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
00h	R/W	LED Current	Brightness <10:3>								**FFh**
01h	R/W	LED Current (Note 12)	Reserved					Brightness <2:0>			**07h**
02h	R/W	Configuration	Brightness Source: **11**=PWMIx SWIRE (linear) 10=PWMIxI^2C (linear) 01=SWIRExI^2C (log) 00=SWIRExI^2C (linear)		Enable faults (OPCP, OTP) **1**= faults enabled 0= faults disabled	Enable VSC (Short Circuit Protection) **1**=VSC enabled 0=VSC disabled	Enable 25V OVP (Note 14) **1**=25V 0=16V	Disable dither (Note 15) **1**=Disabled 0=Enabled	Enable CH1 **1**= CH enabled 0=CH disabled	Enable CH0 **1**=CH enabled 0=CH disabled	**FFh**
03h	R/W	PFM mode setting (Note 13)	PFM peak current: 120mA+22mA x decimal value of Bit <7:4> Max value: 450mA; Default: 296mA				Average inductor current to enter PFM mode: 60mA+11mA x decimal value of Bit <3:0> Max value:225mA; Default: 93mA				**00h**
04h	R/W	Boost operating mode	Boost Slew Rate: 00=Slowest 01=Slow 10=Fast **11**=Fastest		Light load mode setting: **1** = Synchronous Pulse Skipping 0 = PFM	Enable Audio Band Suppression (ABS) **1**=Enabled 0=Disabled	Boost frequency: 00h = 0.464MHz, 08h = 0.729MHz 01h = 0.486MHz, 09h = 0.785MHz 02h = 0.510MHz, **0A**h = 0.850MHz 03h = 0.537MHz, 0Bh = 0.927MHz 04h = 0.567MHz, 0Ch = 1.020MHz 05h = 0.600MHz, 0Dh = 1.133MHz 06h = 0.638MHz, 0Eh = 1.275MHz 07h = 0.680Mhz, 0Fh = 1.457MHz				**FAh**
10h	R	Fault/status read back	OTP occurred (latched)	OVP/LED open occurred (latched)	VSC occurred (latched)	Boost hitting current limit repeatedly (latched)	Boost mode: 0=PFM/skip 1=PWM	LEDs on	CH1 ok	CH0 ok	**0Fh**

NOTES:

11. All other register addresses are reserved
12. Register 01h can be written to at any time. However, the new data will not be applied until register 00h is subsequently written to. This allows 11-bit logarithmic dimming via I^2C, where all 11-bits are loaded, in two I^2C instructions, before the data is applied and output is adjusted.
13. This register is ignored until it is written to. After being written, its new value will override the default settings until the device is reset.
14. Setting this bit Low will set OVP to 16V. This is recommended when using four or less LEDs, and allows a lower voltage rated output capacitor to be used.
15. Dither is used to improved accuracy of logarithmic current steps, but result in lower efficiency, as LED current is modulated at any brightness code that is between 60+Nx64 and 61+Nx64 (N is 0 to 31). Dither should be disabled for linear dimming applications

SWIRE Communication

The SWIRE interface uses a normally high connection for use with open-drain driving schemes and Intersil's SWIRE interface protocol. When SWIRE is held low between 15µs and 45µs, the interface reads logic 1. When SWIRE is held low between 90µs and 120µs the interface reads logic 0. When SWIRE is held low greater that 215µs, the interface loads (accepts) the bits already entered into the brightness control register and updates the maximum LED current. The required minimum high time is 3µs.

If more than the maximum supported bits are entered, all the input bits will be ignored. If less than the maximum supported bits (8 in linear mode and 11 in logarithmic mode) are entered, the number entered will be scaled to full code. For example, in linear mode, 11011 (87% in 5 bits), 110111 (87% in 6 bits), 1101111 (87% in 7 bits) and 11011110 (87% in 8 bits) will all give approximately the same output.

The SWIRE programming is summarized as follows:

- Logic 0 = Negative pulse >90µs and <120µs
- Logic 1 = Negative pulse >15µs and <45µs
- Load = Negative pulse >215µs

The serial interface is automatically reset to 0 when the power is cycled, or register 02h is written to 00h.

Figure 22 shows an example of transmitting and loading the value b'10010110'.

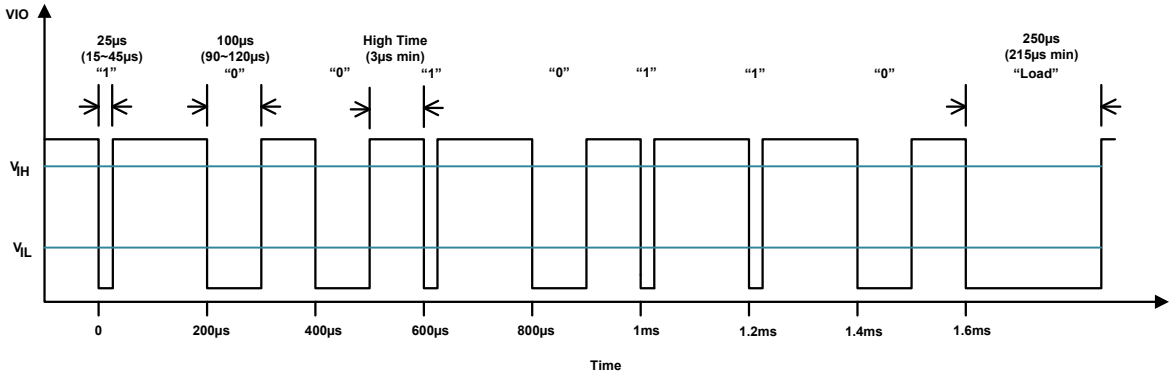


FIGURE 22. SWIRE TIMING DIAGRAM

IC Enable

When the enable (EN) pin voltage is high and VIN and VIN_IO are above rising UVLO thresholds, all ISL97698 circuit blocks are enabled and the boost converter starts to operate. The IC is disabled by pulling the EN pin low, which immediately turns off LED channels and the boost regulator.

When EN is low, the PWM, SWIRE, and I^2C interfaces are all disabled, data most recently written by I^2C in the registers will be maintained.

Boost Converter

The ISL97698 implements a current mode control boost architecture. The boost produces the minimum voltage needed to enable the LED stack with the highest forward voltage drop to run at the programmed current. It has a fast current sense loop and a slow voltage feedback loop. This architecture achieves fast transient response which is essential for portable product backlight applications, in which the backlight must not flicker when the power source is changed from a drained battery to an AC/DC adapter.

Switching Frequency

The boost switching frequency is adjustable with an internal register of the ISL97698. The default value at power-on is 850kHz. The adjustable range is from 460kHz to 1.5MHz. Table 2 on page 12 shows the different frequencies with different register values.

PFM/Synchronous Pulse Skipping

At low output current, the ISL97698 boost regulator transitions from PWM mode to PFM/skip mode to reduce switching losses and maximize efficiency. The regulator transitions from PWM mode to PFM/skip mode when the average inductor current is lower than a set value for 16 successive boost switching cycles. It transitions back from PFM/skip mode to PWM mode when it is switching at the maximum frequency without pulse skipping for 16 successive boost switching cycles, or when the output voltage falls below the target level.

The ISL97698 uses one of two possible modes of operation:

1. Synchronous Pulse Skipping Mode (Default mode, 04h<5>=1): The boost regulator issues a switching cycle when the output voltage has fallen below the set level, but it waits for the next pulse of the internal oscillator for this switching cycle, aligning all cycles to the fixed oscillator frequency.
2. Pure PFM Mode (04h<5>=0): The boost regulator does one switch cycle asynchronously whenever its output falls below its set value and previous cycle is complete.

The different PFM modes can be selected by controlling bit 5 of register 04h. The default setting is Synchronous Pulse Skipping Mode, but is factory configurable to Pure PFM Mode. See"Factory Trimming Option" on page 18.

In both modes, at each boost switching cycle the inductor current reaches the peak value of 300mA (typical). The peak inductor current and average inductor current when it enters PFM mode can be adjusted by writing different values into register 03h (see Table 2 on page 12), or by factory trimming (see"Factory Trimming Option" on page 18).

There is hysteresis built in for the PFM transition. This is to prevent inadvertently going back and forth between PWM and PFM modes.

AUDIO BAND SUPPRESSION (ABS)

The ISL97698 PFM and skip modes feature an ultrasonic mode, which prevents the switching frequency from falling below 30kHz to avoid audible noise in the application. When the time interval between two consecutive switching cycles in PFM or skip mode is more than 33ms (i.e. 30kHz frequency) the regulator reduces the peak inductor current at each cycle, to maintain the frequency above 30kHz. The peak inductor current is reduced in successive steps to 240mA, 200mA, and 162mA. Each step reduces the power delivered per pulse to about 65% of the previous one. This is the Audio Band Suppression (ABS) mode.

Analog Dimming

The ISL97698 controls LED brightness by changing the LED DC current level (analog dimming). Compared with PWM dimming, analog dimming eliminates audible noise and PWM dimming-related EMI concerns and provides higher electrical-to-optical efficiency because of the lower forward voltage of the LEDs at lower current.

This current level can be controlled in 8-bit linear or 11-bit logarithmic fashion, and can be set to between 50µA and 25mA (with 20mA available by factory configuration, for PWM Input dimming and I^2C dimming application). The source of the brightness information can come from I^2C, 1-WIRE (supporting 5, 6, 7, 8, 9, 10 and 11-bit input sequences) or PWMI interfaces. There are 4 possible dimming modes:

1. PWM x SWIRE (linear 8-bit output)

   The default mode if SCL and SDA are pulled HIGH. If SWIRE is not going to be used for dimming control, the SWIRE pin should be tied to GND through a pull-down resistor. If PWMI is not needed, the PWMI pin should be tied HIGH.

   This allows 8-bit PWMI and/or SWIRE control. Additionally, 1-WIRE can be used in combination with PWMI and the resulting LED brightness will be the product of the two input values.

2. PWM x I^2C (linear 8-bit output)

   Can be selected by setting the bits b7:b6 of register 02h to '10'.

   This is very similar to mode 1, but allows both PWMI duty cycle and I^2C data to be combined to set the LED brightness. If PWMI is tied HIGH, register 00h can be written to define an 8-bit linear output (this means the default on-state is 100% LED brightness level).

3. SWIRE x I^2C (logarithmic 11-bit output)

   Can be selected by setting the bits b7:b6 of register 02h to '01', or by tying SCL LOW and SDA HIGH.

   If I^2C is not available, this mode can be used to allow between 5 and 11-bit logarithmic control of the brightness via SWIRE.

   This mode can also be used to allow 11-bit control via I^2C, if SWIRE is not going to be used for dimming control, or it can be the combination of the two interfaces. If SWIRE is not needed, the SWIRE pin should be tied to GND through a pull-down resistor.

   LED current is given by Equations 1 and 2

   $$ILED = 50\mu A \times 1.00304\text{^}N \quad \text{(EQ. 1)}$$

   when N=1, 2... 2047

   $$ILED = 0 \quad \text{(EQ. 2)}$$

   when N=0

   The value of N will be the multiple of the I^2C value from registers 00h and 01h, and the incoming SWIRE value. If the SWIRE resolution is below 11-bits, the value will be internally scaled up to 11-bits.

4. SWIRE x I^2C (linear 8-bit output)

   Can be selected by setting the bit b7:b6 of register 02h to 00, or by tying SCL and SDA LOW.

   This is very similar to mode 3, but has an 8-bit linear output rather than an 11-bit logarithmic output. As such, only register 00h is needed from I^2C and only 8-bits on SWIRE is required. Any additional resolution will be ignored.

   It can be used as a pure SWIRE or I^2C to LED current controller, or with LED current defined as the multiple of the I^2C and SWIRE values.

Note: If SWIRE is not going to be used for dimming control, the SWIRE pin should be tied to GND through a pull-down resistor.

The register settings and pin setups for different dimming modes are listed in Table 3.

TABLE 3. REGISTER SETTING AND PIN SETUP FOR DIFFERENT DIMMING MODES

REGISTER 02h<7:6>	DIMMING MODE	PIN SETUP			
		PWMI	SWIRE	SCL	SDA
11 (default at power-on)	Pure PWMI (Linear)	Input	Low	High	High
	Pure SWIRE (Linear)	High	Input	High	High
	PWMI x SWIRE (Linear)	Input	Input	High	High
10	PWMI x I^2C (Linear)	Input	Low	Input	Input
01	I^2C (Logarithmic)	Low	Low	Input	Input
	Pure SWIRE (Logarithmic)	Low	Input	Low	High
	SWIRE x I^2C (Logarithmic)	Low	Input	Input	Input
00	I^2C (Linear)	Low	Low	Input	Input
	Pure SWIRE (Linear)	Low	Input	Low	Low
	SWIRE x I^2C (Linear)	Low	Input	Input	Input

PWMI FREQUENCIES

PWMI frequencies of up to 10kHz can be decoded at 8-bit resolution. Running at lower PWMI frequencies will result in a more efficient solution because internal oscillator speed is increased to decode higher PWMI frequencies and this requires more input power to operate.

CONTENT ADAPTIVE BRIGHTNESS CONTROL (CABC)

Content Adaptive Brightness Control (CABC) is a control method in which the LED brightness is adjusted depending on the image being displayed. For example, if the images being displayed only contains dark pixels, the backlight brightness can be reduced and the pixel values can be boosted simultaneously to let more light pass through TFT filter, resulting in the same perceived brightness.

CABC is used to save power consumption in many applications. With different options of dimming control mode, ISL97698 provides the system designer with a great design flexibility for CABC.

Maximum LED Current

The maximum LED current is 25mA per channel by default. For PWMI dimming and I^2C dimming applications, the ISL97698 can be factory configurable to set maximum LED current to 20mA (see"Factory Trimming Option" on page 18).

Current Matching and Current Accuracy

Each LED current channel is regulated by a current sink circuit.

The sink terminals of the current source MOSFETs are designed to operate within a range at about 70mV (typical) to optimize power loss versus accuracy requirements. A low headroom voltage reduces power loss in the IC so the LED efficiency is enhanced.

The ISL97698 features exceptional current matching and accuracy over a wide range of LED current levels (1mA to 25mA). See "Electrical Specifications" on page 4.

Dynamic Headroom Control

The ISL97698 features a proprietary Dynamic Headroom Control circuit that detects the highest forward voltage string, or effectively the lowest voltage on one of the two channels and dynamically sets the ideal boost output voltage.

The boost regulates the output to the correct level such that the lowest channel headroom is at the target headroom voltage (70mV). Since both LED stacks are connected to the same output voltage, the other channel will have a higher voltage, but the regulated current sink circuit on each channel will ensure that each channel is at the same target current value which guarantees good channel current accuracy and current matching. The output voltage will regulate cycle by cycle and it is always referenced to the highest forward voltage string in the architecture.

LED Brightness Shutdown

When the LED current is turned off using the PWM, SWIRE, or I^2C interface, the boost regulator remains active, continuing to regulate the output voltage for 25ms. This allows it to quickly turn the LEDs back on. After 25ms, the boost regulator turns off. All input digital interfaces remain active, while EN remains high. The IC will enter a zero current mode if the LED current is off for >30ms, from which it will only awake briefly to accept commands and confirm command validity. Any valid, non-zero brightness command will enable the IC and switch on the LEDs.

Fault Protection and Monitoring

The ISL97698 features extensive protection functions to handle failure conditions (boost over current, LED open circuit, LED short circuit, over temperature) automatically. Refer to Table 4 for details of the fault protections.

The ISL97698 uses feedback from the LEDs to determine when it is in a stable operating region, and prevents apparent faults during transient events from allowing any of the LED stacks to fault out.

OVERCURRENT PROTECTION (OCP)

The boost over-current protection limits the boost NFET current on a cycle-by-cycle basis. When the NFET current reaches the current limit threshold the current PWM switching cycle is terminated and the MOSFET is turned off for the remainder of that cycle. Over-current protection does not disable any of the regulators. Once the fault is removed (NFET current falls below current limit), the device will continue with normal operation.

OPEN CIRCUIT PROTECTION (OPCP)

When one or more of the LEDs becomes an open circuit, it can behave as either an infinite resistance or a gradually increasing finite resistance. The ISL97698 monitors the current in each channel such that any string that reaches the intended output current is considered "good". If there is one string where the LED current falls below the target value, the ISL97698 will initiate a time-out while increasing the boost output voltage to the lesser of the OVP limit or 5.75V current sink headroom of the "good" channel. If the current of the faulty channel is still below the target value at the end of the time-out period, the ISL97698 will declare this channel as "open circuit" and allow the boost output voltage to drop and regulate the "good" one at a minimum headroom voltage.

The 5.75V maximum current sink headroom at open circuit protection is implemented to prevent the CH pin voltage or inductor current from reaching unsafe levels. Under these conditions, if the good CH pin exceeds 5.5V, VOUT will not be allowed to rise further.

OPCP can be disabled by factory trim. See"Factory Trimming Option" on page 18.

SHORT CIRCUIT PROTECTION (SCP)

The short circuit detection circuit monitors the current sink headroom voltage on each channel. When one or more of the LEDs becomes a short circuit, the ISL97698 will continue to operate and keep LED current in regulation in both channels, if the current sink headroom on the faulty channel is under the Channel Short Circuit Threshold (nominally 4.5V). If the current sink headroom on the faulty channel stays above the Channel Short Circuit Threshold over a time-out period (3ms typical), the normal channel will be disabled, allowing both CH pin voltages to reduce to safe-levels. If Short Circuit protection is disabled, the CH pins will instead have a CH overvoltage monitor enabled. Under these conditions, if the CH pin exceeds 5.5V, VOUT will not be allowed to rise further. SCP can be disabled by setting register 02h bit 4 to 0.

UNDERVOLTAGE LOCKOUT (UVLO) OF VIN

If the input voltage (VIN) falls below the VIN_{UVLO} threshold less the UVLO hysteresis, boost will stop switching and the current sink circuit will be disabled. Refer to the "Electrical Specifications" on page 4 for the VIN UVLO specifications.

Note, the digital settings (register values) are not reset to default by the falling VIN UVLO. The register values will be retained, unless VIN falls past a secondary threshold (1V typical). This allows configuration and dimming data to be maintained while still guarantees a reliable power reset. VIN needs to fall below 1V before power is re-applied to ensure a full power cycle (register values are reset).

UNDERVOLTAGE LOCKOUT (UVLO) OF VIN_IO

If the VIN_IO falls below the VIN_IO_{UVLO} threshold less the UVLO hysteresis, boost will stop switching and the current sink circuit will be disabled. Refer to the "Electrical Specifications" on page 4 for the VIN_IO UVLO specifications.

OVER-TEMPERATURE PROTECTION (OTP)

The ISL97698 has an Over Temperature Threshold set to +135°C typical. If this threshold is reached, the boost stops switching, and the channel output current sinks are switched off. The ISL97698 can be restarted if the VIN or EN is cycled (Low then High).

TABLE 4. PROTECTIONS TABLE

FAULT PROTECTION	FAULT TRIGGER	DEVICE REACTION	DELAY TIME FROM A FAULT OCCURRENCE TO DEVICE REACTION	VOUT REGULATED BY
Overcurrent Protection (OCP)	Peak current of boost FET higher than 1A	Terminate PWM; bit 4 of register 10h set (if not during soft start and high current condition is not transient)	PWM terminated immediately. Time-out before reporting the fault in register 10h	Boost current limit
Open Circuit Protection (OPCP)	one or more of the LEDs become open circuit	VOUT rises to 25V or good CH voltage rises to 5.5V (whichever happens first), then channel with open LED switched off; bit 6 of register 10h set and the relevant bit 2 or bit 1 will be cleared	Time-out	VF of the normal channel
Short Circuit Protection (SCP)	One or more LEDs become short circuit and current sink headroom on the faulty channel is above 4.5V	Normal channel switched off; bit 6 of register 10h set and the relevant bit 2 or bit 1 will be cleared	Time-out	VF of the faulty channel
Over-Temperature Protection (OTP)	Die/Junction Temp rising higher than +150°C (typ)	IC shuts down until temperature cools down AND power cycle; bit 7 of register 10h set	Immediate	NA

Power-On Sequence

To power on the IC from shutdown mode and turn on the LEDs, all the four conditions need to be met: 1. VIN is above its UVLO rising threshold; 2. VIN_IO is above its UVLO rising threshold. 3. EN is above logic High threshold. 4. One of the dimming control methods is used to set the LED brightness level to be above zero (refer to "Analog Dimming" on page 14). There is no special sequence implemented between the first three conditions. Refer to Table 5 for when to apply the dimming input signal.

TABLE 5. POWER- ON SEQUENCE

DIMMING INPUT	SEQUENCE
SWIRE	Apply after VIN_IO is on
PWMI	Can be applied any time (No special sequence needed)
I^2C	Apply after VIN, VIN_IO and EN are all on. Note: the register settings will not be reset unless VIN is below its secondary UVLO level (see "Undervoltage Lockout (UVLO) of vin" on page 15).

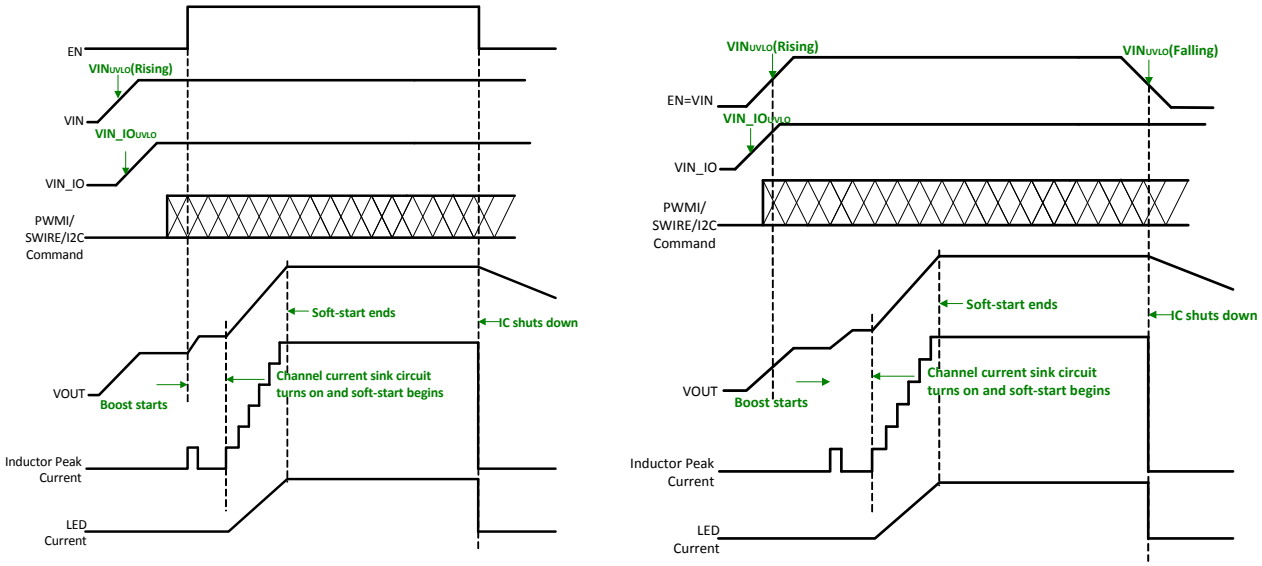
SOFT-START

Once the ISL97698 is powered up, the boost regulator will begin to switch at a low current and frequency. It will continue to do this until VOUT has exceeded ~6.8V, after which the current sources can turn on and boost soft-start will begin. The current in the boost power switch is monitored and the switching is terminated in any cycle when the current reaches the current limit. The ISL97698 includes a soft-start feature where this current limit starts at a low value (125mA). This is stepped up to the maximum 1A current limit in 7 further steps of 125mA over 7ms. Depending on the peak inductor current that is required to regulate the LED current to the target value, the soft start will not always make use of all the steps, so the soft-start will appear to be shorter. At higher battery voltage inputs and lower LED outputs, the number of soft-start steps required is less, so the observed soft-start time is shorter. This feature limits the inrush current at start-up and avoids a drop in the battery voltage due to excessive inrush current.

Note, there will be also an initial inrush current through the body diode of the PFET to the output capacitor (C_{OUT}) when V_{IN} is applied. This is determined by the ramp slew rate of V_{IN} and the values of C_{OUT} and inductor (L).

Power-Off Sequence

To power off the IC and turn off the LEDs, one of the four conditions needs to be met: 1. VIN is below its UVLO falling threshold; 2. VIN_IO is below its UVLO falling threshold. 3. EN is below logic Low threshold. 4. One of the dimming control methods is used to set the LED brightness level to be zero (refer to "Analog Dimming" on page 14).



NOTE: refer to Table 5 for the sequence of dimming input signal

FIGURE 23. ISL97698 POWER ON/OFF DIAGRAM

Component Selection

The design of the boost converter is simplified by an internal compensation scheme allowing easy design without complicated calculations. Therefore, only three external components (input capacitor, boost inductor, output capacitor) are needed. Use the recommendations below to select component values.

INPUT CAPACITOR (C_{IN})

A 2.2µF to 10µF X5R/X7R or equivalent ceramic input capacitor is recommended. The voltage rating of the input capacitor needs to be higher than the maximum V_{IN} in the application.

OUTPUT CAPACITOR (C_{OUT})

A 3.3µF or larger X5R/X7R or equivalent ceramic output capacitor is recommended. The voltage rating of the output capacitor needs to be higher than the maximum VOUT in the application.

Note: Capacitors have a voltage co-efficient that makes their effective capacitance drop as the voltage across them increases. The X5R and X7R ceramic capacitors offer small size and a smaller temperature and voltage coefficient compared to other ceramic capacitors.

INDUCTOR (L)

A 10µH inductor with saturation current rated above maximum operating peak inductor current is recommended.

To determine the required inductor characteristics, firstly, determine the minimum inductor saturation current required for the application. With high LED current, boost operates in continuous conduction mode (CCM). With low LED current, boost operates in discontinuous conduction mode (DCM) and PFM mode.

In CCM, we can calculate the peak inductor current using Equations 4 through 8.

Given these parameters:

a. Input Voltage = VIN
b. Output Voltage = VOUT
c. Switching Frequency = f_{SW}

The duty cycle D can be calculated as:

$$D = 1 - V_{IN}/V_{OUT} \quad \text{(EQ. 3)}$$

Then the inductor ripple can be calculated as

$$\Delta I_{P-P} = (V_{IN})*(D)/(L*f_{SW}*V_{OUT}) \quad \text{(EQ. 4)}$$

then rewrite Equation 4 using Equation 3:

$$\Delta I_{P-P} = (V_{IN})*(V_O - V_{IN})/(L*f_{SW}*V_O) \quad \text{(EQ. 5)}$$

The average inductor current is equal to the average input current, where I_{IAVG} can be calculated from Equation 6.

$$I_{IAVG} = (V_{OUT}*I_{LED})/(V_{IN}*\text{Efficiency}) \quad \text{(EQ. 6)}$$

The peak inductor current then can be calculated from Equation 7:

$$I_{Pk} = \Delta I_{P-P}/2 + I_{IAVG} \quad \text{(EQ. 7)}$$

Substituting Equations 5 and 6 in Equation 7 to calculate I_{Pk}.

$$I_{PK} = 0.5*V_{IN}*(V_O - V_{IN})/(L*f_{SW}*V_O) + (V_O*I_O)/(V_{IN}*EFF) \quad \text{(EQ. 8)}$$

The ISL97698 boost regulator operates in DCM and PFM mode at light load. In PFM mode, it uses a fixed peak inductor current of 296mA. This peak inductor current can be adjusted by writing different values into register 03h<7:4> (see Table 2 on page 12) or by factory trimming (see“Factory Trimming Option” on page 18).

To avoid inductor core saturation, the saturation current of the inductor selected should be 20% higher than the greater of the

peak inductor current (for CCM) and the fixed peak inductor current in PFM mode.

The 296mA peak inductor current in PFM mode is optimized to provide maximum efficiency with a 10µH inductor value. If a smaller value inductor is used, less energy will be delivered per cycle, the boost will need to switch at a higher frequency, and the device efficiency will reduce. Increasing the inductor value will increase the energy delivered per pulse, thus decreasing the switching frequency and subsequently the switching loss of the device. However, note that conduction losses are affected by changing inductor value and/or inductor size. For a given inductor size, DC-resistance (DCR) increases with increasing inductor value: conduction losses go up; for a given inductor value, DCR increases with decreasing inductor size: also resulting increased conduction losses. L = 10µH is the optimal value for ISL97698.

Table 6 shows some recommended inductors for typical ISL97698 applications - small size, handheld TFT-LCD backlight.

TABLE 6. RECOMMENDED INDUCTORS

INDUCTOR PART NUMBER	INDUCTANCE (µH)	DCR (mΩ)	I_{SAT} (A)	Dimension (mm)
VLF302510MT-100M (TDK)	10	310	0.59	3.0x2.5x1.0
DFE252012C (Toko)	10	400	0.85	2.5x2.0x1.2
PIME051E-100M (Cyntec)	10	170	2	5.4x5.2x1.3

Unused LED Channel

Connect the unused LED channel pin to GND. The channel will be disabled at startup.

High Current Applications

Each channel of the ISL97698 supports up to 25mA continuous sink current. The two channels can be paralleled by shorting CH0 and CH1 together to provide up to 50mA in one string of LEDs.

For PWMI dimming and I^2C dimming applications, the peak current can be factory configured to 20mA (See“Factory Trimming Option” on page 18), providing a 40mA option for a single LED string.

Factory Trimming Option

ISL97698 has fuse options that can be factory configured to permanently change maximum LED current, PFM mode, peak inductor current in PFM mode, average inductor current to enter PFM mode, and to permanently disable Open Circuit Protection (OPCP). Please contact your local Intersil sales representative for further information.

General Layout Guidelines

Some general best practices should be followed to create an optimal PCB layout:

1. Careful consideration should be taken with any traces carrying high di/dt pulsating signals. Traces carrying high di/dt pulsating signals should be kept as short and as tight as possible. The current loop generates a magnetic field which can couple to another conductor inducing unwanted voltage. Components should be placed such that current flows through them in a straight line as much as possible. This will help reduce size of loops and reduce the EMI from the PCB.
2. If trace lengths are long, the resistance of the trace increases and can cause some reduction in IC efficiency, and can also cause system instability. Traces carrying power should be made wide and short.
3. In discontinuous conduction mode, the direction of the current is interrupted every few cycles. This may result in large di/dt (transient load current). When injected in the ground plane the current may cause voltage drops, which can interfere with sensitive circuitry. The analog ground and power ground of the IC should be connected very close to the IC to mitigate this issue
4. One plane/layer in the PCB is recommended to be a dedicated ground plane. A large area of metal will have lower resistance, which reduces the return current impedance. More ground plane area minimizes parasitics and avoids corruption of the ground reference.
5. Low frequency digital signals should be isolated from any high frequency signals generated by switching frequency and harmonics. PCB traces should not cross each other. If they must cross due to the layout restriction, then they must cross perpendicularly to reduce the magnetic field interaction.
6. The amount of copper that should be poured (thickness) depends upon the power requirement of the system. Insufficient copper will increase resistance of the PCB, which will increase heat dissipation.
7. Generally, vias should not be used to route high current paths.
8. While designing the layout of switched controllers, do not use the auto routing function of the PCB layout software. Auto routing connects the nets with same electrical name and does not account for ideal trace lengths and positioning.

ISL97698 Specific Layout Guidelines

1. The input capacitor should be connected between bump C2 (VIN)/bump C3 (VIN_IO) and ground with the smallest and thick traces possible. This will help in rejecting high frequency disturbances and will help in proper regulation of the boost regulator and hence the LED current. Use either X7R or X5R dielectric input capacitors. Y5V and Z5U type capacitors are not recommended to use because of their bad temperature characteristics.
2. Inductor should be connected to the LX pin (B1) with wide and short trace. Careful consideration should be made in selecting the inductor as it may cause electromagnetic interference and that may affect normal functioning of the IC. Shielded inductor is recommended. Do not route any digital lines underneath the inductor.
3. The output of the boost regulator (V_{OUT}) is A1. This pin is also the output voltage sense connection for over voltage sensing. The distance of the capacitor from the A1 bump is critical. It is recommended that 10µF/25V capacitor should be placed very close to the IC with thick and short trace. The other end of the output capacitor should be connected to ground with thick and short trace too. The output capacitor should also be close to the LED as possible to minimize the LED ripple current.
4. Digital signals EN, SCL, SDA, SWIRE and PWMI should be isolated from the high di/dt and dv/dt signals. Otherwise, it may cause a glitch on the digital signals resulting in unexpected operation of the IC.
5. I^2C signals, if not used, should be tied to the VIN.
6. EN, if not used, should be tied to the VIN.
7. Bumps D1 and D2 are Channel 0 and Channel 1 (respectively). These are current sinking and monitoring pins. Tie the pin to ground if the channel is not used.
8. The solder pad on the PCB should not be larger than the solder mask opening for the ball pad on the package. The optimal solder joint strength, it is recommended a 1:1 ratio for the two pads.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
September 7, 2017	FN8417.1	Updated title. Added Related Literature section. Added VHEADROOM_RANGE spec to the Electrical Specifications table. Added Note 9. In “Current Matching and Current Accuracy” on page 15, updated the first sentence in the second paragraph for clarification. Applied new header/footer.
September 5, 2013	FN8417.0	Initial release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing, and high-end consumer markets.

For the most updated datasheet, application notes, related documentation, and related parts, see the respective product information page found at www.intersil.com.

For a listing of definitions and abbreviations of common terms used in our documents, visit www.intersil.com/glossary.

You can report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

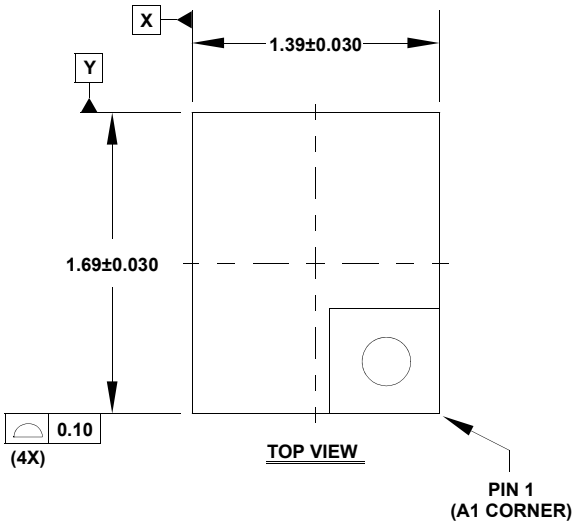
Package Outline Drawing

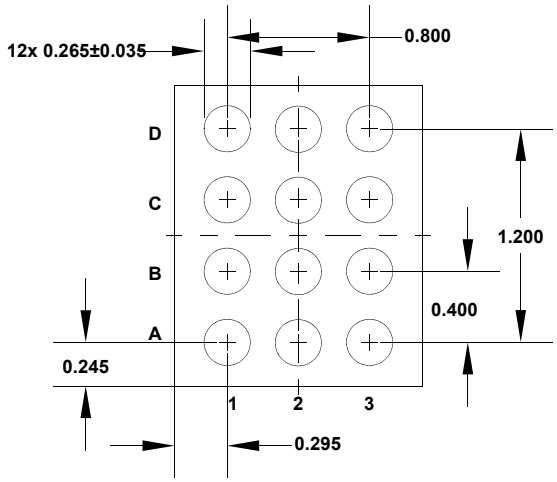
For the most recent package outline drawing, see W3x4.12A.

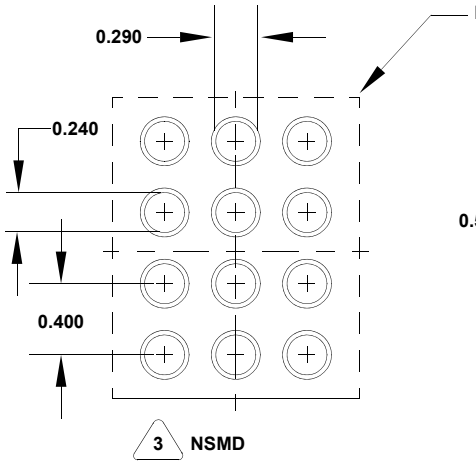
W3x4.12A

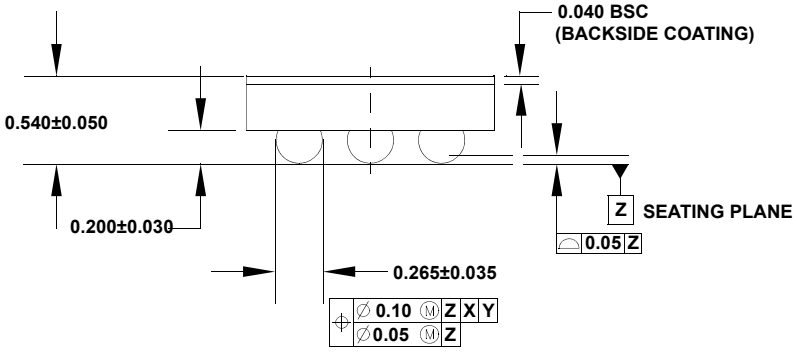
3X4 ARRAY 12 BALLS WITH 0.40 PITCH WAFER LEVEL CHIP SCALE PACKAGE (WLCSP) (BSC)

Rev 1, 1/13









NOTES:

1. All dimensions are in millimeters.
2. Dimensions and tolerance and tolerance per ASMEY 14.5 - 1994, and JESD 95-1 SPP-010.
3. NSMD refers to non-solder mask defined pad design per Intersil Tech Brief www.intersil.com/data/tb/tb451.pdf