

ISL95521

Hybrid Power Boost (HPB) and Narrow VDC (NVDC) Configurations Combo Battery Charger with SMBus Interface

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The [ISL95521](#) is a highly versatile combo battery charger configurable for operating as either a Hybrid Power Boost (HPB) charger or a Narrow VDC (NVDC) charger, supporting 2-, 3-, or 4-cell batteries. Both configurations allow the battery to work with the adapter together to supply the system load when it exceeds the adapter capability, referred to as system Turbo mode. The HPB charger configuration reverse-boosts battery energy to the system bus to help the adapter provide system power in Turbo mode. The NVDC charger configuration quickly turns on BGATE to enable the battery to help the adapter provide system power in Turbo mode.

The ISL95521 uses N-channel MOSFETs (NFETs) for all the switches to achieve the best performance and lowest BOM cost. The internal charge pump is capable of turning on all the NFETs fast or slow depending on the circumstance or the need. The ability to quickly turn on NFETs prevents system bus voltage drop when the battery is suddenly removed in Turbo mode or in battery learn mode.

The ISL95521 provides many protection features including a PROCHOT# indicator for system low voltage, adapter overcurrent, battery overcurrent or overheating, with an array of SMBus programmable parameters for maximum flexibility. The ISL95521 also features hardware based adapter current limit and battery-current limit in addition to SMBus programmable limits.

The ISL95521 provides high accuracy adapter current monitor, battery current monitor, and system power monitor outputs. To provide maximum flexibility for working with high power and low power systems, the ISL95521 provides several configurable current-sense resistor value options to achieve the best trade-off of current sensing accuracy vs power loss.

The ISL95521 uses the Renesas Robust Ripple Regulator (R3™) modulation scheme to provide excellent light-load efficiency and fast dynamic response. The ISL95521 is available in a 32 Ld 4mmx4mm QFN package.

Features

- Configurable as an HPB charger or NVDC charger
- Compliant with Intel PROCHOT# and PSYS requirements
- Adapter current monitor and battery discharging current monitor
- Uses NFET for all the switches
 - Supports battery removal during battery learn mode
 - Actively controlled inrush current to prevent FET damage
- SMBus programmable settings and high accuracy
- Comprehensive protection features;
 - PROCHOT# indicator for system low voltage, adapter overcurrent, battery overcurrent, and system overheating
 - Hardware-based adapter current and battery current limits
 - Supports sudden battery removal in system Turbo mode
- 16 switching frequency options from 350kHz to 1MHz
- Low quiescent current
- SMBus and auto-increment I²C compatible
- Robust Ripple Regulator (R3) modulation scheme provides excellent light-load efficiency and fast dynamic response
- 32 Ld 4mmx4mm QFN package
- Pb-free (RoHS compliant)

Applications

- Devices with rechargeable 2-, 3-, or 4-cell batteries

Related Literature

- [ISL95521](#) device page

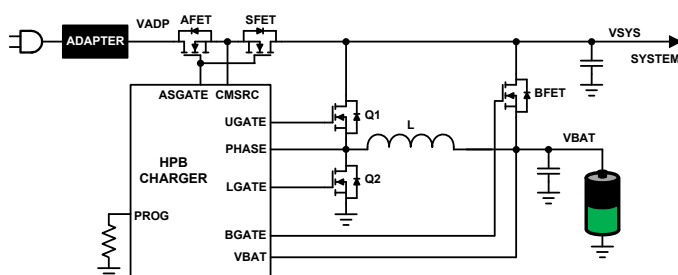


FIGURE 1. HPB CHARGER CONFIGURATION

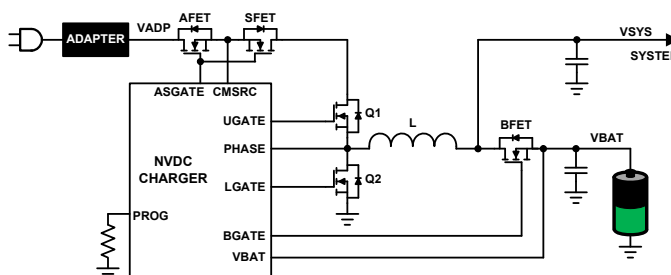


FIGURE 2. NVDC CHARGER CONFIGURATION

Table of Contents

Overview	4
Simplified Application Circuits	4
Block Diagram	8
Ordering Information	9
Pin Configuration	9
Pin Descriptions	10
Absolute Maximum Ratings	12
Thermal Information	12
Recommended Operating Conditions	12
Electrical Specifications	12
Typical Performance	19
General SMBus Architecture	24
Data Validity	24
START and STOP Conditions	24
Acknowledge	24
SMBus Transactions	24
Byte Format	24
SMBus and I ² C Compatibility	25
ISL95521 SMBus Commands	25
Setting Charging Current Limit	27
Setting Discharging Current Limit	27
Setting Adapter Current Limit	27
Setting Two-Level Adapter Current Limit Duration	28
Setting Maximum Charging Voltage	28
Setting Minimum Charging Voltage	28
Setting PROCHOT# Debounce Time	29
Setting PROCHOT# Duration	29
Setting PROCHOT# Threshold for Adapter Overcurrent Condition	29
Setting PROCHOT# Threshold for Battery Over Discharging Current Condition	30
Control Registers	30
Information Registers	34
Application Information	36
R3 Modulator	36
Programming Charger Options	37
Programming Switching Frequency	39
Soft-Start	39
Adapter Presence Detection and ACOK	41
Adapter Overvoltage Protection	41
Power Source Selection	41
Battery Learn Mode	41
HPB Charger Battery Learn Mode Entry/Exit	41
NVDC Charger Battery Learn Mode Entry/Exit	42
Hardware-Based Adapter Current Limit	42
HPB Charger Turbo Mode Support	42
NVDC Charger Turbo Mode Support	44
Two-Level Adapter Current Limit	44
Current Monitor	44
PSYS Monitor	44
Charger Timeout	44
Trickle Charging	44
NVDC Charger System Voltage Regulation	45
Over-Temperature Protection	45
Battery Overvoltage Protection	45
System Bus Short-Circuit Detection	46

Adapter Input Filter	46
Test with e-Load Constant Voltage Mode	46
General Application Information.....	46
Select the LC Output Filter	46
Select the Input Capacitor	47
Select the Switching Power MOSFET.....	47
Select the Bootstrap Capacitor	48
Select the DCIN Filter	48
Layout Guidelines	51
Revision History.....	53
Package Outline Drawing	54

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Overview

Simplified Application Circuits

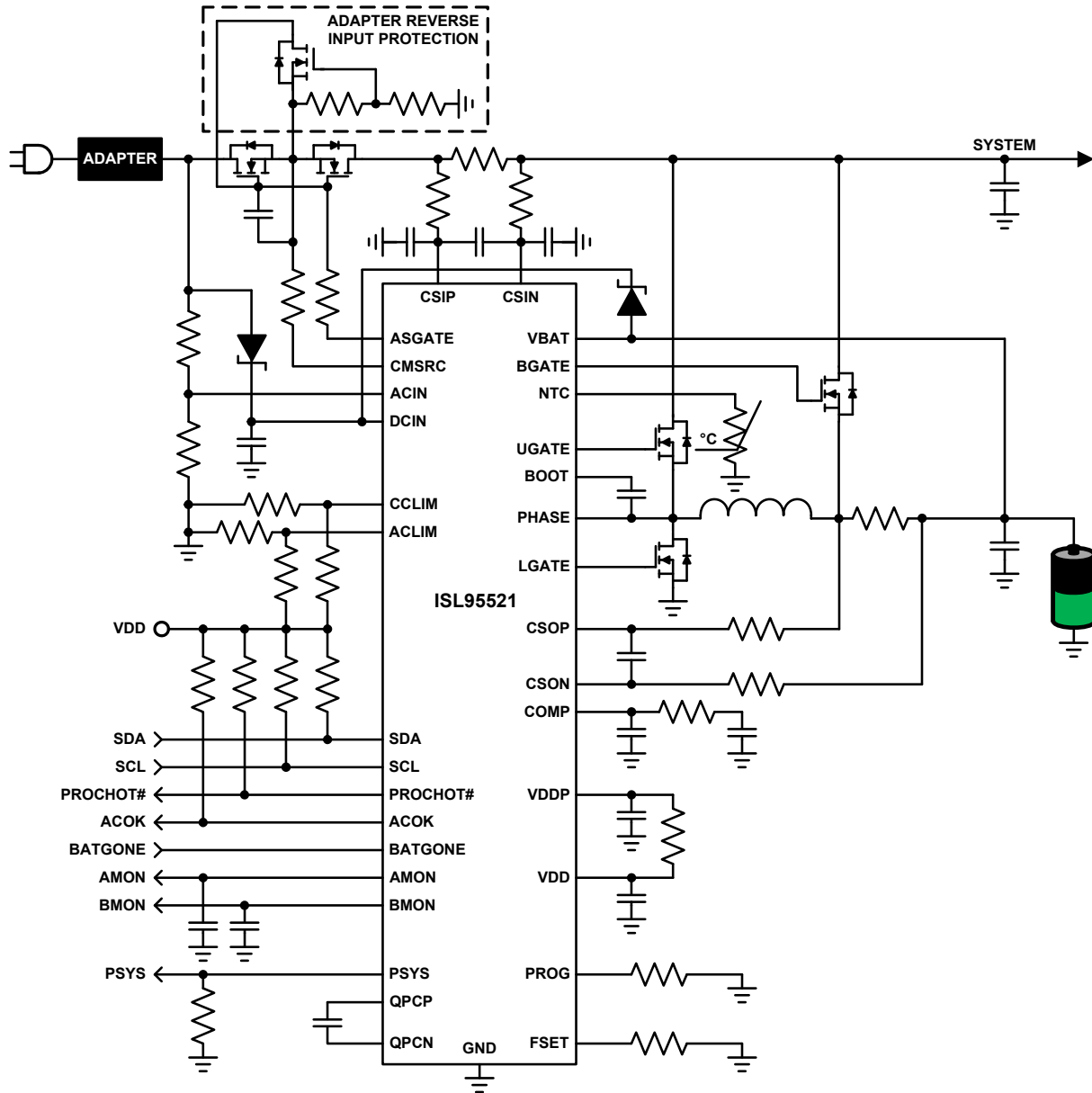


FIGURE 3. TYPICAL APPLICATION CIRCUIT: HPB CHARGER CONFIGURATION WITH TWO NMOS SELECTORS

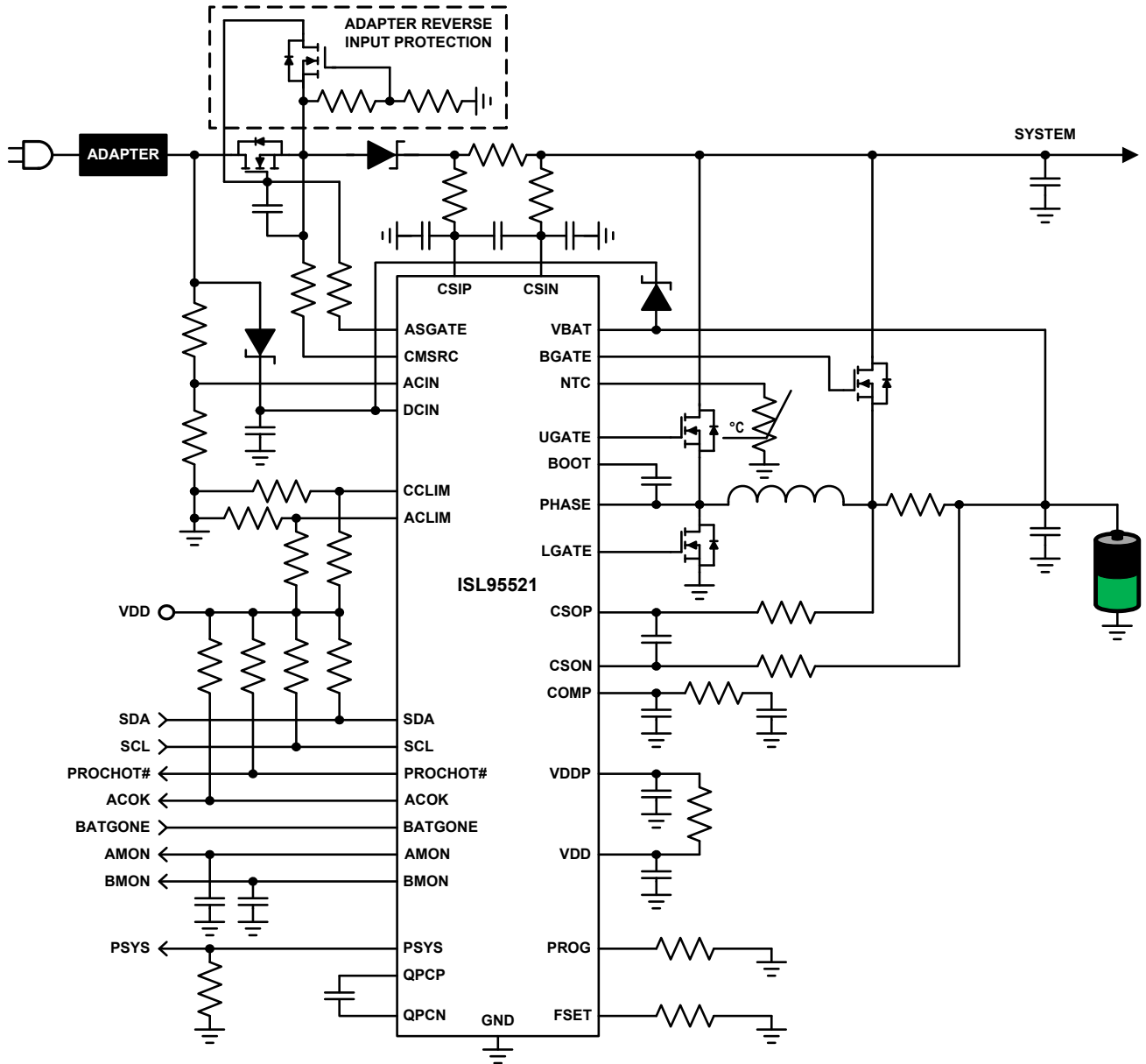


FIGURE 4. TYPICAL APPLICATION CIRCUIT: HPB CHARGER CONFIGURATION WITH ONE NMOS SELECTOR AND SCHOTTKY DIODE

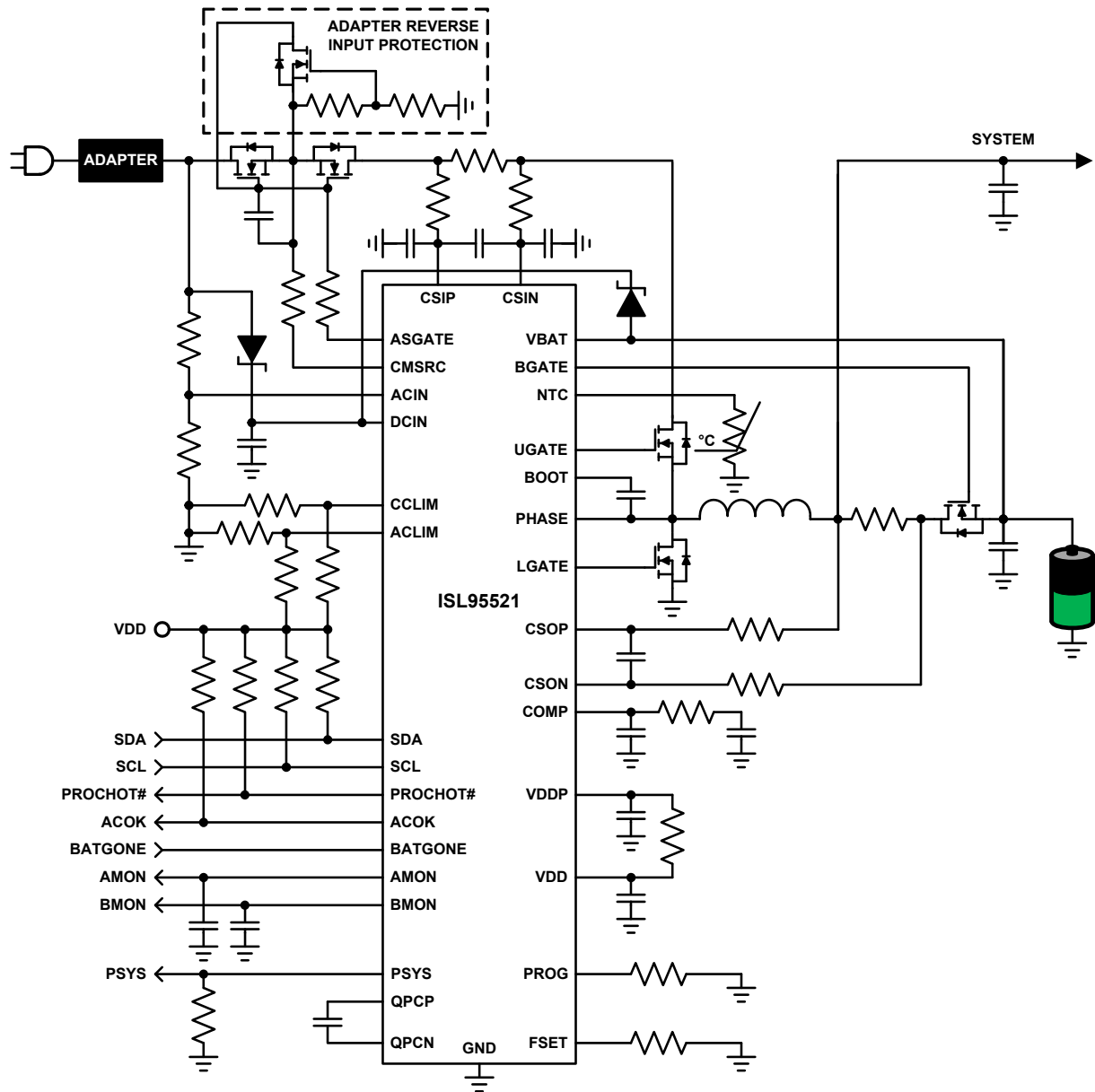


FIGURE 5. TYPICAL APPLICATION CIRCUIT: NVDC CHARGER CONFIGURATION WITH TWO NMOS SELECTORS

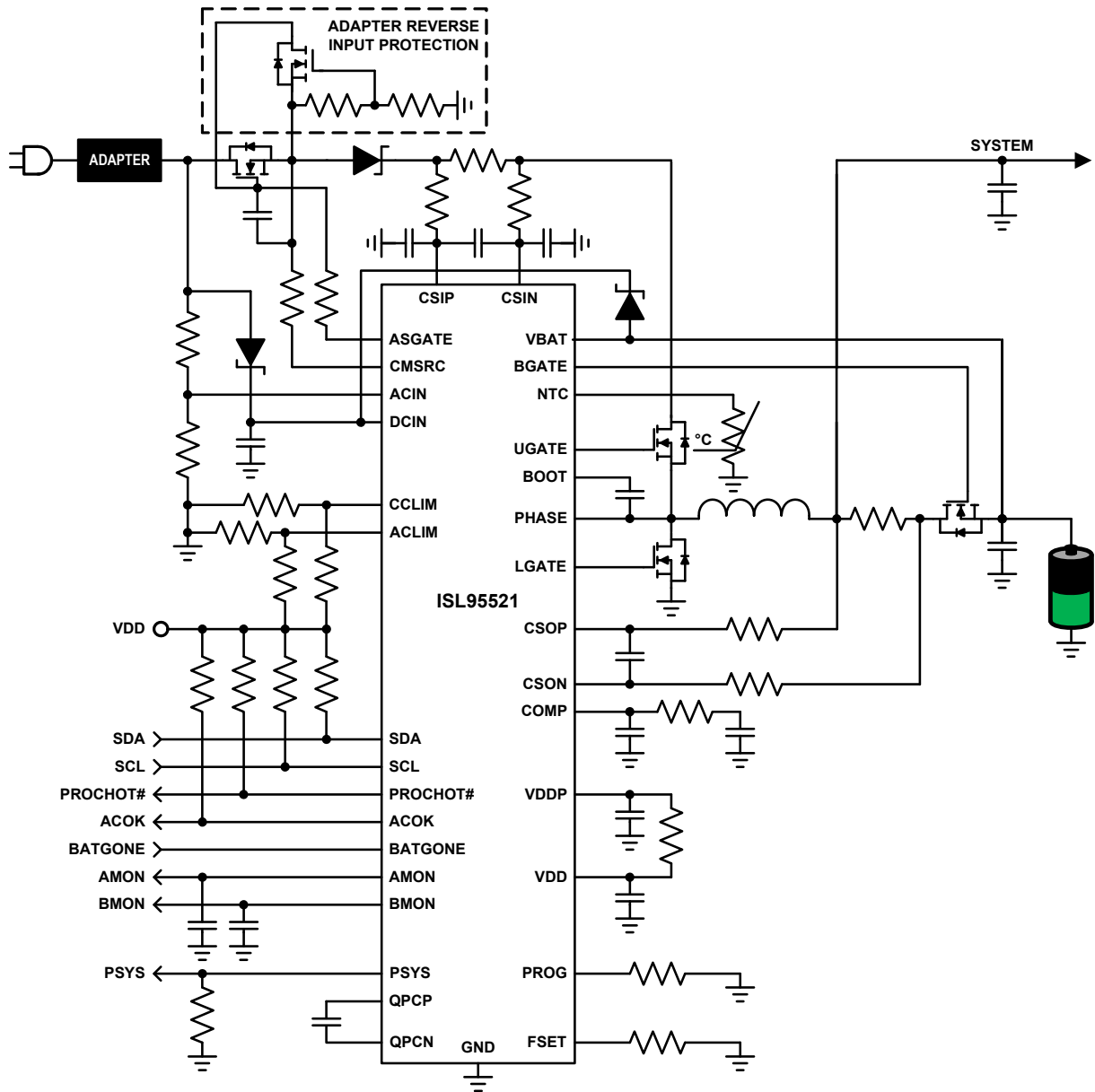


FIGURE 6. TYPICAL APPLICATION CIRCUIT: NVDC CHARGER CONFIGURATION WITH ONE NMOS SELECTOR AND SCHOTTKY DIODE

Block Diagram

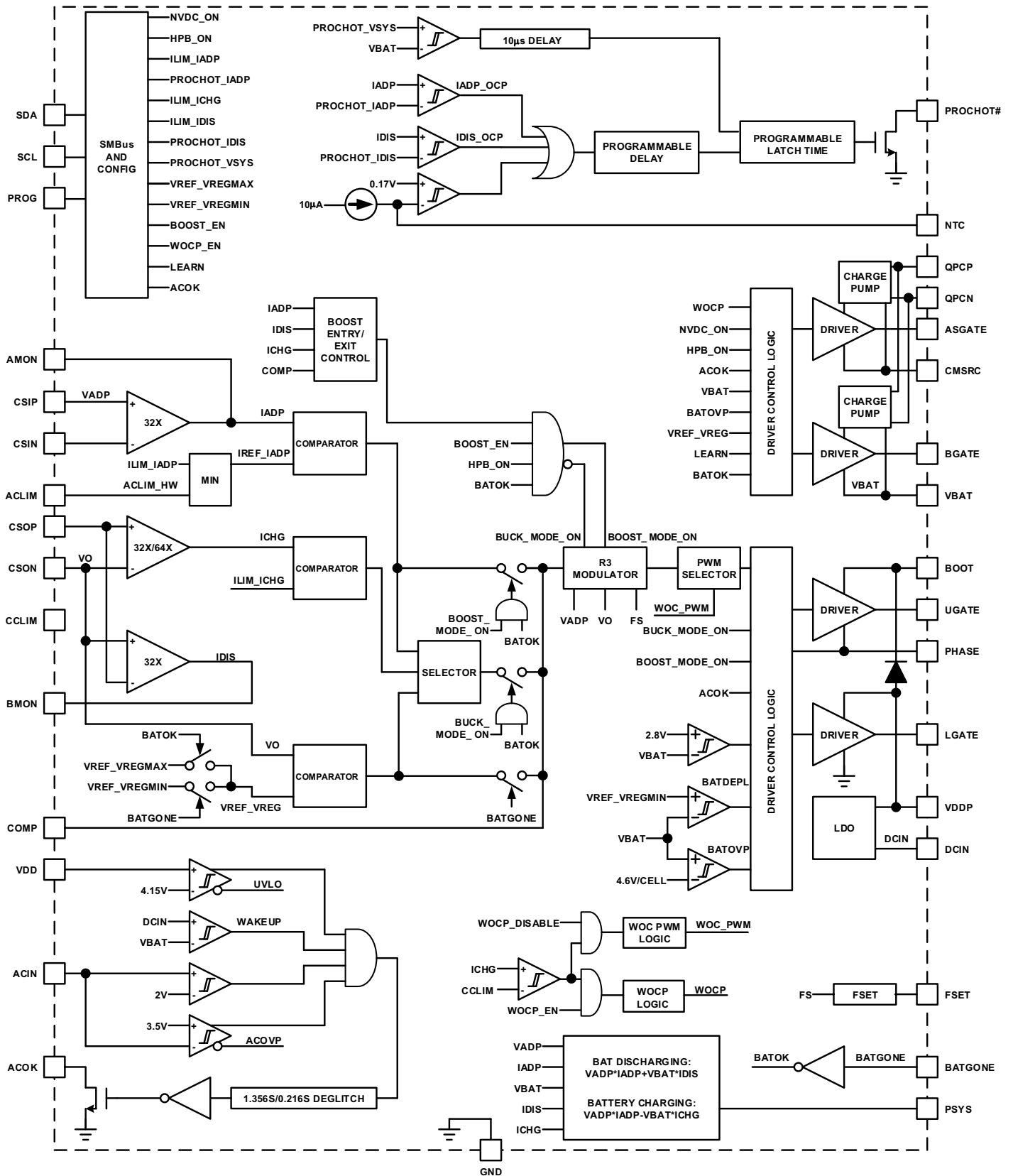


FIGURE 7. BLOCK DIAGRAM

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	Tape and Reel (Units) (Note 1)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL95521HRZ	955 21HRZ	0 to +85	-	32 Ld 4x4 QFN	L32.4x4A
ISL95521HRZ-T	955 21HRZ	0 to +85	6k	32 Ld 4x4 QFN	L32.4x4A

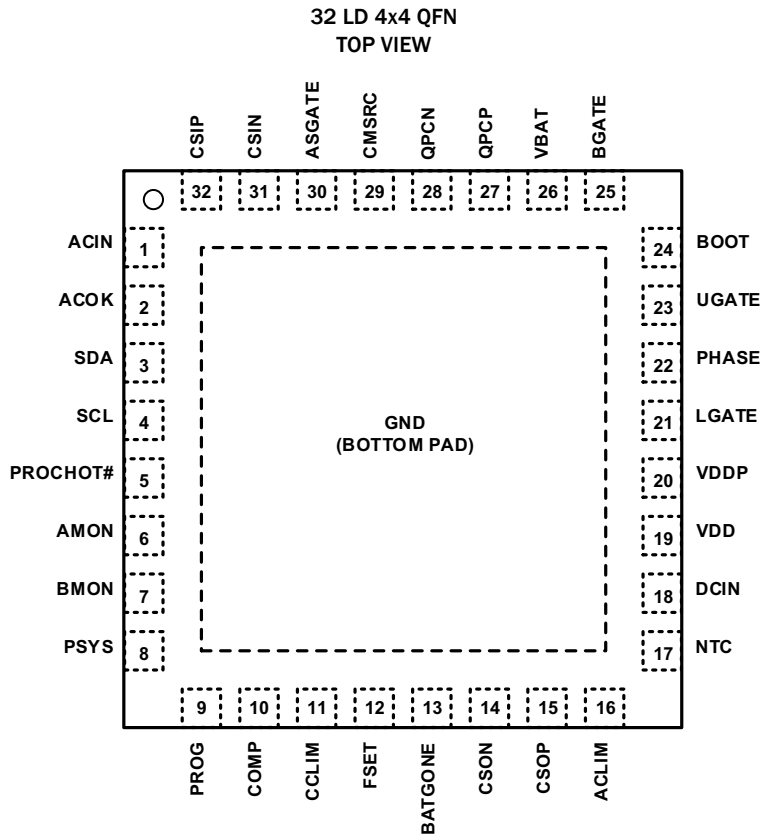
NOTES:

- See [TB347](#) for details about reel specifications.
- These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
- For Moisture Sensitivity Level (MSL), see the [ISL95521](#) device page. For more information about MSL, see [TB363](#).

TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

	CHARGING CURRENT WOCP FUNCTION	SMBus REGISTER ACCEPT ANY COMMAND	ACIN THRESHOLD
ISL95520	No	No	2.6V
ISL95521	Yes	Yes	2V

Pin Configuration



Pin Descriptions

PIN #	PIN NAME	DESCRIPTION
BOTTOM PAD	GND	Signal common of the IC. Unless otherwise stated, signals are referenced to the GND pin. It should also be used as the thermal pad for heat removal.
1	ACIN	Adapter voltage sense. The adapter voltage is "valid" if the ACIN pin voltage is between 2V and 3.5V. If the ACIN pin voltage exceeds 3.5V, the adapter voltage is in the overvoltage condition and the ISL95221 turns off the ASGATE MOSFETs to isolate the adapter from the system.
2	ACOK	Open-drain output to indicate adapter voltage is ready. Pulled low if the adapter voltage is not ready.
3	SDA	SMBus data I/O. Connect to the data line from the host controller or smart battery. Connect a 10kΩ pull-up resistor according to the SMBus specification.
4	SCL	SMBus clock I/O. Connect to the clock line from the host controller or smart battery. Connect a 10kΩ pull-up resistor according to the SMBus specification.
5	PROCHOT#	Open-drain output. Pulled low with SMBus programmable debounce time if any of the four conditions occur: <ol style="list-style-type: none"> 1. Adapter current reaches PROCHOT_IADP. 2. Battery discharging current reaches PROCHOT_IDIS. 3. System bus voltage is below the low system voltage detection threshold (programmable through SMBus). 4. NTC pin voltage is below 170mV. When asserted, it latches on for a minimum SMBus programmable time before it can be cleared.
6	AMON	Adapter current monitor output. $V_{AMON} = 32 \times (V_{CSIP} - V_{CSIN})$. Leave AMON pin floating if not used.
7	BMON	Battery discharging current monitor. $V_{BMON} = 32 \times (V_{CSOP} - V_{CSON})$. Leave BMON pin floating if not used.
8	PSYS	System power monitor output. Connect PSYS pin to GND if not used.
9	PROG	A resistor to GND sets the following configurations: <ol style="list-style-type: none"> 1. HPB charger or NVDC charger. 2. Default number of the battery cells in series. 3. Adapter current sense resistor and battery current sense resistor values. See Table 18 on page 37 for programming options. After POR, pulling PROG pin to 5V enables learn mode.
10	COMP	Error amplifier output. Connect compensation network externally from COMP to GND.
11	CCLIM	The voltage on this pin sets the WOCP threshold for the current flowing into the battery.
12	FSET	A resistor from this pin to GND programs the default switching frequency. See Table 21 on page 39 for programming options.
13	BATGONE	Battery presence indicator input pin to the ISL95521. Logic high indicates the battery has been removed. Logic low indicates the battery is present.
14	CSON	Battery current sense "-" input. Also senses the NVDC charger system voltage.
15	CSOP	Battery current sense "+" input.
16	ACLIM	The voltage on this pin sets the hardware-based adapter current limit. The lower value of the hardware-set adapter current limit and the SMBus set adapter current limit is the actual limit of the adapter current. The hardware-based adapter current limit also sets the regulated inrush current level for ASGATE MOSFET protection.
17	NTC	10μA current source output. Connect an NTC thermistor network from this pin to GND. If the NTC pin voltage is below 170mV, the ISL95521 pulls PROCHOT# low. Other than connecting an NTC thermistor network, this NTC pin comparator can be used as a general purpose comparator for the platform to use.
18	DCIN	Input of an internal 5V output LDO. Recommend connecting a diode-OR from adapter and battery. DCIN pin voltage needs to be higher than VBAT pin voltage for ASGATE to soft-start turning on. Connect a 10Ω DCIN resistor between the DCIN pin and the VADP/VSYS diodes, and connect a 4.7μF (50V) DCIN capacitor to GND. The capacitor must have an effective capacitance higher than 0.4μF at 20V.
19	VDD	5V power supply input for the ISL95521 control circuitry. Connect a 2.2μF (10V) MLCC capacitor to GND. The capacitor must have an effective capacitance higher than 0.4μF at 5V and x1.6 effective capacitance at the BOOT pin at 5V.
20	VDDP	Output of the internal 5V output LDO. The ISL95521 uses it as a FET driver power supply. Connect a 2.2μF (10V) MLCC capacitor to GND. The capacitor must have an effective capacitance higher than 0.4μF at 5V and x1.6 effective capacitance at the BOOT pin at 5V.
21	LGATE	Output of low-side switching FET gate drive. Connect this pin to the gate of the low-side switch FET.

Pin Descriptions (Continued)

PIN #	PIN NAME	DESCRIPTION
22	PHASE	Current return path for the high-side switching FET gate drive. Connect this pin to the node consisting of the high-side switch FET source, the low-side switch FET drain and the output inductor.
23	UGATE	Output of high-side switch FET gate drive. Connect this pin to the gate of the high-side switching FET.
24	BOOT	Connect an MLCC capacitor across the BOOT pin and the PHASE pin. The boot capacitor is charged through an internal bootstrap switch connected from the VDDP pin to the BOOT pin, when the PHASE pin drops below VDDP minus the voltage drop across the internal bootstrap switch. Connect a 0.47 μ F (25V) bootstrap capacitor, which must have an effective capacitance higher than 0.25 μ F at 5V and x50 effective high-side MOSFET gate capacitance.
25	BGATE	Output of the gate drive for the NFET connecting the system voltage and the battery. The behavior of the BGATE depends on whether the ISL95521 is in HPB charger configuration or NVDC charger configuration.
26	VBAT	Current return path for the BGATE gate drive. Also senses the battery voltage. Recommend connecting an RC filter at VBAT pin.
27	QPCP	Internal charge pump "+" input. Connect an MLCC capacitor across the QPCP pin and the QPCN pin.
28	QPCN	Internal charge pump "-" input. Connect an MLCC capacitor across the QPCP pin and the QPCN pin.
29	CMSRC	Common source node of the two back-to-back ASGATE NFETs.
30	ASGATE	Output of the gate drive for the two back-to-back NFETs.
31	CSIN	Adapter current sense "-" input.
32	CSIP	Adapter current sense "+" input. Also senses the input voltage.

Absolute Maximum Ratings

CSIP, CSIN, DCIN, CMSRC, QPCN	-0.3V to +28V
VBAT, CSOP, CSON	-0.3V to +28V
ASGATE, BGATE, QPCP	-0.3V to +33V
VDD, VDDP	-0.3V to +7V
CSIP-CSIN, CSOP-CSON	-0.3V to +0.3V
QPCP-QPCN	-0.3V to +7V
UGATE-PHASE	-0.3V to +7V
BOOT Voltage (BOOT)	-0.3V to +33V
BOOT to PHASE Voltage (BOOT-PHASE)	-0.3V to +7V (DC)
PHASE Voltage (PHASE)	-0.3V to +9V (<10ns)
UGATE Voltage (UGATE)	-0.3V to 28V
LGATE Voltage	-7V (<20ns Pulse Width, 10μJ)
PHASE-5V (<20ns Pulse Width, 10μJ) to BOOT	PHASE-0.3V (DC) to BOOT
Open Drain Outputs, ACOK, PROCHOT#	-0.3V to +7V
All Other Pins	-0.3V to (VDD +0.3V)
Latch-Up (Tested per JESD-78B)	Class 2, Level A

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
32 Ld QFN Package (Notes 4, 5)	39	3
Maximum Storage Temperature Range	-65°C to +150°C	
Maximum Junction Temperature (Plastic Package)	+150°C	
Pb-free Reflow Profile	see TB493	

Recommended Operating Conditions

Ambient Temperature	0°C to +85°C
Junction Temperature	0°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

- θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See [TB379](#).
- For θ_{JC} , the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications Operating Conditions: $V_{DD} = 5V$, $T_A = 0^\circ\text{C}$ to $+85^\circ\text{C}$ unless otherwise noted. **Boldface limits apply across the operating temperature range, 0°C to $+85^\circ\text{C}$.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
QUIESCENT CURRENT AND POR						
Battery Current	$I_{BAT_BGATE_OFF\ NVDC}$	Adapter present, BGATE off, $V_{BAT} = 16.8V$, DCIN current does not come from battery, $I_{BAT} = I_{VBAT}$		40	60	μA
	$I_{BAT_BGATE_ON\ NVDC}$	Battery only, BGATE on, $V_{BAT} = 16.8V$, DCIN current comes from battery, $I_{BAT} = I_{PHASE} + I_{VBAT} + I_{CSOP} + I_{CSON} + I_{DCIN} + I_{CMSRC}$		230	290	μA
	$I_{BAT_BGATE_OFF\ HPB}$	Adapter present, BGATE off, $V_{BAT} = 16.8V$, DCIN current does not come from battery, $I_{BAT} = I_{PHASE} + I_{VBAT} + I_{CSOP} + I_{CSON} + I_{CMSRC}$		115	160	μA
	$I_{BAT_BGATE_ON\ HPB}$	Battery only, BGATE on, $V_{BAT} = 16.8V$, DCIN current comes from battery, $I_{BAT} = I_{PHASE} + I_{VBAT} + I_{CSOP} + I_{CSON} + I_{DCIN} + I_{CSIP} + I_{CSIN} + I_{CMSRC}$		245	345	μA
Quiescent Current	$I_{DCIN_STANDBY\ HPB}$	VADP = 19.2V, AMON, BMON, PSYS all OFF		160	220	μA
	$I_{DCIN_NOSW_1\ HPB}$	VADP = 19.2V, no switching, AMON, BMON, PSYS all OFF		785	900	μA
	$I_{DCIN_NOSW_2\ HPB}$	VADP = 19.2V, no switching, AMON, BMON, PSYS all ON		1070	1250	μA
	$I_{DCIN_SW_H\ HPB}$	VADP = 19.2V, charge enabled, AMON, BMON, PSYS all OFF		1.52	1.82	mA
	$I_{DCIN_SW_N\ NVDC}$	VADP = 19.2V, charge enabled, AMON, BMON, PSYS all OFF		1.45	1.75	mA
VDD Power-on Reset (POR)	POR _{VDD_R}	VDD rising		4.66	4.75	V
	POR _{VDD_F}	VDD falling	4.35	4.44		mV

Electrical Specifications Operating Conditions: $V_{DD} = 5V$, $T_A = 0^\circ C$ to $+85^\circ C$ unless otherwise noted. **Boldface limits apply across the operating temperature range, $0^\circ C$ to $+85^\circ C$.** (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
CHARGING VOLTAGE LIMIT						
Maximum Charging Voltage Accuracy	V_{CHG_MAX}	MaxChargeVoltage = 0x41A0H (16.8V)		16.79		V
			-0.75		0.75	%
		MaxChargeVoltage = 0x3140H (12.608V)		12.6		V
			-0.75		0.75	%
		MaxChargeVoltage = 0x20D0H (8.4V)		8.4		V
			-0.5		0.5	%
Minimum Charging Voltage Accuracy (NVDC 450mV + MinChargeVoltage register setting)	V_{CHG_MIN}	MinChargeVoltage = 0x2A00H (10.752V)	11.02	11.2	11.4	V
		MinChargeVoltage = 0x2000H (8.192V)	8.48	8.64	8.84	V
		MinChargeVoltage = 0x1500H (5.376V)	5.68	5.825	6	V
BATTERY CURRENT LIMIT						
Battery Current Sense Amplifier Input Differential Voltage Range	V_{IBAT_RGE5}	$R_{S2} = 5m\Omega$, charging current ($V_{CSOP} - V_{CSON}$)	0		40.5	mV
	V_{IBAT_RGE10}	$R_{S2} = 10m\Omega$ or $R_{S2} = 20m\Omega$, charging current ($V_{CSOP} - V_{CSON}$)	0		81	mV
	V_{IBAT_RGED}	Discharging current ($V_{CSOP} - V_{CSON}$)	-81		0	mV
Charging Current Limit $R_{S2} = 10m\Omega$ $V_{BAT} > 4.5V$	I_{CHG_ACC10}	ChargeCurrentLimit = 0x1F20H (7968mA)		8030		mA
			-2	0.8	3.5	%
		ChargeCurrentLimit = 0x0FA0H (4000mA)		4040		mA
			-2.2	1	4	%
		ChargeCurrentLimit = 0x07E0H (2016mA)		2050		mA
			-3	1.7	6	%
		ChargeCurrentLimit = 0x03E0H (992mA)		1020		mA
			-3.7	2.8	9.2	%
Charging Current Limit $R_{S2} = 5m\Omega$ $V_{BAT} > 4.5V$	I_{CHG_ACC5}	ChargeCurrentLimit = 0x1F20H (7968mA)		8040		mA
			-2.3	0.9	3.9	%
		ChargeCurrentLimit = 0x0FA0H (4000mA)		4045		mA
			-2.9	1.1	4.6	%
		ChargeCurrentLimit = 0x07E0H (2016mA)		2050		mA
			-4.3	1.7	7	%
		ChargeCurrentLimit = 0x03E0H (992mA)		1020		mA
			-7.4	2.8	12	%
Charging Current Limit $R_{S2} = 5m\Omega$ $V_{BAT} > 4.5V$	I_{CHG_ACC5}	ChargeCurrentLimit = 0x0200H (512mA)		536		mA
			-13.9	4.7	20.4	%
		ChargeCurrentLimit = 0x0100H (256mA) (Not trickle charging mode current)		265		mA
		-34	3.5	35	%	

Electrical Specifications Operating Conditions: $V_{DD} = 5V$, $T_A = 0^\circ C$ to $+85^\circ C$ unless otherwise noted. **Boldface limits apply across the operating temperature range, $0^\circ C$ to $+85^\circ C$.** (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
Trickle Charging Current Limit	$I_{TRKL_ACC10_256}$	$R_{S2} = 10m\Omega$, $V_{BAT} < MinChargeVoltage$	223	275	327	mA
	$I_{TRKL_ACC10_128}$	$R_{S2} = 10m\Omega$, $V_{BAT} < MinChargeVoltage$	95	145	198	mA
	$I_{TRKL_ACC5_256}$	$R_{S2} = 5m\Omega$, $V_{BAT} < MinChargeVoltage$	180	270	357	mA
	$I_{TRKL_ACC5_128}$	$R_{S2} = 5m\Omega$, $V_{BAT} < MinChargeVoltage$	52	140	228	mA
VBAT Trickle Charging Threshold	$V_{TRKL_TH_R}$	MinChargeVoltage = 4.096V, exit trickle charging mode		4.39	4.57	V
	$V_{TRKL_TH_F}$	MinChargeVoltage = 4.096V, enter trickle charging mode	3.85	4.03		V
Discharging Current PROCHOT# Threshold $R_{S2} = 5m\Omega$	$I_{DIS_HOT_TH5}$	DCProchot = 0x2A00H (10752mA)		10848		mA
			-3.5	0.9	5.3	%
		DCProchot = 0x1500H (5376mA)		5450		mA
			-6.4	1.4	9.2	%
ADAPTER CURRENT LIMIT						
Adapter Current Sense Amplifier Input Differential Voltage Range	V_{IADP_RGE}	$R_{S1} = 10m\Omega$ or $R_{S1} = 20m\Omega$, adapter current ($V_{CSIP} - V_{CSIN}$)	0		81	mV
Adapter Current Limit $R_{S1} = 10m\Omega$	I_{ADP_10}	AdapterCurrentLimit = 0x1F20H (8064mA)		8115		mA
			-1.2	0.6	2.5	%
		AdapterCurrentLimit = 0x1000H (4096mA)		4140		mA
			-1.3	1.1	3.5	%
		AdapterCurrentLimit = 0x0800H (2048mA)		2075		mA
			-2.5	1.3	5.2	%
		AdapterCurrentLimit = 0x0400H (1024mA)		1055		mA
			-4	3	10	%
Adapter Current PROCHOT# Threshold $R_{S1} = 10m\Omega$	$I_{ADP_HOT_TH10}$	ACProchot = 0x1500H (5376mA)		5389		mA
			-3.5	0.25	4	%
		ACProchot = 0x0A80H (2688mA)		2728		mA
			-7	1.5	10	%

Electrical Specifications Operating Conditions: $V_{DD} = 5V$, $T_A = 0^\circ C$ to $+85^\circ C$ unless otherwise noted. **Boldface limits apply across the operating temperature range, $0^\circ C$ to $+85^\circ C$.** (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
MONITOR						
AMON Accuracy $V_{AMON} = 32 \times (V_{CSIP} - V_{CSIN})$ $R_{s1} = 10m\Omega$	V_{AMON}	$V_{CSIP} - V_{CSIN} = 80mV$		2544		mV
			-2.5	-0.6	1.3	%
		$V_{CSIP} - V_{CSIN} = 40mV$		1269		mV
			-3.5	-0.85	1.8	%
		$V_{CSIP} - V_{CSIN} = 20mV$		632		mV
			-6	-1.25	3.5	%
		$V_{CSIP} - V_{CSIN} = 10mV$		313		mV
			-10	-2.2	6.6	%
		$V_{CSIP} - V_{CSIN} = 5mV$		154		mV
			-19.5	-3.75	12.5	%
AMON Current Sourcing Capability	$I_{AMON_MAX_SR}$		255	515	800	μA
AMON Current Sinking Capability	$I_{AMON_MAX_SK}$		12	22	32	μA
BMON Accuracy $V_{BMON} = 32 \times (V_{CSOP} - V_{CSIN})$ $R_{s2} = 10m\Omega$	V_{BMON}	$V_{CSOP} - V_{CSIN} = 80mV$		2.603		mV
			-2	1.65	5.4	%
		$V_{CSOP} - V_{CSIN} = 40mV$		1300		mV
			-3	1.55	6	%
		$V_{CSOP} - V_{CSIN} = 20mV$		649		mV
			-5	1.4	8	%
		$V_{CSOP} - V_{CSIN} = 10mV$		327		mV
			-7	2.2	12	%
BMON Current Sourcing Capability	$I_{BMON_MAX_SR}$		120	285	460	μA
BMON Current Sinking Capability	$I_{BMON_MAX_SK}$		5.5	11.4	17.5	μA
PSYS Output Current $R_{s1} = 10m\Omega$ $R_{s2} = 10m\Omega$ PSYS Current Gain = $1.14\mu A/W$	I_{PSYS}	$V_{CSIP} = 19V$, $V_{CSIP} - V_{CSIN} = 80mV$, $V_{BAT} = 12V$, $V_{CSOP} - V_{CSON} = 0mV$		174		μA
			-8.3	0.4	9.1	%
		$V_{CSIP} = 19V$, $V_{CSIP} - V_{CSIN} = 80mV$, $V_{BAT} = 12V$, $V_{CSOP} - V_{CSON} = 20mV$		146.5		μA
			-8.2	0.4	9	%
		$V_{CSIP} = 19V$, $V_{CSIP} - V_{CSIN} = 80mV$, $V_{BAT} = 12V$, $V_{CSOP} - V_{CSON} = -20mV$		199.5		μA
			-8.4	-0.6	7.2	%
		$V_{CSIP} = 0V$, $V_{CSIP} - V_{CSIN} = 0mV$, $V_{BAT} = 12V$, $V_{CSOP} - V_{CSON} = -20mV$		26.2		μA
			-15.2	-4.2	6.8	%
Maximum PSYS Output Voltage	V_{PSYS_MAX}	$I_{PSYS} = 200\mu A$		1.5		V
NTC Source Current	I_{NTC}	NTC = 1V	9.71	10.08	10.44	μA
NTC_PROCHOT# Trip Threshold	V_{NTC_TH}	V_{NTC} falling	161	171	182	mV
NTC_PROCHOT# Hysteresis	V_{NTC_HYS}		18	27	36	mV
ACIN/ACOK COMPARATOR						
ACIN Threshold Rising	$V_{ACIN_TH_R}$	V_{ACIN} rising		2.03	2.15	V
ACIN Threshold Falling	$V_{ACIN_TH_F}$	V_{ACIN} falling	1.9	2		V
ACIN OVP Rising	$V_{ACIN_OVP_TH_R}$	V_{ACIN} rising		3.5	3.7	V

Electrical Specifications Operating Conditions: $V_{DD} = 5V$, $T_A = 0^\circ C$ to $+85^\circ C$ unless otherwise noted. **Boldface limits apply across the operating temperature range, $0^\circ C$ to $+85^\circ C$.** (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
ACIN OVP Falling	$V_{ACIN_OVP_TH_F}$	V_{ACIN} falling	3.3	3.45		V
ACIN Input Leakage Current	I_{ACIN_LEAK}		-1		1	μA
ACOK Input Leakage Current	I_{ACOK_LEAK}		-1		1	μA
ACOK Output Low Current	I_{ACOK}	$V_{ACOK} = 0.3V$		240		μA
ACLIM, CCLIM						
ACLIM Current Limit		$V_{ACLIM} = 2.56V$, $R_{S1} = 10m\Omega$	7970	8075	8175	mA
		$V_{ACLIM} = 1.92V$, $R_{S1} = 10m\Omega$	5970	6060	6150	mA
		$V_{ACLIM} = 1.28V$, $R_{S1} = 10m\Omega$	3975	4050	4125	mA
CCLIM Current Limit		$V_{CCLIM} = 2.56V$, $R_{S1} = 10m\Omega$, $R_{S2} = 5m\Omega$	7855	8070	8265	mA
		$V_{CCLIM} = 1.92V$, $R_{S1} = 10m\Omega$, $R_{S2} = 5m\Omega$	5875	6050	6205	mA
		$V_{CCLIM} = 1.28V$, $R_{S1} = 10m\Omega$, $R_{S2} = 5m\Omega$	3900	4035	4155	mA
		$V_{CCLIM} = 2.56V$, $R_{S1} = 10m\Omega$, $R_{S2} = 10m\Omega$	7860	8065	8250	mA
		$V_{CCLIM} = 1.92V$, $R_{S1} = 10m\Omega$, $R_{S2} = 10m\Omega$	5895	6045	6185	mA
		$V_{CCLIM} = 1.28V$, $R_{S1} = 10m\Omega$, $R_{S2} = 10m\Omega$	3930	4035	4135	mA
		$V_{CCLIM} = 2.56V$, $R_{S1} = 20m\Omega$, $R_{S2} = 20m\Omega$	3930	4030	4130	mA
		$V_{CCLIM} = 1.92V$, $R_{S1} = 20m\Omega$, $R_{S2} = 20m\Omega$	2945	3025	3100	mA
		$V_{CCLIM} = 1.28V$, $R_{S1} = 20m\Omega$, $R_{S2} = 20m\Omega$	1960	2015	2075	mA
PROCHOT#						
PROCHOT# Leakage Current	$I_{PROCHOT\#_LEAK}$		-1		1	μA
PROCHOT# Output Low Current	$I_{PROCHOT\#}$	$V_{PROCHOT\#} = 0.3V$		33		mA
Low VSYS PROCHOT# Trip Threshold	$V_{LOW_VSYS_HOT}$	Control1 register Bit<9:8> = 00	5.48	5.62	5.76	V
		Control1 register Bit<9:8> = 01	5.97	6.11	6.25	V
		Control1 register Bit<9:8> = 10	6.44	6.59	6.73	V
		Control1 register Bit<9:8> = 11	6.9	7.05	7.2	V
PROCHOT# Debounce Time		Prochot# Debounce register Bit<1:0> = 01		102		μs
		Prochot# Debounce register Bit<1:0> = 10		510		μs
PROCHOT# Duration Time		Prochot# Duration register Bit<2:0> = 010		15.3		ms
		Prochot# Duration register Bit<2:0> = 101		1.02		ms
BATGONE THRESHOLD						
BATGONE Threshold Rising	$V_{BATGONE_TH_R}$	$V_{BATGONE}$ rising (battery removal)		2.58	2.75	V
BATGONE Threshold Falling	$V_{BATGONE_TH_F}$	$V_{BATGONE}$ falling (battery insertion)	1.8	2.12		V
LDO						
Output Voltage		$V_{DCIN} = 6V$ to $25V$, $I_{VDDP} = 1mA$	4.8	5.24	5.75	V
		$V_{DCIN} = 6V$, $I_{VDDP} = 30mA$	4.65	5.12	5.65	V
		$V_{DCIN} = 25V$, $I_{VDDP} = 30mA$	4.75	5.22	5.7	V
GATE DRIVER						
UGATE Pull-Up Resistance (Note 7)	R_{UGPU}	200mA source current		1.0	1.5	Ω
UGATE Source Current (Note 7)	I_{UGSRC}	UGATE - PHASE = 2.5V		2.0		A
UGATE Sink Resistance (Note 7)	R_{UGPD}	250mA sink current		1.0	1.5	Ω

Electrical Specifications Operating Conditions: $V_{DD} = 5V$, $T_A = 0^{\circ}C$ to $+85^{\circ}C$ unless otherwise noted. **Boldface limits apply across the operating temperature range, $0^{\circ}C$ to $+85^{\circ}C$.** (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
UGATE Sink Current (Note 7)	I_{UGSNK}	UGATE - PHASE = 2.5V		2.0		A
LGATE Pull-Up Resistance (Note 7)	R_{LGPU}	250mA source current		1.0	1.5	Ω
LGATE Source Current (Note 7)	I_{LGSRC}	LGATE - GND = 2.5V		2.0		A
LGATE Sink Resistance (Note 7)	R_{LGPD}	250mA sink current		0.5	0.9	Ω
LGATE Sink Current (Note 7)	I_{LGSNK}	LGATE - GND = 2.5V		4.0		A
UGATE to LGATE Dead Time	t_{UGFLGR}	UGATE falling to LGATE rising, no load		17		ns
LGATE to UGATE Dead Time	t_{LGFUGR}	LGATE falling to UGATE rising, no load		29		ns
ASGATE Pull-Up Resistance	R_{ASGPU}	1mA source current		500		Ω
ASGATE Sink Resistance	R_{ASGPD}	1mA sink current		1300		Ω
BGATE Pull-Up Resistance	R_{BGPU}	1mA source current		500		Ω
BGATE Sink Resistance	R_{BGPD}	1mA sink current		1300		Ω
BOOTSTRAP SWITCH						
ON-Resistance	R_F			20		Ω
Reverse Leakage	I_R	$V_R = 25V$		0.2		μA
AMPLIFIERS						
Adapter Current Sense Amplifier Input Offset (Note 7)	V_{ACSNS_OFFSET}			0.4		mV
Battery Charging Current Sense Amplifier Input Offset (Note 7)	$V_{ICHGSNS_OFFSET}$			0.4		mV
Battery Discharging Current Sense Amplifier Input Offset (Note 7)	$V_{IDISSNS_OFFSET}$			0.4		mV
Error Amplifier DC Gain (Note 7)	A_{VO_EA}			80		dB
Error Amp Gain-bandwidth Product (Note 7)	GBW_EA	$C_L = 20pF$		5		MHz
COMP Lower Clamp	$V_{COMP_L_CLP}$			1.24	1.4	V
COMP Upper Clamp	$V_{COMP_U_CLP}$		4.9	4.99		V
Over-Temperature Protection						
Over-Temperature Threshold (Note 7)	T_{OTP_R}	Temperature rising		155		$^{\circ}C$
	T_{OTP_F}	Temperature falling		128		$^{\circ}C$
SMBUS						
SDA/SCL Input Low Voltage					0.8	V
SDA/SCL Input High Voltage			2			V
SDA/SCL Input Bias Current		SDA, SCL = 0V, 5V	-1		1	μA
SDA, Output Sink Current (Note 8)		SDA = 0.4V		19		mA
SMBus Frequency	f_{SMB}	Note 8	10		400	kHz
Bus Free Time	t_{BUF}	100kHz, Note 8	4.7			μs
		400kHz, Note 8	1.3			μs
Start Condition Hold Time from SCL	t_{HD_STA}	100kHz, Note 8	4			μs
		400kHz, Note 8	0.6			μs

Electrical Specifications Operating Conditions: $V_{DD} = 5V$, $T_A = 0^\circ C$ to $+85^\circ C$ unless otherwise noted. **Boldface limits apply across the operating temperature range, $0^\circ C$ to $+85^\circ C$.** (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
Start Condition Set-Up Time from SCL	t_{SU_STA}	100kHz, Note 8	4.7			μs
		400kHz, Note 8	0.6			μs
Stop Condition Set-Up Time from SCL	t_{HD_STO}	100kHz, Note 8	4			μs
		400kHz, Note 8	0.6			μs
SDA Hold Time from SCL	t_{HD_DAT}	100kHz, Note 8	300			ns
		400kHz, Note 8	300			ns
SDA Set-Up Time from SCL	t_{SU_DAT}	100kHz, Note 8	250			ns
		400kHz, Note 8	100			ns
SCL Low Period	t_{LOW}	100kHz, Note 8	4.7			μs
		400kHz, Note 8	1.3			μs
SCL High Period	t_{HIGH}	100kHz, Note 8	4			μs
		400kHz, Note 8	0.6			μs
SDA/SCL Rise Time	t_{RISE}	100kHz, 400pF, maximum load, Note 8			1000	ns
		400kHz, 400pF, maximum load, Note 8			300	ns
SDA/SCL Fall Time	t_{FALL}	100kHz, 400pF, maximum load, Note 8			300	ns
		400kHz, 400pF, maximum load, Note 8			300	ns
SMBus Inactivity Time-Out (Note 8)		Maximum period without a SMBus write to MaxChargeVoltage or ChargeCurrent register		175		s

NOTES:

- Parameters with MIN and/or MAX limits are 100% tested at $+25^\circ C$, unless otherwise specified. Temperature limits established by characterization and are not production tested.
- Limits established by characterization and are not production tested.
- Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

Gate Driver Timing Diagram

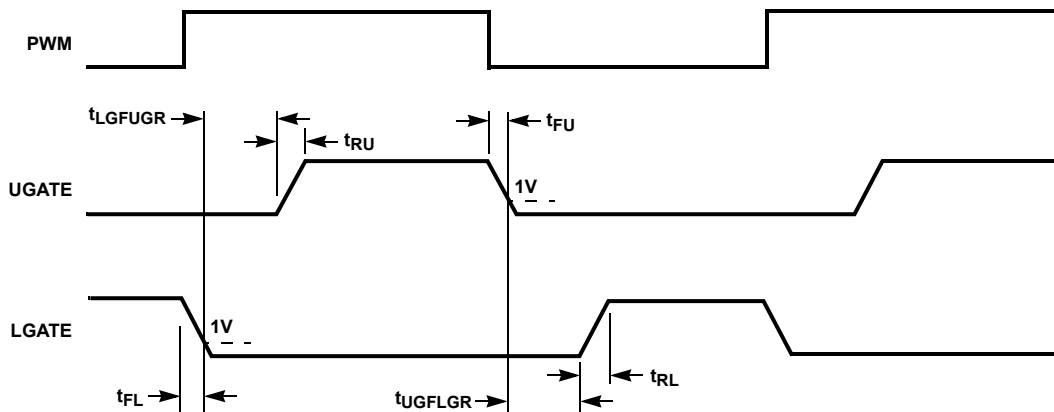


FIGURE 8. GATE DRIVER TIMING DIAGRAM

Typical Performance

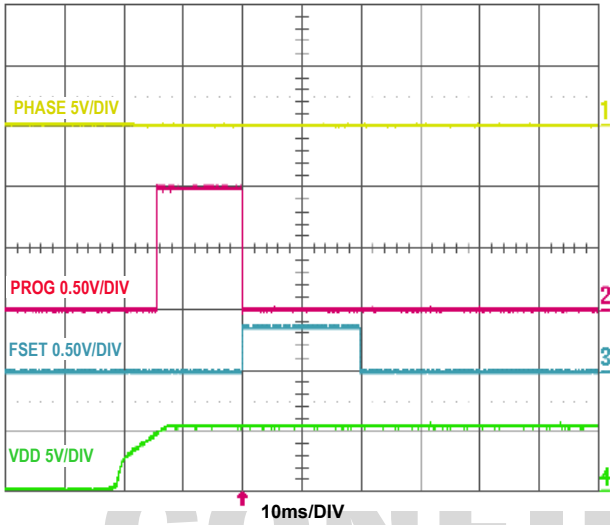


FIGURE 9. POWER-UP, READ PROG AND FSET RESISTORS

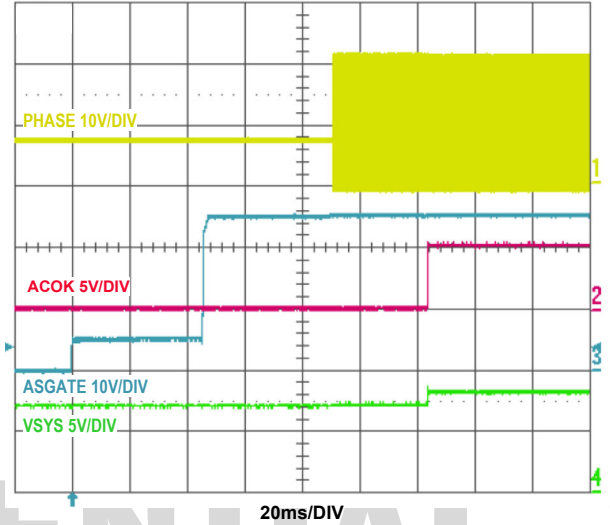


FIGURE 10. NVDC: ADAPTER INSERTION START-UP SEQUENCE

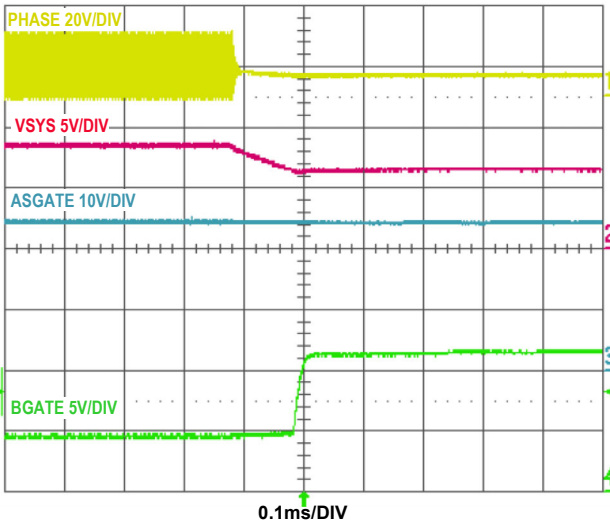


FIGURE 11. NVDC: ENTER LEARN MODE

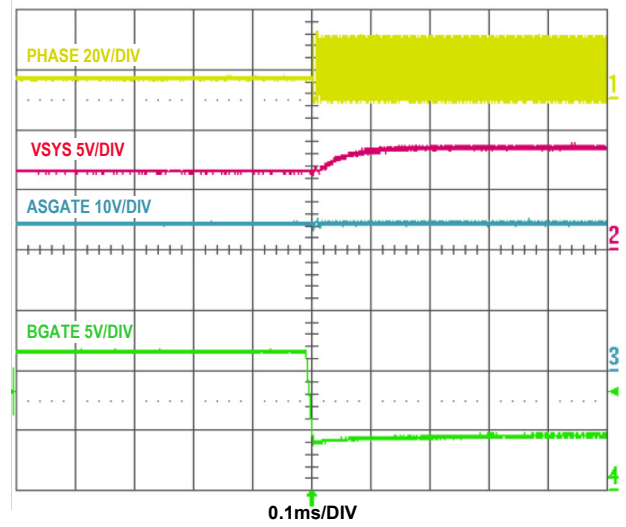


FIGURE 12. NVDC: EXIT LEARN MODE

Typical Performance (Continued)

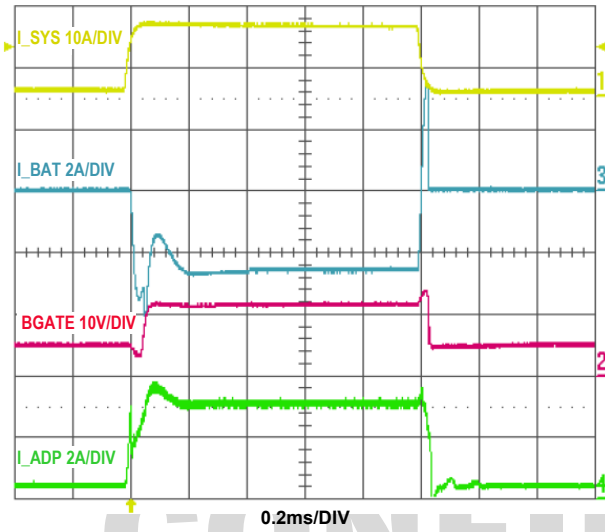


FIGURE 13. NVDC: SYSTEM VOLTAGE REGULATION LOOP AND TURBO MODE TRANSIENT. VADP = 20V, ADAPTERCURRENTLIMIT1 = 3.072A, V_{BAT} = 7V, MAXCHARGEVOLTAGE = 8.192V, 1A TO 12A SYSTEM LOAD STEP

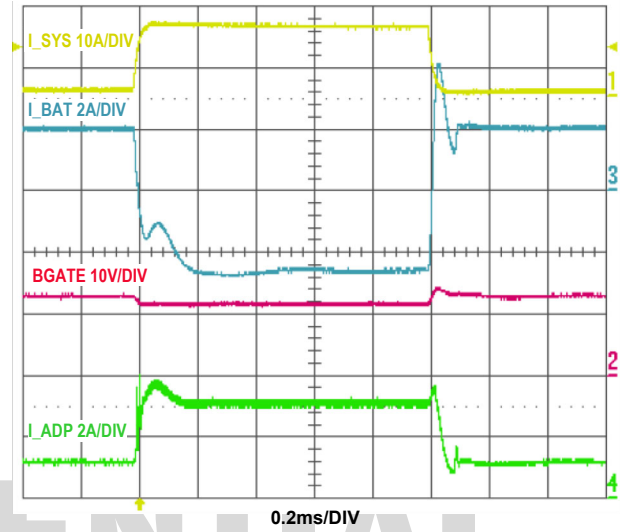


FIGURE 14. NVDC: CHARGING CURRENT LIMIT LOOP AND TURBO MODE TRANSITION. VADP = 20V, ADAPTERCURRENTLIMIT1 = 3.072A, V_{BAT} = 7V, MAXCHARGEVOLTAGE = 8.192V, CHARGECURRENT = 2.016A, 1A TO 12A SYSTEM LOAD STEP

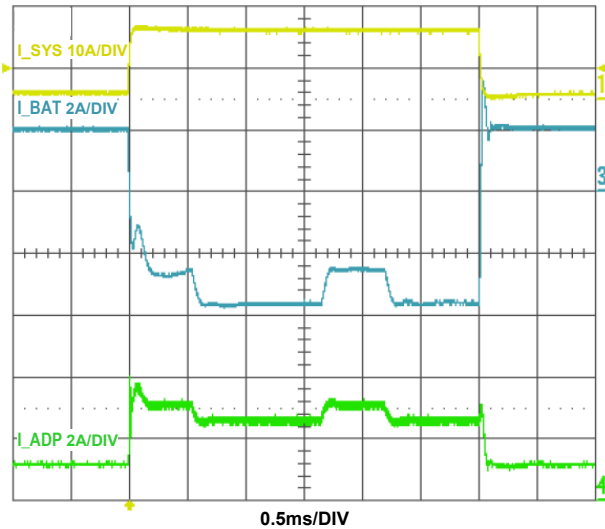


FIGURE 15. TWO LEVEL ADAPTER CURRENT LIMIT. VADP = 20V, ADAPTERCURRENTLIMIT1 = 2.56A, ADAPTERCURRENTLIMIT2 = 3.072A, T₂ = 500μs, T₁ = 1ms, V_{BAT} = 7V, MAXCHARGEVOLTAGE = 8.192V, CHARGECURRENT = 2.016A, 1A TO 12A SYSTEM LOAD STEP

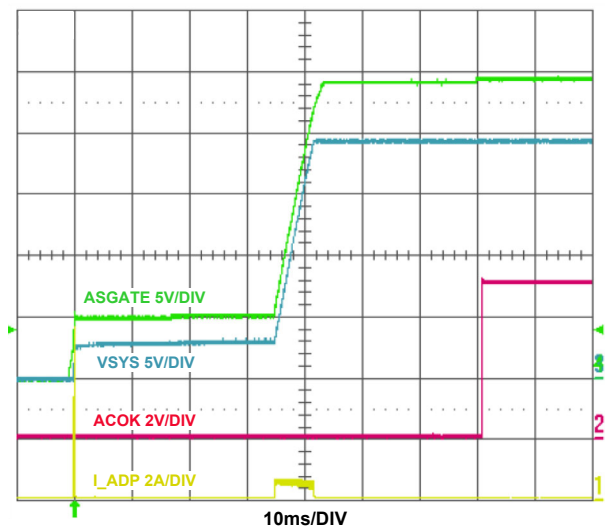


FIGURE 16. HPB: ADAPTER INSERTION ASGATE IN-RUSH CURRENT CONTROL. NO BATTERY, VADP = 20V, 330μF SYSTEM RAIL CAPACITANCE

Typical Performance (Continued)

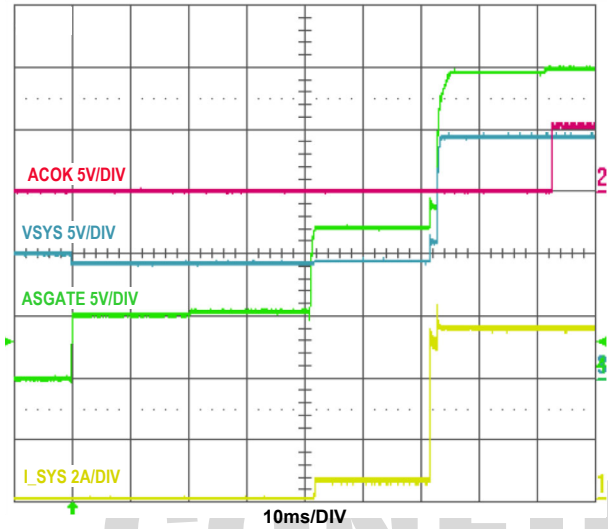


FIGURE 17. HPB: ADAPTER INSERTION ASGATE INRUSH CURRENT CONTROL. $V_{BAT} = 10V$, $V_{ADP} = 20V$, $ACLIM$ SETTING = 5A, SYSTEM LOAD = 5.5A

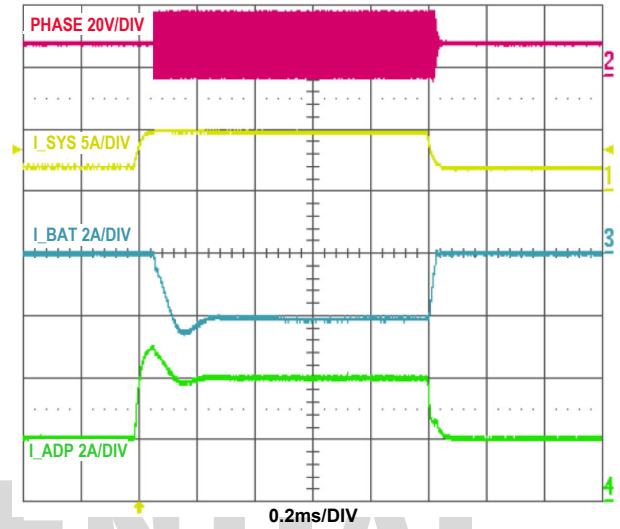


FIGURE 18. HPB: CHARGE DISABLED, ENTER TURBO MODE. $V_{ADP} = 20V$, $V_{BAT} = 10V$, $ADAPTERCURRENTLIMIT1 = 4.096A$, 2A TO 5A LOAD STEP

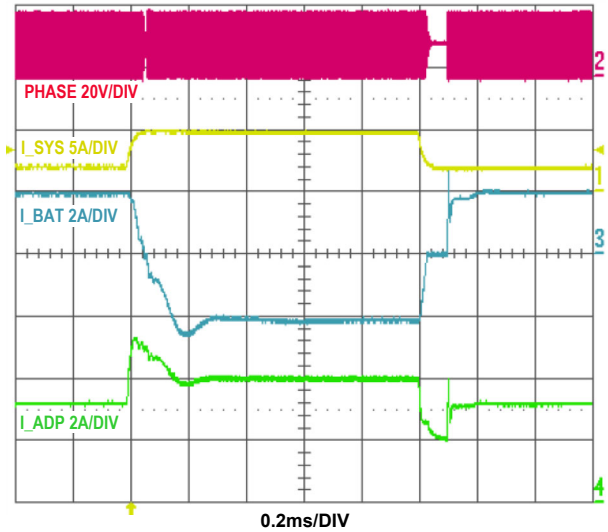


FIGURE 19. HPB: CHARGE ENABLED, ENTER TURBO MODE. $V_{ADP} = 20V$, $V_{BAT} = 10V$, $ADAPTERCURRENTLIMIT1 = 4.096A$, $CHARGECURRENT = 2.016A$, 2A TO 5A LOAD STEP

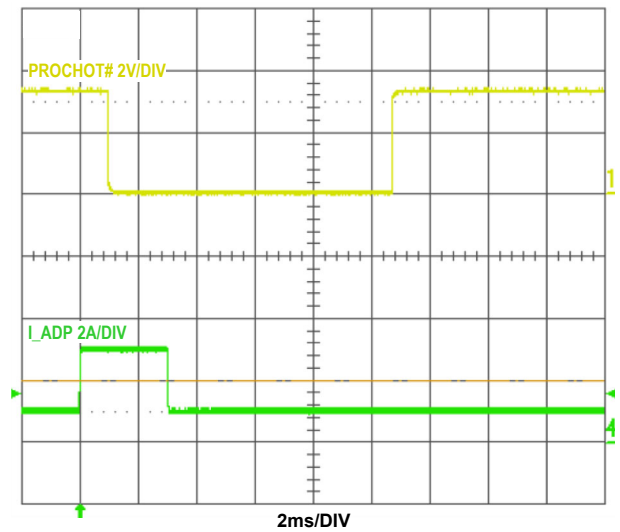


FIGURE 20. ACPROCHOT# ASSERTION. $ACPROCHOT = 2.048A$, $PROCHOTDEBOUNCE = 1ms$, $PROCHOTDURATION = 10ms$

Typical Performance (Continued)

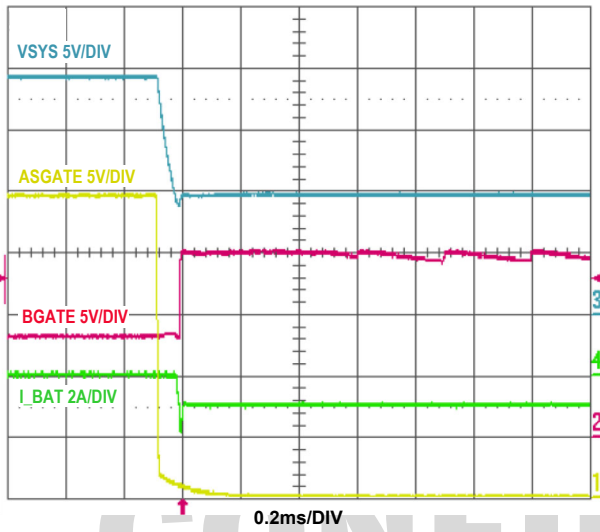


FIGURE 21. HPB: ENTER LEARN MODE

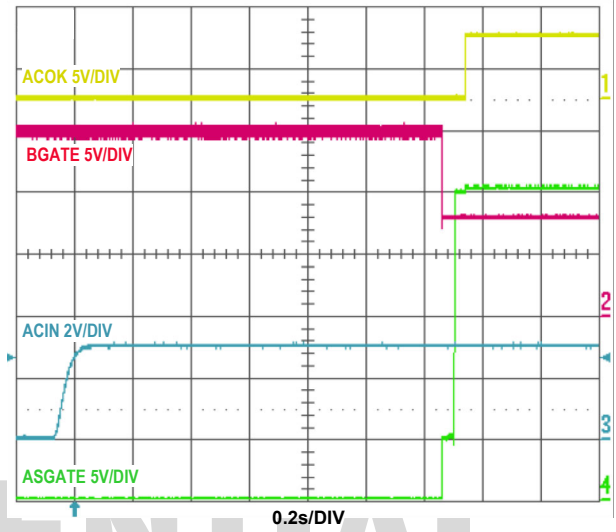


FIGURE 22. HPB: ASGATE TURNING ON DELAY AFTER ADAPTER INSERTION. VADP = 20V, V_{BAT} = 10V, CONTROL2 REGISTER BIT<5> = 0

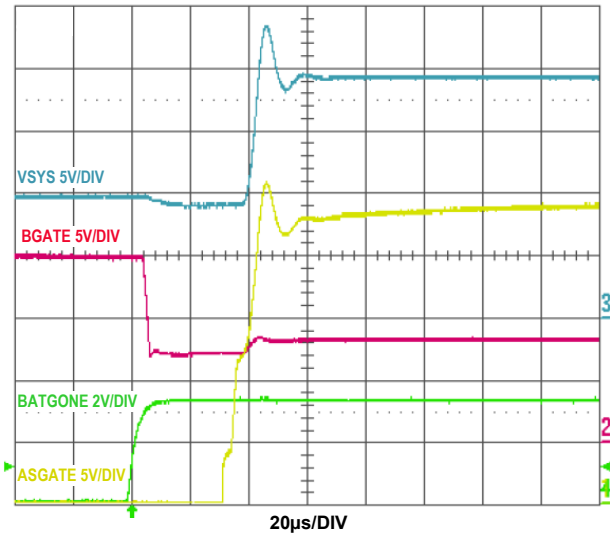


FIGURE 23. HPB: BATTERY SUDDEN REMOVAL IN LEARN MODE BY PULLING BATGONE TO HIGH

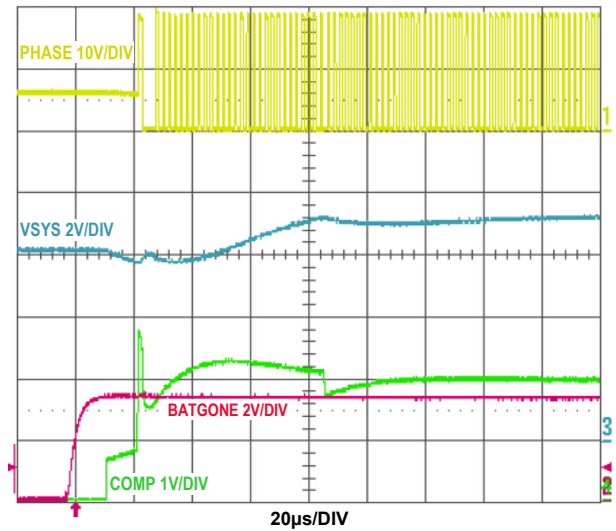


FIGURE 24. NVDC: BATTERY SUDDEN REMOVAL IN LEARN MODE BY PULLING BATGONE TO HIGH

Typical Performance (Continued)

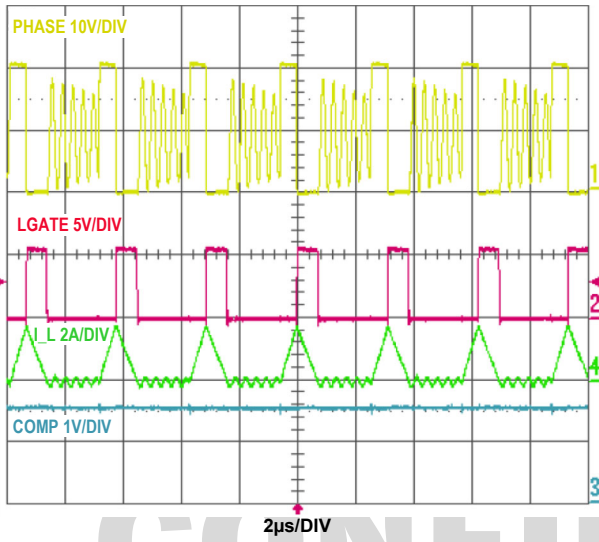


FIGURE 25. DISCONTINUOUS CONDUCTION MODE (DCM) SWITCHING

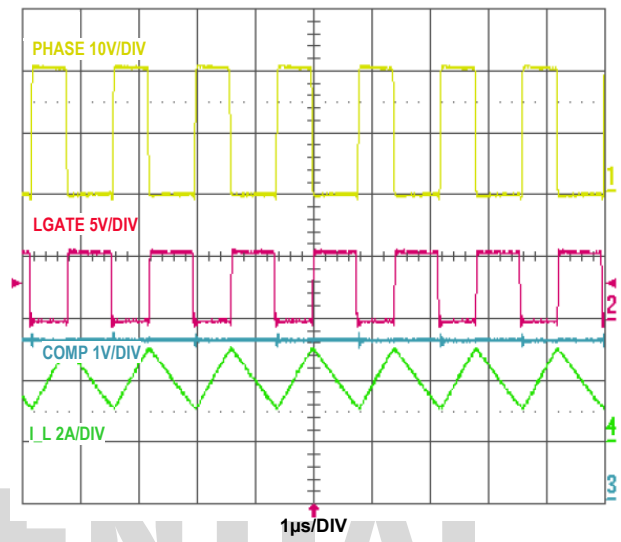


FIGURE 26. CONTINUOUS CONDUCTION MODE (CCM) SWITCHING

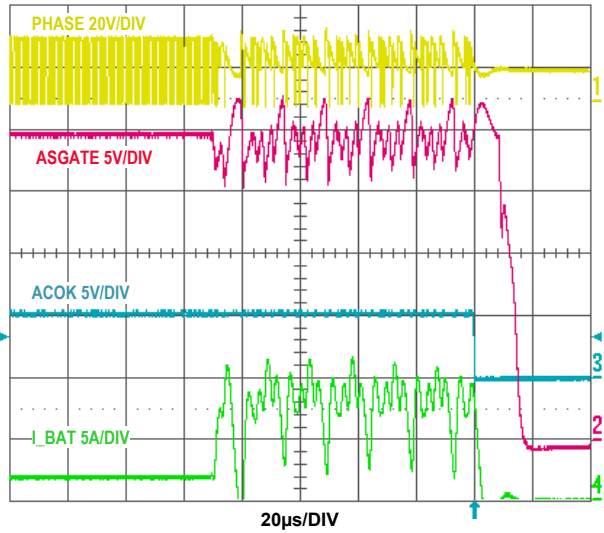


FIGURE 27. WOCP: INDUCTOR SHORT DURING CHARGING.
 VADP = 20V, V_{BAT} = 10V, CHARGE CURRENT = 2A,
 CCLIM = 2V

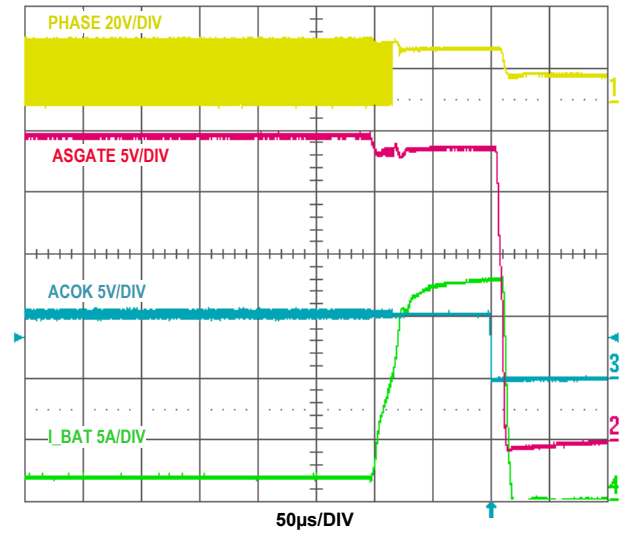


FIGURE 28. WOCP: HIGHSIDE MOSFET SHORT DURING CHARGING.
 VADP = 20V, V_{BAT} = 10V, CHARGE CURRENT = 2A,
 CCLIM = 2V

General SMBus Architecture

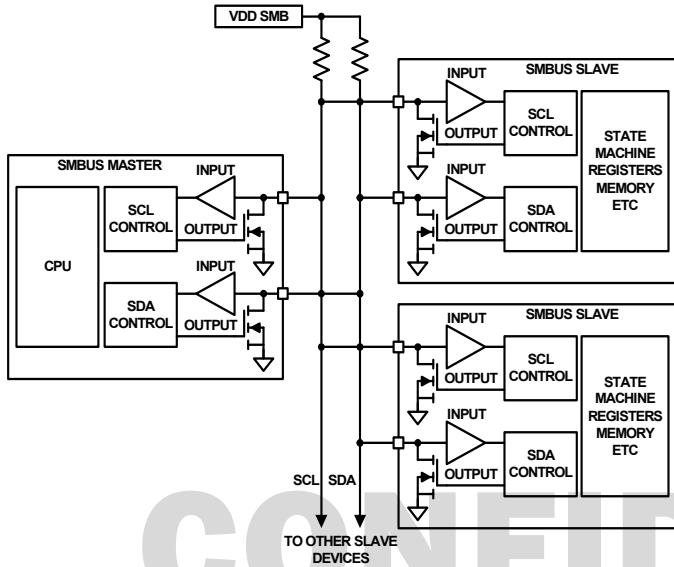


FIGURE 29. GENERAL SMBus ARCHITECTURE

Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. See Figure 30.

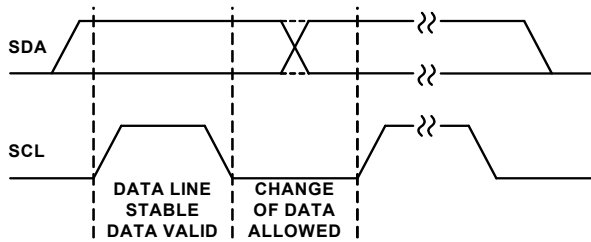


FIGURE 30. DATA VALIDITY

START and STOP Conditions

See Figure 31, the START condition is a HIGH-to-LOW transition of the SDA line while SCL is HIGH.

The STOP condition is a LOW-to-HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition.

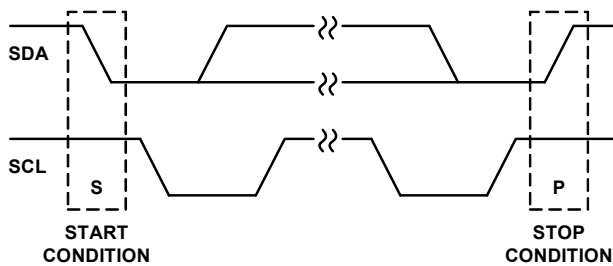


FIGURE 31. START AND STOP WAVEFORMS

Acknowledge

Each address and data transmission uses 9-clock pulses. The ninth pulse is the acknowledge bit (ACK). After the start condition, the master sends 7 slave address bits and a R/W bit during the next 8-clock pulses. During the 9-clock pulse, the device that recognizes its own address holds the data line low to acknowledge (as shown in Figure 32). Both the master and the slave use the ACK bit to acknowledge receipt of register addresses and data.

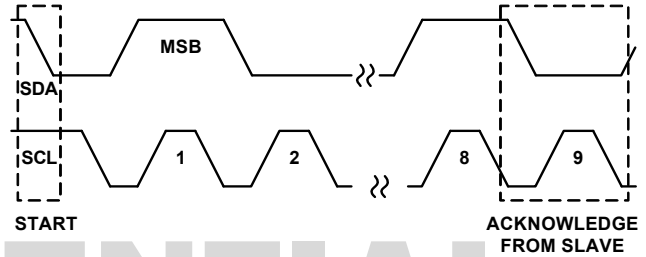


FIGURE 32. ACKNOWLEDGE ON THE SMBus

SMBus Transactions

All transactions start with a control byte sent from the SMBus master device. The control byte begins with a START condition, followed by seven bits of slave address (0001001 for the ISL95521) and the R/W bit. The R/W bit is 0 for a WRITE or 1 for a READ. If any slave device on the SMBus bus recognize its address, it acknowledges by pulling the serial data (SDA) line low for the last clock cycle in the control byte. If no slave exists at that address or it is not ready to communicate, the data line is 1, indicating a Not Acknowledge condition.

When the control byte is sent and the ISL95521 acknowledges it, the second byte sent by the master must be a register address byte such as 0x14 for the ChargeCurrent register. The register address byte tells the ISL95521 which register the master writes or reads. See Table 2 on page 25 for register details. When the ISL95521 receives a register address byte, it responds with an acknowledge.

Byte Format

Every byte put on the SDA line must be 8 bits long and must be followed by an acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first and the Least Significant Bit (LSB) last. The LO BYTE data is transferred before the HI BYTE data. For example, when writing 0x41A0, 0xA0 is written first and 0x41 is sent second.

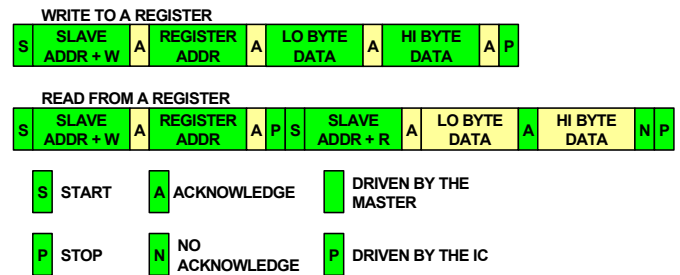


FIGURE 33. SMBus READ AND WRITE PROTOCOL

SMBus and I²C Compatibility

The ISL95521 SMBus minimum input logic high voltage is 2V, so it is compatible with I²C with higher than 2V pull-up power supply.

The ISL95521 SMBus registers are 16 bits, so it is compatible with 16 bits I²C or 8 bits I²C with auto-increment capability.

ISL95521 SMBus Commands

The ISL95521 receives control inputs from the SMBus interface after Power-On Reset (POR). The serial interface complies with System Management Bus Specification, which can be downloaded from www.smbus.org. The ISL95521 uses the SMBus Read Word and Write Word protocols shown in [Figure 33 on page 24](#) to communicate with the host system and a smart battery. The ISL95521 is an SMBus slave device and does not initiate

communication on the bus. It responds to the 7-bit address 0b0001001_:

- Read address = 0b00010011 (0X13H) and
- Write address = 0b00010010 (0X12H).

The data (SDA) and clock (SCL) pins have Schmitt-trigger inputs that can accommodate slow edges. Choose pull-up resistors for SDA and SCL to achieve rise times according to the SMBus specifications.

The ISL95521 allows you to change the SMBus registers to change some functions and options, as shown in [Table 2](#).

The example in this datasheet is based on current sensing resistors $R_{s1} = 10\text{m}\Omega$ and $R_{s2} = 10\text{m}\Omega$ unless specified otherwise. For other current sensing resistor specifications, see [Tables 19](#) and [20](#) on [page 39](#) for more information.

TABLE 2. REGISTERS SUMMARY ($R_{s1} = 10\text{m}\Omega$ AND $R_{s2} = 10\text{m}\Omega$)

REGISTER NAMES	REGISTER ADDRESS	READ/ WRITE	NUMBER OF BITS	DESCRIPTION	POR BIT STATE
ChargeCurrentLimit	0X14H	R/W	8	Bits <12:5> are used. If Bit<0> is interpreted as 1mA, resolution is 32mA and POR default value is 0A.	<12:5> 00000000
DischargeCurrentLimit	0X40H	R/W	6	Bits <12:7> are used. If Bit<0> is interpreted as 1mA, resolution is 128mA and POR default value is 8.064A.	<12:7> 111111
AdapterCurrentLimit1	0X3FH	R/W	6	Bits<12:7> are used. If Bit<0> is interpreted as 1mA, resolution is 128mA and POR default value is 8.064A.	<12:7> 111111
AdapterCurrentLimit2	0X3BH	R/W	6	Bits<12:7> are used. If Bit<0> is interpreted as 1mA, resolution is 128mA and POR default value is 8.064A.	<12:7> 111111
T1	0X37H	R/W	3	Bits<2:0> are used. If 2-level adapter current limit function is enabled and is tripped, T1 configures the effective duration of AdapterCurrentLimit1 register. POR default value is 500 μ s.	<2:0> 110
T2	0X38H	R/W	3	Bits<2:0> are used. If 2-level adapter current limit function is enabled and is tripped, T2 configures the effective duration of AdapterCurrentLimit2 register. POR default value is 100 μ s.	<2:0> 001
MaxChargeVoltage	0X15H	R/W	11	Bits <14:4> are used. If Bit<0> is interpreted as 1mV, resolution is 16mV. The POR default value is based on PROG pin cell number programming: 2-cell: 8.192V 3-cell: 12.288V 4-cell: 16.4V MaxChargeVoltage register should always be programmed higher than MinChargeVoltage register.	

TABLE 2. REGISTERS SUMMARY ($R_{s1} = 10m\Omega$ AND $R_{s2} = 10m\Omega$) (Continued)

REGISTER NAMES	REGISTER ADDRESS	READ/ WRITE	NUMBER OF BITS	DESCRIPTION	POR BIT STATE
MinChargeVoltage	0X3EH	R/W	6	Bits <13:8> are used. If Bit<0> is interpreted as 1mV, resolution is 256mV. The POR default value is based on PROG pin cell number programming: 2-cell: 5.376V 3-cell: 8.064V 4-cell: 10.752V MinChargeVoltage register should always be programmed lower than MaxChargeVoltage register.	
ProchotDebounce	0X39H	R/W	2	Bits<1:0> are used. Set the debounce time before asserting the Prochot# signal for NTC_Prochot#, ACProchot# and DCProchot#. POR default value is 100 μ s.	<1:0> 01
ProchotDuration	0X3AH	R/W	3	Bits<2:0> are used. Set the minimum duration of Prochot# signal latch-up when asserted. POR default value is 10ms.	<2:0> 011
ACProchot	0X47H	R/W	6	Bits<12:7> are used. Set PROCHOT# threshold for adapter overcurrent condition. If Bit<0> is interpreted as 1mA, resolution is 128mA and POR default value is 6.144A.	<12:7> 110000
DCProchot	0X48H	R/W	6	Sets PROCHOT# threshold for battery over-discharging current condition. Bits <12:7> are used. If Bit<0> is interpreted as 1mA, resolution is 128mA and POR default value is 4.096A.	<12:7> 100000
Control1	0X3DH	R/W	16	See Control1 register Table 14 on page 30 .	
Control2	0X3CH	R/W	12	See Control2 register Table 15 on page 32 .	
Information1	0X46H	R	8	Various information reported over SMBus. See Information1 register Table 16 on page 34 .	
Information2	0X45H	R/W	8	PROG pin resistor reading result report. Also configures the 20m Ω current sensing resistor option. See Information2 register Table 17 on page 35 .	
ManufacturerID	0XFEH	R		ASCII for "I".	0X49H
DeviceID	0XFFH	R			0X09H

Setting Charging Current Limit

To set the charging current limit, write a 16-bit ChargeCurrentLimit command (0X14H or 0b00010100) using the Write Word protocol shown in [Figure 33 on page 24](#) and the data format shown in [Table 3](#).

The ISL95521 limits the charging current by limiting the $V_{CSOP} - V_{CSOIN}$ voltage. By using the recommended current sense resistor values shown in [Table 18 on page 37](#), the register's LSB always translates to 1mA of charging current. The ChargeCurrentLimit register accepts any charging current command but only the valid register bits are written to the register. **Note:** It is not recommended to set the charging current limit lower than 96mA.

After POR, the ChargeCurrentLimit register is reset to 0x0000H. To set the battery charging current value, write a valid, non-zero number to the ChargeCurrentLimit register. The ChargeCurrentLimit register can be read back to verify its contents.

[Tables 22 and 23 on page 43](#) show the conditions to enable fast charging according to the ChargeCurrentLimit register setting for HPB configuration and NVDC configuration respectively.

TABLE 3. CHARGECURRENTLIMIT REGISTER 0x14H ($R_{s1} = 10m\Omega$ AND $R_{s2} = 10m\Omega$). (SEE [Table 19 on page 38](#) FOR OTHER CONFIGURATIONS)

BIT	DESCRIPTION
<4:0>	Not used
<5>	0 = Add 0mA of charging current limit. 1 = Add 32mA of charging current limit.
<6>	0 = Add 0mA of charging current limit. 1 = Add 64mA of charging current limit.
<7>	0 = Add 0mA of charging current limit. 1 = Add 128mA of charging current limit.
<8>	0 = Add 0mA of charging current limit. 1 = Add 256mA of charging current limit.
<9>	0 = Add 0mA of charging current limit. 1 = Add 512mA of charging current limit.
<10>	0 = Add 0mA of charging current limit. 1 = Add 1024mA of charging current limit.
<11>	0 = Add 0mA of charging current limit. 1 = Add 2048mA of charging current limit.
<12>	0 = Add 0mA of charging current limit. 1 = Add 4096mA of charging current limit.
<15:13>	Not used

Setting Discharging Current Limit

To set the battery discharging current limit in turbo/boost mode, write a 16-bit DischargeCurrentLimit command (0X40H or 0b01000000) using the Write Word protocol shown in [Figure 33](#) and the data format shown in [Table 4](#).

The ISL95521 limits the HPB charger battery discharging current in turbo/boost mode by limiting the $V_{CSOIN} - V_{CSOP}$ voltage. By using the recommended current sense resistor values shown in [Table 18](#), the register's LSB always translates to 1mA inductor current. The DischargeCurrentLimit register accepts any current commands but only the valid register bits are written to the register.

After POR, the DischargeCurrentLimit register is reset to 0x1F80H. To set the battery discharging current limit in turbo/boost mode, write a valid, non-zero number to the DischargeCurrentLimit register. The DischargeCurrentLimit register can be read back to verify their contents.

TABLE 4. DISCHARGECURRENTLIMIT REGISTER 0x40H ($R_{s1} = 10m\Omega$ AND $R_{s2} = 10m\Omega$). (SEE [Table 19](#) FOR OTHER CONFIGURATIONS)

BIT	DESCRIPTION
<6:0>	Not used
<7>	0 = Add 0mA of discharging current limit. 1 = Add 128mA of discharging current limit.
<8>	0 = Add 0mA of discharging current limit. 1 = Add 256mA of discharging current limit.
<9>	0 = Add 0mA of discharging current limit. 1 = Add 512mA of discharging current limit.
<10>	0 = Add 0mA of discharging current limit. 1 = Add 1024mA of discharging current limit.
<11>	0 = Add 0mA of discharging current limit. 1 = Add 2048mA of discharging current limit.
<12>	0 = Add 0mA of discharging current limit. 1 = Add 4096mA of discharging current limit.
<15:13>	Not used

Setting Adapter Current Limit

To set the adapter current limit, write a 16-bit AdapterCurrentLimit1 command (0X3FH or 0b00111111) and/or AdapterCurrentLimit2 command (0X3BH or 0b00111011) using the Write Word protocol shown in [Figure 33](#) and the data format shown in [Table 5 on page 28](#).

The ISL95521 limits the adapter current by limiting the $V_{CSIP} - V_{CSIN}$ voltage. By using the recommended current sense resistor value as [Table 18](#) shows, the register's LSB always translates to 1mA adapter current. Any adapter current limit command is accepted but only the valid register bits are written to the AdapterCurrentLimit1 and AdapterCurrentLimit2 registers. The minimum adapter current limit command is 128mA and a 0A command is rejected.

After POR, the AdapterCurrentLimit1 and AdapterCurrentLimit2 register are reset to 0x1F80. The AdapterCurrentLimit1 and AdapterCurrentLimit2 registers can be read back to verify their contents.

To set a second level adapter current limit, write a 16-bit AdapterCurrentLimit2 (0X3BH or 0b00111011) command using the Write Word protocol shown in [Figure 33](#) and the data format as shown in [Table 5](#).

The AdapterCurrentLimit2 register has the same specification as the AdapterCurrentLimit1 register. See ["Two-Level Adapter Current Limit" on page 44](#) for detailed operation.

TABLE 5. ADAPTERCURRENTLIMIT1 REGISTER 0x3FH AND ADAPTERCURRENTLIMIT2 REGISTER 0x3BH ($R_{s1} = 10m\Omega$ AND $R_{s2} = 10m\Omega$)

BIT	DESCRIPTION
<6:0>	Not used
<7>	0 = Add 0mA of adapter current limit. 1 = Add 128mA of adapter current limit.
<8>	0 = Add 0mA of adapter current limit. 1 = Add 256mA of adapter current limit.
<9>	0 = Add 0mA of adapter current limit. 1 = Add 512mA of adapter current limit.
<10>	0 = Add 0mA of adapter current limit. 1 = Add 1024mA of adapter current limit.
<11>	0 = Add 0mA of adapter current limit. 1 = Add 2048mA of adapter current limit.
<12>	0 = Add 0mA of adapter current limit. 1 = Add 4096mA of adapter current limit.
<15:13>	Not used

Setting Two-Level Adapter Current Limit Duration

For two-level adapter current limit, write a 16-bit T1 command (0X37H or 0b00110111) using the Write Word protocol shown in [Figure 33 on page 24](#) and the data format shown in [Table 6](#) to set the AdapterCurrentLimit1 duration as the adapter current limit. Write a 16-bit T2 command (0X38H or 0b00111000) to set AdapterCurrentLimit2 duration as the adapter current limit. T1 register and T2 register accept any command but only the valid register bits are written. See [“Two-Level Adapter Current Limit” on page 44](#) for detailed operation.

TABLE 6. T1 REGISTER 0x37H

BIT	DESCRIPTION
<2:0>	000 = 0ms 001 = 20ms 010 = 15ms 011 = 10ms 100 = 5ms 101 = 1ms 110 = 0.5ms 111 = 0.1ms
<15:3>	Not used

TABLE 7. T2 REGISTER 0x38H

BIT	DESCRIPTION
<2:0>	000 = 15 μ s 001 = 100 μ s 010 = 500 μ s 011 = 1ms 100 = 300 μ s 101 = 750 μ s 110 = 3ms 111 = 10ms
<15:3>	Not used

Setting Maximum Charging Voltage

To set the maximum charging voltage, write a 16-bit MaxChargeVoltage command (0X15H or 0b00010101) using the Write Word protocol shown in [Figure 33](#) and the data format as shown in [Table 8](#).

The maximum charging voltage range is 7.168V to 18.432V. The MaxChargeVoltage register accepts any voltage command but only the valid register bits are written to the register.

The MaxChargeVoltage register sets the battery full charging voltage limit. For NVDC configuration, the MaxChargeVoltage register setting is also the system bus voltage regulation point when the battery is present but is not in charge. See [“NVDC Charger System Voltage Regulation” on page 45](#) for details.

The CSON pin senses the battery voltage for maximum charging voltage regulation. For NVDC configuration, the CSON pin is also the system bus voltage regulation sense point.

TABLE 8. MAXCHARGEVOLTAGE REGISTER 0x15H

BIT	DESCRIPTION
<3:0>	Not used
<4>	0 = Add 0mV of charging voltage. 1 = Add 16mV of charging voltage.
<5>	0 = Add 0mV of charging voltage. 1 = Add 32mV of charging voltage.
<6>	0 = Add 0mV of charging voltage. 1 = Add 64mV of charging voltage.
<7>	0 = Add 0mV of charging voltage. 1 = Add 128mV of charging voltage.
<8>	0 = Add 0mV of charging voltage. 1 = Add 256mV of charging voltage.
<9>	0 = Add 0mV of charging voltage. 1 = Add 512mV of charging voltage.
<10>	0 = Add 0mV of charging voltage. 1 = Add 1024mV of charging voltage.
<11>	0 = Add 0mV of charging voltage. 1 = Add 2046mV of charging voltage.
<12>	0 = Add 0mV of charging voltage. 1 = Add 4096mV of charging voltage.
<13>	0 = Add 0mV of charging voltage. 1 = Add 8192mV of charging voltage.
<14>	0 = Add 0mV of charging voltage. 1 = Add 16384mV of charging voltage.
<15>	Not used

Setting Minimum Charging Voltage

To set the minimum charging voltage, write a 16-bit MinChargeVoltage command (0X3EH or 0b00111110) using the Write Word protocol shown in [Figure 33](#) and the data format as shown in [Table 9 on page 29](#).

The minimum charging voltage range is 2.048V to 16.128V. The MinChargeVoltage register accepts any voltage command but only the valid register bits are written to the register. The MinChargeVoltage register value should be set lower than the MaxChargeVoltage register value.

The MinChargeVoltage register sets the battery voltage threshold for entry and exit of the trickle charge mode. The VBAT pin senses the battery voltage to compare with the MinChargeVoltage register setting. See [“Trickle Charging” on page 44](#) for details.

For NVDC configuration, the MinChargeVoltage register setting is also the system voltage regulation point when the battery is not present. The CSON pin is the system voltage regulation sense point. See [“NVDC Charger System Voltage Regulation” on page 45](#) for details.

TABLE 9. MINCHARGEVOLTAGE REGISTER 0x3EH

BIT	DESCRIPTION
<7:0>	Not used
<8>	0 = Add 0mV of charging voltage. 1 = Add 256mV of charging voltage.
<9>	0 = Add 0mV of charging voltage. 1 = Add 512mV of charging voltage.
<10>	0 = Add 0mV of charging voltage. 1 = Add 1024mV of charging voltage.
<11>	0 = Add 0mV of charging voltage. 1 = Add 2048mV of charging voltage.
<12>	0 = Add 0mV of charging voltage. 1 = Add 4096mV of charging voltage.
<13>	0 = Add 0mV of charging voltage. 1 = Add 8192mV of charging voltage.
<15:14>	Not used

Setting PROCHOT# Debounce Time

To set the PROCHOT# signal debounce time before its assertion for ACProchot, DCProchot, and NTC_Prochot, write a 16-bit PROCHOT# debounce time (0X39H or 0b00111001) using the Write Word protocol shown in [Figure 33](#) and the data format as shown in [Table 10](#). The Prochot# Debounce Time register accepts any command but only the valid register bits are written.

The low system voltage Prochot# has a fixed debounce time as 10 μ s.

TABLE 10. PROCHOTDEBOUNCE REGISTER 0x39H

BIT	DESCRIPTION
<1:0>	00 = 10 μ s 01 = 100 μ s 10 = 500 μ s 11 = 1ms
<15:2>	Not used

Setting PROCHOT# Duration

To set the PROCHOT# signal latch-up duration when asserted for ACProchot, DCProchot, and NTC_Prochot and low system voltage Prochot, write a 16-bit PROCHOT# Duration command (0X3AH or 0b01111010) using the Write Word protocol shown in [Figure 33](#) and the data format shown in [Table 11](#). The Prochot# Duration register accepts any command but only the valid register bits are written.

TABLE 11. PROCHOT# DURATION REGISTER 0x3Ah

BIT	DESCRIPTION
<2:0>	000 = 0ms 001 = 20ms 010 = 15ms 011 = 10ms 100 = 5ms 101 = 1ms 110 = 500 μ s 111 = 100 μ s
<15:3>	Not used

Setting PROCHOT# Threshold for Adapter Overcurrent Condition

To set the PROCHOT# assertion threshold for adapter overcurrent condition, write a 16-bit ACProchot command (0X47H or 0b01000111) using the Write Word protocol shown in [Figure 33](#) and the data format shown in [Table 12](#). By using the recommended current sense resistor value as [Table 18 on page 37](#) shows, the register's LSB always translates to 1mA adapter current. The ACProchot register accepts any command but only the valid register bits are written to the register.

After POR, the ACProchot register is reset to 0x1800H. The ACProchot register can be read back to verify its contents.

If the adapter current exceeds the ACProchot register setting, the PROCHOT# signal asserts after the debounce time programmed by the ProchotDebounce register and latches on for a minimum time programmed by the ProchotDuration register.

For HPB configuration, the ACProchot function is disabled when it is in standby mode because the standby mode turns off the internal comparator reference, which is indicated by Information1 register bit<8>.

TABLE 12. ACPROCHOT REGISTER 0x47H (R_{s1} = 10m Ω AND R_{s2} = 10m Ω . SEE [Table 19](#) FOR OTHER CONFIGURATIONS)

BIT	DESCRIPTION
<6:0>	Not used
<7>	0 = Add 0mA of ACProchot threshold. 1 = Add 128mA of ACProchot threshold.
<8>	0 = Add 0mA of ACProchot threshold. 1 = Add 256mA of ACProchot threshold.
<9>	0 = Add 0mA of ACProchot threshold. 1 = Add 512mA of ACProchot threshold.
<10>	0 = Add 0mA of ACProchot threshold. 1 = Add 1024mA of ACProchot threshold.
<11>	0 = Add 0mA of ACProchot threshold. 1 = Add 2048mA of ACProchot threshold.
<12>	0 = Add 0mA of ACProchot threshold. 1 = Add 4096mA of ACProchot threshold.
<15:13>	Not used

Setting PROCHOT# Threshold for Battery Over Discharging Current Condition

To set the PROCHOT# signal assertion threshold for battery over discharging current condition, write a 16-bit DCProchot command (0X48H or 0b01001000) using the Write Word protocol shown in [Figure 33](#) and the data format shown in [Table 13](#). By using the recommended current sense resistor value as [Table 18](#) shows, the register's LSB always translates to 1mA adapter current. The DCProchot register accepts any command but only the valid register bits are written to the register.

After POR, the DCProchot register is reset to 0x1000H. The DCProchot register can be read back to verify its contents.

If the battery discharging current exceeds the DCProchot register setting, the PROCHOT# signal asserts after the debounce time programmed by the ProchotDebounce register and latches on for a minimum time programmed by the ProchotDuration register.

In battery only mode, DCProchot function works only when PSYS or NTC is enabled, because enabling PSYS or NTC activates the internal comparator reference. The Information1 register Bit<8> indicates if the internal comparator reference is active or not.

When the adapter is present, the internal comparator reference is always active unless it is in standby mode for HPB configuration.

TABLE 13. DCPROCHOT REGISTER 0x48H ($R_{s1} = 10m\Omega$ AND $R_{s2} = 10m\Omega$. SEE [Table 19](#) FOR OTHER CONFIGURATIONS)

BIT	DESCRIPTION
<6:0>	Not used
<7>	0 = Add 0mA of DCProchot threshold. 1 = Add 128mA of DCProchot threshold.
<8>	0 = Add 0mA of DCProchot threshold. 1 = Add 256mA of DCProchot threshold.
<9>	0 = Add 0mA of DCProchot threshold. 1 = Add 512mA of DCProchot threshold.
<10>	0 = Add 0mA of DCProchot threshold. 1 = Add 1024mA of DCProchot threshold.
<11>	0 = Add 0mA of DCProchot threshold. 1 = Add 2048mA of DCProchot threshold.
<12>	0 = Add 0mA of DCProchot threshold. 1 = Add 4096mA of DCProchot threshold.
<15:13>	Not used

Control Registers

To change certain functions or options after POR, write a 16-bit control command to Control1 register (0X3DH or 0b00111101) or Control2 register (0X3CH or 0b00111100) using the Write Word protocol shown in [Figure 33](#) and the data format shown in [Tables 14](#) and [15](#), respectively.

TABLE 14. CONTROL1 REGISTER 0x3DH

BIT	BIT NAME	DESCRIPTION	POR STATE
<0>	Standby Mode	1 = The charger enters standby mode. 0 = The charger exits standby mode. Standby mode control bit is valid for HPB configuration only and is valid only when the adapter is present; it has no effect for NVDC configuration. When the ISL95521 enters Standby mode, it turns off the internal references (indicated by Information1 register Bit<8>) and stops switching to enter a low power consumption mode with minimum quiescent current. If PSYS is already enabled, it cannot enter Standby mode.	0
<1>	Learn Mode	1 = The charger enters learn mode. 0 = The charger exits learn mode. The SMBus learn mode control is valid only when the PROG pin is not pulled to 5V after POR.	0
<2>	AMON	1 = Turn on adapter current monitor AMON function. 0 = Turn off adapter current monitor AMON function.	0
<3>	BMON	1 = Turn on battery discharging current monitor BMON function. 0 = Turn off battery discharging current monitor BMON function. BMON function is disabled if battery voltage is less than 3.5V to avoid battery over discharged.	0
<4>	PSYS	1 = Turn on system power monitor PSYS function. 0 = Turn off system power monitor PSYS function. PSYS function does not include the power provided by battery if battery voltage is less than 3.5V. For HPB configuration, when the adapter is present, if it enters Standby mode already, PSYS cannot be turned on.	0

TABLE 14. CONTROL1 REGISTER 0x3DH (Continued)

BIT	BIT NAME	DESCRIPTION	POR STATE
<5>	Low System Voltage Detection	<p>1 = Turn on low system voltage detect function. 0 = Turn off low system voltage detect function.</p> <p>Bit<5> is valid only when the internal comparator reference is active, which is indicated by Information1 register Bit<8>.</p> <p>In battery only mode, low system voltage detection function works only when PSYS or NTC is enabled, because enabling PSYS or NTC activates the internal comparator reference.</p> <p>When adapter is present, the internal comparator reference is always active unless it is in standby mode for HPB configuration.</p> <p>For HPB configuration, ISL95521 senses the system voltage through CSIP pin. For NVDC configuration, ISL95521 senses the system voltage through CSON pin.</p>	0
<6>	NTC	<p>1 = Turn on NTC function. 0 = Turn off NTC function.</p> <p>When turned on, if the NTC pin voltage is less than 170mV, the PROCHOT# signal asserts after the debounce time programmed by the ProchotDebounce register and latches on for a minimum time programmed by the ProchotDuration register.</p> <p>For NTC function to work, the internal reference indicated by Information1 register Bit<8> needs to be active.</p> <p>When the adapter is present, the NTC function is always turned on unless it is in Standby mode then Bit<6> is invalid.</p> <p>In battery only mode, Bit<6> is valid to turn on or off the NTC function only when PSYS is turned off; NTC function is always turned on automatically if PSYS is turned on.</p>	0
<7>	Fast Learn Mode Exit	<p>1 = Fast learn mode exit. 0 = Slow learn mode exit.</p> <p>For fast learn mode exit, it turns on ASGATE MOSFETs instantly without going through the ASGATE soft-start turning on procedure when the BATGONE pin voltage goes from logic low to high.</p> <p>For slow learn mode exit, it goes through the ASGATE soft-start turning on procedure 1.3s or 163ms (which is set by Control2 register Bit<5>) after BATGONE pin voltage goes from logic low to high.</p> <p>This Fast Learn Mode Exit control bit is valid only when the battery is removed during learn mode and it only works for HPB configuration and has no effect for NVDC configuration.</p>	0
<9:8>	Threshold for Low System Voltage Detection	<p>If the Control register Bit<5> = 1, Bits<9:8> programs the low system voltage detection threshold. If the system voltage is below this threshold, the PROCHOT# signal asserts after a fixed 10μs debounce time and latches on for a minimum time programmed by the ProchotDuration register.</p> <p>00 = 5.6V threshold. 01 = 6.06V threshold. 10 = 6.53V threshold. 11 = 7V threshold.</p> <p>Valid only when Control1 register Bit<5> = 1.</p>	00
<10>	Turbo/Boost Mode	<p>1 = Disable Turbo/Boost mode. 0 = Enable Turbo/Boost mode.</p>	1
<11>	Charging Current WOCP	<p>1 = Disable charging current way overcurrent protection function. 0 = Enable charging current way overcurrent protection function.</p>	0
<12>	Enable Charging	<p>0 = Disable charging. 1 = Enable charging.</p>	1

TABLE 14. CONTROL1 REGISTER 0x3DH (Continued)

BIT	BIT NAME	DESCRIPTION	POR STATE
<14:13>	Force The Number Of Battery Cells In Series	<p>Bits<14:13> can overwrite the number of battery cells in series that programmed by PROG pin. When Bit<14:13> is written, only the POR default MaxChargeVoltage register value and MinChargeVoltage register value changes according to the cell number. The battery 4.6V/cell overvoltage protection threshold also changes according to the cell number.</p> <p>The MaxChargeVoltage register setting should be always smaller than battery overvoltage threshold 4.6V*cell#.</p> <p>Bits<14:13> if not used, keep its POR code based on PROG pin cell# setting.</p> <p>00 = Not available and is ignored if written. 01 = 2-cell 10 = 3-cell 11 = 4-cell</p>	PROG cell#
<15>	SMBus Timeout	<p>The ISL95521 includes a timer to ensure the SMBus master is active and to prevent overcharging the battery. If the adapter is present and if the ISL95521 does not receive a write to the MaxChargeVoltage or ChargeCurrentLimit registers within 175s, the ISL95521 terminates charging. If a timeout occurs, writing the MaxChargeVoltage or ChargeCurrentLimit register reenables charging.</p> <p>0 = Enable the SMBus timeout function. 1 = Disable the SMBus timeout function.</p>	0

TABLE 15. CONTROL2 REGISTER 0x3CH

BIT	BIT NAME	DESCRIPTION	POR STATE
<3:0>	Frequency Setting	<p>Overwrite the switching frequency set by the FSET pin. See the default CCM switching frequency programming Table 21 on page 39 for the correlation.</p> <p>1111 = 992kHz (equivalent to R_FSET = 0Ω) 1110 = 838kHz 1101 = 729kHz 1100 = 642kHz 1011 = 678kHz 1010 = 614kHz 1001 = 561kHz 1000 = 517kHz 0111 = 513kHz 0110 = 477kHz 0101 = 449kHz 0100 = 421kHz 0011 = 417kHz 0010 = 395kHz 0001 = 375kHz 0000 = Switching frequency set by FSET pin</p> <p>To keep the switching frequency set by PROG pin resistor, leave Bit<3:0> as it is or write code 0000, which sets the same frequency as the PROG pin resistor does.</p>	0000
<4>	Release Adapter Current Limit when No Battery	<p>When there is no battery, Bit<4> enables or releases adapter current limit for NVDC configuration.</p> <p>0 = Enable adapter current limit function. 1 = Release adapter current limit function.</p>	0
<5>	ASGATE Turn-On Delay	<p>0 = Set ASGATE turn on delay to 1.3s from adapter plugged in. 1 = Set ASGATE turn on delay to 163ms from adapter plugged in.</p>	0
<6>	Two-level Adapter Current Limit Function	<p>0 = Disable two-level adapter current limit function. 1 = Enable two-level adapter current limit function.</p>	1

TABLE 15. CONTROL2 REGISTER 0x3CH (Continued)

BIT	BIT NAME	DESCRIPTION	POR STATE
<7> <12>	Trickle Charging Current	Bit<12> and Bit<7> can be combined together to change the trickle charging current value. Bit <12>:<7> =: <0>:<0> = 256mA trickle charging current. <0>:<1> = 128mA trickle charging current. <1>:<0> = 128mA trickle charging current. <1>:<1> = 64mA trickle charging current. 64mA trickle charging current option is valid only for “R _{s1} = 10mΩ, R _{s2} = 10mΩ” and “R _{s1} = 20mΩ, R _{s2} = 20mΩ” configurations for both NVDC charger and HPB charger.	0:1
<8>	Adapter OVP	0 = Enable adapter OVP function; 1 = Disable adapter OVP function. If adapter OVP function is enabled, the ISL95521 turns off ASGATE and pulls down ACOK when ACIN > 3.5V.	0
<9>	PSYS Current Gain	For “R _{s1} = 10mΩ, R _{s2} = 5mΩ” and “R _{s1} = 10mΩ, R _{s2} = 10mΩ” configuration: 0 = 1.14μA/W 1 = 0.285μA/W For “R _{s1} = 20mΩ, R _{s2} = 10mΩ” and “R _{s1} = 20mΩ, R _{s2} = 20mΩ” configuration: 0 = 2.28μA/W 1 = 0.57μA/W	0
<10>	ACLIM Inrush Current Limit Time	0 = Set soft-start ACLIM in-rush current limit period as 1ms when adapter plugged in. 1 = Set soft-start ACLIM in-rush current limit period as 4ms when adapter plugged in.	0
<11>	BGATE OFF Timing	Bit<11> is valid for HPB configuration only. It changes the BGATE FET turning off timing when adapter plugged in. 0 = Turn OFF BGATE FET according to battery voltage (see “Soft-Start” on page 39 for details). 1 = Turn OFF BGATE FET before turning on ASGATE FETs.	0
<13>	ACLIM Function	Bit<13> configures ACLIM to be functional all the time or only during ASGATE turning on procedure to limit the inrush current. 0 = ACLIM function is ON all the time. 1 = ACLIM function is OFF after ACOK assertion.	0
<15:14>	DCM LGATE Turning OFF Timing	Bit<15:14> adjusts the LGATE turning OFF timing when the buck switcher is in DCM operation to minimize the MOSFETs body diode conduction time. By default, LGATE turns OFF when the inductor current is positive (from PHASE node to output). 00 = Earliest LGATE turning OFF when PHASE pin voltage is about -6mV. 01 = Earlier LGATE turning OFF when PHASE pin voltage is about -4mV. 10 = Early LGATE turning OFF when PHASE pin voltage is about -2mV. 11 = Late LGATE turning OFF when PHASE pin voltage is about 0mV.	00

Information Registers

To read the information register, write a 16-bit Information1 command (0X46H or 0b01000110) or Information2 command (0X45H or 0b01000101) using the Read Word protocol shown in [Figure 33](#) and the data format shown in [Tables 16](#) and [17](#), respectively.

TABLE 16. INFORMATION1 REGISTER 0x46H

BIT	BIT NAME	W/R	DESCRIPTION
<0>	Adapter Present	R	0 = The adapter is not present. 1 = The adapter is present.
<1>	ASGATE ON	R	0 = ASGATE is OFF. 1 = ASGATE is ON.
<2>	VBAT<MinChargeVoltage	R	0 = VBAT>MinChargeVoltage. 1 = VBAT<MinChargeVoltage. Valid only when Information1 register Bit<8> = 1.
<3>	VSYS<Low System Voltage Setting	R	0 = VSYS>Low System Voltage Setting programmed by Control1 register Bit<9:8>. 1 = VSYS<Low System Voltage Setting programmed by Control1 register Bit<9:8>. Valid only when Information1 register Bit<8> = 1.
<4>	NTC_PROCHOT#	R	0 = NTC_PROCHOT# not asserted. 1 = NTC_PROCHOT# asserted. Valid only when Information1 register Bit<8> = 1.
<5>	In trickle charge mode	R	0 = Not in trickle charge mode. 1 = In trickle charge mode. Bit<5> is valid for NVDC configuration only.
<6>	In Turbo/Boost mode	R	0 = Not in Turbo/Boost mode. 1 = In Turbo/Boost mode. For NVDC configuration, if BGATE is already ON before entering turbo mode, BGATE stays ON after entering turbo mode; Bit<6> does not indicate the turbo mode in this case.
<7>	ACProchot	R	0 = ACProchot# not asserted. 1 = ACProchot# asserted.
<8>	Reference Active	R	0 = Reference is not active. 1 = Reference is active. When Bit<8> = 1, Information Register Bits <4:2> are valid. When adapter is present, the internal comparator reference is always active; unless it is in standby mode for HPB charger configuration. In battery only mode, the default internal reference is not active, unless PSYS or NTC is enabled.

TABLE 17. INFORMATION2 REGISTER 0x45H

BIT	BIT NAME	W/R	DESCRIPTION	POR STATE
<0> <8>	R _{s1}	W/R	If R _{s1} = 20mΩ (R _{s1} = 20mΩ and R _{s2} = 10mΩ or R _{s1} = 20mΩ and R _{s2} = 20mΩ), both Bit<8> and Bit<0> need to be programmed as 1 to have correct internal current sensing scaling. Bit<8>:<0>: <0>:<0> = R _{s1} = 10mΩ <0>:<1> = R _{s1} = 10mΩ <1>:<0> = R _{s1} = 10mΩ <1>:<1> = R _{s1} = 20mΩ	0:0
<3:1>			Not used. Internally hard wired as <3:1> = 010.	
<5:4>	Cell number	R	00 = Not available. 01 = 2-cell 10 = 3-cell 11 = 4-cell	
<6>	Current sensing resistor	R	0 = "R _{s1} :R _{s2} = 2:1" (R _{s1} = 10mΩ and R _{s2} = 5mΩ or R _{s1} = 20mΩ and R _{s2} = 10mΩ) 1 = "R _{s1} :R _{s2} = 1:1" (R _{s1} = 10mΩ and R _{s2} = 10mΩ or R _{s1} = 20mΩ and R _{s2} = 20mΩ) Together with Bit<8> and Bit<0> R _{s1} setting, it can be figured out that R _{s1} = 10mΩ or R _{s1} = 20mΩ.	
<7>	Charger Configuration	R	0 = HPB charger configuration 1 = NVDC charger configuration	
<15:9>			Not used	

Application Information

R3 Modulator

The ISL95521 uses the Renesas patented R3 (Robust Ripple Regulator™) modulation scheme. The R3 modulator combines the best features of fixed frequency PWM and hysteric PWM while eliminating many of their shortcomings. [Figure 34](#) conceptually shows the R3 modulator circuit and [Figure 35](#) shows the operation principles in steady state.

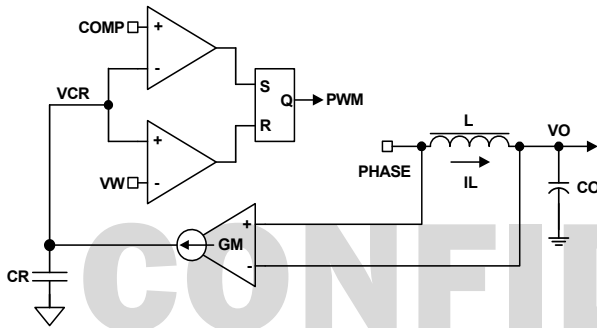


FIGURE 34. R3 MODULATOR

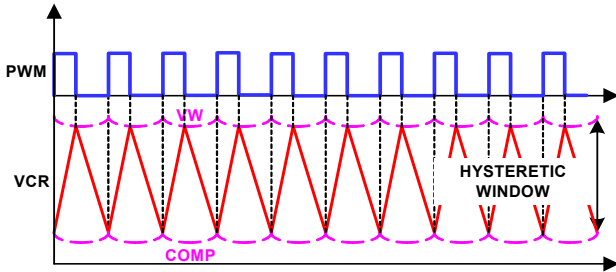


FIGURE 35. R3 MODULATOR OPERATION PRINCIPLES IN STEADY STATE

There is a fixed voltage window between VW and COMP. This voltage window is called the VW window in the following discussion. The modulator charges the ripple capacitor C_r with a current source equal to $g_m(V_{IN} - V_o)$ during PWM on-time and discharges the ripple capacitor C_r with a current source equal to $g_m V_o$, during PWM off-time, where g_m is a gain factor. The C_r voltage V_{cr} therefore emulates the inductor current waveform. The modulator turns off the PWM pulse when V_{cr} reaches VW and turns on the PWM pulse when it reaches COMP.

Since the modulator works with V_{cr} , which is large amplitude and noise free synthesized signal, it achieves lower phase jitter than conventional hysteric mode modulator.

[Figure 36](#) shows the operation principles during dynamic response. The COMP voltage rises during dynamic response, turning on PWM pulses earlier and more frequently temporarily, which allows for higher control loop bandwidth than conventional fixed frequency PWM modulator at the same steady state switching frequency.

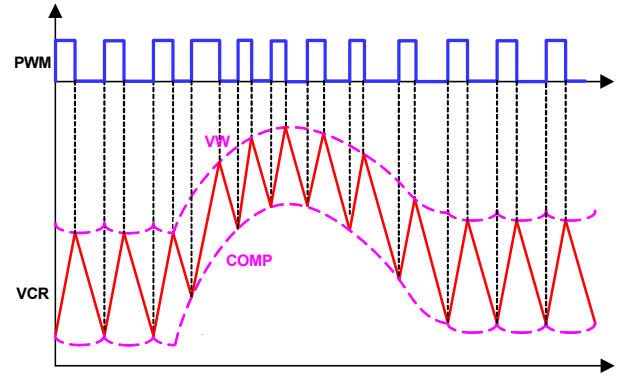


FIGURE 36. R3 MODULATOR OPERATION PRINCIPLES IN DYNAMIC RESPONSE

The R3 modulator can operate in diode emulation (DE) mode to increase light-load efficiency. In DE mode, the low-side MOSFET conducts when the current is flowing from source-to-drain and does not allow reverse current, emulating a diode. As shown in [Figure 37](#), when LGATE is on, the low-side MOSFET carries current, creating negative voltage on the phase node due to the voltage drop across the ON-resistance. The IC monitors the current by monitoring the phase node voltage. It turns off LGATE when the phase node voltage reaches zero to prevent the inductor current from reversing the direction and creating unnecessary power loss.

If the load current is light enough, as [Figure 37](#) shows, the inductor current reaches and stays at zero before the next phase node pulse and the regulator is in Discontinuous Conduction Mode (DCM). If the load current is heavy enough, the inductor current never reaches 0A and the regulator is in CCM although the controller is in DE mode.

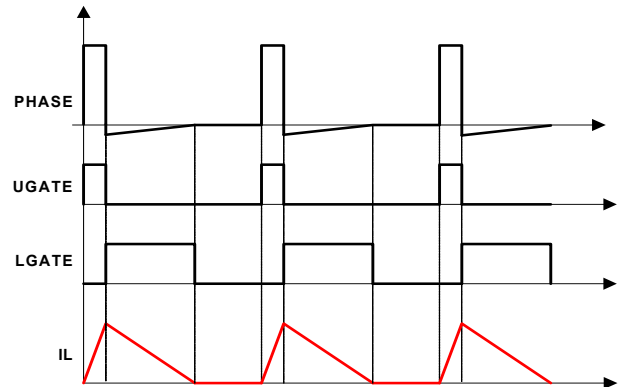


FIGURE 37. DIODE EMULATION

In DCM operation, to turn off LGATE when the inductor current reaches near zero, the ISL95521 provides Control2 register Bit<15:14> to adjust the LGATE turning off timing. The default timing purposely turns off LGATE a little earlier than the inductor current zero crossing. The SMBus Bit can adjust the timing more aggressively towards the precise zero-crossing point to minimize the MOSFETs body diode conduction time for higher efficiency at light load. However, it is not recommended to turn off LGATE after the inductor current zero crossing, which can feed energy back to the adapter side.

Figure 38 on page 37 shows the operation principle in diode emulation mode at light load. The load gets incrementally lighter in the three cases from top to bottom. The PWM on-time is determined by the VW window size, therefore is the same, making the inductor current triangle the same in the three cases. The R3 modulator clamps the ripple capacitor voltage V_{Cr} in DE mode to make it mimic the inductor current. It takes the COMP voltage longer to hit V_{Cr} , naturally stretching the switching period. The inductor current triangles move further apart from each other such that the inductor current average value is equal to the load current. The reduced switching frequency helps increase light-load efficiency.

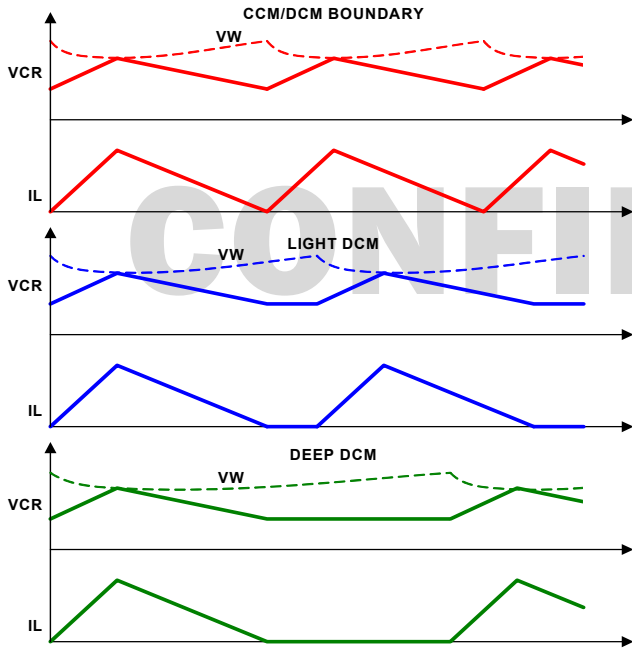


FIGURE 38. PERIOD STRETCHING

Programming Charger Options

The resistor from the PROG pin to GND programs the configuration of the ISL95521 as a HPB charger or NVDC charger, as well as the default number of battery cells in series and the default values of the adapter and battery current sense resistors R_{S1} and R_{S2} . Table 18 shows the programming options.

TABLE 18. PROG PIN PROGRAMMING OPTIONS

PROG-GND RESISTANCE (kΩ)	CHARGER TYPE	CURRENT SENSE RESISTOR VALUE	DEFAULT # OF BATTERY CELLS IN SERIES	
TYP (1% STANDARD RESISTOR)				
0	NVDC	$R_{S1}:R_{S2} = 2:1$ $R_{S1} = 10m\Omega$ $R_{S2} = 5m\Omega$	3	
22.6			4	
38.3			2	
69.8		HPB	$R_{S1}:R_{S2} = 1:1$ $R_{S1} = 10m\Omega$ $R_{S2} = 10m\Omega$	3
86.6				4
102				2
150	$R_{S1} = 20m\Omega$ $R_{S2} = 20m\Omega$		4	
165			2	
182			3	
215	HPB	$R_{S1}:R_{S2} = 2:1$ $R_{S1} = 10m\Omega$ $R_{S2} = 5m\Omega$	4	
237			2	
255			3	

Before soft-start and when V_{DD} voltage reaches its POR value, the ISL95521 sources $10\mu A$ current out of the PROG pin and reads the PROG pin voltage to determine the resistor value. However, application environmental noise can pollute the PROG pin voltage and cause incorrect reading. If noise is a concern, it is recommended to connect a capacitor from the PROG pin to GND to provide filtering. The resistor and the capacitor RC time constant should be less than $40\mu s$, so the PROG pin voltage can rise to steady state before the ISL95521 reads it.

The ISL95521 can be programmed in two different battery charger configurations.

Figure 1 on page 1 shows the typical application circuit for a HPB charger. In this configuration, the ISL95521 connects the system voltage rail to either the adapter or the battery. In turbo event, which means the system is drawing more power than the adapter's power rating, the ISL95521 operates as a boost converter to reverse-boost the battery energy to the system voltage rail, so the battery works with the adapter together to supply the system power.

Figure 5 on page 6 shows the typical application circuit for NVDC charger. In this configuration, the ISL95521 connects the system voltage rail to either the output of the buck switcher or the battery. In Turbo event, the ISL95521 turns on the BGATE to discharge the battery so the battery works with the adapter together to supply the system power.

The PROG pin resistor programs the ratio of the current sensing resistor values R_{S1} and R_{S2} as 2:1 or 1:1. Therefore, four sets of R_{S1} and R_{S2} current sensing resistor values can be used:

- $R_{S1} = 10\text{m}\Omega$, $R_{S2} = 5\text{m}\Omega$
- $R_{S1} = 10\text{m}\Omega$, $R_{S2} = 10\text{m}\Omega$
- $R_{S1} = 20\text{m}\Omega$, $R_{S2} = 10\text{m}\Omega$
- $R_{S1} = 20\text{m}\Omega$, $R_{S2} = 20\text{m}\Omega$

If $20\text{m}\Omega$ R_{S1} is used, the SMBus Information2 register Bit<0> and Bit<8> both need to be set as 1 for the appropriate internal current sensing scaling.

Smaller current sense resistor values reduce the power loss while larger current sense resistor values give better accuracy.

The PROG pin resistor configures the internal current sense gain automatically for different R_{S1} and R_{S2} , such that the SMBus command remains the same for $20\text{m}\Omega$ or $10\text{m}\Omega$ R_{S1} and for $10\text{m}\Omega$ or $5\text{m}\Omega$ R_{S2} . For example, the AdapterCurrentLimit1 register, AdapterCurrentLimit2 register, and the ACProchot register can be programmed with the same SMBus command

value, regardless of whether R_{S1} is $20\text{m}\Omega$ or $10\text{m}\Omega$, to obtain the same current. The ChargeCurrent register, DischargeCurrentLimit register, and DCProchot register can be programmed with the same SMBus command value, regardless of whether R_{S2} is $10\text{m}\Omega$ or $5\text{m}\Omega$, to obtain the same current. Using any option would result in $1\text{mA}/\text{LSB}$ correlation in the SMBus commands.

If R_{S1} and R_{S2} values are different from the PROG pin programming table, the SMBus command needs to be scaled accordingly to obtain the correct current.

Upon POR, the ISL95521 uses the default number of cells in series as [Table 18 on page 37](#) shows and sets the default MaxChargeVoltage register value and default MinChargeVoltage register value accordingly. When SMBus communication is established, the SMBus can program a different number of battery cells in series through SMBus Control1 register Bit<14:13>.

[Tables 19](#) and [20](#) show the adapter current and battery current related settings according to different R_{S1} and R_{S2} options.

TABLE 19. CURRENT SENSING RESISTOR CONFIGURATIONS

CURRENT SENSING RESISTORS		REGISTERS			Kpsys ($\mu\text{A}/\text{W}$)	
		CHARGECURRENT	DISCHARGECURRENTLIMIT* DCPROCHOT**	ADAPTERCURRENTLIMIT1* ADAPTERCURRENTLIMIT2* ACPROCHOT**	CONTROL2 Bit<9> = 0	CONTROL2 Bit<9> = 1
1	$R_{S1} = 10\text{m}\Omega$ $R_{S2} = 5\text{m}\Omega$	Bit<12:5> Max = 1FE0h, 8.160A Min = 0020h, 32mA Default = 0000h, 0A	Bit<13:8> Max = 3F00h, 16.128A Min = 0100h, 256mA *Default = 3F00h, 16.128A **Default = 2000h, 8.192A	Bit<12:7> Max = 1F80h, 8.064A Min = 0080h, 128mA *Default = 1F80h, 8.064A **Default = 1800h, 6.144A	1.14	0.285
2	$R_{S1} = 10\text{m}\Omega$ $R_{S2} = 10\text{m}\Omega$	Bit<12:5> Max = 1FE0h, 8.160A Min = 0020h, 32mA Default = 0000h, 0A	Bit<12:7> Max = 1F80h, 8.064A Min = 0080h, 128mA *Default = 1F80h, 8.064A **Default = 1000h, 4.096A	Bit<12:7> Max = 1F80h, 8.064A Min = 0080h, 128mA *Default = 1F80h, 8.064A **Default = 1800h, 6.144A	1.14	0.285
3	$R_{S1} = 20\text{m}\Omega$ $R_{S2} = 10\text{m}\Omega$	Bit<11:4> Max = 0FF0, 4.080A Min = 0010, 16mA Default = 0000h, 0A	Bit<12:7> Max = 1F80h, 8.064A Min = 0080h, 128mA *Default = 1F80h, 8.064A **Default = 1000h, 4.096A	Bit<11:6> Max = 0FC0h, 4.032A Min = 0040h, 64mA *Default = 0FC0h, 4.032A **Default = 0C00h, 3.072A	2.28	0.57
4	$R_{S1} = 20\text{m}\Omega$ $R_{S2} = 20\text{m}\Omega$	Bit<11:4> Max = 0FF0, 4.080A Min = 0010, 16mA Default = 0000h, 0A	Bit<11:6> Max = 0FC0h, 4.032A Min = 0040h, 64mA *Default = 0FC0h, 4.032A **Default = 0800h, 2.048A	Bit<11:6> Max = 0FC0h, 4.032A Min = 0040h, 64mA *Default = 0FC0h, 4.032A **Default = 0C00h, 3.072A	2.28	0.57

TABLE 20. CURRENT SENSING RESISTOR CONFIGURATIONS

	CURRENT SENSING RESISTORS	ADAPTER CURRENT LIMITED BY ACLIM	CHARGING CURRENT LIMITED BY CCLIM	TRICKLE CHARGE		NVDC PRE-CHARGE PERIOD CURRENT LIMIT (mA)	HPB t1~t2 PERIOD CURRENT LIMIT (mA)	AMON	BMON
				128mA	256mA				
1	R _{S1} = 10mΩ R _{S2} = 5mΩ	V _{ACLIM} /(32*R _{S1})	V _{CCLIM} /(64*R _{S2})	128	256	256	625	32*R _{S1} *I _{ADP}	32*R _{S2} *I _{BAT}
2	R _{S1} = 10mΩ R _{S2} = 10mΩ	V _{ACLIM} /(32*R _{S1})	V _{CCLIM} /(32*R _{S2})	128	256	256	625	32*R _{S1} *I _{ADP}	32*R _{S2} *I _{BAT}
3	R _{S1} = 20mΩ R _{S2} = 10mΩ	V _{ACLIM} /(32*R _{S1})	V _{CCLIM} /(64*R _{S2})	128	256	128	312.5	32*R _{S1} *I _{ADP}	32*R _{S2} *I _{BAT}
4	R _{S1} = 20mΩ R _{S2} = 20mΩ	V _{ACLIM} /(32*R _{S1})	V _{CCLIM} /(32*R _{S2})	128	256	128	312.5	32*R _{S1} *I _{ADP}	32*R _{S2} *I _{BAT}

Programming Switching Frequency

The resistor from the FSET pin to GND programs the default CCM switching frequency, as shown in [Table 21](#). Before soft-start, the ISL95521 sources 10μA current out of the FSET pin and reads the FSET pin voltage to determine the resistor value. However, application environmental noise can pollute the FSET pin voltage and cause incorrect reading. If noise is a concern, it is recommended to connect a capacitor from the FSET pin to GND to provide filtering. The resistor and the capacitor RC time constant should be less than 40μs, so the FSET pin voltage can rise to steady state before the ISL95521 reads it.

TABLE 21. DEFAULT CCM SWITCHING FREQUENCY OPTIONS

FSET-GND RESISTANCE (kΩ)	SWITCHING FREQUENCY (kHz)	
	TYP (±15%) (1% STANDARD RESISTOR)	4-CELL WITH PERIOD STRETCH
0	992	500
22.6	838	430
38.3	729	375
54.9	642	335
69.8	678	460
86.6	614	420
102	561	390
118	517	360
133	513	420
150	477	390
165	449	370
182	421	350
200	417	360
215	395	340
237	375	330
255	350	310

In DE mode of operation, the ISL95521 employs a phase comparator to monitor the PHASE node voltage during low-side switching FET on-time to detect the inductor current zero crossing. The phase comparator needs a minimum on-time of the low-side switching FET for it to recognize inductor current zero crossing. If the low-side switching FET on-time is too short for the phase comparator to successfully recognize the inductor zero crossing, the ISL95521 can lose diode emulation ability. To prevent such scenario, the ISL95521 employs a minimum low-side switching FET on-time. When the intended low-side switching FET on-time is shorter than the minimum value, the ISL95521 stretches the switching period to keep the low-side switching FET on-time at the minimum value, which causes the CCM switching frequency to drop below the set point. This effect is only pronounced in applications using 4-cell battery and high switching frequency setting.

The switching frequency can be changed through SMBus Control2 register Bit<3:0> after POR. See SMBus Control2 register programming table for detailed description.

Soft-Start

When the DCIN pin voltage is higher than 5V, an internal LDO starts to regulate and outputs 5V on the VDDP pin, which is the power supply for the gate drives.

The VDD pin is the 5V power supply for the ISL95521 control circuitry. Renesas recommends using an R-C filter to generate the VDD pin voltage from the VDDP pin voltage. When the VDD pin voltage exceeds its POR, the ISL95521 sources 10μA current out of the PROG pin and reads the pin voltage to determine the PROG resistor value; it sources 10μA current out of the FSET pin and reads the pin voltage to determine the FSET resistor value. The PROG resistor and the FSET resistor values programs the configurations of the ISL95521.

Soft-start begins when the VDD pin voltage exceeds its POR, the ACIN pin voltage exceeds 2V, DCIN pin voltage is higher than the VBAT pin voltage and after the 1.3s or 163ms delay set by Control2 register Bit<5>.

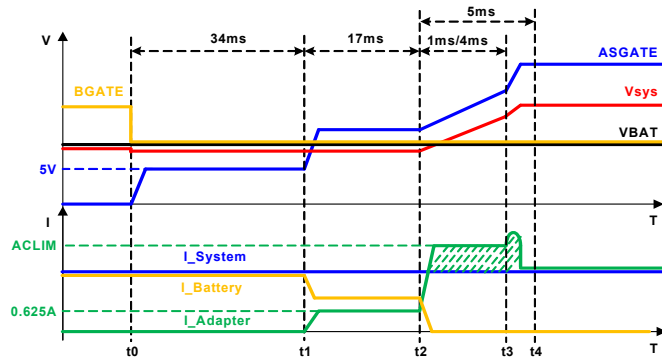


FIGURE 39. SOFT-START WITH $V_{BAT} < 4.5V$ OR $V_{BAT} > 7$

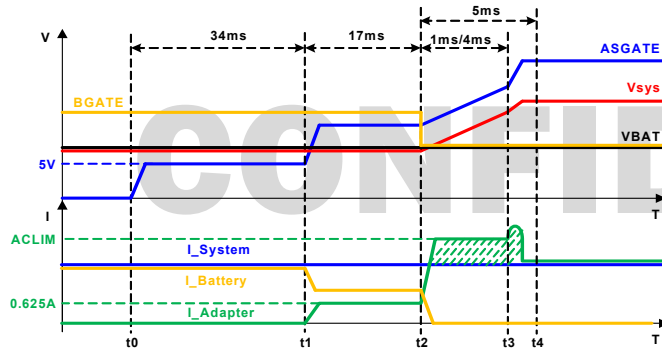


FIGURE 40. SOFT-START WITH $4.5V < V_{BAT} < 7V$

In both HPB charger and NVDC charger configurations, during soft-start, the ISL95521 limits the adapter current in several steps. See Figure 39, at t_0 , the ISL95521 outputs $20\mu A$ current source to charge the ASGATE pin voltage to 5V and holds the ASGATE pin voltage at 5V for 34ms until t_1 . From t_1 to t_2 , the ISL95521 limits the adapter current at 0.625A ($R_{S1} = 10m\Omega$) for 17ms. From t_2 to t_3 , the ISL95521 limits the adapter current at the value set by the ACLIM pin voltage for the next 1ms (default, 4ms option is available through SMBus Control2 register Bit<10>). From t_3 to t_4 , the ISL95521 outputs $20\mu A$ for another 4ms (or 1ms) to fully turn on ASGATE without actively limiting the adapter current. ACOK is asserted high after the ASGATE is fully turned on. The stepped soft-start scheme carefully bias up the system and protects the back-to-back ASGATE FETs against potential damage caused by the inrush current.

Figure 41 shows HPB configuration without battery soft-start waveform when the system load is less than 0.625A. During t_1 through t_2 , the ISL95521 charges the system bus capacitor with (0.625A - system load) current and reaches the adapter voltage level by t_2 . There is not any inrush current after t_2 .

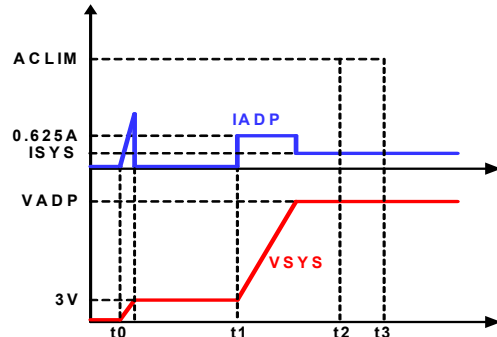


FIGURE 41. NO BATTERY SOFT-START WITH $ISYS < 0.625A$

Figure 42 shows HPB configuration without battery soft-start waveform when the system load is greater than 0.625A but less than the ACLIM-set current level. During t_1 through t_2 , the system bus voltage stays at 3V because there is not enough current to overcome the load to charge the system bus capacitors. During t_2 through t_3 , the ISL95521 charges the system bus capacitor with (ACLIM - system load) current and reaches the adapter voltage by t_3 . There is no inrush current after t_3 .

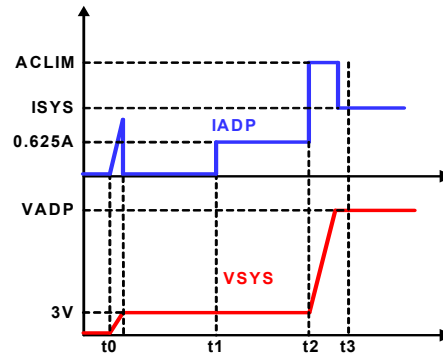


FIGURE 42. NO BATTERY SOFT-START WITH $0.625A < ISYS < ACLIM$

Figure 43 shows HPB configuration without battery soft-start waveform when the system load is greater than the ACLIM-set current level, which is not a recommended mode of operation. During t_1 through t_3 , the system bus voltage stays at 3V because there is not enough current to overcome the load to charge the system bus capacitors. During t_3 through t_4 , the ISL95521 fully turns on the ASGATE and lets the adapter charge the system bus capacitor without current limit.

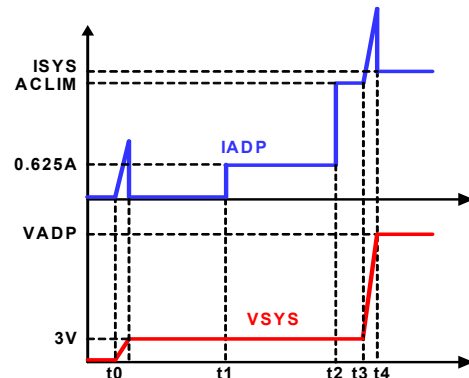


FIGURE 43. NO BATTERY SOFT-START WITH $ISYS > ACLIM$

In HPB charger configuration, the ISL95521 can determine when to turn off the BGATE MOSFET to prevent system voltage disturbance. BGATE MOSFET turns off at t_0 before ASGATE ramps up if $V_{BAT} < 4.5V$ or $V_{BAT} > 7V$ as shown in [Figure 39 on page 40](#) and remains on until t_2 if $4.5V < V_{BAT} < 7V$ as shown in [Figure 40 on page 40](#). Such a scheme prevents the system bus voltage from dropping by MOSFET body-diode voltage drop caused by BGATE MOSFET turning off early. There is a period of time when BGATE and ASGATE are both on, during which a maximum $0.625A$ ($R_{s1} = 10m\Omega$) current flows into the battery if system load current is zero. This should not pose any danger to the battery. But if this scheme is not desired, Control2 register Bit<11> can turn off BGATE before ASGATE ramps up regardless the battery voltage.

In NVDC charger configuration, after fully turning on ASGATE, the ISL95521 starts the switcher. If $V_{BAT} > 3.5V$, BGATE MOSFET remains on for about 28ms after the buck regulator starts switching to prevent the system bus from dropping by a MOSFET body-diode voltage drop caused by BGATE MOSFET turning off early. This 28ms switching is called precharging switching. During the 28ms, the current that flows into battery is controlled at 256mA or 128mA based on the current sensing resistor configuration (see [Table 20 on page 39](#)). If $V_{BAT} < 3.5V$, BGATE MOSFET turns off before the 28ms precharging switching to avoid the charging current to the depleted battery. ACOK signal is asserted high after the precharging switching period.

Adapter Presence Detection and ACOK

ACOK is an open-drain output pin indicating the presence of the adapter and readiness of the adapter to supply power to the system bus. The ISL95521 actively pulls low ACOK in the absence of the adapter.

Use a voltage divider from the adapter voltage to set the ACIN pin voltage. The ISL95521 monitors the ACIN pin voltage to determine the presence of the adapter. When the ACIN pin voltage exceeds 2V, the DCIN pin voltage is higher than the VBAT pin voltage and ASGATE is fully turned on, the ISL95521 allows the external circuit to pull up the ACOK pin. For NVDC configuration, the ISL95521 allows the external circuit to pull up the ACOK pin after the precharging switching period.

For the buck converter to work properly to charge the battery, the ACIN pin voltage divider should be selected such that the minimum adapter voltage set by the ACIN pin voltage divider is higher than the maximum battery voltage. There is a delay between the ACIN pin voltage rising above 2V and ASGATE starting to turn on. The default value of the delay is 1.3s. The delay can be changed to 163ms through SMBus Control2 register Bit<5>.

Adapter Overvoltage Protection

If the ACIN voltage exceeds 3.5V, the ISL95521 considers an adapter overvoltage condition has occurred. It turns off ASGATE MOSFETs to isolate the adapter from the system and deasserts the ACOK signal by pulling it low.

When the ACIN voltage drops below 3.5V, after the 1.3s or 163ms debounce time set by Control2 register Bit<5>, it goes through the ASGATE soft-start to turn on ASGATE.

The adapter OVP function can be disabled through the SMBus Control2 register Bit<8>.

Power Source Selection

The ISL95521 automatically selects the adapter and/or the battery as the source for system power.

The BGATE pin drives an NFET that connects/disconnects the battery from the system and the switcher.

The ASGATE pin drives a pair of back-to-back common source NFETs to connect/disconnect the adapter from the system and the battery.

If the adapter is present, the ISL95521 turns on ASGATE to connect the adapter to the system. In HPB charger configuration, it also turns off BGATE to disconnect the battery from the system when it turns on ASGATE.

If the adapter is absent, the ISL95521 turns off ASGATE and turns on BGATE to connect the battery to the system. If system bus voltage is higher than the battery voltage, the ISL95521 waits until the system bus voltage decays to battery voltage before turning on BGATE to avoid inrush current into the battery.

Battery Learn Mode

The ISL95521 supports battery learn mode. The ISL95521 enters battery learn mode when it receives SMBus Control command (see [Table 14 on page 30](#)), or when the PROG pin voltage is externally pulled to 5V after POR. It is not possible to pull up the PROG pin to 5V if the PROG pin to GND resistor value is chosen to be 0Ω . The ISL95521 exits battery learn mode when it receives the SMBus control command as [Table 14](#) shows, or when the PROG pin voltage is no longer pulled to 5V.

HPB Charger Battery Learn Mode Entry/Exit

In HPB charger configuration battery learn mode, the ISL95521 turns off ASGATE and turns on BGATE regardless of whether the adapter is present or not. This mode of operation is used when it is desired to supply the system power from the battery even when the adapter is plugged in, such as calibration of the battery fuel gauge, hence the name "battery learn mode". The Information1 register Bit<1> indicates ASGATE on or off.

Upon entering battery learn mode, the ISL95521 only turns on BGATE when the system bus voltage decays to battery voltage to avoid inrush current from system bus to battery.

The three ways of exiting HPB charger configuration battery learn mode are:

- Receive battery learn mode exit command through SMBus.
- The PROG pin voltage drops below 5V.
- BATGONE pin voltage goes from logic low-to-high.

In the first two cases, after the ASGATE turn on delay of 1.3s or 163ms (set by Control2 register Bit<5>), the ISL95521 goes through the soft-start process to turn on ASGATE and turn off BGATE as described in ["Soft-Start" on page 39](#).

In the last case, the ISL95521 uses its maximum gate drive strength to turn on ASGATE quickly to prevent system voltage collapse. This action can be completed within $\sim 35\mu s$ after the BATGONE pin voltage level goes to logic high. If the soft-start process is still preferred in this case, use SMBus Control1 register Bit<7> to configure the preference.

NVDC Charger Battery Learn Mode Entry/Exit

In NVDC charger configuration battery learn mode, the ISL95521 turns on BGATE, keeps ASGATE on but turns off the switcher regardless of whether the adapter is present or not.

Upon entering battery learn mode, the ISL95521 only turns on BGATE when the system bus voltage decays to battery voltage to avoid inrush current from system bus to battery.

The three ways of exiting NVDC charger configuration battery learn mode are the same as for HPB charger configuration battery learn mode:

- Receive battery learn mode exit command through SMBus
- The PROG pin voltage drops below 5V
- BATGONE pin voltage goes from logic low-to-high

In all these cases, the ISL95521 resumes switching immediately to supply power to the system bus from the adapter to prevent system voltage collapse.

Hardware-Based Adapter Current Limit

The ACLIM pin voltage set hardware-based adapter current limit provides an extra level of protection in the unlikely event of SMBus communication failure.

[Equation 1](#) gives the relationship between the ACLIM pin voltage and the hardware-based adapter current limit, where $V_{ACLIMHW}$ is ACLIM pin voltage in Volts and $I_{ACLIMHW}$ is the hardware-based adapter current limit in Amperes.

$$I_{ACLIMHW} = \frac{V_{ACLIMHW}}{32 \times R_{s1}} \quad (\text{EQ. 1})$$

[Equation 1](#) is true for all current sensing resistor configurations.

The ISL95521 uses the lower value of the hardware-set adapter current limit and the SMBus programmed adapter current limit as the actual adapter current limit.

The ACLIM pin voltage also sets the ASGATE soft-start current limit level from t2 to t3. The ACLIM current limit function can be disabled through SMBus Control2 register Bit<13> after ACOK assertion, such that ACLIM pin is only used for ASGATE soft-start current limit from t2 to t3 as shown in [“Soft-Start” on page 39](#).

HPB Charger Turbo Mode Support

Turbo mode refers to the scenario when the system draws more power than the adapter’s power rating. It prompts the need for the switcher to change from forward buck mode of operation to reverse boost mode of operation to reverse the energy flow. Such mode of operation enables the battery to help the adapter provide the required system power. Such operation has been widely used in many systems, such as “sun mode” and “eclipse mode” for bidirectional battery charger/discharger used on satellites with solar panels as the power source acting as the adapter (reference “A zero voltage switching bidirectional battery charger/discharger for the NASA EOS Satellite”, Dan M. Sable, Fred C. Lee and Bo H. Cho, APEC 1992 Conference Proceedings).

In HPB charger configuration, the ISL95521 normally operates the switcher as a synchronous buck converter with diode emulation. When the buck converter is in light load condition, it enters DCM operation with reduced switching frequency to increase efficiency. From the description of the R3 modulator operational principle, the COMP pin voltage is lower at lighter load and can reach the low clamp.

In Turbo mode, the ISL95521 operates the switcher in reverse-boost mode to boost energy from the battery to the adapter voltage rail, such that the adapter current is limited at the adapter current limit set point while the battery supplies the additional power required by the system.

The Control1 register Bit<10> enables/disables the Turbo/Boost function. See [Table 14 on page 30](#) for details.

The ISL95521 enters Turbo mode when all of the following criteria are met:

- Adapter current is within 80mA of AdapterCurrentLimit1 (or AdapterCurrentLimit2 if two level adapter current limit function is enabled) register setting.
- Battery charging current is less than 150mA.
- COMP pin voltage is lower than 1.4V.

Meeting these criteria means that the ISL95521 only enters Turbo mode precisely when it is absolutely necessary. For example, assuming the adapter voltage is 20V, the adapter current limit is 4A (80W rating) and the ISL95521 is charging 8V battery at 5A rate (40W charging power). If the system load increases from 0W to 79W instantaneously, the adapter current increases from 2A to 5.95A instantaneously, exceeding the 4A current limit level. However, the adapter current loop takes control and decreases the charging current to limit the adapter current at 4A, eventually providing 79W system power and 1W battery charging power. In such case, the ISL95521 does not need to enter Turbo mode adapter and can conserve battery energy. In the same example, if the system load increases from 0W to 81W instantaneously, the adapter current increases from 2A to 6.05A instantaneously, exceeding the 4A current limit level. The adapter current loop takes control and decreases the charging current to limit the adapter current at 4A. Thus, the ISL95521 eventually determines that it needs to enter Turbo mode so the adapter provides 80W and the battery provides 1W, to provide 81W to the system.

The interaction of the control loops within the ISL95521, including the adapter current loop, the charging current loop and the battery full charging voltage loop, determines the timing of the Turbo mode entry. The timing strongly depends on the control loop compensation design and the interaction among the loops. In the previous example, compared with system power instantaneously increasing from 0W to 81W, system power instantaneously increasing from 0W to 160W causes the ISL95521 to enter Turbo mode much faster because the loops drive the circuit parameters to meet the three Turbo mode entry criteria much quicker when the adapter is more severely overloaded.

The ISL95521 exits Turbo mode when one of the following criteria are met:

- Battery charging current exceeds 150mA ($R_{S2} = 10m\Omega$).
- Adapter current is less than AdapterCurrentLimit register setting and COMP voltage is lower than 1.4V.
- Battery discharging current is less than 140mA (for $R_{S2} = 10m\Omega$) for 140ms.

In Turbo mode, if the battery discharging current reaches the DischargeCurrentLimit register set value, ISL95521 limits the battery discharging current even if the adapter current exceeds the adapter current limit setting.

[Table 22](#) shows the ISL95521 HPB configuration charge function and turbo/boost function control truth table.

TABLE 22. HPB CHARGER BEHAVIOR TRUTH TABLE

TURBO/BOOST MODE CONTROL BIT	ENABLECHARGING CONTROL BIT	CHARGECURRENT REGISTER		
0 = ENABLE BOOST 1 = DISABLE BOOST	0 = DISABLE CHARGING 1 = ENABLE CHARGING	0 = 0A COMMAND 1 = NON ZERO VALID COMMAND	CHARGE?	BOOST?
0	0	0	NO	YES
0	0	1	NO	YES
0	1	0	NO	YES
0	1	1	YES (Fast charge and trickle charge enabled)	YES
1	0	0	NO	NO
1	0	1	NO	NO
1	1	0	NO	NO
1	1	1	YES (Fast charge and trickle charge enabled)	NO

TABLE 23. NVDC CHARGER BEHAVIOR TRUTH TABLE

TURBO/BOOST MODE CONTROL BIT	ENABLECHARGING CONTROL BIT	CHARGECURRENT REGISTER	BGATE ON/OFF	
0 = ENABLE TURBO 1 = DISABLE TURBO	0 = DISABLE CHARGING 1 = ENABLE CHARGING	0 = 0A COMMAND 1 = NON ZERO VALID COMMAND	SYSTEM LOAD NOT IN TURBO MODE RANGE	SYSTEM LOAD IN TURBO MODE RANGE
0	0	0	OFF	ON
0	0	1	OFF	ON
0	1	0	OFF	ON
0	1	1	ON for fast charge; trickle charge enabled	ON
1	0	0	OFF	OFF
1	0	1	OFF	OFF
1	1	0	OFF	OFF
1	1	1	ON for fast charge; trickle charge enabled	ON

NVDC Charger Turbo Mode Support

In NVDC charger configuration and Turbo mode, the ISL95521 turns on the BGATE FET to limit the adapter current at the adapter current limit set point while the battery supplies the rest of the power required by the system. To turn on BGATE in Turbo mode, the CSON pin voltage needs to be 175mV lower than the VBAT pin voltage. If the ISL95521 detects 150mA charging current or if the battery discharging current is less than 140mA for 140ms, it turns off BGATE to exit Turbo mode. See [Table 23](#) for BGATE operation.

Two-Level Adapter Current Limit

In a real system, Turbo event usually does not last very long. It is often no longer than milliseconds, a time length during which the adapter can supply current higher than its DC rating. The ISL95521 employs two-level adapter current limit to fully take advantage of adapter's surge capability and minimize the power draw from the battery.

[Figure 44](#) shows the two SMBus-programmable adapter current limit levels, AdapterCurrentLimit1 and AdapterCurrentLimit2, as well as the durations t1 and t2. The two level adapter current limit function is initiated when the adapter current reaches the AdapterCurrentLimit1 register setting and it starts at AdapterCurrentLimit2 for t2 duration and then changes to AdapterCurrentLimit1 for t1 duration before repeating the pattern. These parameters can set adapter current limit with an envelope that allows the adapter to temporarily output surge current without requiring the charger to enter Turbo mode. Such operation maximizes battery life.

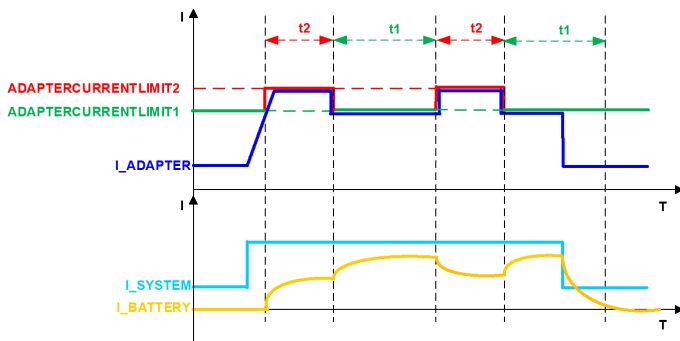


FIGURE 44. TWO LEVEL ADAPTER CURRENT LIMIT

AdapterCurrentLimit1 register value can be higher or lower than AdapterCurrentLimit2 value.

The two-level adapter current limit function can be enabled and disabled through SMBus Control2 register Bit<6>. When the two-level adapter current limit function is disabled, only AdapterCurrentLimit1 value is used as the adapter current limit and AdapterCurrentLimit2 value is ignored.

Current Monitor

The ISL95521 provides an adapter current monitor through the AMON pin and a battery discharging current monitor through BMON pin. The AMON pin voltage is 32x the ($V_{CSIP} - V_{CSIN}$) voltage and the BMON pin voltage is 32x the ($V_{CSON} - V_{CSOP}$) voltage.

AMON and BMON function can be enabled or disabled through SMBus Control1 register Bit<2> and Bit<3>, respectively (see [Table 14 on page 30](#)).

PSYS Monitor

The ISL95521 PSYS pin provides a measure of the instantaneous power consumption of the entire platform. The PSYS pin outputs a current source described by [Equation 2](#).

$$I_{PSYS} = K_{PSYS} \times (V_{ADP} \times I_{ADP} + V_{BAT} \times I_{BAT}) \quad (\text{EQ. 2})$$

K_{PSYS} is based on current sensing resistors R_{S1} and R_{S2} configuration and is selectable through SMBus Control2 register Bit<9>. See [Table 19 on page 38](#) for details. V_{ADP} is the adapter voltage in Volts, I_{ADP} is the adapter current in Amperes, V_{BAT} is the battery voltage and I_{BAT} is the battery discharging current. When the battery is discharging, I_{BAT} is a positive value; when the battery is being charged, I_{BAT} is a negative value. The battery voltage V_{BAT} is detected through the CSON pin to maximize the power monitor accuracy in NVDC configuration trickle charge mode.

The PSYS information includes the power loss of the charger circuit and the actual power delivered to the system. Resistor R_{PSYS} connected between the PSYS pin and GND converts the PSYS information from current to voltage.

The PSYS function can be enabled or disabled through SMBus Control1 register Bit<4> as shown in [Table 14 on page 30](#).

Charger Timeout

The ISL95521 includes a timer to ensure the SMBus master is active and to prevent overcharging the battery. The ISL95521 terminates charging if the charger has not received a write to the MaxChargeVoltage or ChargeCurrent register within 175s. If a time out occurs, MaxChargeVoltage or ChargeCurrent register must be written to re-enable charging.

The ISL95521 allows you to disable the charger timeout function through SMBus Control1 register Bit<15> as [Table 14](#) shows.

Trickle Charging

The ISL95521 supports trickle charge to an overly discharged battery. It can activate the trickle charge function when the battery voltage is lower than MinChargeVoltage setting. The VBAT pin is the battery voltage sense point for trickle charge mode.

To enable trickle charge, set EnableCharging control bit to 1 and set ChargeCurrent register to a valid non-zero value. To disable trickle charge, either set EnableCharging control bit to 0 or set ChargeCurrent register to 0. [Table 22 on page 43](#) shows the condition to enable HPB configuration trickle charge mode. [Table 23 on page 43](#) shows the condition to enable the NVDC configuration trickle charge mode.

The trickle charging current can be programmed to be 256mA, 128mA or 64mA through SMBus Control2 register Bit<7> and Bit<12> as shown in [Table 15 on page 32](#).

In HPB charger configuration, the ISL95521 charges the battery at 256mA, 128mA, or 64mA in trickle charge mode.

In NVDC charger configuration trickle charge mode, the ISL95521 regulates the system voltage at 450mV above the

MinChargeVoltage register value. An independent control loop regulates BGATE FET gate voltage to regulate the battery charging current at 256mA, 128mA, or 64mA.

When the battery voltage is charged to 175mV above the MinChargeVoltage register value, the ISL95521 enters fast charging mode by limiting the charging current at the ChargeCurrentLimit register setting.

The ISL95521 CSON pin sinks about 20µA current and the CSOP pin sinks about 35µA current to provide the bias power for the battery current sensing amplifier. If there is a resistor series in the CSON pin, the voltage drop on this resistor creates a small offset such that the actual battery charging current becomes slightly smaller. If there is a resistor series in the CSOP pin, the voltage drop on this resistor creates a small offset such that the actual battery charging current becomes slightly larger. These two resistors can slightly tweak the actual battery charging current.

NVDC Charger System Voltage Regulation

If the battery is absent, the ISL95521 regulates the system bus voltage at the higher value of 7.168V and the MinChargeVoltage register setting.

If the battery is present but BGATE is turned off, the ISL95521 regulates the system bus voltage at the higher value of 7.168V and the MaxChargeVoltage register setting.

The CSON pin senses the system bus voltage.

To ensure the system voltage does not collapse when the battery is absent, the ISL95521 does not limit the adapter current if the system power draw causes the adapter current to exceed the adapter current limit. This function can be enabled or disabled through SMBus Control2 register Bit<4>.

Charging Current WOC

The ISL95521 provides the WOC (Way-Overcurrent Protection) function for the current flowing into the battery against the highside MOSFET short and inductor short scenarios. It employs the CCLIM pin to set the WOC threshold. ISL95521 monitors the CSOP-CSON voltage and compares it with the WOC threshold. When the WOC comparator is tripped, it either terminates the PWM switching pulse, or turns off ASGATE and deassert ACOK, configurable through SMBus Control1 register Bit<11>.

When the WOC function is enabled through Control1 register Bit<11>, if the WOC comparator is tripped, the ISL95521 counts once within every 20µs. Whenever ISL95521 counts to 7 times in 656ms, it turns off ASGATE and deassert ACOK immediately. After the 1.3s or 163ms debounce time set by Control2 register Bit<5>, it goes through the ASGATE soft-start to retry.

When the WOC function is disabled through Control1 register Bit<11>, as long as the WOC comparator is tripped within every 20µs, it terminates the PWM switching pulse immediately for the rest of the time of the 20µs.

The CCLIM pin voltage sets the charging current WOC threshold. Equations 3 and 4 give the relationship between the CCLIM pin voltage and the WOC threshold, where $V_{CCLIMHW}$ is the CCLIM pin voltage in Volts and I_{WOC} is the WOC threshold in Amperes.

$$I_{WOC} = 1.23 \times \frac{V_{CCLIMHW}}{64 \times R_{S2}} \quad (\text{EQ. 3})$$

Equation 3 is true for $R_{S1}:R_{S2} = 2:1$ ($R_{S1} = 10\text{m}\Omega$ and $R_{S2} = 5\text{m}\Omega$ or $R_{S1} = 20\text{m}\Omega$ and $R_{S2} = 10\text{m}\Omega$).

$$I_{WOC} = \frac{V_{CCLIMHW}}{32 \times R_{S2}} \quad (\text{EQ. 4})$$

Equation 4 is true for $R_{S1}:R_{S2} = 1:1$ ($R_{S1} = 10\text{m}\Omega$ and $R_{S2} = 10\text{m}\Omega$ or $R_{S1} = 20\text{m}\Omega$ and $R_{S2} = 20\text{m}\Omega$).

The WOC comparator monitors the peak current crossing the battery current sensing resistor R_{S2} , so the WOC threshold needs to be set at least half of the inductor ripple current higher than the SMBus-programmed charging current command to avoid the false tripping in normal charging.

For the WOC function to work properly, it needs to connect an RC filter from the CSON pin to ground to increase the overcurrent detection sensitivity. This RC filter time constant should be selected carefully and cannot be too large, otherwise the WOC could be falsely tripped by the current overshoot flowing into the battery when ISL95521 exits turbo mode after system bus load release. Meanwhile, the WOC threshold should be set high enough to avoid the false trip by the current overshoot flowing into the battery.

The current spike flowing into the battery could cause a voltage spike at the battery connector due to the battery current path impedance. For the NVDC charger, one should pay attention to this voltage spike at VBAT pin so as not to trip the battery 4.6V/cell OVP function, otherwise the BGATE FET turns off due to the battery OVP such that the current flowing on R_{S2} is gone. It is recommended to add an RC filter at VBAT in this scenario.

Over-Temperature Protection

The ISL95521 turns off the internal LDO for self-protection when the junction temperature exceeds +155°C. The internal LDO stays off until the junction temperature falls below +128°C.

In HPB charger configuration, the ISL95521 puts the charger in standby mode after declaring over-temperature protection.

In NVDC charger configuration, the ISL95521 stops switching after declaring over-temperature protection.

When the temperature falls below +128°C, the ISL95521 enables the internal LDO and resumes operation.

Battery Overvoltage Protection

The battery overvoltage protection function prevents the battery from being overcharged.

In HPB charger configuration, the ISL95521 stops switching if battery voltage is higher than MaxChargeVoltage register setting. If the battery voltage is higher than 4.6V/cell, it stops charging.

In NVDC charger configuration, the ISL95521 stops switching if the system bus voltage is higher than MaxChargeVoltage register value; if the battery voltage is higher than 4.6V/cell, it turns off BGATE to stop charging.

The MaxChargeVoltage register setting should be less than 4.6V/cell.

System Bus Short-Circuit Detection

If the ACIN pin is pulled below 2V by the system bus excessive current or short-circuit, the ISL95521 turns off ASGATE to isolate the adapter from the system bus. When the ACIN pin voltage rises above 2V again and after the 1.3s or 163ms delay programmed by Control2 register Bit<5>, ASGATE turns on again with soft-start.

An external circuit, as shown in Figure 45, can detect the system bus short-circuit. If the system bus is short-circuit, the ACIN pin is pulled below 2V by diode D₁, so ASGATE cannot turn on. While in normal operation, ASGATE still can turn on when the system bus is charged up above 2V through D₁.

In normal operation, to charge up the system bus above 2V through D₁ quickly, the ACIN pin voltage divider resistor values need to be small, which in sequence causes larger constant power consumption on the ACIN pin voltage divider resistors. Two optional circuits (as shown in Figure 45) can be dedicated to charge up the system bus. Renesas recommends using option 1 circuit for HPB configuration and option 2 circuit for NVDC configuration.

For option 2 circuit, the R₃ and R₄ voltage divider voltage, that is, the Q₁ gate voltage, needs to be 2V higher than the Q₁ gate source threshold voltage such that Q₁ can be turned on and the system bus can be charged up above 2V through R₂ and Q₁. Meanwhile, the R₃ and R₄ voltage divider voltage needs to be less than the final system bus voltage such that Q₁ can be turned off in normal operation to avoid the leakage current through Q₁.

It should be noted that with the option 1 circuit there is leakage current through R₁ and D₂ when the adapter voltage is higher than the system bus voltage such as in Learn mode or for NVDC configuration.

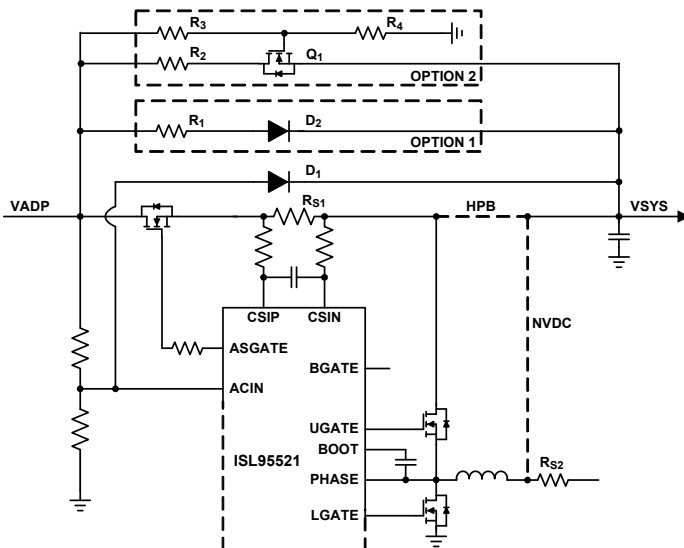


FIGURE 45. EXTERNAL SYSTEM BUS SHORT DETECTION CIRCUIT

Adapter Input Filter

The adapter cable parasitic inductance and capacitance can cause some voltage ring or overshoot spike at the adapter connector node when the adapter is hot plugged in. This voltage spike could damage the ASGATE MOSFET or the ISL95521 pins

connecting to the adapter connector node. One low cost solution is to add an RC snubber circuit at the adapter connector node to clamp the voltage spike as shown in Figure 46. A practical value of the RC snubber is 2.2Ω to 2.2μF while the appropriate values and power rating should be carefully characterized based on the actual design. Meanwhile it is not recommended to add a pure capacitor at the adapter connector node, which can cause an even bigger voltage spike due to the adapter cable or the adapter current path parasitic inductance.

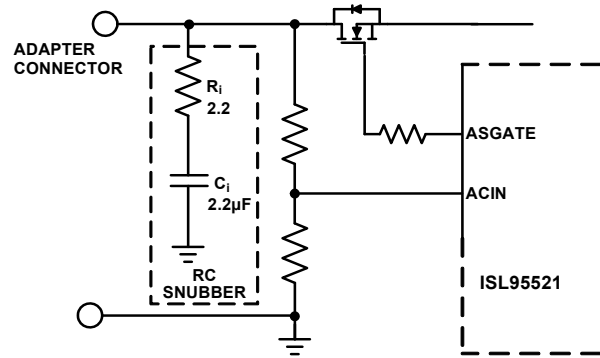


FIGURE 46. ADAPTER INPUT RC SNUBBER CIRCUIT

Test with e-Load Constant Voltage Mode

An electronic load in constant voltage mode (e-Load in CV mode) often emulates a battery in testing a battery charger. However, an e-Load in CV mode does not accurately emulate the characteristics of a real battery, particularly the ESR. Such discrepancy can result in much more exaggerated output voltage switching ripple observed by the battery charger and present inaccurate test results. It is recommended to add a capacitor, such as 680μF, at the terminal of the e-Load to better match the impedance of a real battery, such that the test result better represents that with a real battery. As a precaution for potentially testing with an e-load with large ESR, it is recommended to add an R-C filter at the VBAT pin to smooth the switching ripple observed by the ISL95521. The recommended range of the R-C time constant is 200μs to 1ms.

General Application Information

This design guide provides a high-level explanation of the steps necessary to design a single-phase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced in the following section. In addition to this guide, complete reference designs that include schematics, bill of materials and example board layouts are provided.

Select the LC Output Filter

The duty cycle of an ideal buck converter in CCM is a function of the input and the output voltage. This relationship is written by Equation 5:

$$D = \frac{V_{OUT}}{V_{IN}} \quad (\text{EQ. 5})$$

The output inductor peak-to-peak ripple current is written by [Equation 6](#):

$$I_{P-P} = \frac{V_{OUT} \cdot (1-D)}{f_{SW} \cdot L} \quad (\text{EQ. 6})$$

A typical step-down DC/DC converter has an I_{P-P} of 20% to 40% of the maximum DC output load current for a practical design. The value of I_{P-P} is selected based upon several criteria such as MOSFET switching loss, inductor core loss and the resistive loss of the inductor winding.

The DC copper loss of the inductor can be estimated by [Equation 7](#):

$$P_{COPPER} = I_{LOAD}^2 \cdot DCR \quad (\text{EQ. 7})$$

Where I_{LOAD} is the converter output DC current.

The copper loss can be significant so attention has to be given to the DCR selection. Another factor to consider when choosing the inductor is its saturation characteristics at elevated temperatures. A saturated inductor could cause destruction of circuit components.

A DC/DC buck regulator must have output capacitance C_O into which ripple current I_{P-P} can flow. Current I_{P-P} develops a corresponding ripple voltage V_{P-P} across C_O , which is the sum of the voltage drop across the capacitor ESR and of the voltage change stemming from charge moved in and out of the capacitor. These two voltages are written by [Equations 8 and 9](#):

$$\Delta V_{ESR} = I_{P-P} \cdot ESR \quad (\text{EQ. 8})$$

$$\Delta V_C = \frac{I_{P-P}}{8 \cdot C_O \cdot f_{SW}} \quad (\text{EQ. 9})$$

If the output of the converter has to support a load with high pulsating current, several capacitors need to be paralleled to reduce the total ESR until the required V_{P-P} is achieved. The inductance of the capacitor can cause a brief voltage dip if the load transient has an extremely high slew rate. Low inductance capacitors should be considered in this scenario. A capacitor dissipates heat as a function of RMS current and frequency. Be sure that I_{P-P} is shared by a sufficient quantity of paralleled capacitors so that they operate below the maximum rated RMS current at f_{SW} . Take into account that the rated value of a capacitor can fade as much as 50% as the DC voltage across it increases.

Select the Input Capacitor

The important parameters for the input capacitance are the voltage rating and the RMS current rating. For reliable operation, select capacitors with voltage and current ratings above the maximum input voltage and capable of supplying the RMS current required by the switching circuit. Their voltage rating should be at least 1.25x greater than the maximum input voltage, while a voltage rating of 1.5x is a preferred rating. [Figure 47 on page 47](#) is a graph of the input capacitor RMS ripple current, normalized relative to output load current, as a function of

duty cycle and is adjusted for converter efficiency. The normalized RMS ripple current calculation is written as [Equation 10](#):

$$I_{C_{IN}(RMS,NORMALIZED)} = \frac{I_{MAX} \cdot \sqrt{D \cdot (1-D) + \frac{D \cdot k^2}{12}}}{I_{MAX}} \quad (\text{EQ. 10})$$

where:

- I_{MAX} is the maximum continuous I_{LOAD} of the converter
- k is a multiplier (0 to 1) corresponding to the inductor peak-to-peak ripple amplitude expressed as a percentage of I_{MAX} (0% to 100%)
- D is the duty cycle that is adjusted to take into account the efficiency of the converter, which is written as [Equation 11](#):

$$D = \frac{V_{OUT}}{V_{IN} \cdot \text{EFF}} \quad (\text{EQ. 11})$$

In addition to the capacitance, some low ESL ceramic capacitance is recommended to decouple between the drain of the high-side MOSFET and the source of the low-side MOSFET.

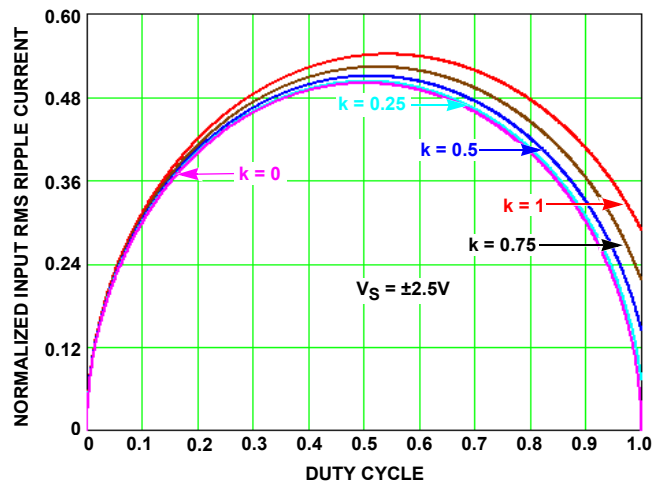


FIGURE 47. NORMALIZED RMS INPUT CURRENT AT EFF = 1

Select the Switching Power MOSFET

Typically, a MOSFET cannot tolerate even brief excursions beyond their maximum drain-to-source voltage rating. The MOSFETs used in the power stage of the converter should have a maximum VDS rating that exceeds the sum of the upper voltage tolerance of the input power source and the voltage spike that occurs when the MOSFET switches off.

There are several power MOSFETs readily available that are optimized for DC/DC converter applications. The preferred high-side MOSFET emphasizes low gate charge so that the device spends the least amount of time dissipating power in the linear region. Unlike the low-side MOSFET which has the drain-to-source voltage clamped by its body diode during turn off, the high-side MOSFET turns off with a VDS of approximately $V_{IN} - V_{OUT}$, plus the spike across it. The preferred low-side MOSFET emphasizes low $r_{DS(ON)}$ when fully saturated to minimize conduction loss. It should be noted that this is an optimal configuration of MOSFET selection for low duty cycle applications ($D < 50\%$). For higher

output, low input voltage solutions, a more balanced MOSFET selection for high- and low-side devices can be warranted.

For the low-side (LS) MOSFET, the power loss can be assumed to be conductive only and is written as [Equation 12](#):

$$P_{CON_LS} \approx I_{LOAD}^2 \cdot r_{DS(ON)_LS} \cdot (1 - D) \quad (\text{EQ. 12})$$

For the high-side (HS) MOSFET, its conduction loss is written by [Equation 13](#):

$$P_{CON_HS} = I_{LOAD}^2 \cdot r_{DS(ON)_HS} \cdot D \quad (\text{EQ. 13})$$

For the high-side MOSFET, the switching loss is written as [Equation 14](#):

$$P_{SW_HS} = \frac{V_{IN} \cdot I_{VALLEY} \cdot t_{ON} \cdot f_{SW}}{2} + \frac{V_{IN} \cdot I_{PEAK} \cdot t_{OFF} \cdot f_{SW}}{2} \quad (\text{EQ. 14})$$

where:

- I_{VALLEY} is the difference of the DC component of the inductor current minus 1/2 of the inductor ripple current
- I_{PEAK} is the sum of the DC component of the inductor current plus 1/2 of the inductor ripple current
- t_{ON} is the time required to drive the device into saturation
- t_{OFF} is the time required to drive the device into cut-off

Renesas recommends using a 2.2 μ F (10V) VDD/VDDP capacitor that has an effective capacitance higher than 0.4 μ F at 5V and x1.6 effective capacitance at the BOOT pin at 5V.

Select the Bootstrap Capacitor

The selection of the bootstrap capacitor is written by [Equation 15](#):

$$C_{BOOT} = \frac{Q_g}{\Delta V_{BOOT}} \quad (\text{EQ. 15})$$

where:

- Q_g is the total gate charge required to turn on the high-side MOSFET
- ΔV_{BOOT} is the maximum allowed voltage decay across the boot capacitor each time the high-side MOSFET is switched on

As an example, suppose the high-side MOSFET has a total gate charge Q_g of 25nC at $V_{GS} = 5V$ and a ΔV_{BOOT} of 200mV. The calculated bootstrap capacitance is 0.125 μ F; for a comfortable margin, select a capacitor that is double the calculated capacitance. In this example, 0.22 μ F is sufficient. Use an X7R or X5R ceramic capacitor.

Renesas recommends using a 2.2 μ F (10V) VDD/VDDP capacitor that has an effective capacitance higher than 0.4 μ F at 5V and x1.6 effective capacitance at the BOOT pin at 5V.

Select the DCIN Filter

An R-C filter is connected at the DCIN pin. Renesas recommends connecting a 10 Ω DCIN resistor between the DCIN pin and the VADP/VSYS diodes, and connecting a 4.7 μ F (50V) DCIN capacitor with an effective capacitance higher than 0.4 μ F at 20V to GND.

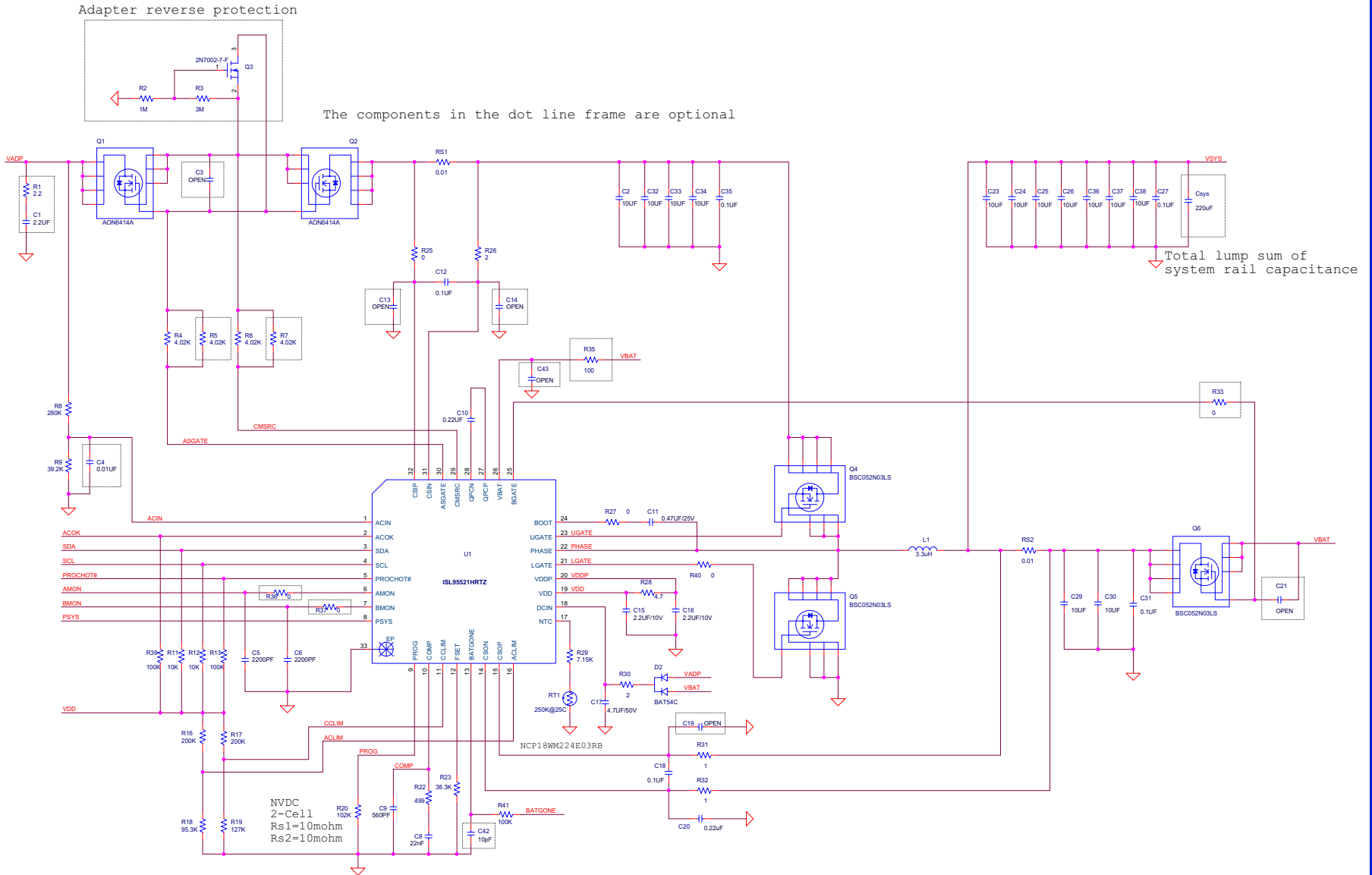
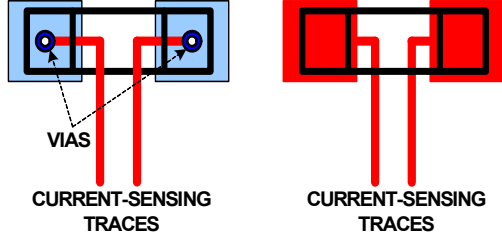


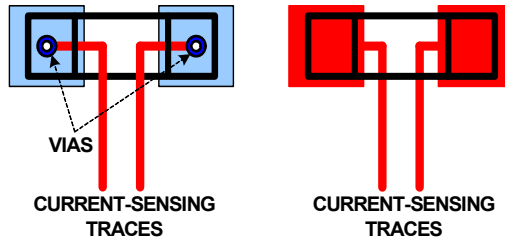
FIGURE 49. ISL95521 NVDC CONFIGURATION REFERENCE DESIGN

Layout Guidelines

PIN #	SYMBOL	LAYOUT GUIDELINES
BOTTOM PAD	GND	Connect this ground pad to the ground plane through low impedance path. Renesas recommends using at least five vias to connect to ground planes in PCB to ensure there is sufficient thermal dissipation directly under the IC.
1	ACIN	Place the voltage divider resistors and the optional decoupling capacitor in general proximity of the controller.
2	ACOK	No special consideration.
3	SDA	
4	SCLK	
5	PROCHOT#	
6	AMON	
7	BMON	No special consideration.
8	PSYS	
9	PROG	Place the PROG programming resistor in general proximity of the controller.
10	COMP	Place the compensation components in general proximity of the controller.
11	CCLIM	Place the CCLIM voltage divider resistors in general proximity of the controller.
12	FSET	Place the FSET programming resistor in general proximity of the controller.
13	BATGONE	Place the 100kΩ resistor series in the BATGONE signal trace and the optional decoupling capacitor in general proximity of the controller.
14	CSON	Run two dedicated trace with decent width in parallel (close to each other to minimize the loop area) from the two terminals of the battery current-sensing resistor to the IC. Place the differential mode and common-mode RC filter components in general proximity of the controller.
15	CSOP	<p>Route the current-sensing traces through vias to connect the center of the pads; or route the traces into the pads from the inside of the current-sensing resistor. The following drawings show the two preferred ways of routing current sensing traces.</p>  <p style="text-align: center;">VIAS</p> <p style="text-align: center;">CURRENT-SENSING TRACES</p> <p style="text-align: center;">CURRENT-SENSING TRACES</p>
16	ACLIM	Place the ACLIM voltage divider resistors in general proximity of the controller.
17	NTC	Place the resistor series with the NTC thermistor in general proximity of the controller. Place the NTC thermistor at the point where the temperature to be monitored. Note if the NTC thermistor is too close to the switching components, it can couple the switching noise to the NTC pin.
18	DCIN	Place the OR diodes and the RC filter in general proximity of the controller.
19	VDD	Place the RC filter from VDDP pin in general proximity of the controller.
20	VDDP	Place the decoupling capacitor in general proximity of the controller.
21	LGATE	Run LGATE trace in parallel with UGATE and PHASE traces on the same PCB layer. Use decent width. Avoid any sensitive analog signal trace from crossing over or getting close.

Layout Guidelines (Continued)

PIN #	SYMBOL	LAYOUT GUIDELINES
22	PHASE	<p>Run these two traces in parallel fashion with decent width. Avoid any sensitive analog signal trace from crossing over or getting close. Renesas recommends routing PHASE trace to high-side MOSFET source pin instead of general copper.</p> <p>Place the IC close to the switching MOSFET's gate terminals and keep the gate drive signal traces short for a clean MOSFET drive. The IC can be placed on the opposite side of the switching MOSFETs.</p> <p>Place the input capacitors as close as possible to the switching high-side MOSFET drain and the low-side MOSFET source; and use shortest PCB trace connection. Place these capacitors on the same PCB layer with the MOSFETs instead of on different layers and using vias to make the connection.</p> <p>Place the inductor input terminal to the switching high-side MOSFET drain and low-side MOSFET source terminal as close as possible. Minimize this phase node area to lower the electrical and magnetic field radiation but make this phase node area big enough to carry the current. Place the inductor and the switching MOSFETs on the same layer of the PCB.</p>
23	UGATE	
24	BOOT	
25	BGATE	Use decent width trace from the IC to the BGATE MOSFET gate.
26	VBAT	<p>Place the RC filter in general proximity of the controller. Run a dedicated trace from the battery positive connection point to the IC.</p> <p>In HPB configuration, separate this trace with the trace connecting the CSON pin.</p>
27	QPCP	Place the charge pump flying capacitor in general proximity of the controller. Route trace with decent width.
28	QPCN	
29	CMSRC	Run these two traces in parallel fashion with decent width.
30	ASGATE	
31	CSIN	<p>Place the battery current sensing resistor right next to the inductor output. Run two dedicated trace with decent width in parallel (close to each other to minimize the loop area) from the two terminals of the adapter current-sensing resistor to the IC. Place the differential mode and common-mode RC filter components in general proximity of the controller.</p> <p>Route the current-sensing traces through vias to connect the center of the pads; or route the traces into the pads from the inside of the current-sensing resistor. The following drawings show the two preferred ways of routing current-sensing traces.</p>
32	CSIP	



Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
Jul 18, 2019	FN8771.2	<p>Added related literature section on page 1. Updated links throughout document. Ordering Information table on page 9 - Added ISL95521HRZ-T and tape and reel column. Removed ISL95521COMBO-HYBEVZ and ISL95521COMBONVDCEVZ evaluation boards Modified pin descriptions for pins 18, 19, 20, and 24 on pages 10 and 11. Added information about recommended VDD/VDDP capacitors to the "Select the Switching Power MOSFET" section on page 47. Added information about recommended bootstrap capacitors to the "Select the Bootstrap Capacitor" section on page 46. Added "Select the DCIN Filter" section on page 48. Updated Figure 48 on page 49 and Figure 49 on page 50 Updated package outline drawing from rev 4 to rev 5. Changes:</p> <ul style="list-style-type: none"> - Side View: Changed "A" to "X" for detail name. Removed "0.050" dimension as it is already listed in Detail X. Corrected arrow with dimension (0.90±0.10) to point to correct dimension line. - Bottom View: Removed 'b' next to Note 4 reference. This is no longer needed. Removed diagonal line inside exposed pad. Notes - Removed 'b' from Note 4 no longer needed. <p>Removed About Intersil section. Updated disclaimer.</p>
Sep 23, 2015	FN8771.1	<p>In "Electrical Specifications" on page 12 updated the following: -Battery Current "IBAT_BGATE_ON NVDC" changed typical to 230µA and maximum to 290µA. In "Electrical Specifications" on page 15 updated the following: -ACIN Threshold Rising - changed typical to 2.03V. -ACIN Threshold Falling - changed typical to 2V and minimum to 1.9V -ACIN OVP Rising - changed typical to 3.5V, -ACIN OVP Falling - changed minimum to 3.3V</p>
Sep 16, 2015	FN8771.0	Initial Release

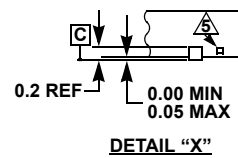
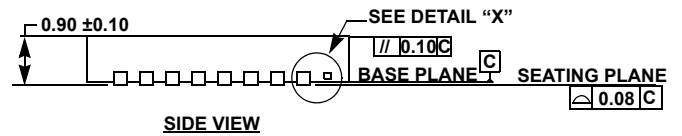
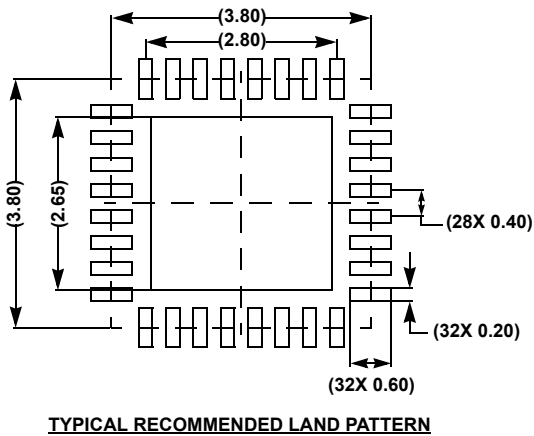
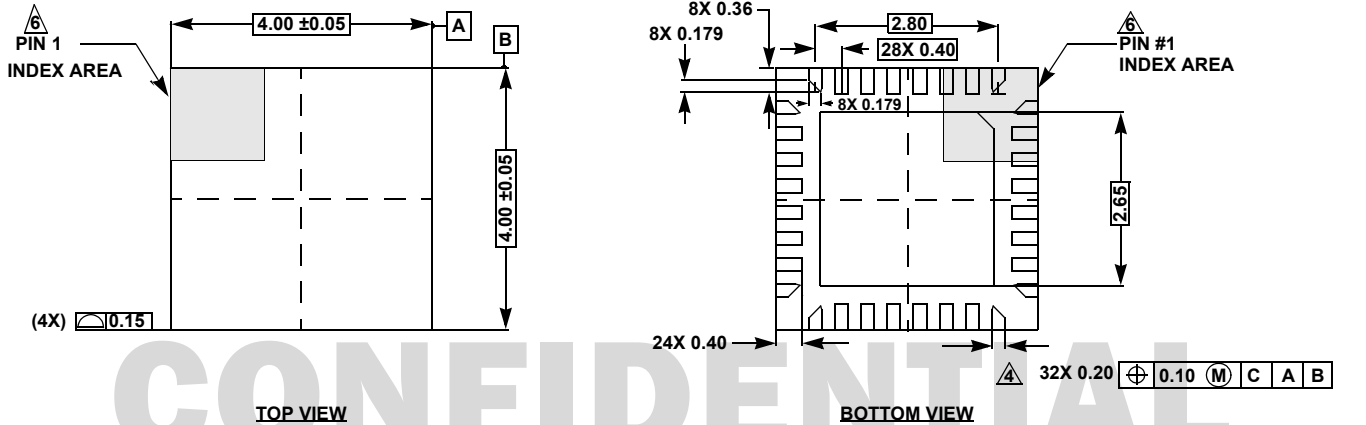
Package Outline Drawing

For the most recent package outline drawing, see [L32.4x4A](#).

L32.4x4A

32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

Rev 5, 2/16



NOTES:

1. Dimensions are in millimeters.
Dimensions in () for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.25mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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(Rev.4.0-1 November 2017)

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