ISL95520

Hybrid Power Boost (HPB) and Narrow VDC (NVDC) Configurations Combo Battery Charger With SMBus Interface

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The ISL95520 is a highly versatile combo battery charger configurable for operating as either a Hybrid Power Boost (HPB) charger or a Narrow VDC (NVDC) charger, supporting 2-, 3-, or 4-cell batteries. Both configurations allow the battery to work with the adapter together to supply the system load when it exceeds the adapter capability, referred to as system Turbo mode. The HPB charger configuration reverse-boosts battery energy to the system bus to help the adapter provide system power in Turbo mode. The NVDC charger configuration quickly turns on BGATE to enable the battery to help the adapter provide system power in Turbo mode.

The ISL95520 uses N-channel MOSFETs (NFETs) for all the switches to achieve the best performance and lowest BOM cost. The internal charge pump is capable of turning on all the NFETs fast or slow depending on the circumstance or the need. The ability to quickly turn on NFETs prevents system bus voltage drop when the battery is suddenly removed in Turbo mode or in battery learn mode.

The ISL95520 provides many protection features including a PROCHOT# indicator for system low voltage, adapter overcurrent, battery overcurrent or overheating, with an array of SMBus programmable parameters for maximum flexibility. The ISL95520 also features hardware based adapter current limit and battery-current limit in addition to SMBus programmable limits.

The ISL95520 provides high accuracy adapter current monitor, battery current monitor, and system power monitor outputs. To provide maximum flexibility for working with high power and low power systems, the ISL95520 provides several configurable current-sense resistor value options to achieve the best trade-off of current sensing accuracy vs power loss.

The ISL95520 uses the Renesas patented Robust Ripple Regulator (R3™) modulation scheme to provide excellent light-load efficiency and fast dynamic response. The ISL95520 is available in a 32 Ld 4x4mm^2 QFN package.

Features

- Configurable as an HPB charger or NVDC charger
- Compliant with Intel PROCHOT# and PSYS requirements
- Adapter current monitor and battery discharging current monitor
- Uses NFETs for all the switches
  - Supports battery removal during battery learn mode
  - Actively controlled inrush current to prevent FET damage
- SMBus programmable settings and high accuracy
- Comprehensive protection features:
  - PROCHOT# indicator for system low voltage, adapter overcurrent, battery overcurrent, and system overheating
  - Hardware-based adapter-current and battery-current limits
  - Supports sudden battery removal in system Turbo mode
- 16 switching frequency options from 350kHz to 1MHz
- Low quiescent current
- Robust Ripple Regulator (R3) modulation scheme provides excellent light-load efficiency and fast dynamic response
- 32 Ld 4x4mm^2 QFN package
- Pb-free (RoHS compliant)

Applications

- Devices with rechargeable 2-, 3- or 4-cell batteries

Related Literature

For a full list of related documents, visit our website:

- ISL95520 device page

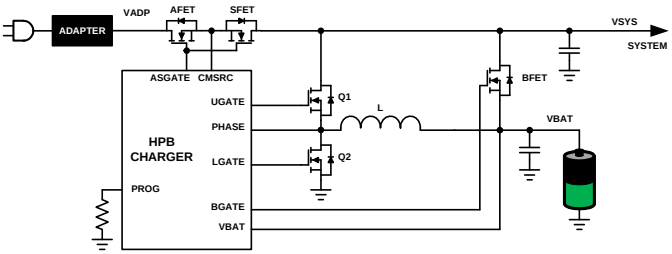

FIGURE 1. HPB CHARGER CONFIGURATION

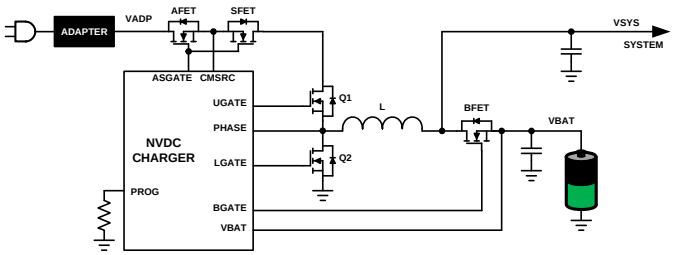

FIGURE 2. NVDC CHARGER CONFIGURATION

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Simplified Application Circuits

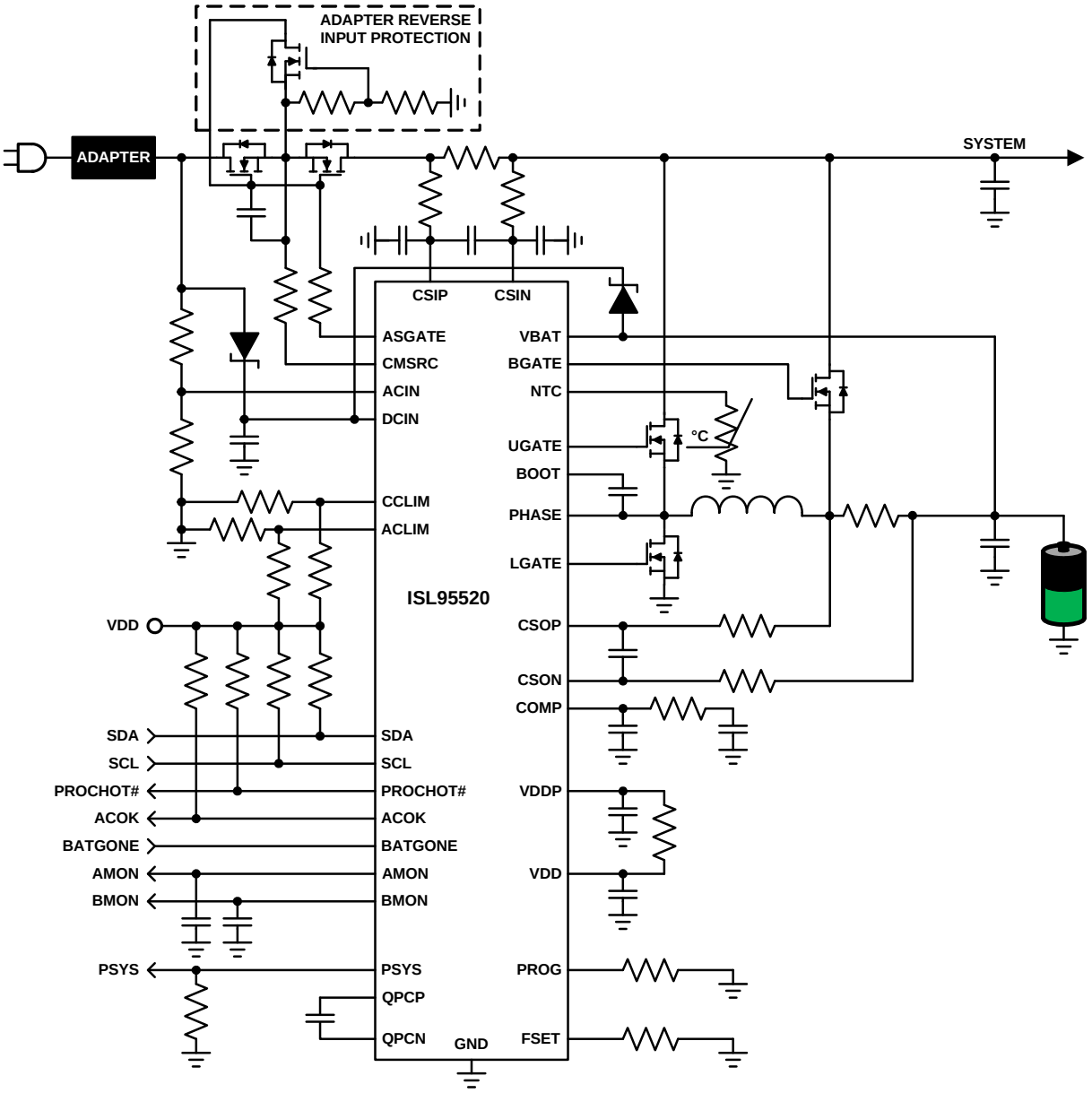


FIGURE 3. TYPICAL APPLICATION CIRCUIT: HPB CHARGER CONFIGURATION WITH TWO NMOS SELECTORS

Simplified Application Circuits (Continued)

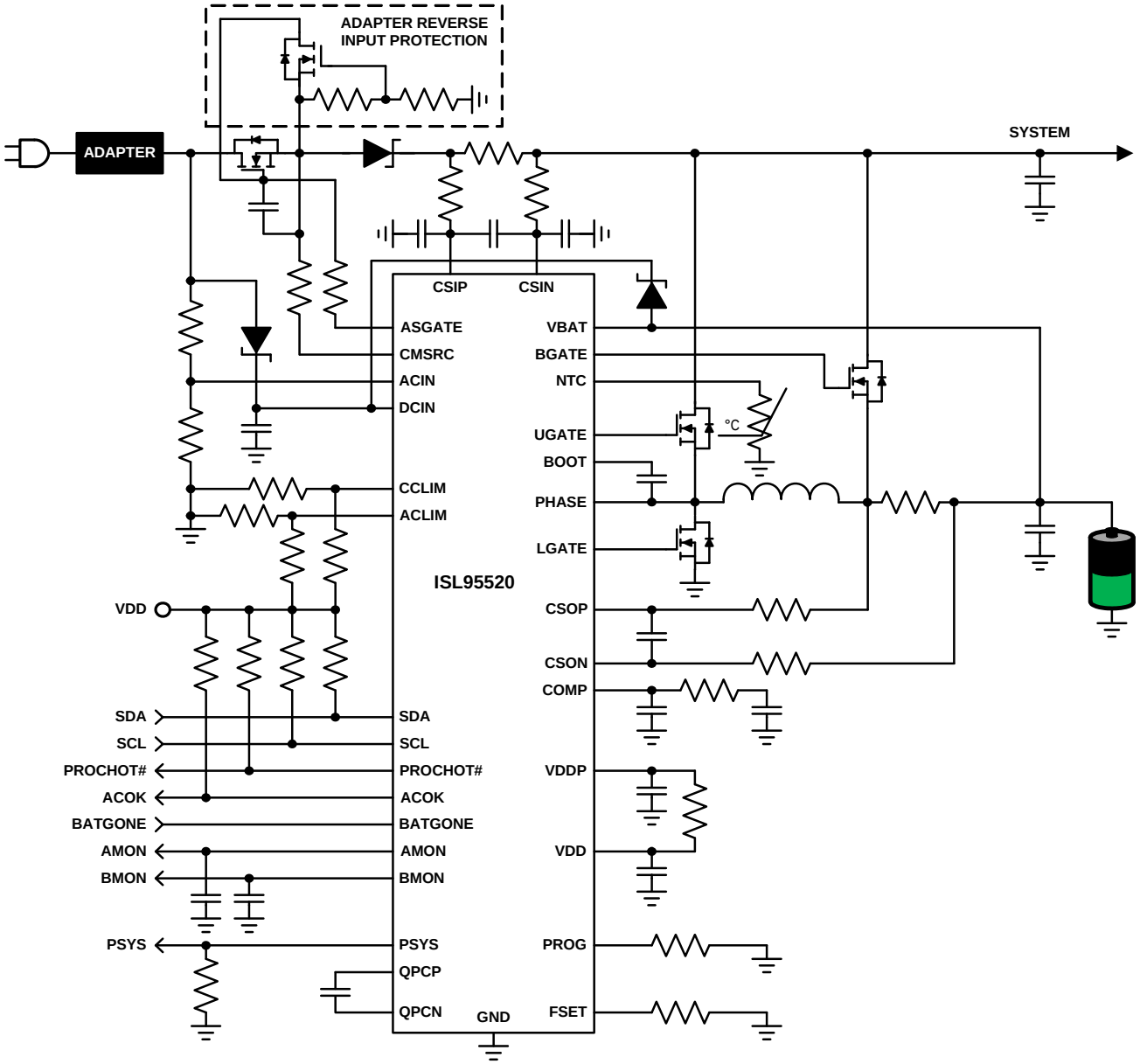


FIGURE 4. TYPICAL APPLICATION CIRCUIT: HPB CHARGER CONFIGURATION WITH ONE NMOS SELECTOR AND SCHOTTKY DIODE

Simplified Application Circuits (Continued)

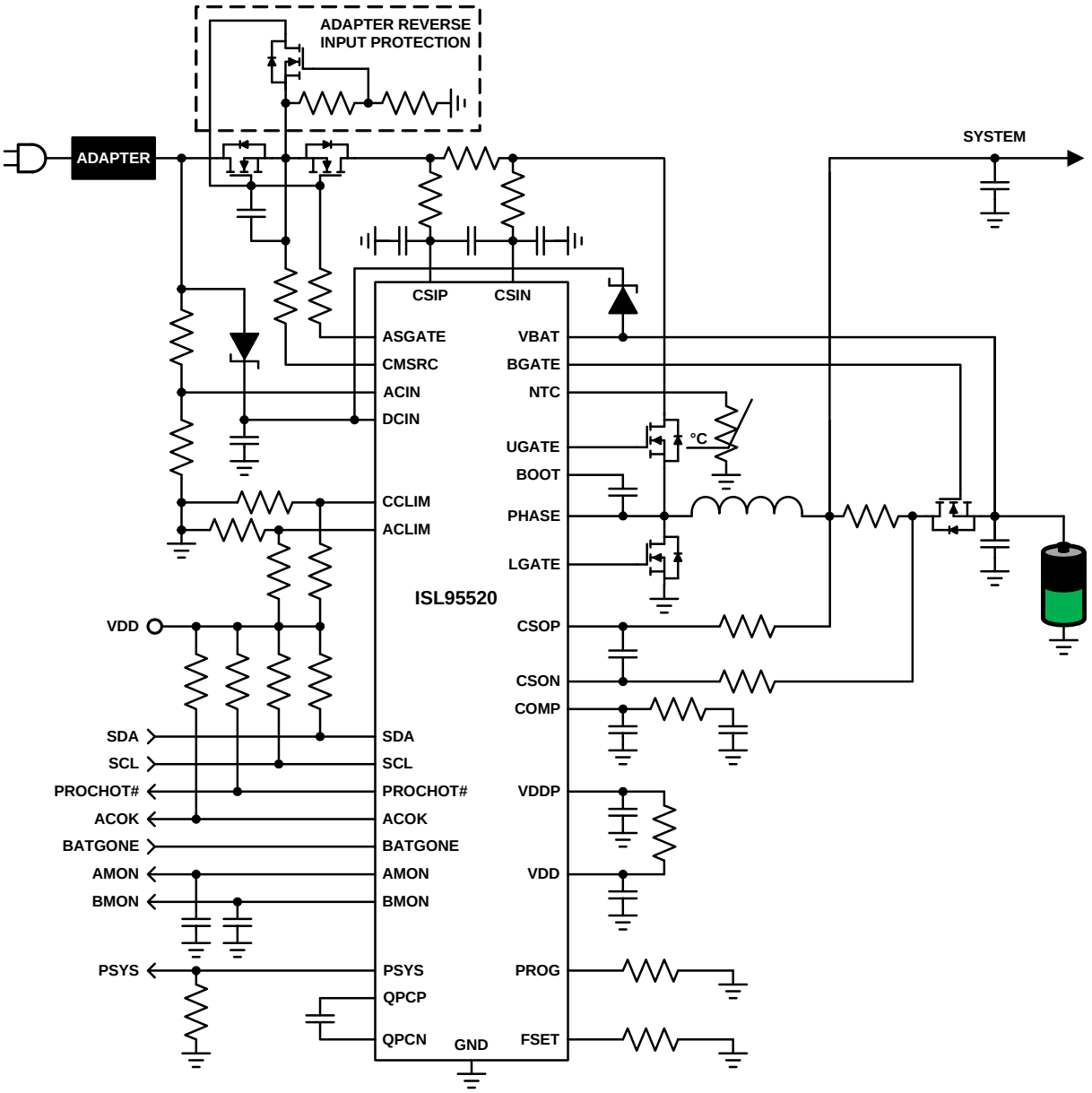


FIGURE 5. TYPICAL APPLICATION CIRCUIT: NVDC CHARGER CONFIGURATION WITH TWO NMOS SELECTORS

Simplified Application Circuits (Continued)

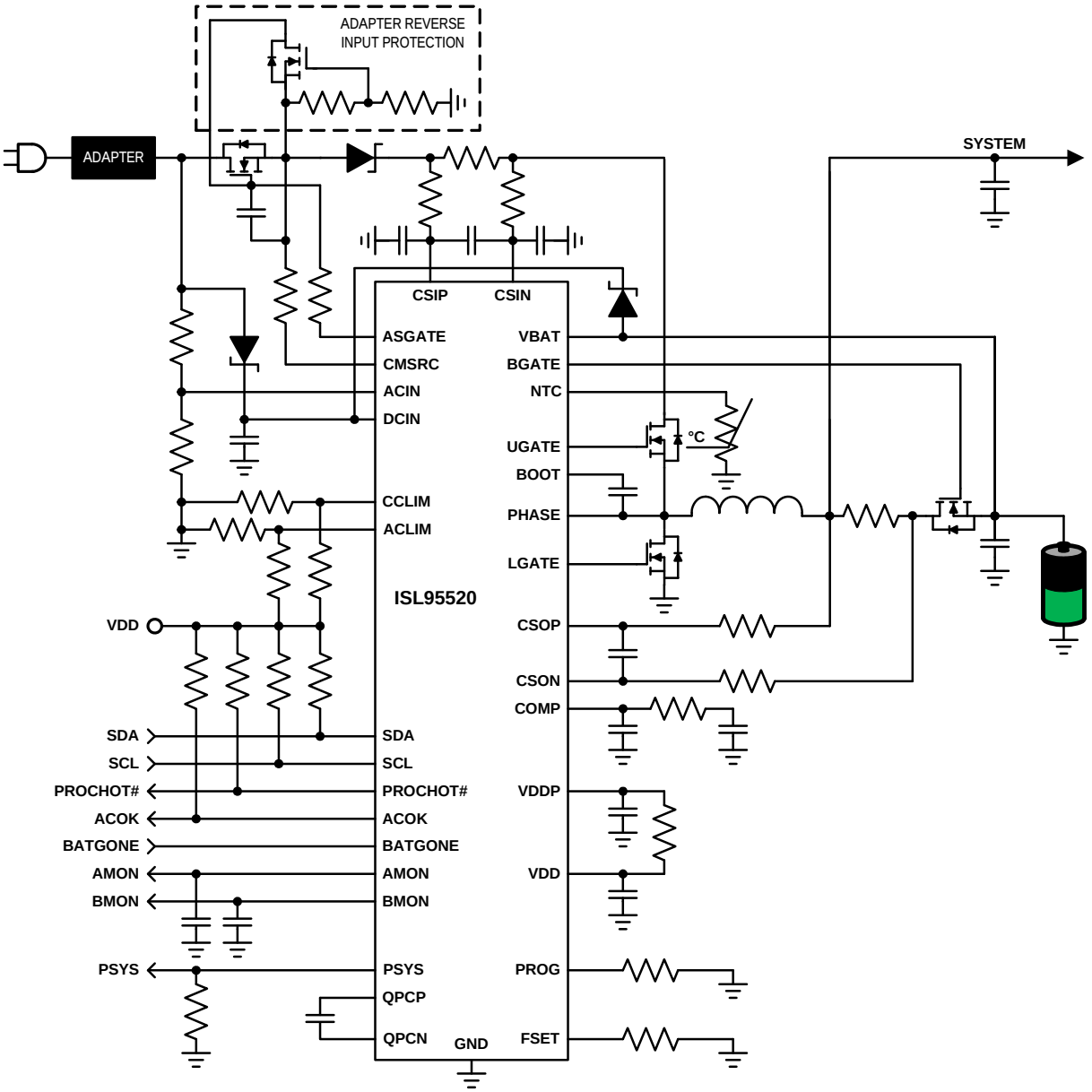


FIGURE 6. TYPICAL APPLICATION CIRCUIT: NVDC CHARGER CONFIGURATION WITH ONE NMOS SELECTOR AND SCHOTTKY DIODE

Block Diagram

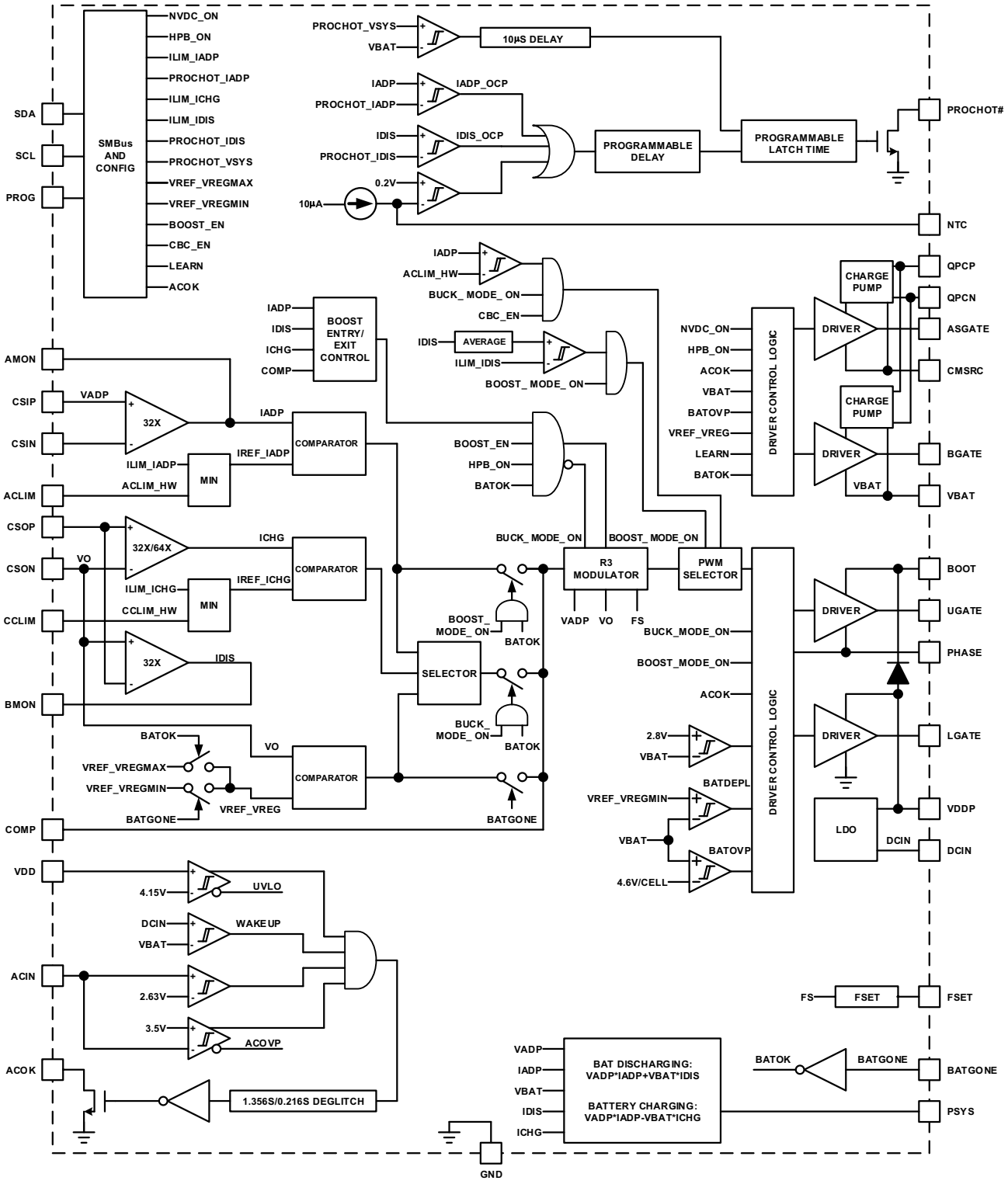


FIGURE 7. BLOCK DIAGRAM

Ordering Information

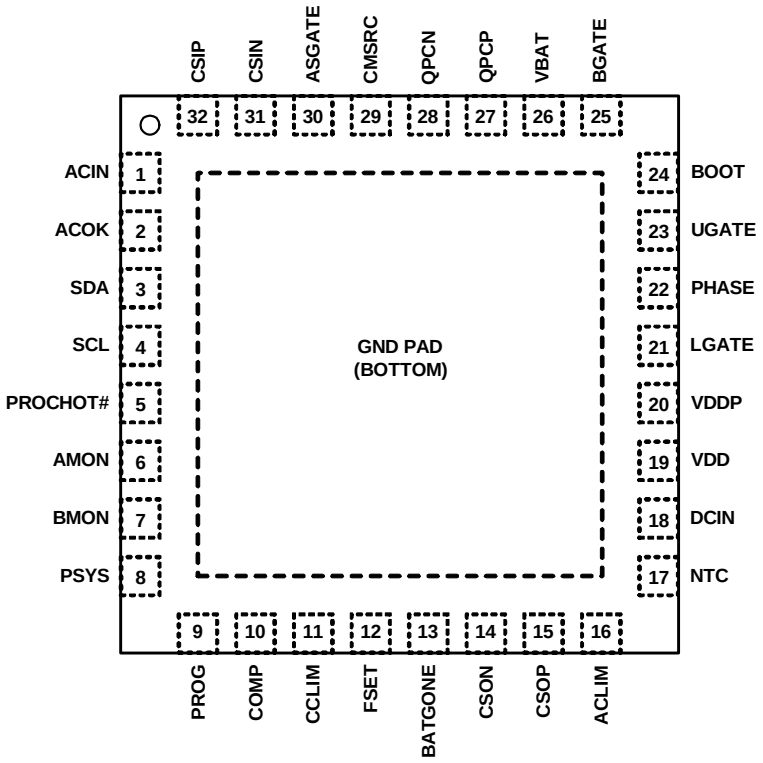
PART NUMBER (Notes 2, 3)	PART MARKING	TEMP. RANGE (°C)	TAPE AND REEL (UNITS) (Note 1)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL95520HRZ	955 20HRZ	0 to +85	-	32 Ld 4x4 QFN	L32.4x4A
ISL95520HRZ-T	955 20HRZ	0 to +85	6k	32 Ld 4x4 QFN	L32.4x4A

NOTES:

1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL95520 device page. For more information about MSL, see TB363.

Pin Configuration

32 LD 4x4 QFN
TOP VIEW



Pin Descriptions

PIN #	PIN NAME	DESCRIPTION
BOTTOM PAD	GND	Signal common to the IC. Unless otherwise stated, signals are referenced to the GND pin. Use this pad as the thermal pad for heat removal.
1	ACIN	Adapter voltage sense. The adapter voltage is valid if the ACIN pin voltage is between 2.63V and 3.5V. If the ACIN pin voltage exceeds 3.5V, the adapter voltage is in the overvoltage condition and the ISL95520 turns off the ASGATE MOSFETs to isolate the adapter from the system.
2	ACOK	Open-drain output to indicate the adapter voltage is ready. Pulled low if the adapter voltage is not ready.
3	SDA	SMBus data I/O. Connect to the data line from the host controller or smart battery. Connect a 10kΩ pull-up resistor according to the SMBus specification.
4	SCL	SMBus clock I/O. Connect to the clock line from the host controller or smart battery. Connect a 10kΩ pull-up resistor according to the SMBus specification.

Pin Descriptions (Continued)

PIN #	PIN NAME	DESCRIPTION
5	PROCHOT#	Open-drain output. Pulled low with the SMBus programmable debounce time if any of the four conditions occur: • Adapter current reaches PROCHOT_IADP. • Battery discharging current reaches PROCHOT_IDIS. • System bus voltage is below the low system voltage detection threshold (programmable through SMBus). • NTC pin voltage is below 170mV. When asserted, this pin latches on for a minimum SMBus programmable time before it can be cleared.
6	AMON	Adapter current monitor output. V_{AMON} = 32x (V_{CSIP} - V_{CSIN}). Leave this pin floating if not used.
7	BMON	Battery discharging current monitor. V_{BMON} = 32x (V_{CSON} - V_{CSOP}). Leave this pin floating if not used.
8	PSYS	System power monitor output. Connect this pin to GND if not used.
9	PROG	A resistor to GND sets the following configurations: • HPB charger or NVDC charger. • Default number of the battery cells in series. • Adapter current sense resistor and battery current sense resistor values. See Table 17 on page 36 for programming options. After POR, pulling the PROG pin to 5V enables learn mode.
10	COMP	Error amplifier output. Connect the compensation network externally from COMP to GND.
11	CCLIM	The voltage on this pin sets the hardware-based charging current limit (CCLIM). The lower value of the hardware-set CCLIM and the SMBus-set ChargeCurrent command is the actual limit of the battery charging current.
12	FSET	A resistor from this pin to GND programs the default switching frequency. See Table 20 on page 38 for programming options.
13	BATGONE	Battery presence indicator input pin to the ISL95520. Logic high indicates the battery has been removed. Logic low indicates the battery is present.
14	CSON	Battery current sense “–” input. Also used to sense NVDC charger system voltage.
15	CSOP	Battery current sense “+” input.
16	ACLIM	The voltage on this pin sets the hardware-based adapter current limit. The lower value of the hardware-set adapter current limit and the SMBus set adapter current limit is the actual limit of the adapter current. The hardware-based adapter current limit also becomes the adapter current cycle-by-cycle current limit threshold if the cycle-by-cycle current limit function is enabled through SMBus. The hardware-based adapter current limit also sets the regulated inrush current level for ASGATE MOSFET protection.
17	NTC	10µA current source output. Connect an NTC thermistor network from this pin to GND. If the NTC pin voltage is below 170mV, the ISL95520 pulls PROCHOT# low. Other than connecting an NTC thermistor network, this NTC pin comparator can be used as a general purpose comparator for the platform.
18	DCIN	Input for an internal 5V output LDO. Renesas recommends connecting a diode-OR from the adapter and battery. The DCIN pin voltage needs to be higher than the VBAT pin voltage for ASGATE to soft-start turning on. Connect a 10Ω DCIN resistor between the DCIN pin and the VADP/VSYS diodes, and connect a 4.7µF (50V) DCIN capacitor to GND. The capacitor must have an effective capacitance higher than 0.4µF at 20V.
19	VDD	5V power supply input for the ISL95520 control circuitry. Connect a 2.2µF (10V) MLCC capacitor to GND. The capacitor must have an effective capacitance higher than 0.4µF at 5V and x1.6 effective capacitance at the BOOT pin at 5V.
20	VDDP	Output of the internal 5V-output LDO. The ISL95520 uses this pin as the FET driver power supply. Connect a 2.2µF (10V) MLCC capacitor to GND. The capacitor must have an effective capacitance higher than 0.4µF at 5V and x1.6 effective capacitance at the BOOT pin at 5V.
21	LGATE	Output of the low-side switching FET gate drive. Connect this pin to the gate of the low-side switch FET.
22	PHASE	Current return path for the high-side switching FET gate drive. Connect this pin to the node consisting of the high-side switch FET source, the low-side switch FET drain, and the output inductor.
23	UGATE	Output of the high-side switch FET gate drive. Connect this pin to the gate of the high-side switching FET.
24	BOOT	Connect an MLCC capacitor across the BOOT pin and PHASE pin. The boot capacitor is charged through an internal bootstrap switch connected from the VDDP pin to the BOOT pin, when the PHASE pin drops below VDDP minus the voltage drop across the internal bootstrap switch. Connect a 0.47µF (25V) bootstrap capacitor, which must have an effective capacitance higher than 0.25µF at 5V and x50 effective high-side MOSFET gate capacitance.

Pin Descriptions (Continued)

PIN #	PIN NAME	DESCRIPTION
25	BGATE	Output of the gate drive for the NFET connecting the system voltage and the battery. The behavior of the BGATE depends on whether the ISL95520 is in the HPB charger configuration or the NVDC charger configuration.
26	VBAT	Current return path for the BGATE gate drive. Also used to sense battery voltage. Renesas recommends connecting an R-C filter at the VBAT pin.
27	QPCP	Internal charge pump “+” input. Connect an MLCC capacitor across the QPCP pin and QPCN pin.
28	QPCN	Internal charge pump “-” input. Connect an MLCC capacitor across the QPCP pin and QPCN pin.
29	CMSRC	Common source node of the two back-to-back ASGATE NFETs.
30	ASGATE	Output of the gate drive for the two back-to-back NFETs.
31	CSIN	Adapter current sense “-” input.
32	CSIP	Adapter current sense “+” input. Also used to sense input voltage.

Absolute Maximum Ratings

CSIP, CSIN, DCIN, CMSRC, QPCN . . . . . -0.3V to +28V
VBAT, CSOP, CSON . . . . . -0.3V to +28V
ASGATE, BGATE, QPCP . . . . . -0.3V to +33V
VDD, VDDP. . . . . -0.3V to +7V
CSIP-CSIN, CSOP-CSON . . . . . -0.3V to +0.3V
QPCP-QPCN . . . . . -0.3V to +7V
UGATE-PHASE . . . . . -0.3V to +7V
BOOT Voltage (BOOT) . . . . . -0.3V to +33V
BOOT to PHASE Voltage (BOOT-PHASE). . . . . -0.3V to +7V(DC)
. . . . . -0.3V to +9V(<10ns)
PHASE Voltage (PHASE) . . . . . -0.3V to 28V
. . . . . -7V (<20ns Pulse Width, 10µJ)
UGATE Voltage (UGATE) . . . . . PHASE-0.3V(DC) to BOOT
. . . . . PHASE-5V (<20ns Pulse Width, 10µJ) to BOOT
LGATE Voltage. . . . . -2.5V (<20ns Pulse Width, 5µJ) to VDDP+0.3V
Open Drain Outputs, ACOK, PROCHOT# . . . . . -0.3V to +7V
All Other Pins . . . . . -0.3V to (VDD +0.3V)

ESD Rating
Human Body Model (Tested per JESD22-A114E) 3kV
Machine Model (Tested per JESD22-A115-A) 200V
Charged Device Model (Tested per JESD22-C101A) 750V
Latch-Up (Tested per JESD-78B) . . . . . Class 2, Level A

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
32 Ld QFN Package (Notes 4, 5)	39	3

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Storage Temperature Range. . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Ambient Temperature HRZ . . . . . 0°C to +85°C
Junction Temperature HRZ . . . . . 0°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Operating Conditions: V_{DD} = 5V, T_A = 0°C to +85°C unless otherwise noted. **Boldface limits apply across the operating temperature range, 0°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
QUIESCENT CURRENT AND POR						
Battery Current	$I_{BAT\_BGATE\_OFF\_NVDC}$	Adapter present, BGATE off, V_{BAT} = 16.8V, DCIN current does not come from battery, I_BAT = I_VBAT		40	60	µA
	$I_{BAT\_BGATE\_ON\_NVDC}$	Battery only, BGATE on, V_{BAT} = 16.8V, DCIN current comes from battery, I_BAT = I_PHASE+ I_VBAT+ I_CSOP+ I_CSON+ I_DCIN I+ I_CMSRC		130	190	µA
	$I_{BAT\_BGATE\_OFF\_HPB}$	Adapter present, BGATE off, V_{BAT} = 16.8V, DCIN current does not come from battery, I_BAT = I_PHASE+ I_VBAT+ I_CSOP+ I_CSON+ I_CMSRC		115	160	µA
	$I_{BAT\_BGATE\_ON\_HPB}$	Battery only, BGATE on, V_{BAT} = 16.8V, DCIN current comes from battery, I_BAT = I_PHASE+ I_VBAT+ I_CSOP+ I_CSON+I_DCIN+I_CSIP+I_CSIN+ I_CMSRC		245	345	µA
Quiescent Current	$I_{DCIN\_STANDBY\_HPB}$	VADP = 19.2V, AMON, BMON, PSYS all OFF		160	220	µA
	$I_{DCIN\_NOSW\_1\_HPB}$	VADP = 19.2V, no switching, AMON, BMON, PSYS all OFF		785	900	µA
	$I_{DCIN\_NOSW\_2\_HPB}$	VADP = 19.2V, no switching, AMON, BMON, PSYS all ON		1070	1250	µA
	$I_{DCIN\_SW\_H\_HPB}$	VADP = 19.2V, Charge enabled, AMON, BMON, PSYS all OFF		1.52	1.82	mA
	$I_{DCIN\_SW\_N\_NVDC}$	VADP = 19.2V, Charge enabled, AMON, BMON, PSYS all OFF		1.45	1.75	mA
VDD Power-on Reset (POR)	POR_{VDD_R}	VDD rising		4.66	**4.75**	V
	POR_{VDD_F}	VDD falling	**4.35**	4.44		mV

Electrical Specifications Operating Conditions: V_{DD} = 5V, T_A = 0°C to +85°C unless otherwise noted. **Boldface limits apply across the operating temperature range, 0°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
CHARGING VOLTAGE LIMIT						
Maximum Charging Voltage Accuracy	V_{CHG_MAX}	MaxChargeVoltage = 0x41A0H (16.8V)		16.79		V
			-0.75		**0.75**	%
		MaxChargeVoltage = 0x3140H (12.608V)		12.6		V
			-0.75		**0.75**	%
		MaxChargeVoltage = 0x20D0H (8.4V)		8.4		V
			-0.5		**0.5**	%
Minimum Charging Voltage Accuracy (NVDC 450mV + MinChargeVoltage register setting)	V_{CHG_MIN}	MinChargeVoltage = 0x2A00H (10.752V)	**11.02**	11.2	**11.4**	V
		MinChargeVoltage = 0x2000H (8.192V)	8.48	8.64	8.84	V
		MinChargeVoltage = 0x1500H (5.376V)	5.68	5.825	6	V
BATTERY CURRENT LIMIT						
Battery Current Sense Amplifier Input Differential Voltage Range	V_{IBAT_RGE5}	Rs_2 = 5mΩ, charging current (V_{CSOP} - V_{CSON})	**0**		**40.5**	mV
	V_{IBAT_RGE10}	Rs_2 = 10mΩ or Rs_2 = 20mΩ, charging current (V_{CSOP} - V_{CSON})	**0**		**81**	mV
	V_{IBAT_RGED}	Discharging current (V_{CSOP} - V_{CSON})	**-81**		**0**	mV
Charging Current Limit Rs_2 = 10mΩ V_{BAT} > 4.5V	I_{CHG_ACC10}	ChargeCurrentLimit = 0x1F20H (7968mA)		8030		mA
			-2	0.8	**3.5**	%
		ChargeCurrentLimit = 0x0FA0H (4000mA)		4040		mA
			-2.2	1	**4**	%
		ChargeCurrentLimit = 0x07E0H (2016mA)		2050		mA
			-3	1.7	**6**	%
		ChargeCurrentLimit = 0x03E0H (992mA)		1020		mA
			-3.7	2.8	**9.2**	%
		ChargeCurrentLimit = 0x0200H (512mA)		536		mA
			-5.8	4.7	**15.2**	%
		ChargeCurrentLimit = 0x0100H (256mA) (not trickle charging mode current)		270		mA
			-17	5.5	**27**	%
Charging Current Limit Rs_2 = 5mΩ V_{BAT} > 4.5V	I_{CHG_ACC5}	ChargeCurrentLimit = 0x1F20H (7968mA)		8040		mA
			-2.3	0.9	**3.9**	%
		ChargeCurrentLimit = 0x0FA0H (4000mA)		4045		mA
			-2.9	1.1	**4.6**	%
		ChargeCurrentLimit = 0x07E0H (2016mA)		2050		mA
			-4.3	1.7	**7**	%
		ChargeCurrentLimit = 0x03E0H (992mA)		1020		mA
			-7.4	2.8	**12**	%
		ChargeCurrentLimit = 0x0200H (512mA)		536		mA
			-13.9	4.7	**20.4**	%
		ChargeCurrentLimit = 0x0100H (256mA) (Not trickle charging mode current)		265		mA
			-34	3.5	**35**	%
Trickle Charging Current Limit	$I_{TRKL\_ACC10\_256}$	Rs_2 = 10mΩ, V_{BAT} < MinChargeVoltage	**223**	275	**327**	mA
	$I_{TRKL\_ACC10\_128}$	Rs_2 = 10mΩ, V_{BAT} < MinChargeVoltage	**95**	145	**198**	mA
	$I_{TRKL\_ACC5\_256}$	Rs_2 = 5mΩ, V_{BAT} < MinChargeVoltage	**180**	270	**357**	mA
	$I_{TRKL\_ACC5\_128}$	Rs_2 = 5mΩ, V_{BAT} < MinChargeVoltage	**52**	140	**228**	mA

Electrical Specifications Operating Conditions: V_{DD} = 5V, T_A = 0°C to +85°C unless otherwise noted. **Boldface limits apply across the operating temperature range, 0°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_{BAT} Trickle Charging Threshold	$V_{TRKL\_TH\_R}$	MinChargeVoltage = 4.096V, exit trickle charging mode		4.39	**4.57**	V
	$V_{TRKL\_TH\_F}$	MinChargeVoltage = 4.096V, enter trickle charging mode	**3.85**	4.03		V
Discharging Current PROCHOT# Threshold Rs_2 = 5mΩ	$I_{DIS\_HOT\_TH5}$	DCProchot = 0x2A00H (10752mA)		10848		mA
			-3.5	0.9	**5.3**	%
		DCProchot = 0x1500H (5376mA)		5450		mA
			-6.4	1.4	**9.2**	%
ADAPTER CURRENT LIMIT						
Adapter Current Sense Amplifier Input Differential Voltage Range	V_{IADP_RGE}	Rs_1 = 10mΩ or Rs_1 = 20mΩ, adapter current (V_{CSIP} - V_{CSIN})	**0**		**81**	mV
Adapter Current Limit Rs_1 = 10mΩ	I_{ADP_10}	AdapterCurrentLimit = 0x1F20H (8064mA)		8115		mA
			-1.2	0.6	**2.5**	%
		AdapterCurrentLimit = 0x1000H (4096mA)		4140		mA
			-1.3	1.1	**3.5**	%
		AdapterCurrentLimit = 0x0800H (2048mA)		2075		mA
			-2.5	1.3	**5.2**	%
		AdapterCurrentLimit = 0x0400H (1024mA)		1055		mA
			-4	3	**10**	%
		AdapterCurrentLimit = 0x0200H (512mA)		545		mA
			-6	6.5	**19**	%
		AdapterCurrentLimit = 0x0100H (256mA)		290		mA
			-12	13.3	**40**	%
Adapter Current PROCHOT# Threshold Rs_1 = 10mΩ	$I_{ADP\_HOT\_TH10}$	ACProchot = 0x1500H (5376mA)		5389		mA
			-3.5	0.25	**4**	%
		ACProchot = 0x0A80H (2688mA)		2728		mA
			-7	1.5	**10**	%
MONITOR						
AMON Accuracy V_{AMON} = 32x(V_{CSIP}-V_{CSIN}) Rs_1 = 10mΩ	V_{AMON}	V_{CSIP}-V_{CSIN} = 80mV		2544		mV
			-2.5	-0.6	**1.3**	%
		V_{CSIP}-V_{CSIN} = 40mV		1269		mV
			-3.5	-0.85	**1.8**	%
		V_{CSIP}-V_{CSIN} = 20mV		632		mV
			-6	-1.25	**3.5**	%
		V_{CSIP}-V_{CSIN} = 10mV		313		mV
			-10	-2.2	**6.6**	%
		V_{CSIP}-V_{CSIN} = 5mV		154		mV
			-19.5	-3.75	**12.5**	%
AMON Current Sourcing Capability	$I_{AMON\_MAX\_SR}$		**255**	515	**800**	µA
AMON Current Sinking Capability	$I_{AMON\_MAX\_SK}$		**12**	22	**32**	µA

Electrical Specifications Operating Conditions: V_{DD} = 5V, T_A = 0°C to +85°C unless otherwise noted. **Boldface limits apply across the operating temperature range, 0°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
BMON Accuracy V_{BMON} = 32 x (V_{CSON}-V_{CSOP}) Rs_2 = 10mΩ	V_{BMON}	V_{CSON} - V_{CSOP} = 80mV		2.603		mV
			-2	1.65	**5.4**	%
		V_{CSON} - V_{CSOP} = 40mV		1300		mV
			-3	1.55	**6**	%
		V_{CSON} - V_{CSOP} = 20mV		649		mV
			-5	1.4	**8**	%
		V_{CSON} - V_{CSOP} = 10mV		327		mV
			-7	2.2	**12**	%
BMON Current Sourcing Capability	$I_{BMON\_MAX\_SR}$		**120**	285	**460**	µA
BMON Current Sinking Capability	$I_{BMON\_MAX\_SK}$		**5.5**	11.4	**17.5**	µA
PSYS Output Current Rs_1 = 10mΩ Rs_2 = 10mΩ PSYS Current Gain = 1.14µA/W	I_{PSYS}	V_{CSIP} = 19V, V_{CSIP} - V_{CSIN} = 80mV, V_{BAT} = 12V, V_{CSOP} - V_{CSON} = 0mV		174		µA
			-8.3	0.4	**9.1**	%
		V_{CSIP} = 19V, V_{CSIP} - V_{CSIN} = 80mV, V_{BAT} = 12V, V_{CSOP} - V_{CSON} = 20mV		146.5		µA
			-8.2	0.4	**9**	%
		V_{CSIP} = 19V, V_{CSIP} - V_{CSIN} = 80mV, V_{BAT} = 12V, V_{CSOP} - V_{CSON} = -20mV		199.5		µA
			-8.4	-0.6	**7.2**	%
		V_{CSIP} = 0V, V_{CSIP}-V_{CSIN} = 0mV, V_{BAT} = 12V, V_{CSOP}-V_{CSON} = -20mV		26.2		µA
			-15.2	-4.2	**6.8**	%
Maximum PSYS Output Voltage	V_{PSYS_MAX}	I_{PSYS} = 200µA		1.5		V
NTC Source Current	I_{NTC}	NTC = 1V	**9.71**	10.08	**10.44**	µA
NTC_PROCHOT# Trip Threshold	V_{NTC_TH}	V_{NTC} falling	**161**	171	**182**	mV
NTC_PROCHOT# Hysteresis	V_{NTC_HYS}		**18**	27	**36**	mV
ACIN/ACOK Comparator						
ACIN Threshold Rising	$V_{ACIN\_TH\_R}$	V_{ACIN} rising		2.63	**2.75**	V
ACIN Threshold Falling	$V_{ACIN\_TH\_F}$	V_{ACIN} falling	**2.5**	2.58		V
ACIN OVP Rising	$V_{ACIN\_OVP\_TH\_R}$	V_{ACIN} rising		3.51	**3.7**	V
ACIN OVP Rising	$V_{ACIN\_OVP\_TH\_F}$	V_{ACIN} falling	**3.35**	3.45		V
ACIN Input Leakage Current	I_{ACIN_LEAK}		**-1**		**1**	µA
ACOK Input Leakage Current	I_{ACOK_LEAK}		**-1**		**1**	µA
ACOK Output Low Current	I_{ACOK}	V_{ACOK} = 0.3V		240		µA
ACLIM, CCLIM						
ACLIM Current Limit		V_{ACLIM} = 2.56V, Rs_1 = 10mΩ	**7970**	8075	**8175**	mA
		V_{ACLIM} = 1.92V, Rs_1 = 10mΩ	**5970**	6060	**6150**	mA
		V_{ACLIM} = 1.28V, Rs_1 = 10mΩ	**3975**	4050	**4125**	mA
CCLIM Current Limit		V_{CCLIM} = 2.56V, Rs_1 = 10mΩ, Rs_2 = 5mΩ	**7855**	8070	**8265**	mA
		V_{CCLIM} = 1.92V, Rs_1 = 10mΩ, Rs_2 = 5mΩ	**5875**	6050	**6205**	mA
		V_{CCLIM} = 1.28V, Rs_1 = 10mΩ, Rs_2 = 5mΩ	**3900**	4035	**4155**	mA
		V_{CCLIM} = 2.56V, Rs_1 = 10mΩ, Rs_2 = 10mΩ	**7860**	8065	**8250**	mA
		V_{CCLIM} = 1.92V, Rs_1 = 10mΩ, Rs_2 = 10mΩ	**5895**	6045	**6185**	mA
		V_{CCLIM} = 1.28V, Rs_1 = 10mΩ, Rs_2 = 10mΩ	**3930**	4035	**4135**	mA
		V_{CCLIM} = 2.56V, Rs_1 = 20mΩ, Rs_2 = 20mΩ	**3930**	4030	**4130**	mA
		V_{CCLIM} = 1.92V, Rs_1 = 20mΩ, Rs_2 = 20mΩ	**2945**	3025	**3100**	mA
		V_{CCLIM} = 1.28V, Rs_1 = 20mΩ, Rs_2 = 20mΩ	**1960**	2015	**2075**	mA

Electrical Specifications Operating Conditions: V_{DD} = 5V, T_A = 0°C to +85°C unless otherwise noted. **Boldface limits apply across the operating temperature range, 0°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
PROCHOT#						
PROCHOT# Leakage Current	$I_{PROCHOT\#\_LEAK}$		**-1**		**1**	µA
PROCHOT# Output Low Current	$I_{PROCHOT\#}$	$V_{PROCHOT\#}$ = 0.3V		33		mA
Low VSYS PROCHOT# Trip Threshold	$V_{LOW\_VSYS\_HOT}$	Control1 register bit<9:8> = 00	**5.48**	5.62	**5.76**	V
		Control1 register bit<9:8> = 01	**5.97**	6.11	**6.25**	V
		Control1 register bit<9:8> = 10	**6.44**	6.59	**6.73**	V
		Control1 register bit<9:8> = 11	**6.9**	7.05	**7.2**	V
PROCHOT# Debounce Time		Prochot# Debounce register bit<1:0> = 01		102		µs
		Prochot# Debounce register bit<1:0> = 10		510		µs
PROCHOT# Duration Time		Prochot# Duration register bit<2:0> = 010		15.3		ms
		Prochot# Duration register bit<2:0> = 101		1.02		ms
BATGONE THRESHOLD						
BATGONE Threshold Rising	$V_{BATGONE\_TH\_R}$	$V_{BATGONE}$ rising (battery removal)		2.58	**2.75**	V
BATGONE Threshold Falling	$V_{BATGONE\_TH\_F}$	$V_{BATGONE}$ falling (battery insertion)	**1.8**	2.12		V
LDO						
Output Voltage		V_{DCIN} = 6V to 25V, I_VDDP = 1mA	**4.8**	5.24	**5.75**	V
		V_{DCIN} = 6V, I_VDDP = 30mA	**4.65**	5.12	**5.65**	V
		V_{DCIN} = 25V, I_VDDP = 30mA	**4.75**	5.22	**5.7**	V
GATE DRIVER						
UGATE Pull-up Resistance (Note 7)	R_{UGPU}	200mA source current		1.0	**1.5**	Ω
UGATE Source Current (Note 7)	I_{UGSRC}	UGATE - PHASE = 2.5V		2.0		A
UGATE Sink Resistance (Note 7)	R_{UGPD}	250mA sink current		1.0	**1.5**	Ω
UGATE Sink Current (Note 7)	I_{UGSNK}	UGATE - PHASE = 2.5V		2.0		A
LGATE Pull-up Resistance (Note 7)	R_{LGPU}	250mA source current		1.0	**1.5**	Ω
LGATE Source Current (Note 7)	I_{LGSRC}	LGATE - GND = 2.5V		2.0		A
LGATE Sink Resistance (Note 7)	R_{LGPD}	250mA sink current		0.5	**0.9**	Ω
LGATE Sink Current (Note 7)	I_{LGSNK}	LGATE - GND = 2.5V		4.0		A
UGATE to LGATE Deadtime	t_{UGFLGR}	UGATE falling to LGATE rising, no load		17		ns
LGATE to UGATE Deadtime	t_{LGFUGR}	LGATE falling to UGATE rising, no load		29		ns
ASGATE Pull-up Resistance	R_{ASGPU}	1mA source current		500		Ω
ASGATE Sink Resistance	R_{ASGPD}	1mA sink current		1300		Ω
BGATE Pull-up Resistance	R_{BGPU}	1mA source current		500		Ω
BGATE Sink Resistance	R_{BGPD}	1mA sink current		1300		Ω
BOOTSTRAP SWITCH						
ON-resistance	R_F			20		Ω
Reverse Leakage	I_R	V_R = 25V		0.2		µA
AMPLIFIERS						
Adapter Current Sense Amplifier Input Offset (Note 7)	V_{ACSNS_OFFSET}			0.4		mV
Battery Charging Current Sense Amplifier Input Offset (Note 7)	$V_{ICHGSNS\_OFFSET}$			0.4		mV
Battery Discharging Current Sense Amplifier Input Offset (Note 7)	$V_{IDISSNS\_OFFSET}$			0.4		mV
Error Amplifier DC Gain (Note 7)	A_{VO_EA}			80		dB

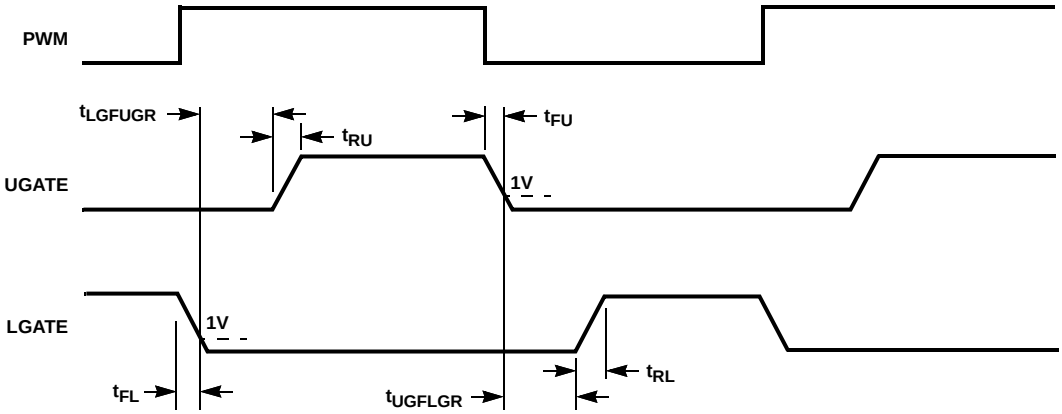
Electrical Specifications Operating Conditions: V_{DD} = 5V, T_A = 0°C to +85°C unless otherwise noted. **Boldface limits apply across the operating temperature range, 0°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
Error Amp Gain-Bandwidth Product (Note 7)	GBW_EA	C_L = 20pF		5		MHz
COMP Lower Clamp	$V_{COMP\_L\_CLP}$			1.24	**1.4**	V
COMP Upper Clamp	$V_{COMP\_U\_CLP}$		**4.9**	4.99		V
Over-Temperature Protection						
Over-Temperature Threshold (Note 7)	T_{OTP_R}	Temperature rising		155		°C
	T_{OTP_F}	Temperature falling		128		°C
SMBUS						
SDA/SCL Input Low Voltage					**0.8**	V
SDA/SCL Input High Voltage			**2**			V
SDA/SCL Input Bias Current		SDA, SCL = 0V, 5V	**-1**		**1**	µA
SDA, Output Sink Current (Note 8)		SDA = 0.4V, on		19		mA
SMBus Frequency	f_{SMB}	Note 8	**10**		**400**	kHz
Bus Free Time	t_{BUF}	100kHz, Note 8	**4.7**			µs
		400kHz, Note 8	**1.3**			µs
Start Condition Hold Time from SCL	t_{HD_STA}	100kHz, Note 8	**4**			µs
		400kHz, Note 8	**0.6**			µs
Start Condition Set-up Time from SCL	t_{SU_STA}	100kHz, Note 8	**4.7**			µs
		400kHz, Note 8	**0.6**			µs
Stop Condition Set-up Time from SCL	t_{HD_STO}	100kHz, Note 8	**4**			µs
		400kHz, Note 8	**0.6**			µs
SDA Hold Time from SCL	t_{HD_DAT}	100kHz, Note 8	**300**			ns
		400kHz, Note 8	**300**			ns
SDA Set-up Time from SCL	t_{SU_DAT}	100kHz, Note 8	**250**			ns
		400kHz, Note 8	**100**			ns
SCL Low Period	t_{LOW}	100kHz, Note 8	**4.7**			µs
		400kHz, Note 8	**1.3**			µs
SCL High Period	t_{HIGH}	100kHz, Note 8	**4**			µs
		400kHz, Note 8	**0.6**			µs
SDA/SCL Rise Time	t_{RISE}	100kHz, 400pF, maximum load, Note 8			**1000**	ns
		400kHz, 400pF, maximum load, Note 8			**300**	ns
SDA/SCL Fall Time	t_{FALL}	100kHz, 400pF, maximum load, Note 8			**300**	ns
		400kHz, 400pF, maximum load, Note 8			**300**	ns
SMBus Inactivity Time-out (Note 8)		Maximum period without a SMBus write to MaxChargeVoltage or ChargeCurrent register		175		s

NOTES:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
7. Limits established by characterization and are not production tested.
8. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

Gate Driver Timing Diagram



Typical Performance

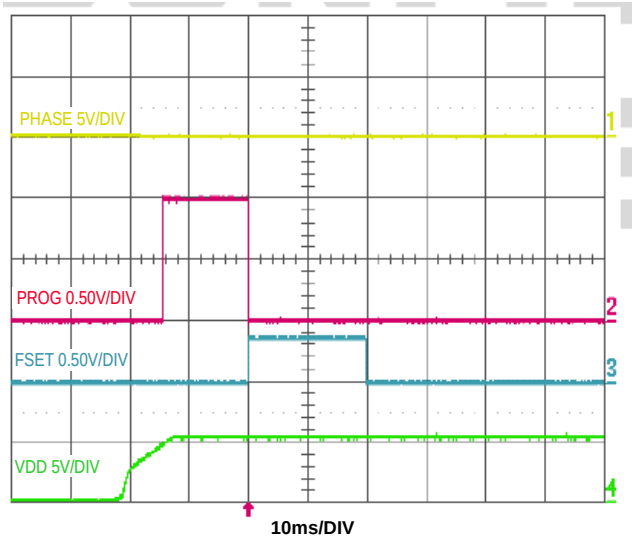


FIGURE 8. POWER-UP, READ PROG, AND FSET RESISTORS

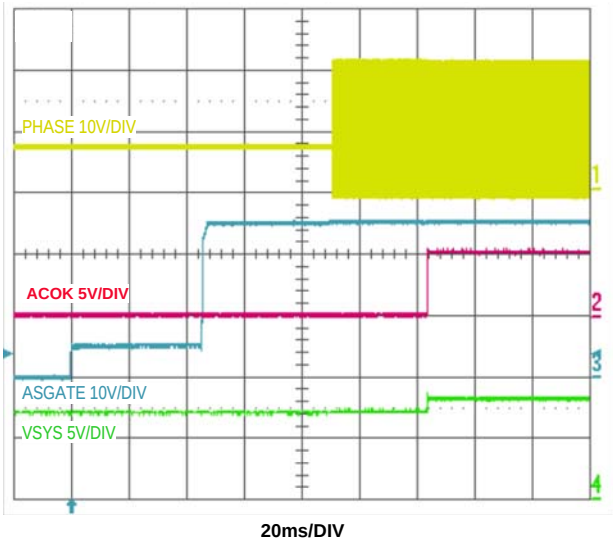


FIGURE 9. NVDC: ADAPTER INSERTION START-UP SEQUENCE

Typical Performance (Continued)

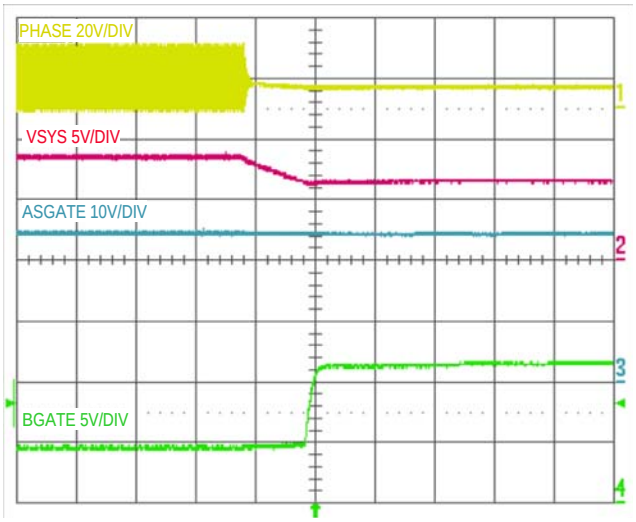


FIGURE 10. NVDC: ENTER LEARN MODE

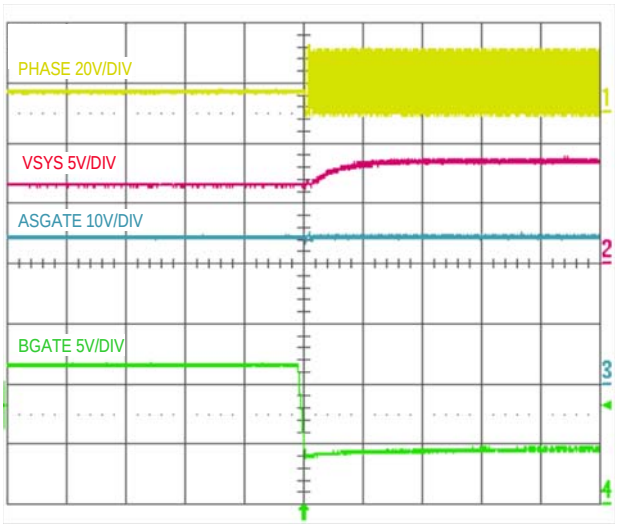


FIGURE 11. NVDC: EXIT LEARN MODE

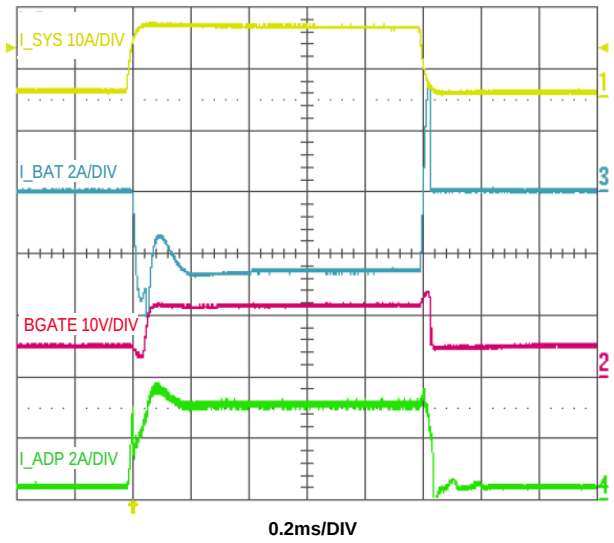


FIGURE 12. NVDC: SYSTEM VOLTAGE REGULATION LOOP AND TURBO MODE TRANSIENT. VADP = 20V, ADAPTERCURRENTLIMIT1 = 3.072A, V_{BAT} = 7V, MAXCHARGEVOLTAGE = 8.192V, 1A to 12A SYSTEM LOAD STEP

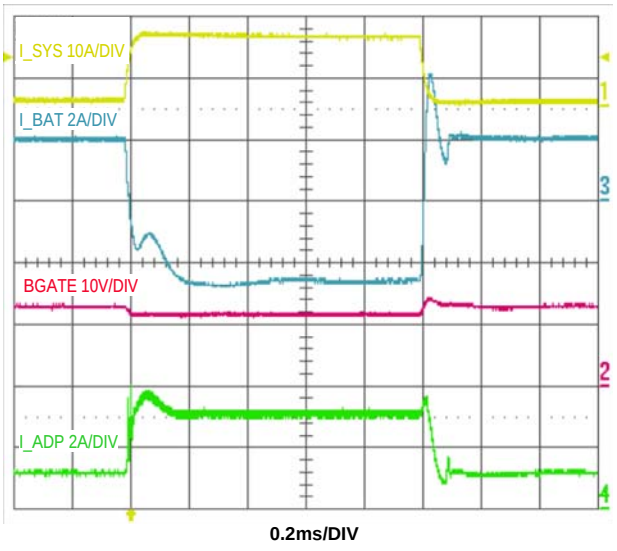


FIGURE 13. NVDC: CHARGING CURRENT LIMIT LOOP AND TURBO MODE TRANSITION. VADP = 20V, ADAPTERCURRENTLIMIT1 = 3.072A, V_{BAT} = 7V, MAXCHARGEVOLTAGE = 8.192V, CHARGECURRENT = 2.016A, 1A-12A SYSTEM LOAD STEP

Typical Performance (Continued)

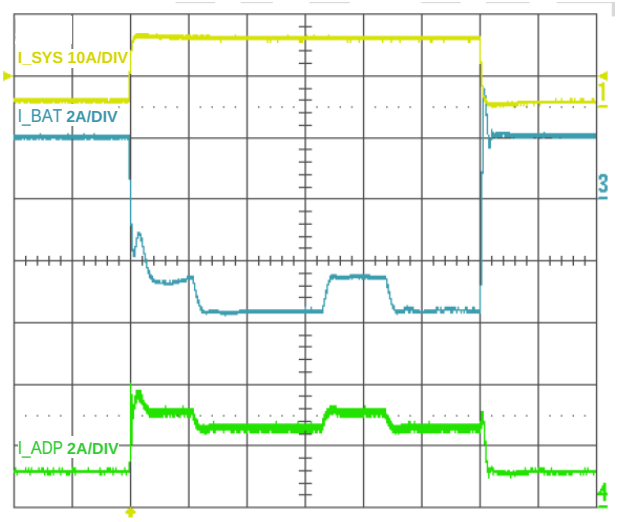


FIGURE 14. TWO LEVEL ADAPTER CURRENT LIMIT. VADP = 20V, ADAPTERCURRENTLIMIT1 = 2.56A, ADAPTERCURRRENTLIMIT2 = 3.072A, T1 = 500µs, T2 = 1ms, V_{BAT} = 7V, MAXCHARGEVOLTAGE = 8.192V, CHARGECURRENT = 2.016A, 1A to 12A SYSTEM LOAD STEP

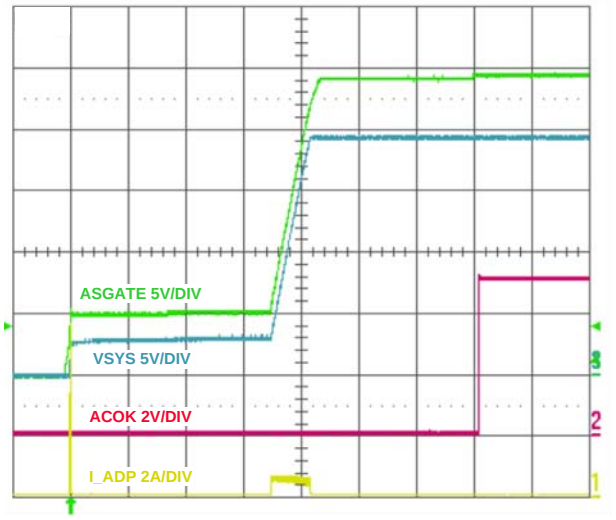


FIGURE 15. HPB: ADAPTER INSERTION ASGATE IN-RUSH CURRENT CONTROL. NO BATTERY, VADP = 20V, 330µF SYSTEM RAIL CAPACITANCE

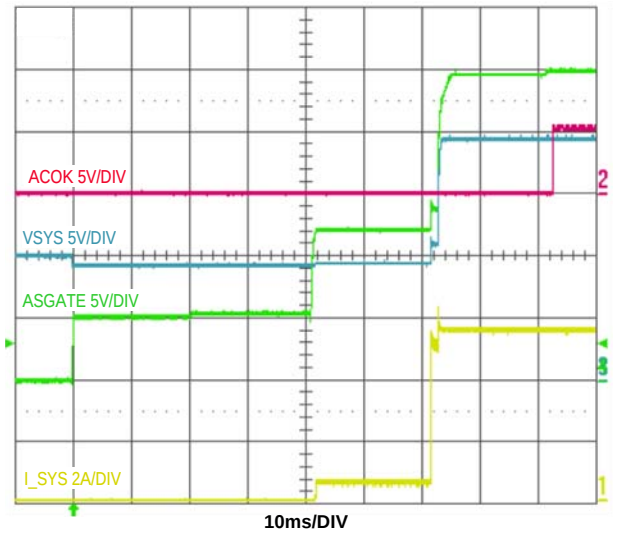


FIGURE 16. HPB: ADAPTER INSERTION ASGATE IN-RUSH CURRENT CONTROL. V_{BAT} = 10V, VADP = 20V, ACLIM SETTING = 5A, SYSTEM LOAD = 5.5A

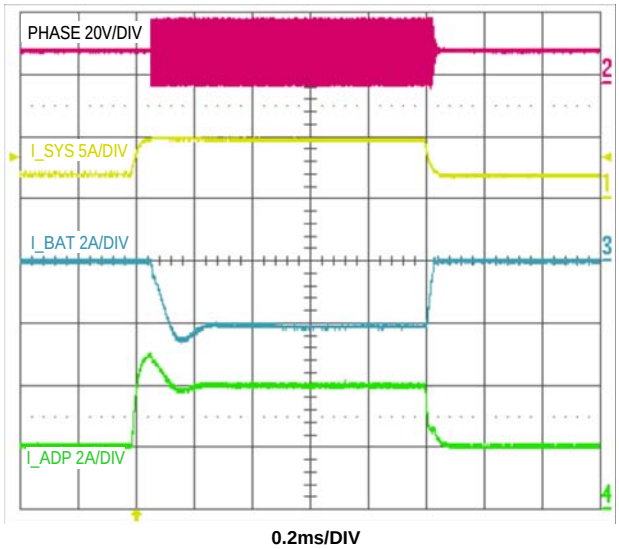


FIGURE 17. HPB: CHARGE DISABLED, ENTER TURBO MODE. VADP = 20V, V_{BAT} = 10V, ADAPTERCURRENTLIMIT1 = 4.096A, 2A to 5A LOAD STEP

Typical Performance (Continued)

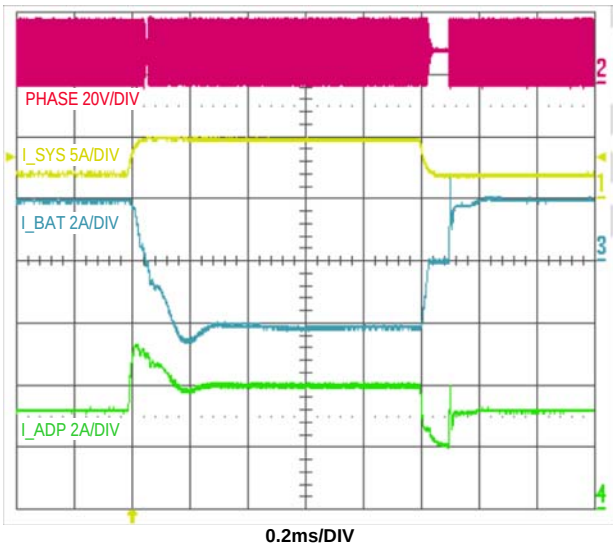


FIGURE 18. HPB: CHARGE ENABLED, ENTER TURBO MODE. VADP = 20V, V_{BAT} = 10V, ADAPTERCURRENTLIMIT1 = 4.096A, CHARGECURRENT = 2.016A, 2A to 5A LOAD STEP

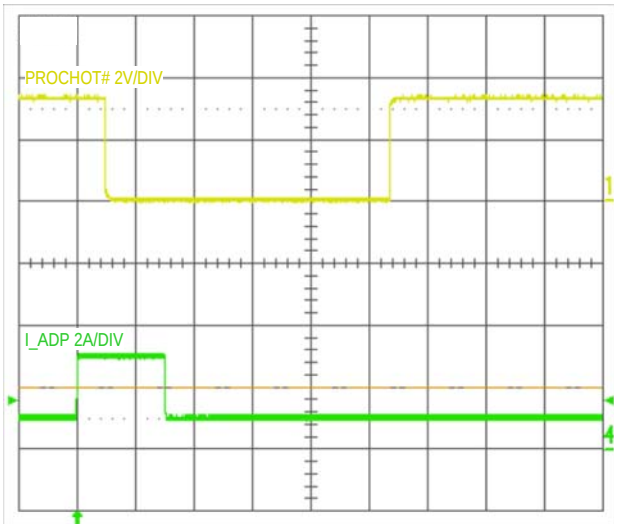


FIGURE 19. ACPROCHOT# ASSERTION. ACPROCHOT = 2.048A, PROCHOTDEBOUNCE = 1ms, PROCHOTDURATION = 10ms

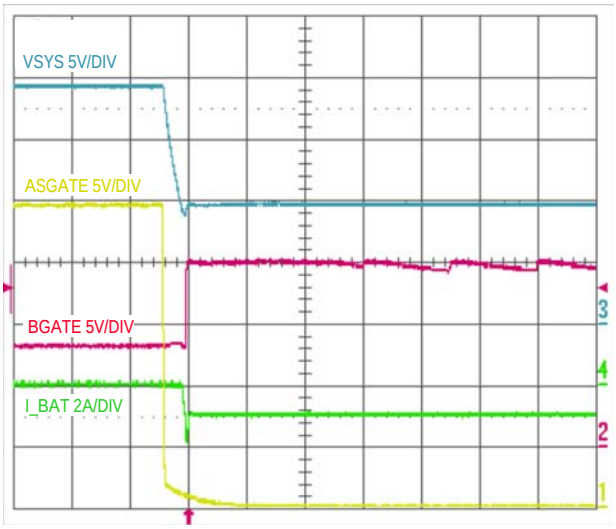


FIGURE 20. HPB: ENTER LEARN MODE

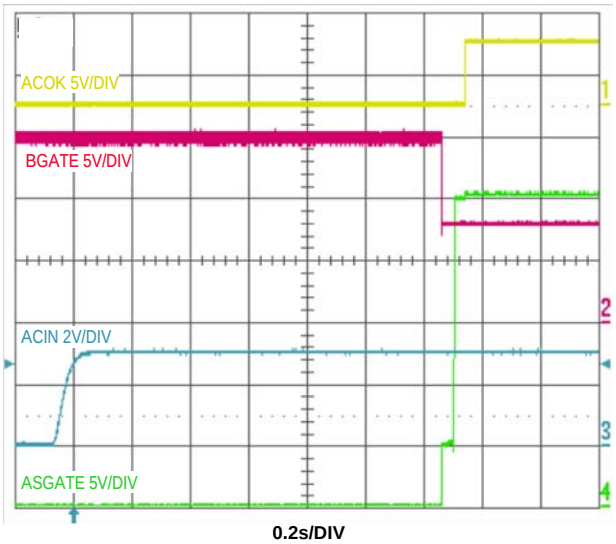


FIGURE 21. HPB: ASGATE TURNING ON DELAY AFTER ADATPER INSERTION. VADP = 20V, V_{BAT} = 10V, CONTROL2 REGISTER BIT<5> = 0

Typical Performance (Continued)

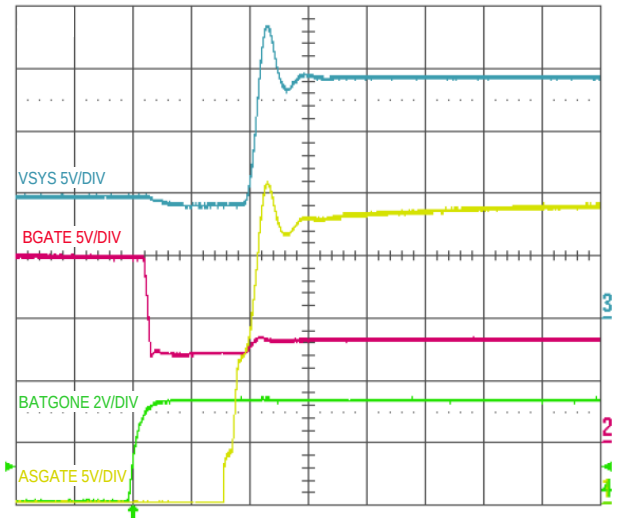


FIGURE 22. HPB: BATTERY SUDDEN REMOVAL IN LEARN MODE BY PULLING BATGONE TO HIGH

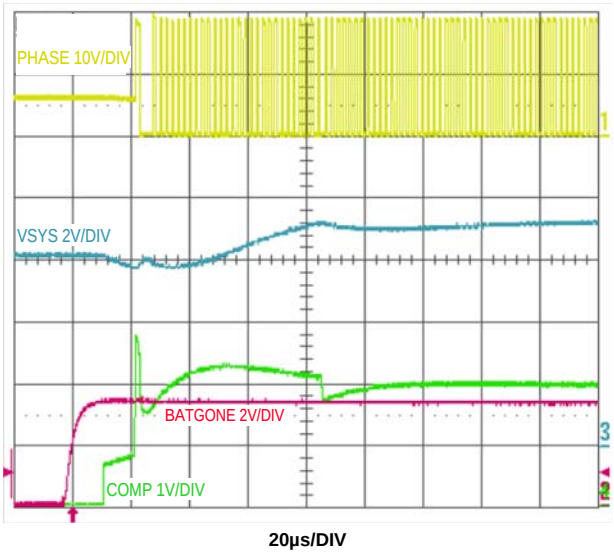


FIGURE 23. NVDC: BATTERY SUDDEN REMOVAL IN LEARN MODE BY PULLING BATGONE TO HIGH

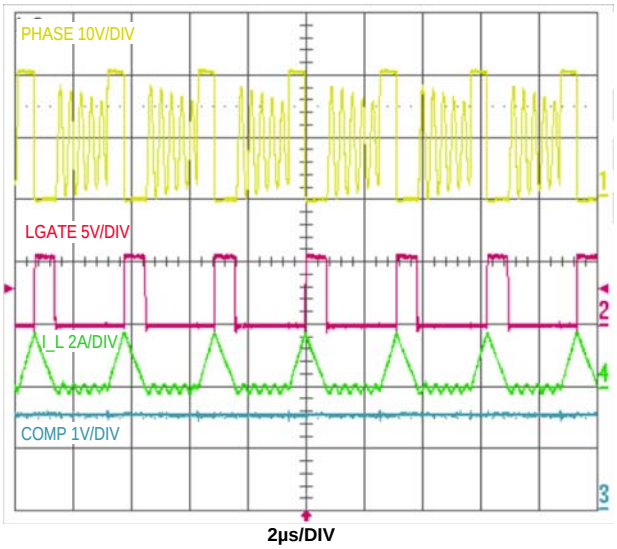


FIGURE 24. DISCONTINUOUS CONDUCTION MODE (DCM) SWITCHING

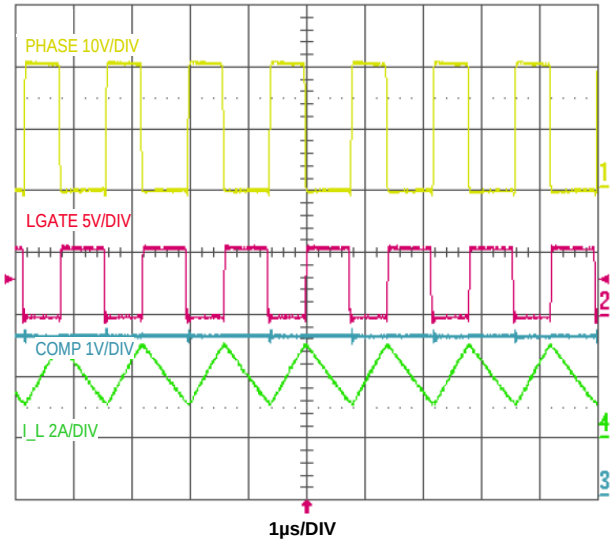


FIGURE 25. CONTINUOUS CONDUCTION MODE (CCM) SWITCHING

General SMBus Architecture

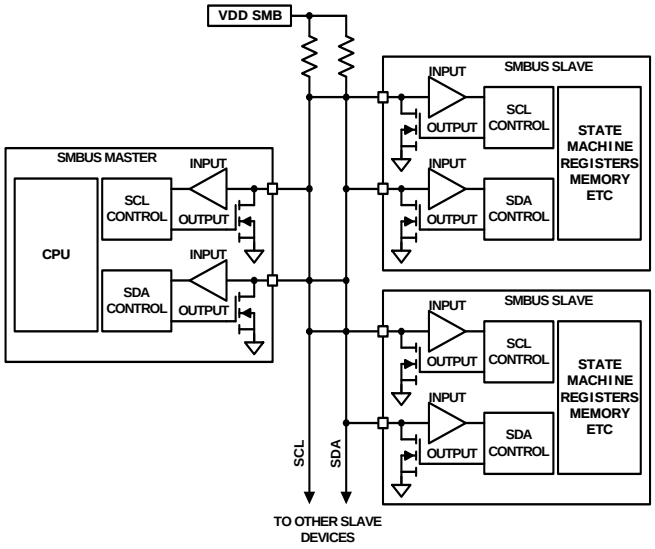


FIGURE 26. GENERAL SMBus ARCHITECTURE

Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH-or-LOW state of the data line can change only when the clock signal on the SCL line is LOW. See Figure 27.

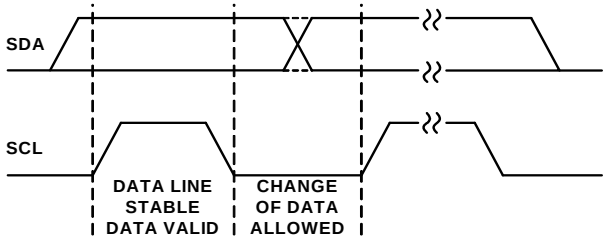


FIGURE 27. DATA VALIDITY

START and STOP Conditions

In Figure 28, the START condition is a HIGH-to-LOW transition of the SDA line while SCL is HIGH.

The STOP condition is a LOW-to-HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition.

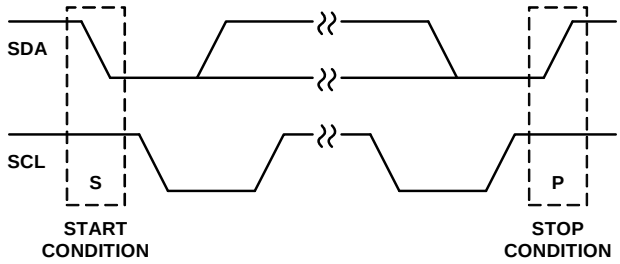


FIGURE 28. START AND STOP WAVEFORMS

Acknowledge

Each address and data transmission uses 9-clock pulses. The ninth pulse is the acknowledge bit (ACK). After the start condition, the master sends 7 slave address bits and a R/$\overline{W}$ bit during the next 8-clock pulses. During the 9-clock pulse, the device that recognizes its own address holds the data line low to acknowledge (as shown in Figure 29). Both the master and the salve use the ACK bit to acknowledge receipt of register addresses and data.

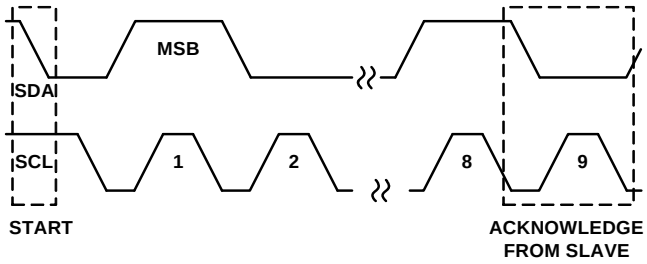


FIGURE 29. ACKNOWLEDGE ON THE SMBus

SMBus Transactions

All transactions start with a control byte sent from the SMBus master device. The control byte begins with a Start condition, followed by seven bits of slave address (0001001 for the ISL95520) and the R/$\overline{W}$ bit. The R/$\overline{W}$ bit is 0 for a WRITE or 1 for a READ. If any slave device on the SMBus bus recognize its address, it acknowledges by pulling the serial data (SDA) line low for the last clock cycle in the control byte. If no slave exists at that address or it is not ready to communicate, the data line is a 1, which indicates a Not Acknowledge condition.

When the control byte is sent and the ISL95520 acknowledges it, the second byte sent by the master must be a register address byte, such as 0x14 for the ChargeCurrent register. The register address byte tells the ISL95520 which register the master writes or reads. See Table 1 on page 24 for register details. When the ISL95520 receives a register address byte, it responds with an acknowledge.

Byte Format

Every byte put on the SDA line must be 8 bits long and must be followed by an acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first and the Least Significant Bit (LSB) last. The LO BYTE data is transferred before the HI BYTE data. For example, when writing 0x41A0, 0xA0 is written first and 0x41 is sent second.

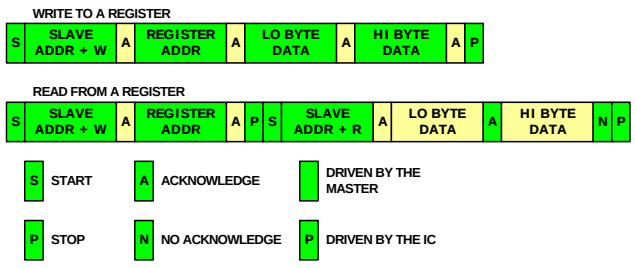


FIGURE 30. SMBus READ AND WRITE PROTOCOL

ISL95520 SMBus Commands

The ISL95520 receives control inputs from the SMBus interface after Power On Reset (POR). The serial interface complies with System Management Bus Specification, which can be downloaded from www.smbus.org. The ISL95520 uses the SMBus Read-Word and Write-Word protocols shown in Figure 30 on page 23 to communicate with the host system and a smart battery. The ISL95520 is an SMBus slave device and does not initiate communication on the bus. It responds to the 7-bit address 0b0001001_:

Read address = 0b00010011 (0X13H)

Write address = 0b00010010 (0X12H).

The data (SDA) and clock (SCL) pins have Schmitt-trigger inputs that can accommodate slow edges. Choose pull-up resistors for SDA and SCL to achieve rise times according to the SMBus specifications.

The ISL95520 allows you to change the SMBus registers to change some functions and options, as shown in Table 1.

The illustration in this datasheet is based on current sensing resistors Rs_1 = 10mΩ and Rs_2 = 10mΩ unless specified otherwise. For other current sensing resistors specifications, see Tables 18 and 19 for more information.

TABLE 1. REGISTERS SUMMARY (Rs_1 = 10mΩ AND Rs_2 = 10mΩ)

REGISTER TYPE A: Accepts any command, but only the valid register bits are written to the register. B: All commands beyond the valid register bits are ignored.						
REGISTER NAMES	**REGISTER ADDRESS**	**READ/ WRITE**	**REGISTER TYPE**	**NUMBER OF BITS**	**DESCRIPTION**	**POR BIT STATE**
ChargeCurrentLimit	0X14H	R/W	A	8	Bits <12:5> are used. If Bit<0> is interpreted as 1mA, the resolution is 32mA and the POR default value is 0A.	<12:5> 00000000
DischargeCurrentLimit	0X40H	R/W	B	6	Bits <12:7> are used. If Bit<0> is interpreted as 1mA, the resolution is 128mA and the POR default value is 8.064A.	<12:7> 111111
AdapterCurrentLimit1	0X3FH	R/W	B	6	Bits<12:7> are used. If Bit<0> is interpreted as 1mA, the resolution is 128mA and the POR default value is 8.064A.	<12:7> 111111
AdapterCurrentLimit2	0X3BH	R/W	B	6	Bits<12:7> are used. If Bit<0> is interpreted as 1mA, the resolution is 128mA and the POR default value is 8.064A.	<12:7> 111111
T1	0X37H	R/W	A	3	Bits<2:0> are used. If the 2-level adapter current limit function is enabled and is tripped, T1 configures the effective duration of the AdapterCurrentLimit1 register. The POR default value is 500µs.	<2:0> 110
T2	0X38H	R/W	A	3	Bits<2:0> are used. If the 2-level adapter current limit function is enabled and is tripped, T2 configures the effective duration of the AdapterCurrentLimit2 register. The POR default value is 100µs.	<2:0> 001
MaxChargeVoltage	0X15H	R/W	A	11	Bits <14:4> are used. If Bit<0> is interpreted as 1mV, the resolution is 16mV. The POR default value is based on the PROG pin cell number programming: 2-cell: 8.192V 3-cell: 12.288V 4-cell: 16.4V The MaxChargeVoltage register should always be programmed higher than the MinChargeVoltage register.	

TABLE 1. REGISTERS SUMMARY (Rs_1 = 10mΩ AND Rs_2 = 10mΩ) (Continued)

REGISTER TYPE

A: Accepts any command, but only the valid register bits are written to the register.

B: All commands beyond the valid register bits are ignored.

REGISTER NAMES	REGISTER ADDRESS	READ/ WRITE	REGISTER TYPE	NUMBER OF BITS	DESCRIPTION	POR BIT STATE
MinChargeVoltage	0X3EH	R/W	B	6	Bits <13:8> are used. If Bit<0> is interpreted as 1mV, the resolution is 256mV. The POR default value is based on the PROG pin cell number programming: 2-cell: 5.376V 3-cell: 8.064V 4-cell: 10.752V The MinChargeVoltage register should always be programmed lower than the MaxChargeVoltage register.	
ProchotDebounce	0X39H	R/W	A	2	Bits<1:0> are used. Sets the debounce time before asserting the Prochot# signal for NTC_Prochot#, ACProchot#, and DCProchot#. The POR default value is 100µs.	<1:0> 01
ProchotDuration	0X3AH	R/W	A	3	Bits<2:0> are used. Sets the minimum duration of Prochot# signal latch-up when asserted. The POR default value is 10ms.	<2:0> 011
ACProchot	0X47H	R/W	B	6	Bits<12:7> are used. Sets the PROCHOT# threshold for adapter overcurrent condition. If Bit<0> is interpreted as 1mA, the resolution is 128mA and the POR default value is 6.144A.	<12:7> 110000
DCProchot	0X48H	R/W	B	6	Sets the PROCHOT# threshold for battery over-discharging current condition. Bits <12:7> are used. If Bit<0> is interpreted as 1mA, the resolution is 128mA and the POR default value is 4.096A.	<12:7> 100000
Control1	0X3DH	R/W	-	16	See Control1 register (Table 13).	
Control2	0X3CH	R/W	-	12	See Control2 register (Table 14).	
Information1	0X46H	R	-	8	Various information reported over SMBus. See Information1 register (Table 15).	
Information2	0X45H	R/W	-	8	PROG pin resistor reading result report. Also configures the 20mΩ current sensing resistor option. See Information2 register (Table 16).	
ManufacturerID	0XFEH	R	-		ASCII for “I”.	0X49H
DeviceID	0XFFH	R	-			0X08H

Setting Charging Current Limit

To set the charging current limit, write a 16-bit ChargeCurrentLimit command (0X14H or 0b00010100) using the Write-Word protocol shown in Figure 30 and the data format shown in Table 2.

The ISL95520 limits the charging current by limiting the V_{CSOP}-V_{CSON} voltage. By using the recommended current sense resistor values shown in Table 17, the register's LSB always translates to 1mA of charging current. The ChargeCurrentLimit register accepts any charging current command, but only the valid register bits are written to the register. It is not recommended to set charging current limit lower than 96mA.

After POR, the ChargeCurrentLimit register is reset to 0x0000H. To set the battery charging current value, write a valid, non-zero number to the ChargeCurrentLimit register. The ChargeCurrentLimit register can be read back to verify its contents.

Tables 21 and 22 show the conditions to enable fast charging according to the ChargeCurrentLimit register setting for the HPB configuration and NVDC configuration, respectively.

TABLE 2. CHARGECURRENTLIMIT REGISTER 0x14H (Rs_1 = 10mΩ AND Rs_2 = 10mΩ. (SEE Table 18 FOR OTHER CONFIGURATIONS)

BIT	DESCRIPTION
<4:0>	Not used.
<5>	0 = Add 0mA of charging current limit. 1 = Add 32mA of charging current limit.
<6>	0 = Add 0mA of charging current limit. 1 = Add 64mA of charging current limit.
<7>	0 = Add 0mA of charging current limit. 1 = Add 128mA of charging current limit.
<8>	0 = Add 0mA of charging current limit. 1 = Add 256mA of charging current limit.
<9>	0 = Add 0mA of charging current limit. 1 = Add 512mA of charging current limit.
<10>	0 = Add 0mA of charging current limit. 1 = Add 1024mA of charging current limit.
<11>	0 = Add 0mA of charging current limit. 1 = Add 2048mA of charging current limit.
<12>	0 = Add 0mA of charging current limit. 1 = Add 4096mA of charging current limit.
<15:13>	Not used.

Setting Discharging Current Limit

To set the discharging current limit, write a 16-bit DischargeCurrentLimit command (0X40H or 0b01000000) using the Write-Word protocol shown in Figure 30 and the data format shown in Table 3.

The ISL95520 limits the HPB charger battery discharging current by limiting the V_{CSON}-V_{CSOP} voltage in turbo/boost mode. By using the recommended current sense resistor values shown in Table 17, the register's LSB always translates to 1mA discharging current. All discharging current limit command values beyond the valid register bits are ignored.

After POR, the DischargeCurrentLimit register is reset to 0x1F80H. To set the battery discharging current limit, write a valid, non-zero number to the ChargeCurrentLimit register. The DischargeCurrentLimit register can be read back to verify its contents.

TABLE 3. DISCHARGECURRENTLIMIT REGISTER 0x40H (Rs_1 = 10mΩ AND Rs_2 = 10mΩ. SEE Table 18 FOR OTHER CONFIGURATIONS)

BIT	DESCRIPTION
<6:0>	Not used.
<7>	0 = Add 0mA of discharging current limit. 1 = Add 128mA of discharging current limit.
<8>	0 = Add 0mA of discharging current limit. 1 = Add 256mA of discharging current limit.
<9>	0 = Add 0mA of discharging current limit. 1 = Add 512mA of discharging current limit.
<10>	0 = Add 0mA of discharging current limit. 1 = Add 1024mA of discharging current limit.
<11>	0 = Add 0mA of discharging current limit. 1 = Add 2048mA of discharging current limit.
<12>	0 = Add 0mA of discharging current limit. 1 = Add 4096mA of discharging current limit.
<15:13>	Not used.

Setting Adapter Current Limit

To set the adapter current limit, write a 16-bit AdapterCurrentLimit1 command (0X3FH or 0b00111111) and/or AdapterCurrentLimit2 command (0X3BH or 0b00111011) using the Write-Word protocol shown in Figure 30 and the data format shown in Table 4.

The ISL95520 limits the adapter current by limiting the V_{CSIP}-V_{CSIN} voltage. By using the recommended current sense resistor value as Table 17 shows, the register's LSB always translates to 1mA adapter current. All adapter current limit commands beyond the valid register bits are ignored. The minimum adapter current limit command is 128mA and 0A commands are rejected.

After POR, the AdapterCurrentLimit1 and AdapterCurrentLimit2 registers are reset to 0x1FC0. The AdapterCurrentLimit1 and AdpaterCurrentLimit2 registers can be read back to verify their contents.

To set a second level adapter current limit, write a 16-bit AdapterCurrentLimit2 (0X3BH or 0b00111011) command using the Write-Word protocol shown in Figure 30 and the data format shown in Table 4.

The AdapterCurrentLimit2 register has the same specification as the AdapterCurrentLimit1 register. See "Two-Level Adapter Current Limit" on page 43 for detailed operation.

TABLE 4. ADAPTERCURRENTLIMIT1 REGISTER 0x3FH AND ADAPTERCURRENTLIMIT2 REGISTER 0X3BH (Rs_1 = 10mΩ AND Rs_2 = 10mΩ)

BIT	DESCRIPTION
<6:0>	Not used.
<7>	0 = Add 0mA of adapter current limit. 1 = Add 128mA of adapter current limit.
<8>	0 = Add 0mA of adapter current limit. 1 = Add 256mA of adapter current limit.
<9>	0 = Add 0mA of adapter current limit. 1 = Add 512mA of adapter current limit.
<10>	0 = Add 0mA of adapter current limit. 1= Add 1024mA of adapter current limit.
<11>	0 = Add 0mA of adapter current limit. 1 = Add 2048mA of adapter current limit.
<12>	0 = Add 0mA of adapter current limit. 1 = Add 4096mA of adapter current limit.
<15:13>	Not used.

Setting Two-Level Adapter Current Limit Duration

For the two-level adapter current limit, write a 16-bit T1 command (0X37H or 0b00110111) using the Write-Word protocol shown in Figure 30 and the data format shown in Table 5 to set the AdapterCurrentLimit1 duration as the adapter current limit; write a 16-bit T2 command (0X38H or 0b00111000) to set the AdapterCurrentLimit2 duration as the adapter current limit. The T1 register and T2 register accept any command, but only the valid register bits are written. See "Two-Level Adapter Current Limit" on page 43 for detailed operation.

TABLE 5. T1 Register 0x37H

BIT	DESCRIPTION
<2:0>	000 = 0ms 001 = 20ms 010 = 15ms 011 = 10ms 100 = 5ms 101 = 1ms 110 = 0.5ms 111 = 0.1ms
<15:3>	Not used.

TABLE 6. T2 REGISTER 0x38H

BIT	DESCRIPTION
<2:0>	000 = 15µs 001 = 100µs 010 = 500µs 011 = 1ms 100 = 300µs 101 = 750µs 110 = 3ms 111 = 10ms
<15:3>	Not used.

Setting Maximum Charging Voltage

To set the maximum charging voltage, write a 16-bit MaxChargeVoltage command (0X15H or 0b00010101) using the Write-Word protocol shown in Figure 30 and the data format shown in Table 7.

The maximum charging voltage range is 7.168V to 18.432V. The MaxChargeVoltage register accepts any voltage command, but only the valid register bits are written to the register.

The MaxChargeVoltage register sets the battery full charging voltage limit. For the NVDC configuration, the MaxChargeVoltage register setting is also the system bus voltage regulation point when the battery is present but is not in charge. See "NVDC Charger System Voltage Regulation" on page 44 for details.

The CSON pin senses the battery voltage for maximum charging voltage regulation and should be connected close to the battery. For the NVDC configuration, the CSON pin is also the system bus voltage regulation sense point.

TABLE 7. MAXCHARGEVOLTAGE REGISTER 0x15H

BIT	DESCRIPTION
<3:0>	Not used.
<4>	0 = Add 0mV of charging voltage. 1 = Add 16mV of charging voltage.
<5>	0 = Add 0mV of charging voltage. 1 = Add 32mV of charging voltage.
<6>	0 = Add 0mV of charging voltage. 1 = Add 64mV of charging voltage.
<7>	0 = Add 0mV of charging voltage. 1 = Add 128mV of charging voltage.
<8>	0 = Add 0mV of charging voltage. 1 = Add 256mV of charging voltage.
<9>	0 = Add 0mV of charging voltage. 1 = Add 512mV of charging voltage.
<10>	0 = Add 0mV of charging voltage. 1 = Add 1024mV of charging voltage.
<11>	0 = Add 0mV of charging voltage. 1 = Add 2046mV of charging voltage.
<12>	0 = Add 0mV of charging voltage. 1 = Add 4096mV of charging voltage.
<13>	0 = Add 0mV of charging voltage. 1 = Add 8192mV of charging voltage.
<14>	0 = Add 0mV of charging voltage. 1 = Add 16384mV of charging voltage.
<15>	Not used.

Setting Minimum Charging Voltage

To set the minimum charging voltage, write a 16-bit MinChargeVoltage command (0X3EH or 0b00111110) using the Write-Word protocol shown in Figure 30 and the data format shown in Table 8.

The minimum charging voltage range is 2.048V to 16.128V. All minimum charging voltage commands beyond the valid register bits are ignored. The MinChargeVoltage register value should be set lower than the MaxChargeVoltage register value.

The MinChargeVoltage register sets the battery voltage threshold for entry and exit of trickle charge mode. The VBAT pin senses the battery voltage to compare with the MinChargeVoltage register setting. See "Trickle Charging" on page 43 for details.

For the NVDC configuration, MinChargeVoltage register setting is also the system voltage regulation point when the battery is not present. The CSON pin is the system voltage regulation sense point. See "NVDC Charger System Voltage Regulation" on page 44 for details.

TABLE 8. MINCHARGEVOLTAGE REGISTER 0x3EH

BIT	DESCRIPTION
<7:0>	Not used.
<8>	0 = Add 0mV of charging voltage. 1 = Add 256mV of charging voltage.
<9>	0 = Add 0mV of charging voltage. 1 = Add 512mV of charging voltage.
<10>	0 = Add 0mV of charging voltage. 1 = Add 1024mV of charging voltage.
<11>	0 = Add 0mV of charging voltage. 1 = Add 2048mV of charging voltage.
<12>	0 = Add 0mV of charging voltage. 1 = Add 4096mV of charging voltage.
<13>	0 = Add 0mV of charging voltage. 1 = Add 8192mV of charging voltage.
<15:14>	Not used.

Setting PROCHOT# Debounce Time

To set the PROCHOT# signal debounce time before its assertion for ACProchot, DCProchot, and NTC_Prochot, write a 16-bit PROCHOT# debounce time (0X39H or 0b00111001) using the Write-Word protocol shown in Figure 30 and the data format shown in Table 9. The Prochot# Debounce Time register accepts any command, but only the valid register bits are written.

The low system voltage Prochot# has a fixed debounce time of 10µs.

TABLE 9. PROCHOTDEBOUNCE REGISTER 0x39H

BIT	DESCRIPTION
<1:0>	00 = 10µs 01 = 100µs 10 = 500µs 11 = 1ms
<15:2>	Not used

Setting PROCHOT# Duration

To set the PROCHOT# signal latch-up duration when asserted for ACProchot, DCProchot and NTC_Prochot and low system voltage Prochot, write a 16-bit PROCHOT# Duration command (0X3AH or 0b01111010) using the Write-Word protocol shown in Figure 30 and the data format shown in Table 10. The Prochot# Duration register accepts any command, but only the valid register bits are written.

TABLE 10. PROCHOT# DURATION REGISTER 0x3Ah

BIT	DESCRIPTION
<2:0>	000 = 0ms 001 = 20ms 010 = 15ms 011 = 10ms 100 = 5ms 101 = 1ms 110 = 500µs 111 = 100µs
<15:3>	Not used.

Setting PROCHOT# Threshold for Adapter Overcurrent Condition

To set the PROCHOT# assertion threshold for adapter overcurrent condition, write a 16-bit ACProchot command (0X47H or 0b01000111) using the Write-Word protocol shown in Figure 30 and the data format shown in Table 11. By using the recommended current sense resistor value as Table 17 shows, the register's LSB always translates to 1mA adapter current. All ACProchot command values beyond the valid register bits are ignored.

After POR, the ACProchot register is reset to 0x1800H. The ACProchot register can be read back to verify its contents.

If the adapter current exceeds the ACProchot register setting, the PROCHOT# signal asserts after the debounce time programmed by the ProchotDebounce register and latches on for a minimum time programmed by the ProchotDuration register.

For HPB configuration, ACProchot function is disabled when it is in standby mode since the standby mode turns off the internal comparator reference, which is indicated by Information1 register Bit<8>.

TABLE 11. ACPROCHOT REGISTER 0x47H (Rs_1 = 10mΩ AND Rs_2 = 10mΩ. SEE Table 18 FOR OTHER CONFIGURATIONS)

BIT	DESCRIPTION
<6:0>	Not used.
<7>	0 = Add 0mA of ACProchot threshold. 1 = Add 128mA of ACProchot threshold.
<8>	0 = Add 0mA of ACProchot threshold. 1 = Add 256mA of ACProchot threshold.
<9>	0 = Add 0mA of ACProchot threshold. 1 = Add 512mA of ACProchot threshold.
<10>	0 = Add 0mA of ACProchot threshold. 1 = Add 1024mA of ACProchot threshold.
<11>	0 = Add 0mA of ACProchot threshold. 1 = Add 2048mA of ACProchot threshold.
<12>	0 = Add 0mA of ACProchot threshold. 1 = Add 4096mA of ACProchot threshold.
<15:13>	Not used.

Setting PROCHOT# Threshold for Battery Over Discharging Current Condition

To set the PROCHOT# signal assertion threshold for battery over discharging current conditions, write a 16-bit DCProchot command (0X48H or 0b01001000) using the Write-Word protocol shown in Figure 30 and the data format shown in Table 12. By using the recommended current sense resistor value as Table 17 shows, the register's LSB always translates to 1mA adapter current. All DCProchot command beyond the valid register bits are ignored.

After POR, the DCProchot register is reset to 0x1000H. The DCProchot register can be read back to verify its contents.

If the battery discharging current exceeds the DCProchot register setting, the PROCHOT# signal asserts after the debounce time programmed by the ProchotDebounce register and latches on for a minimum time programmed by the ProchotDuration register.

In battery only mode, the DCProchot function works only when PSYS or NTC is enabled, because enabling PSYS or NTC activates the internal comparator reference. The Information1 register bit<8> indicates whether the internal comparator reference is active or not.

When the adapter is present, the internal comparator reference is always active unless it is in standby mode for the HPB configuration.

TABLE 12. DCPROCHOT REGISTER 0x48H (Rs_1 = 10mΩ AND Rs_2 = 10mΩ. SEE Table 18 FOR OTHER CONFIGURATIONS)

BIT	DESCRIPTION
<6:0>	Not used.
<7>	0 = Add 0mA of DCProchot threshold. 1 = Add 128mA of DCProchot threshold.
<8>	0 = Add 0mA of DCProchot threshold. 1 = Add 256mA of DCProchot threshold.
<9>	0 = Add 0mA of DCProchot threshold. 1 = Add 512mA of DCProchot threshold.
<10>	0 = Add 0mA of DCProchot threshold. 1 = Add 1024mA of DCProchot threshold.
<11>	0 = Add 0mA of DCProchot threshold. 1 = Add 2048mA of DCProchot threshold.
<12>	0 = Add 0mA of DCProchot threshold. 1 = Add 4096mA of DCProchot threshold.
<15:13>	Not used.

Control Registers

To change certain functions or options after POR, write a 16-bit control command to the Control1 register (0X3DH or 0b00111101) or Control2 register (0X3CH or 0b00111100) using the Write-Word protocol shown in Figure 30 and the data format shown in Tables 13 and 14, respectively.

TABLE 13. CONTROL1 REGISTER 0x3DH

BIT	BIT NAME	DESCRIPTION	POR STATE
<0>	Standby Mode	1 = The charger enters Standby mode. 0 = The charger exits Standby mode. The Standby mode control bit is valid for the HPB configuration only and is valid only when the adapter is present; it has no effect in the NVDC configuration. When the ISL95520 enters Standby mode, it turns off the internal references (indicated by Information1 register bit<8>) and stops switching to enter a low power consumption mode with minimum quiescent current. If PSYS is already enabled, it cannot enter Standby mode.	0
<1>	Learn Mode	1 = The charger enters Learn mode. 0 = The charger exits Learn mode. The SMBus Learn mode control is valid only when PROG pin is not pulled to 5V after POR. For the NVDC configuration, Learn mode can be enabled only when both PSYS Bit<4> and NTC Bit<6> are disabled.	0
<2>	AMON	1 = Turn on the adapter current monitor AMON function. 0 = Turn off the adapter current monitor AMON function.	0
<3>	BMON	1 = Turn on the battery discharging current monitor BMON function. 0 = Turn off the battery discharging current monitor BMON function. The BMON function is disabled if the battery voltage is less than 3.5V to avoid battery over discharge.	0

TABLE 13. CONTROL1 REGISTER 0x3DH (Continued)

BIT	BIT NAME	DESCRIPTION	POR STATE
<4>	PSYS	1 = Turn on the system power monitor PSYS function. 0 = Turn off the system power monitor PSYS function. The PSYS function does not include the power provided by the battery if the battery voltage is less than 3.5V. For the HPB configuration, if the adapter is present and enters Standby mode already, PSYS cannot be turned on.	0
<5>	Low System Voltage Detection	1 = Turn on the low system voltage detect function. 0 = Turn off the low system voltage detect function. Bit<5> is valid only when the internal comparator reference is active, which is indicated by Information1 register Bit<8>. In Battery Only mode, the low system voltage detection function works only when PSYS or NTC are enabled, because enabling PSYS or NTC activates the internal comparator reference. When the adapter is present, the internal comparator reference is always active unless it is in standby mode for HPB configuration. For the HPB configuration, ISL95520 senses the system voltage through CSIP pin. For the NVDC configuration, ISL95520 senses the system voltage through CSON pin.	0
<6>	NTC	1 = Turn on the NTC function. 0 = Turn off the NTC function. When turned on, if the NTC pin voltage is less than 170mV, the PROCHOT# signal asserts after the debounce time programmed by the ProchotDebounce register and latches on for a minimum time programmed by the ProchotDuration register. For the NTC function to work, the internal reference indicated by Information1 register Bit<8> needs to be active. When the adapter is present, the NTC function is always turned on unless it is in Standby mode, in which case Bit<6> is invalid. In Battery Only mode, Bit<6> is valid to turn the NTC function on or off only when PSYS is turned off; the NTC function is always turned on automatically if PSYS is turned on.	0
<7>	Fast Learn Mode Exit	1 = Fast Learn mode exit. 0 = Slow Learn mode exit. For Fast Learn mode exit, it turns on ASGATE MOSFETs instantly without going through the ASGATE soft-start turning on procedure when the BATGONE pin voltage goes from logic low-to-high. For Slow Learn mode exit, it goes through the ASGATE soft-start turning on procedure 1.3s or 163ms (which is set by Control2 register bit<5>) after the BATGONE pin voltage goes from logic low to high. The Fast Learn Mode Exit control bit is valid only when the battery is removed during Learn mode. It works for the HPB configuration only and has no effect for the NVDC configuration.	0
<9:8>	Threshold for Low System Voltage Detection	If the Control register Bit<5> = 1, Bits<9:8> program the low system voltage detection threshold. If the system voltage is below this threshold, the PROCHOT# signal asserts after a fixed 10µs debounce time and latches on for a minimum time programmed by the ProchotDuration register. 00 = 5.6V threshold 01 = 6.06V threshold 10 = 6.53V threshold 11 = 7V threshold Valid only when Control1 register Bit<5> = 1.	00
<10>	Turbo/Boost Mode	1 = Disable Turbo/Boost mode. 0 = Enable Turbo/Boost mode.	1

TABLE 13. CONTROL1 REGISTER 0x3DH (Continued)

BIT	BIT NAME	DESCRIPTION	POR STATE
<11>	Adapter Current Cycle-By-Cycle Limit	1 = Enable the adapter current cycle-by-cycle limit function. 0 = Disable the adapter current cycle-by-cycle limit function. The adapter current cycle-by-cycle limit function is valid only when the charger is in Buck mode.	0
<12>	Enable Charging	0 = Disable charging. 1 = Enable charging.	1
<14:13>	Force The Number Of Battery Cells In Series	Bits<14:13> can overwrite the number of battery cells in series that are programmed by the PROG pin. When Bits<14:13> are written, only the POR default MaxChargeVoltage register value and MinChargeVoltage register value change according to the cell number. The battery 4.6V/cell overvoltage protection threshold also changes according to the cell number. The MaxChargeVoltage register setting should be always smaller than the battery overvoltage threshold 4.6V*cell#. If Bits<14:13> are not used, keep their POR code based on the PROG pin cell# setting. 00 = Not available and ignored if written 01 = 2-Cell 10 = 3-Cell 11 = 4-Cell	PROG cell#
<15>	SMBus Timeout	The ISL95520 includes a timer to ensure the SMBus master is active and to prevent overcharging the battery. If the adapter is present and if the ISL95520 does not receive a write to the MaxChargeVoltage or ChargeCurrentLimit register within 175s, the ISL95520 terminates charging. If a timeout occurs, writing the MaxChargeVoltage or ChargeCurrentLimit register re-enables charging. 0 = Enable the SMBus timeout function. 1 = Disable the SMBus timeout function.	0

TABLE 14. CONTROL2 REGISTER 0x3CH

BIT	BIT NAME	DESCRIPTION	POR STATE
<3:0>	Frequency Setting	Overwrites the switching frequency set by the FSET pin. See Table 20 (default CCM switching frequency programming table) for the correlation. 1111 = 992kHz (equivalent to R_FSET = 0Ω) 1110 = 838kHz 1101 = 729kHz 1100 = 642kHz 1011 = 678kHz 1010 = 614kHz 1001 = 561kHz 1000 = 517kHz 0111 = 513kHz 0110 = 477kHz 0101 = 449kHz 0100 = 421kHz 0011 = 417kHz 0010 = 395kHz 0001 = 375kHz 0000= Switching frequency set by FSET pin To keep the switching frequency set by the PROG pin resistor, leave Bit<3:0> as it is or write code 000, which sets the same frequency as the PROG pin resistor does.	0000
<4>	Release Adapter Current Limit when No Battery	When there is no battery, Bit<4> enables or release adapter current limit for NVDC configuration. 0 = Enable adapter current limit function. 1 = Release adapter current limit function.	0

TABLE 14. CONTROL2 REGISTER 0x3CH (Continued)

BIT	BIT NAME	DESCRIPTION	POR STATE
<5>	ASGATE Turn On Delay	0 = Set ASGATE turn on delay to 1.3s from when the adapter is plugged in. 1 = Set ASGATE turn on delay to 163ms from when the adapter is plugged in.	0
<6>	Two-level Adapter Current Limit Function	0 = Disable two-level adapter current limit function. 1 = Enable two-level adapter current limit function.	1
<7> <12>	Trickle Charging Current	Bit<12> and Bit<7> can be combined together to change the trickle charging current value. Bit <12>:<7> =: <0>:<0> = 256mA trickle charging current <0>:<1> = 128mA trickle charging current <1>:<0> = 128mA trickle charging current <1>:<1> = 64mA trickle charging current The 64mA trickle charging current option is valid only for NVDC and only for "Rs_1 = 10mΩ, Rs_2 = 10mΩ" and "Rs_1 = 20mΩ, Rs_2 = 20mΩ" configurations.	0:1
<8>	Adapter OVP	0 = Enable the adapter OVP function. 1 = Disable the adapter OVP function. If the adapter OVP function is enabled, the ISL95520 turns off ASGATE and pulls down ACOK when ACIN > 3.5V.	0
<9>	PSYS Current Gain	For "Rs_1 = 10mΩ, Rs_2 = 5mΩ" and "Rs_1 = 10mΩ, Rs_2 = 10mΩ" configuration: 0 = 1.14µA/W 1 = 0.285µA/W For "Rs_1 = 20mΩ, Rs_2 = 10mΩ" and "Rs_1 = 20mΩ, Rs_2 = 20mΩ" configuration: 0 = 2.28µA/W 1 = 0.57µA/W	0
<10>	ACLIM Inrush Current Limit Time	0 = Set soft-start ACLIM in-rush current limit period as 1ms when adapter is plugged in. 1 = Set soft-start ACLIM in-rush current limit period as 4ms when adapter is plugged in.	0
<11>	BGATE OFF Timing	Bit<11> is valid for the HPB configuration only. It changes the BGATE FET turning off timing when the adapter is plugged in. 0 = Turn OFF BGATE FET according to battery voltage (see "Soft-Start" on page 38 for details). 1 = Turn OFF BGATE FET before turning on ASGATE FETs.	0
<13>	ACLIM Function	Bit<13> configures ACLIM to be functional all the time or only during ASGATE turning on procedure to limit the inrush current. 0 = ACLIM function is ON all the time. 1 = ACLIM function is OFF after ACOK assertion.	0
<15:14>	DCM LGATE Turning OFF Timing	Bit<15:14> adjusts the LGATE turning OFF timing when the buck switcher is in DCM operation to minimize the MOSFET's body diode conduction time. By default, LGATE turns OFF when the inductor current is positive (from PHASE node to output). 00 = Earliest LGATE turning OFF when PHASE pin voltage is about -6mV. 01 = Earlier LGATE turning OFF when PHASE pin voltage is about -4mV. 10 = Early LGATE turning OFF when PHASE pin voltage is about -2mV. 11 = Late LGATE turning OFF when PHASE pin voltage is about 0mV.	00

Information Registers

To read the information register, write a 16-bit Information1 command (0X46H or 0b01000110) or Information2 command (0X45H or 0b01000101) using the Read-Word protocol shown in Figure 30 and the data format shown in Tables 15 and 16 respectively.

TABLE 15. INFORMATION1 REGISTER 0x46H

BIT	BIT NAME	W/R	DESCRIPTION
<0>	Adapter Present	R	0 = The adapter is not present. 1 = The adapter is present.
<1>	ASGATE ON	R	0 = ASGATE is OFF. 1 = ASGATE is ON.
<2>	VBAT<MinChargeVoltage	R	0 = VBAT > MinChargeVoltage. 1 = VBAT < MinChargeVoltage. Valid only when Information1 register Bit<8> = 1.
<3>	VSYS<Low System Voltage Setting	R	0 = VSYS > Low System Voltage Setting programmed by Control1 register bit<9:8>. 1 = VSYS < Low System Voltage Setting programmed by Control1 register bit<9:8>. Valid only when Information1 register bit<8> = 1.
<4>	NTC_PROCHOT#	R	0 = NTC_PROCHOT# is not asserted. 1 = NTC_PROCHOT# is asserted. Valid only when Information1 register Bit<8> = 1.
<5>	In trickle charge mode	R	0 = Not in trickle charge mode. 1 = In trickle charge mode. Bit<5> is valid for NVDC configuration only.
<6>	In Turbo/Boost mode	R	0 = Not in Turbo/Boost mode. 1 = In Turbo/Boost mode. For the NVDC configuration, if BGATE is already ON before entering turbo mode, BGATE stays ON after entering Turbo mode; Bit<6> does not indicate Turbo mode in this case.
<7>	ACProchot	R	0 = ACProchot# is not asserted. 1 = ACProchot# is asserted.
<8>	Reference Active	R	0 = Reference is not active. 1 = Reference is active. When Bit<8> = 1, Information Register Bits <4:2> are valid. When the adapter is present, the internal comparator reference is always active; unless it is in Standby mode for HPB charger configuration. In Battery Only mode, the default internal reference is not active, unless PSYS or NTC are enabled.

TABLE 16. INFORMATION2 REGISTER 0x45H

BIT	BIT NAME	W/R	DESCRIPTION	POR STATE
<0> <8>	Rs1	W/R	If Rs_1 = 20mΩ (Rs_1 = 20mΩ and Rs_2 = 10mΩ or Rs_1 = 20mΩ and Rs_2 = 20mΩ), both Bit<8> and Bit<0> need to be programmed as 1 to have correct internal current sensing scaling. Bit<8>:<0>: <0>:<0> = Rs_1 = 10mΩ <0>:<1> = Rs_1 = 10mΩ <1>:<0> = Rs_1 = 10mΩ <1>:<1> = Rs_1 = 20mΩ	0:0
<3:1>			Not used. Internally hard wired as <3:1>=010.	
<5:4>	Cell number	R	00 = Not available 01 = 2-cell 10 = 3-cell 11 = 4-cell	
<6>	Current sensing resistor	R	0 = "Rs_1:Rs_2 = 2:1" (Rs_1 = 10mΩ and Rs_2 = 5mΩ or Rs_1 = 20mΩ and Rs_2 = 10mΩ) 1 = "Rs_1:Rs_2 = 1:1" (Rs_1 = 10mΩ and Rs_2 = 10mΩ or Rs_1 = 20mΩ and Rs_2 = 20mΩ) Together with the Bit<8> and Bit<0> Rs_1 setting, it can be figured out that Rs_1 = 10mΩ or Rs_1 = 20mΩ.	
<7>	Charger Configuration	R	0 = HPB charger configuration 1 = NVDC charger configuration	
<15:9>			Not used.	

Application Information

R3™ Modulator

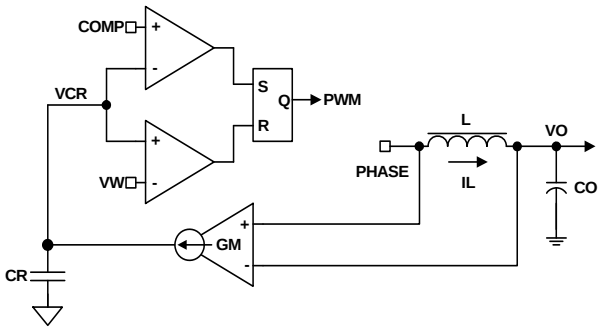


FIGURE 31. R3 MODULATOR

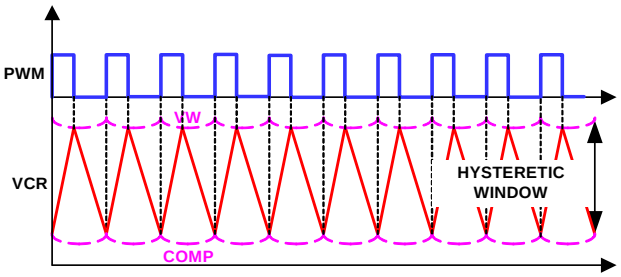


FIGURE 32. R3 MODULATOR OPERATION PRINCIPLES IN STEADY STATE

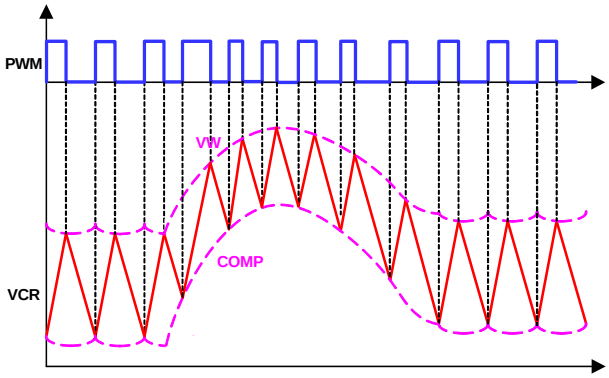


FIGURE 33. R3 MODULATOR OPERATION PRINCIPLES IN DYNAMIC RESPONSE

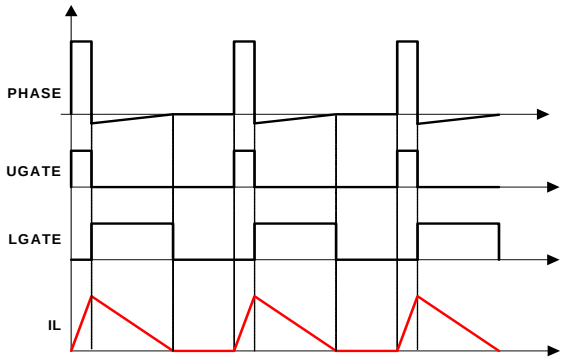


FIGURE 34. DIODE EMULATION

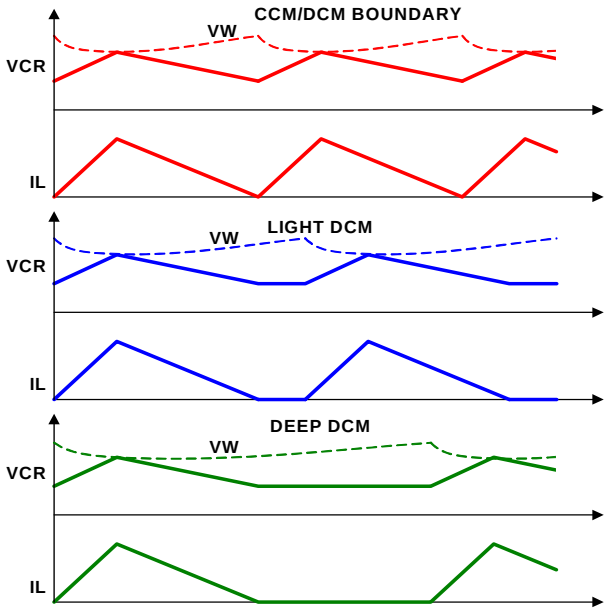


FIGURE 35. PERIOD STRETCHING

The ISL95520 uses the Renesas patented R3 (Robust Ripple Regulator) modulation scheme. The R3 modulator combines the best features of fixed frequency PWM and hysteric PWM while eliminating many of their shortcomings. Figure 31 conceptually shows the R3 modulator circuit and Figure 32 shows the operation principles in steady state.

There is a fixed voltage window called the VW window between VW and COMP. The modulator charges the ripple capacitor C_r with a current source equal to $g_m(V_{IN} - V_o)$ during PWM on-time and discharges the ripple capacitor C_r with a current source equal to $g_m V_o$, during PWM off-time, where g_m is a gain factor. The C_r voltage V_{cr} therefore emulates the inductor current waveform. The modulator turns off the PWM pulse when V_{cr} reaches VW and turns on the PWM pulse when it reaches COMP.

Because the modulator works with V_{cr}, which is large amplitude and noise free synthesized signal, it achieves lower phase jitter than conventional hysteretic mode modulators.

Figure 33 shows the operation principles during dynamic response. The COMP voltage rises during dynamic response, turning on PWM pulses earlier and more frequently temporarily, which allows for higher control loop bandwidth than conventional fixed frequency PWM modulators at the same steady state switching frequency.

The R3 modulator can operate in Diode Emulation (DE) mode to increase light load efficiency. In DE mode, the low-side MOSFET conducts when the current is flowing from source-to-drain and does not allow reverse current, therefore emulating a diode. As shown in Figure 34, when LGATE is on, the low-side MOSFET carries current, which creates negative voltage on the phase node due to the voltage drop across the ON-resistance. The IC monitors the current by monitoring the phase node voltage. It turns off LGATE when the phase node voltage reaches zero to prevent the inductor current from reversing the direction and creating unnecessary power loss.

If the load current is light enough, as Figure 34 shows, the inductor current reaches zero and stays there before the next phase node pulse, and the regulator is in Discontinuous Conduction Mode (DCM). If the load current is heavy enough, the inductor current never reaches 0A and the regulator is in CCM although the controller is in DE mode.

In DCM operation, to turn off LGATE when inductor current reaches near zero, the ISL95520 provides Control2 register Bits<15:14> to adjust the LGATE turning off timing. The default timing purposely turns off LGATE slightly earlier than the inductor current zero crossing. The SMBus bit can adjust the timing more aggressively towards the precise zero-crossing point to minimize the MOSFET's body diode conduction time for higher efficiency at light load. However, do not turn off LGATE after the inductor current zero crossing, because this may feed energy back to the adapter side.

Figure 35 shows the operation principle in DE mode at light load. The load gets incrementally lighter in the three cases from top to bottom. The PWM on-time is determined by the VW window size, and therefore is the same, so the inductor current triangle is the same in the three cases. The R3 modulator clamps the ripple capacitor voltage V_{cr} in DE mode to make it mimic the inductor current. The COMP voltage takes longer to reach V_{crs}, which naturally stretches the switching period. The inductor current triangles move farther apart from each other so that the inductor current average value is equal to the load current. The reduced switching frequency helps increase light load efficiency.

Programming Charger Options

TABLE 17. PROG PIN PROGRAMING OPTIONS

PROG-GND RESISTANCE (kΩ) TYP (1% STANDARD RESISTOR)	CHARGER TYPE	CURRENT SENSE RESISTOR VALUE	DEFAULT # OF BATTERY CELLS IN SERIES
0	NVDC	Rs_1:Rs_2 = 2:1 Rs_1 = 10mΩ Rs_2 = 5mΩ or Rs_1 = 20mΩ Rs_2 = 10mΩ	3
22.6			4
38.3			2
69.8		Rs_1:Rs_2 = 1:1 Rs_1 = 10mΩ Rs_2 = 10mΩ or Rs_1 = 20mΩ Rs_2 = 20mΩ	3
86.6			4
102			2
150	HPB		4
165			2
182			3
215		Rs_1:Rs_2 = 2:1 Rs_1 = 10mΩ Rs_2 = 5mΩ or Rs_1 = 20mΩ Rs_2 = 10mΩ	4
237			2
255			3

The resistor from the PROG pin to GND programs the configuration of the ISL95520 as an HPB charger or NVDC charger, as well as the default number of battery cells in series and the default values of the adapter and battery current sense resistors Rs_1 and Rs_2. Table 17 shows the programming options.

Before soft-start and when V_{DD} voltage reaches its POR value, the ISL95520 sources 10µA current out of the PROG pin and reads the PROG pin voltage to determine the resistor value. However, application environmental noise may pollute the PROG pin voltage and cause incorrect readings. If noise is a concern, connect a capacitor from the PROG pin to GND to provide filtering. The resistor and the capacitor RC time constant should be less than 40µs, so the PROG pin voltage can rise to steady state before the ISL95520 reads it.

The ISL95520 can be programmed in two different battery charger configurations.

Figure 1 on page 1 shows the typical application circuit for a HPB charger. In this configuration, the ISL95520 connects the system voltage rail to either the adapter or the battery. In Turbo events, which means the system is drawing more power than the adapter's power rating, the ISL95520 operates as a boost converter to reverse-boost the battery energy to the system voltage rail, so the battery works with the adapter together to supply the system power.

Figure 5 on page 6 shows the typical application circuit for the NVDC charger. In this configuration, the ISL95520 connects the system voltage rail to either the output of the buck switcher or the battery. In Turbo events, the ISL95520 turns on the BGATE to discharge the battery so the battery works with the adapter together to supply the system power.

The PROG pin resistor programs the ratio of the current sensing resistor values Rs_1 and Rs_2 as 2:1 or 1:1. Therefore, four sets of Rs_1 and Rs_2 current sensing resistor values can be used:

- Rs_1 = 10mΩ, Rs_2 = 5mΩ
- Rs_1 = 10mΩ, Rs_2 = 10mΩ
- Rs_1 = 20mΩ, Rs_2 = 10mΩ
- Rs_1 = 20mΩ, Rs_2 = 20mΩ

If 20mΩ Rs_1 is used, the SMBus Information2 register Bit<0> and Bit<8> both need to be set as 1 for the appropriate internal current sensing scaling.

Smaller current sense resistor values reduce the power loss, while larger current sense resistor values give better accuracy.

The PROG pin resistor configures the internal current sense gain automatically for different Rs_1 and Rs_2, so that the SMBus command keeps same for 20mΩ or 10mΩ Rs_1 and for 10mΩ or 5mΩ Rs_2, that is, the AdapterCurrentLimit1 register, AdapterCurrentLimit2 register, and ACProchot register can be programmed with the same SMBus command value, regardless of whether Rs_1 is 20mΩ or 10mΩ, to obtain the same current; the ChargeCurrent register, DischargeCurrent register, and DCProchot register can be programmed with the same SMBus command value, regardless of whether Rs_2 is 10mΩ or 5mΩ, to obtain the same current. Using any option results in a 1mA/LSB correlation in the SMBus commands.

If the Rs_1 and Rs_2 values are different from the PROG pin programming table, the SMBus command needs to be scaled accordingly to obtain the correct current.

Upon POR, the ISL95520 uses the default number of cells in series as Table 17 shows and sets the default MaxChargeVoltage register value and default MinChargeVoltage register value accordingly. When SMBus communication is established, the SMBus can program a different number of battery cells in series through SMBus Control1 register Bit<14:13>.

Tables 18 and 19 show the adapter current and battery current related settings according to different Rs_1 and Rs_2 options.

TABLE 18. CURRENT SENSING RESISTOR CONFIGURATIONS

CURRENT SENSING RESISTORS		REGISTERS			K_{PSYS} (µA/W)	
		CHARGECURRENT	DISCHARGECURRENT* DCPROCHOT**	ADAPTERCURRENTLIMIT1* ADAPTERCURRENTLIMIT2* ACPROCHOT**	CONTROL2 Bit<9> = 0	CONTROL2 Bit<9> = 1
1	Rs_1 = 10m0h Rs_2 = 5mΩ	Bit<12:5> Max = 1FE0h, 8.160A Min = 0020h, 32mA Default = 0000h, 0A	Bit<13:8> Max = 3F00h, 16.128A Min = 0100h, 256mA *Default = 3F00h, 16.128A **Default = 2000h, 8.192A	Bit<12:7> Max = 1F80h, 8.064A Min = 0080h, 128mA *Default = 1F80h, 8.064A **Default = 1800h, 6.144A	1.14	0.285
2	Rs_1 = 10m0h Rs_2 = 10mΩ	Bit<12:5> Max = 1FE0h, 8.160A Min = 0020h, 32mA Default = 0000h, 0A	Bit<12:7> Max = 1F80h, 8.064A Min = 0080h, 128mA *Default = 1F80h, 8.064A **Default = 1000h, 4.096A	Bit<12:7> Max = 1F80h, 8.064A Min = 0080h, 128mA *Default = 1F80h, 8.064A **Default = 1800h, 6.144A	1.14	0.285
3	Rs_1 = 20m0h Rs_2 = 10mΩ	Bit<11:4> Max = 0FF0, 4.080A Min = 0010, 16mA Default = 0000h, 0A	Bit<12:7> Max = 1F80h, 8.064A Min = 0080h, 128mA *Default = 1F80h, 8.064A **Default = 1000h, 4.096A	Bit<11:6> Max = 0FC0h, 4.032A Min = 0040h, 64mA *Default = 0FC0h, 4.032A **Default = 0C00h, 3.072A	2.28	0.57
4	Rs_1 = 20m0h Rs_2 = 20mΩ	Bit<11:4> Max = 0FF0, 4.080A Min = 0010, 16mA Default = 0000h, 0A	Bit<11:6> Max = 0FC0h, 4.032A Min = 0040h, 64mA *Default = 0FC0h, 4.032A **Default = 0800h, 2.048A	Bit<11:6> Max = 0FC0h, 4.032A Min = 0040h, 64mA *Default = 0FC0h, 4.032A **Default = 0C00h, 3.072A	2.28	0.57

TABLE 19. CURRENT SENSING RESISTOR CONFIGURATIONS

CURRENT SENSING RESISTORS		ADAPTER CURRENT LIMITED BY ACLIM	CHARGING CURRENT LIMITED BY CCLIM	TRICKLE CHARGE		NVDC PRE-CHARGE PERIOD CURRENT LIMIT	HPB t1~t2 PERIOD CURRENT LIMIT	AMON	BMON
				128mA	256mA				
1	Rs_1 = 10moh Rs_2 = 5mΩ	$V_{ACLIM}/(32*Rs_1)$	$V_{CCLIM}/(64*Rs_2)$	128	256	256mA	625mA	$32*Rs_1*Iadp$	$32*Rs_2*Ibat$
2	Rs_1 = 10moh Rs_2 = 10mΩ	$V_{ACLIM}/(32*Rs_1)$	$V_{CCLIM}/(32*Rs_2)$	128	256	256mA	625mA	$32*Rs_1*Iadp$	$32*Rs_2*Ibat$
3	Rs_1 = 20moh Rs_2 = 10mΩ	$V_{ACLIM}/(32*Rs_1)$	$V_{CCLIM}/(64*Rs_2)$	128	256	128mA	312.5mA	$32*Rs_1*Iadp$	$32*Rs_2*Ibat$
4	Rs_1 = 20moh Rs_2 = 20mΩ	$V_{ACLIM}/(32*Rs_1)$	$V_{CCLIM}/(32*Rs_2)$	128	256	128mA	312.5mA	$32*Rs_1*Iadp$	$32*Rs_2*Ibat$

Programming Switching Frequency

TABLE 20. DEFAULT CCM SWITCHING FREQUENCY OPTIONS

FSET-GND RESISTANCE (kΩ)	SWITCHING FREQUENCY (kHz)	
TYP. (1% STANDARD RESISTOR)	TYP (±15%)	4-CELL WITH PERIOD STRETCH
0	992	500
22.6	838	430
38.3	729	375
54.9	642	335
69.8	678	460
86.6	614	420
102	561	390
118	517	360
133	513	420
150	477	390
165	449	370
182	421	350
200	417	360
215	395	340
237	375	330
255	350	310

The resistor from the FSET pin to GND programs the default CCM switching frequency, as shown in Table 20. Before soft-start, the ISL95520 sources 10µA current out of the FSET pin and reads the FSET pin voltage to determine the resistor value. However, application environmental noise may pollute the FSET pin voltage and cause incorrect readings. If noise is a concern, connect a capacitor from the FSET pin to GND to provide filtering. The resistor and the capacitor RC time constant should be less than 40µs, so the FSET pin voltage can rise to steady state before the ISL95520 reads it.

In DE mode, the ISL95520 uses a phase comparator to monitor the PHASE node voltage during low-side switching FET on-time to detect the inductor current zero crossing. The phase comparator needs a minimum on-time of the low-side switching FET for it to recognize inductor current zero crossing. If the low-side switching FET on-time is too short for the phase comparator to successfully recognize the inductor zero crossing, the ISL95520 may lose diode emulation ability. To prevent this scenario, the ISL95520 uses a minimum low-side switching FET on-time. When the intended low-side switching FET on-time is shorter than the minimum value, the ISL95520 stretches the switching period to keep the low-side switching FET on-time at the minimum value, which causes the CCM switching frequency to drop below the set point. This effect is only pronounced in applications using 4-cell battery and high switching frequency setting.

The switching frequency can be changed through SMBus Control2 register Bit<3:0> after POR. See Table 14 (SMBus Control2 register programming table) for a detailed description.

Soft-Start

When the DCIN pin voltage is higher than 5V, an internal LDO starts to regulate and output 5V on the VDDP pin, which is the power supply for the gate drives.

The VDD pin is the 5V power supply for the ISL95520 control circuitry. Renesas recommends using an R-C filter to generate the VDD pin voltage from the VDDP pin voltage. When the VDD pin voltage exceeds its POR, the ISL95520 sources 10µA current out of the PROG pin and reads the pin voltage to determine the PROG resistor value; it then sources 10µA current out of the FSET pin and reads the pin voltage to determine the FSET resistor value. The PROG resistor and the FSET resistor values program the ISL95520 configurations.

Soft-start begins when the VDD pin voltage exceeds its POR, the ACIN pin voltage exceeds 2.63V, the DCIN pin voltage is higher than the VBAT pin voltage, and after the 1.3s or 163ms delay set by Control2 register Bit<5>.

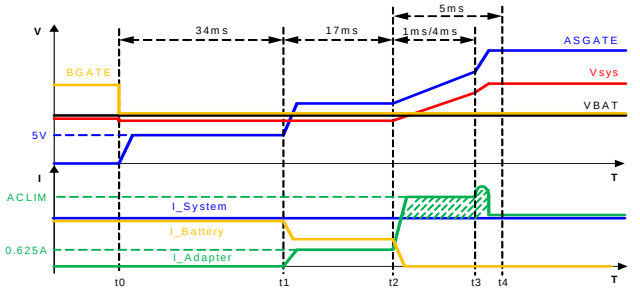


FIGURE 36. SOFT-START WITH VBAT < 4.5V or VBAT > 7

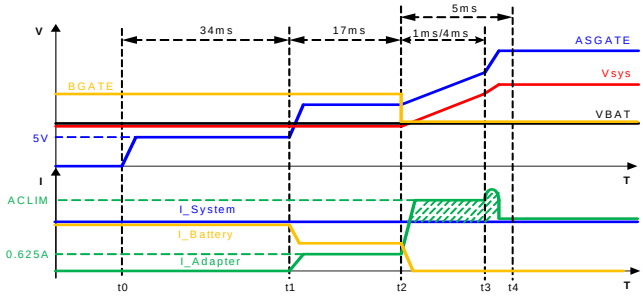


FIGURE 37. SOFT-START WITH 4.5V < VBAT < 7V

During soft-start, in both the HPB charger and NVDC charger configurations, the ISL95520 limits the adapter current in several steps. Figure 36 shows that the ISL95520 outputs 20µA current source at t0 to charge the ASGATE pin voltage to 5V and holds the ASGATE pin voltage at 5V for 34ms until t1. From t1 to t2, the ISL95520 limits the adapter current at 0.625A (Rs_1 = 10mΩ) for 17ms. From t2 to t3, the ISL95520 limits the adapter current at the value set by the ACLIM pin voltage for the next 1ms (default, a 4ms option is available through SMBus Control2 register Bit<10>). From t3 to t4, the ISL95520 outputs 20µA for another 4ms (or 1ms) to fully turn on ASGATE without actively limiting the adapter current. ACOK is asserted high after ASGATE is fully turned on. The stepped soft-start scheme carefully biases up the system and protects the back-to-back ASGATE FETs against potential damage caused by the inrush current.

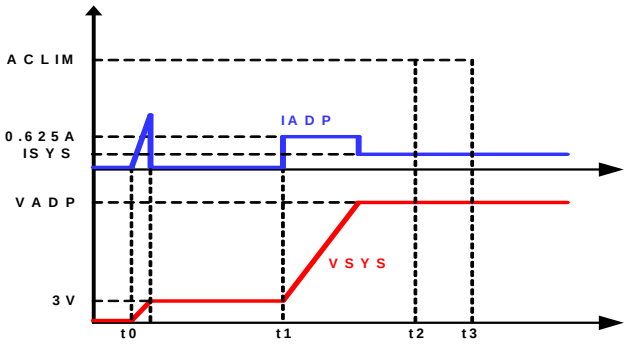


FIGURE 38. NO BATTERY SOFT-START WITH ISYS < 0.625A

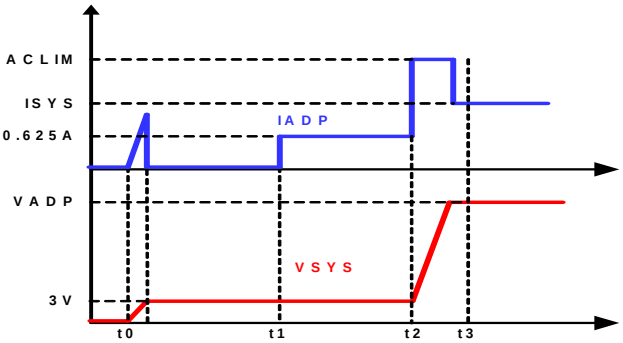


FIGURE 39. NO BATTERY SOFT-START WITH 0.625A < ISYS < ACLIM

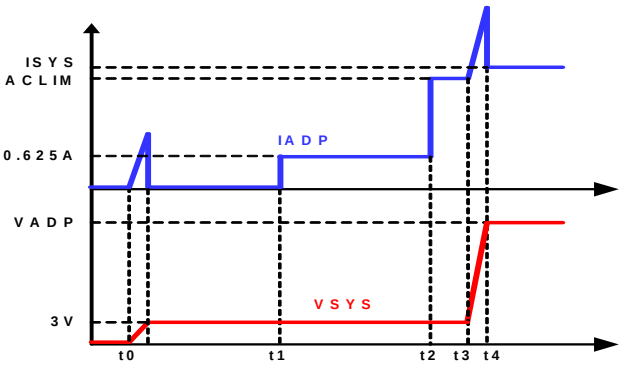


FIGURE 40. NO BATTERY SOFT-START WITH ISYS > ACLIM

Figure 38 shows the HPB configuration without a battery soft-start waveform when the system load is less than 0.625A. During t1 through t2, the ISL95520 charges the system bus capacitor with (0.625A - system load) current and reaches the adapter voltage level by t2. There is no inrush current after t2.

Figure 39 shows the HPB configuration without a battery soft-start waveform when the system load is greater than 0.625A but less than the ACLIM-set current level. During t1 through t2, the system bus voltage stays at 3V because there is not enough current to overcome the load-to-charge the system bus capacitors. During t2 through t3, the ISL95520 charges the system bus capacitor with (ACLIM - system load) current and reaches the adapter voltage by t3. There is no inrush current after t3.

Figure 40 shows the HPB configuration without a battery soft-start waveform when the system load is greater than the ACLIM-set current level, which is not a recommended mode of operation. During t1 through t3, the system bus voltage stays at 3V because there is not enough current to overcome the load to charge the system bus capacitors. During t3 through t4, the ISL95520 fully turns on the ASGATE and lets the adapter charge the system bus capacitor without current limit.

In the HPB charger configuration, the ISL95520 can determine when to turn off the BGATE MOSFET to prevent system voltage disturbance. The BGATE MOSFET turns off at t0 before ASGATE ramps up if VBAT < 4.5V or VBAT > 7V as shown in Figure 37 and remains on until t2 if 4.5V < VBAT< 7V as shown in Figure 37. This scheme prevents the system bus voltage from dropping by the MOSFET body-diode voltage drop caused by BGATE MOSFET turning off early. There is a period of time when BGATE and ASGATE are both on, during which a maximum 0.625A (Rs_1 = 10mΩ) current flows into the battery if the system load current is zero. This current flow does not pose any danger to the battery. However, if this scheme is not wanted, Control2 register Bit<11> can turn off BGATE before ASGATE ramps up regardless of the battery voltage.

In the NVDC charger configuration, after fully turning on ASGATE, the ISL95520 starts the switcher. If VBAT > 3.5V, the BGATE MOSFET remains on for about 28ms after the buck regulator starts switching to prevent the system bus from dropping by a MOSFET body-diode voltage drop caused by the BGATE MOSFET turning off early. This 28ms switching is called pre-charging switching. During the 28ms, the current that flows into the battery is controlled at 256mA or 128mA based on the current sensing resistor configuration (see Table 19). If VBAT < 3.5V, the BGATE MOSFET turns off before the 28ms pre-charging switching to avoid charging current to the depleted battery. The ACOK signal is asserted high after the pre-charging switching period.

Adapter Presence Detection and ACOK

ACOK is an open-drain output pin indicating the presence of the adapter and readiness of the adapter to supply power to the system bus. The ISL95520 actively pulls ACOK low in the absence of the adapter.

Use a voltage divider from the adapter voltage to set the ACIN pin voltage. The ISL95520 monitors the ACIN pin voltage to determine the presence of the adapter. When the ACIN pin voltage exceeds 2.63V, the DCIN pin voltage is higher than the VBAT pin voltage, and ASGATE is fully turned on, the ISL95520 allows the external circuit to pull-up the ACOK pin. For the NVDC configuration, the ISL95520 allows the external circuit to pull-up the ACOK pin after the pre-charging switching period.

For the buck converter to work properly to charge the battery, select the ACIN pin voltage divider such that the minimum adapter voltage set by the ACIN pin voltage divider is higher than the maximum battery voltage. There is a delay between the ACIN pin voltage rising above 2.63V and ASGATE starting to turn on. The default value of the delay is 1.3s. The delay can be changed to 163ms through SMBus Control2 register Bit<5>.

Adapter Overvoltage Protection

If the ACIN voltage exceeds 3.5V, an adapter overvoltage condition occurs. The ISL95520 turns off the ASGATE MOSFETs to isolate the adapter from the system and deasserts the ACOK signal by pulling it low.

The adapter OVP function can be disabled through the SMBus Control2 register Bit<8>.

Power Source Selection

The ISL95520 automatically selects the adapter and/or the battery as the source for system power.

The BGATE pin drives an NFET that connects/disconnects the battery from the system and the switcher.

The ASGATE pin drives a pair of back-to-back common source NFETs to connect/disconnect the adapter from the system and the battery.

If the adapter is present, the ISL95520 turns on ASGATE to connect the adapter to the system. In the HPB charger configuration, the ISL95520 also turns off BGATE to disconnect the battery from the system when it turns on ASGATE.

If the adapter is absent, the ISL95520 turns off ASGATE and turns on BGATE to connect the battery to the system. If the system bus voltage is higher than the battery voltage, the ISL95520 waits until the system bus voltage decays to the battery voltage before turning on BGATE to avoid inrush current into the battery.

Battery Learn Mode

The ISL95520 enters Battery Learn mode when it receives the SMBus Control command (see Table 13), or when the PROG pin voltage is externally pulled to 5V after POR. It is not possible to pull-up the PROG pin to 5V if the PROG pin to GND resistor value is 0Ω. The ISL95520 exits Battery Learn mode when it receives the SMBus control command as Table 13 shows, or when the PROG pin voltage is no longer pulled to 5V.

HPB Charger Battery Learn Mode Entry/Exit

In HPB charger configuration Battery Learn mode, the ISL95520 turns off ASGATE and turns on BGATE regardless of whether the adapter is present. This mode of operation is used to supply the system power from the battery even when the adapter is plugged in, such as calibration of the battery fuel gauge, hence the name “Battery Learn mode”. The Information1 register Bit<1> indicates ASGATE on or off.

Upon entering Battery Learn mode, the ISL95520 only turns on BGATE when the system bus voltage decays to battery voltage to avoid inrush current from the system bus to battery.

The three ways of exiting HPB charger configuration Battery Learn mode are:

1. Receive the battery learn mode exit command through SMBus.
2. The PROG pin voltage drops below 5V.
3. The BATGONE pin voltage goes from logic low-to-high.

In cases 1 and 2, after the ASGATE turn on delay of 1.3s or 163ms set by Control2 register Bit<5>, the ISL95520 goes through the soft-start process to turn on ASGATE and turn off BGATE as described in “Soft-Start” on page 38.

In case 3, the ISL95520 uses its maximum gate drive strength to turn on ASGATE quickly to prevent system voltage collapse. This action can be completed within ~35µs after the BATGONE pin voltage level goes to logic high. If the soft-start process is still preferred in this case, use SMBus Control1 register Bit<7> to configure the preference.

NVDC Charger Battery Learn Mode Entry/Exit

In NVDC charger configuration Battery Learn mode, the ISL95520 turns on BGATE and keeps ASGATE on, but turns off the switcher regardless of whether the adapter is present.

Upon entering battery learn mode, the ISL95520 only turns on BGATE when the system bus voltage decays to the battery voltage to avoid inrush current from system bus to battery.

The three ways of exiting NVDC charger configuration battery learn mode are the same as for HPB charger configuration Battery Learn mode:

1. Receive battery learn mode exit command through SMBus
2. The PROG pin voltage drops below 5V
3. BATGONE pin voltage goes from logic low-tµo-high

In all these cases, the ISL95520 resumes switching immediately to supply power to the system bus from the adapter to prevent system voltage collapse.

In the NVDC charger configuration, Battery Learn mode can only be enabled when both the PSYS (Control1 register Bit<4>) and NTC (Control1 register Bit<6>) functions are disabled.

Hardware-Based Charging Current Limit

The CCLIM pin voltage sets the hardware-based charging current limit to provide an extra level of protection in the unlikely event of SMBus communication failure or an errant command.

Equation 1 gives the relationship between the CCLIM pin voltage and the hardware-based charging current limit, where $V_{CCLIMHW}$ is the CCLIM pin voltage in Volts and $I_{CCLIMHW}$ is the hardware-based charging current limit in Amperes.

$$I_{CCLIMHW} = \frac{V_{CCLIMHW}}{64 \times Rs2} \quad \text{(EQ. 1)}$$

Equation 1 is true for Rs_1:Rs_2 = 2:1 (Rs_1 = 10mΩ and Rs_2 = 5mΩ or Rs_1 = 20mΩ and Rs_2 = 10mΩ).

$$I_{CCLIMHW} = \frac{V_{CCLIMHW}}{32 \times Rs2} \quad \text{(EQ. 2)}$$

Equation 2 is true for Rs_1:Rs_2 = 1:1 (Rs_1 = 10mΩ and Rs_2 = 10mΩ or Rs_1 = 20mΩ and Rs_2 = 20mΩ).

The ISL95520 uses the lower value of the hardware-set charging current limit and the SMBus programmed charging current limit as the actual charging current limit.

Hardware-Based Adapter Current Limit

The ACLIM pin voltage-set, hardware-based adapter current limit provides an extra level of protection in the unlikely event of SMBus communication failure.

Equation 3 gives the relationship between the ACLIM pin voltage and the hardware-based adapter current limit, where $V_{ACLIMHW}$

is ACLIM pin voltage in Volts and $I_{ACLIMHW}$ is the hardware-based adapter current limit in Amperes.

$$I_{ACLIMHW} = \frac{V_{ACLIMHW}}{32 \times Rs1} \quad \text{(EQ. 3)}$$

Equation 3 is true for all current sensing resistor configurations.

The ISL95520 uses the lower value of the hardware-set adapter current limit and the SMBus programmed adapter current limit as the actual adapter current limit.

The ACLIM pin voltage also sets the ASGATE soft-start current limit level from t2 to t3.

Cycle-By-Cycle Current Limit

The ISL95520 provides a cycle-by-cycle adapter current limit function. When the cycle-by-cycle adapter current limit function is enabled through SMBus Control1 register Bit<11>, the ISL95520 turns off the high-side switching FET when the adapter current peak value reaches the hardware-based adapter current limit set by the ACLIM pin voltage. The cycle-by-cycle adapter current limit function is applicable only when the switcher is in Buck mode.

The cycle-by-cycle current limit function is based on the peak value of the adapter current. The SMBus programmed adapter current limit is based on the average value.

Renesas recommends setting the hardware-based adapter current limit above the SMBus programmed adapter current limit so that the adapter current peak value does not trigger the cycle-by-cycle current limit in normal operation.

The ACLIM current limit function, including the cycle-by-cycle adapter current limit function, can be disabled through SMBus Control2 register Bit<13> after ACOK assertion, so that the ACLIM pin is used only for the ASGATE soft-start current limit from t2 to t3 as shown in "Soft-Start" on page 38.

The ISL95520 also provides the cycle-by-cycle battery discharging current limit function for the HPB charger configuration. When the ISL95520 is in Turbo-Boost mode as described in "HPB Charger Turbo Mode Support", the battery discharges current through the reverse boost switcher as supplemental power of the adapter to support the system load. The ISL95520 monitors the average battery discharging current by sensing the CSON-CSOP voltage. Whenever the average battery discharging current reaches the DischargeCurrentLimit register set value, it turns off the low-side switching FET to limit the battery discharging current. Because the battery supplemental power to the system bus is limited in this cycle-by-cycle battery discharging current limit scenario, the adapter current could exceed the adapter current limit setting and the adapter could be overloaded.

HPB Charger Turbo Mode Support

Turbo mode refers to the scenario when the system draws more power than the adapter's power rating. Turbo mode prompts the need for the switcher to change from Forward Buck operation mode to Reverse Boost mode to reverse the energy flow. This mode of operation enables the battery to help the adapter provide the required system power. This operation is widely used in many systems, such as "sun mode" and "eclipse mode" for bidirectional battery charger/discharger used on satellites with solar panels as the power source acting as the adapter. For more information, see "A zero voltage switching bidirectional battery charger/discharger for the NASA EOS Satellite", Dan M. Sable, Fred C.Lee and Bo H. Cho, APEC 1992 Conference Proceedings.

In the HPB charger configuration, the ISL95520 normally operates the switcher as a synchronous buck converter with diode emulation. When the buck converter is in a light load condition, it enters DCM operation with reduced switching frequency to increase efficiency. From the description of the R3 modulator operational principle, the COMP pin voltage is lower at lighter loads and may reach the low clamp.

In Turbo mode, the ISL95520 operates the switcher in Reverse-Boost mode to boost energy from the battery to the adapter voltage rail, so that the adapter current is limited at the adapter current limit set point while the battery supplies the additional power required by the system.

Control1 register Bit<10> enables/disables the Turbo/Boost function. See Table 13 for details.

The ISL95520 enters Turbo mode when all of the following three criteria are met:

1. Adapter current is within 80mA of the AdapterCurrentLimit1 (or AdapterCurrentLimit2 if the two level adapter current limit function is enabled) register setting.
2. The battery charging current is less than 150mA.
3. The COMP pin voltage is lower than 1.4V.

Meeting these three criteria means that the ISL95520 only enters Turbo mode precisely when it is absolutely necessary. For example, assume the adapter voltage is 20V, the adapter current limit is 4A (80W rating), and the ISL95520 is charging an 8V battery at 5A rate (40W charging power). If the system load increases from 0W to 79W instantaneously, the adapter current increases from 2A to 5.95A instantaneously and exceeds the 4A current limit level. However, the adapter current loop takes control and decreases the charging current order to limit the adapter current at 4A, and eventually provides 79W system power and 1W battery charging power. In this case, the ISL95520 does not need to enter Turbo mode adapter and can conserve battery energy. In the same example, if the system load increases from 0W to 81W instantaneously, the adapter current increases from 2A to 6.05A instantaneously and exceeds the 4A current limit level. The adapter current loop takes control and decreases the charging current to limit the adapter current at 4A. Therefore, the ISL95520 eventually determines that it needs to enter Turbo mode, so the adapter provides 80W and battery provides 1W to provide 81W to the system.

The interaction of the control loops within the ISL95520, including the adapter current loop, the charging current loop, and the battery full charging voltage loop, determines when the device enters Turbo mode. The timing strongly depends on the control loop compensation design and the interaction among the loops. In the previous example, compared with system power instantaneously increasing from 0W to 81W, instantaneously increasing system power from 0W to 160W causes the ISL95520 to enter Turbo mode much faster because the loops drive the circuit parameters to meet the three Turbo-mode-entry criteria much more quickly when the adapter is more severely overloaded.

The ISL95520 exits Turbo mode when one of the following three criteria are met:

1. Battery charging current exceeds 150mA (Rs_2 = 10mΩ).
2. Adapter current is less than the AdapterCurrentLimit register setting and the COMP voltage is lower than 1.4V.
3. Battery discharging current is less than 140mA (for Rs_2 = 10mΩ) for 140ms.

When the ISL95520 enters Turbo mode, if the first few UGATE switching pulses cause the inductor current peak to temporarily increase above 150mA, the ISL95520 may mistakenly exit Turbo mode before re-entering it, which creates a “chatter” behavior. If this behavior occurs, select an appropriate time constant of the battery current sense filter, such as 20µs RC value, to filter out the peaking of the inductor current information seen by the ISL95520. Excessively large filter time constants may result in slower loop response and affect system dynamic response, such as Turbo mode entry speed.

If the average battery discharging current reaches the DischargeCurrentLimit register set value, the ISL95520 limits the battery discharging current at the DischargeCurrentLimit register set value by turning off the low-side switching FET even if the adapter current exceeds the adapter current limit setting.

Table 21 shows the ISL95520 HPB configuration charge function and Turbo/boost function control truth table.

TABLE 21. HPB CHARGER BEHAVIOR TRUTH TABLE

TURBO/BOOST MODE CONTROL BIT	ENABLECHARGING CONTROL BIT	CHARGECURRENT REGISTER		
0 = ENABLE BOOST 1 = DISABLE BOOST	0 = DISABLE CHARGING 1 = ENABLE CHARGING	0 = 0A COMMAND 1 = NON ZERO VALID COMMAND	CHARGE?	BOOST?
0	0	0	NO	YES
0	0	1	NO	YES
0	1	0	NO	YES
0	1	1	YES (Fast charge and Trickle charge enabled)	YES
1	0	0	NO	NO
1	0	1	NO	NO
1	1	0	NO	NO
1	1	1	YES (Fast charge and Trickle charge enabled)	NO

TABLE 22. NVDC CHARGER BEHAVIOR TRUTH TABLE

TURBO/BOOST MODE CONTROL BIT	ENABLECHARGING CONTROL BIT	CHARGECURRENT REGISTER	BGATE ON/OFF	
0 = ENABLETURBO 1 = DISABLE TURBO	0 = DISABLE CHARGING 1 = ENABLE CHARGING	0 = 0A COMMAND 1 = NON ZERO VALID COMMAND	SYSTEM LOAD NOT IN TURBO MODE RANGE	SYSTEM LOAD IN TURBO MODE RANGE
0	0	0	OFF	ON
0	0	1	OFF	ON
0	1	0	OFF	ON
0	1	1	ON for fast charge; Trickle charge enabled	ON
1	0	0	OFF	OFF
1	0	1	OFF	OFF
1	1	0	OFF	OFF
1	1	1	ON for fast charge; Trickle charge enabled	ON

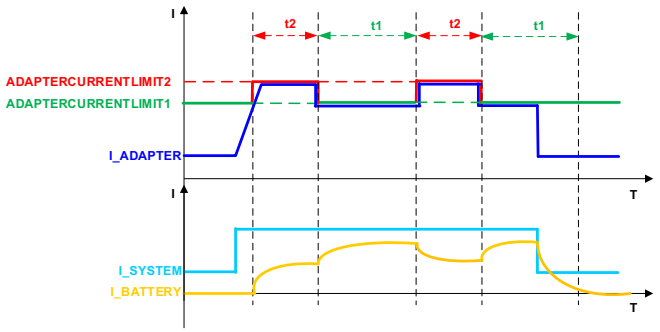


FIGURE 41. TWO LEVEL ADAPTER CURRENT LIMIT

NVDC Charger Turbo Mode Support

In the NVDC charger configuration and Turbo mode, the ISL95520 turns on the BGATE FET to limit the adapter current at the adapter current limit set point while the battery supplies the rest of the power required by the system. To turn on BGATE in Turbo mode, the CSON pin voltage needs to be 175mV lower than the VBAT pin voltage. If the ISL95520 detects 150mA charging current or if the battery discharging current is less than 140mA for 140ms, it turns off BGATE to exit Turbo mode. See Table 22 for BGATE operation.

Two-Level Adapter Current Limit

In a real system, Turbo events usually do not last very long. They are often no longer than milliseconds, a time length during which the adapter can supply current higher than its DC rating. The ISL95520 uses a two-level adapter current limit in order to fully take advantage of the adapter's surge capability and minimize the power draw from the battery.

Figure 41 shows the two SMBus-programmable adapter current limit levels, AdapterCurrentLimit1 and AdapterCurrentLimit2, as well as the durations t1 and t2. The two-level adapter current limit function is initiated when the adapter current reaches the AdapterCurrentLimit1 register setting, starts at AdapterCurrentLimit2 for duration t2, then changes to AdapterCurrentLimit1 for duration t1 before repeating the pattern. These parameters can set the adapter current limit with an envelope that allows the adapter to temporarily output surge current without requiring the charger to enter Turbo mode. This operation maximizes battery life.

The AdapterCurrentLimit1 register value can be higher or lower than the AdapterCurrentLimit2 value.

The two-level adapter current limit function can be enabled and disabled through SMBus Control2 register Bit<6>. When the two-level adapter current limit function is disabled, only the AdapterCurrentLimit1 value is used; the adapter current limit and AdapterCurrentLimit2 value are ignored.

Current Monitor

The ISL95520 provides an adapter current monitor through the AMON pin and a battery discharging current monitor through the BMON pin. The AMON pin voltage is 32x the (V_{CSIP}-V_{CSIN}) voltage and the BMON pin voltage is 32x the (V_{CSON}-V_{CSOP}) voltage.

AMON and BMON functionality can be enabled or disabled through SMBus Control1 register Bit<2> and Bit<3>, respectively, as Table 13 shows.

PSYS Monitor

The ISL95520 PSYS pin provides a measure of the instantaneous power consumption of the entire platform. The PSYS pin outputs a current source described by Equation 4.

$$I_{PSYS} = K_{PSYS} \times (V_{ADP} \times I_{ADP} + V_{BAT} \times I_{BAT}) \quad \text{(EQ. 4)}$$

K_{PSYS} is based on the current sensing resistor Rs_1 and Rs_2 configuration and is selectable through SMBus Control2 register Bit<9>. See Table 18 for details. V_{ADP} is the adapter voltage in Volts, I_{ADP} is the adapter current in Amperes, V_{BAT} is the battery voltage, and I_{BAT} is the battery discharging current. When the battery is discharging, I_{BAT} is a positive value; when the battery is being charged, I_{BAT} is a negative value. The battery voltage V_{BAT} is detected through the CSON pin to maximize the power monitor accuracy in the NVDC configuration Trickle Charge mode.

The PSYS information includes the power loss of the charger circuit and the actual power delivered to the system. Resistor R_{PSYS} connected between the PSYS pin and GND converts the PSYS information from current to voltage.

The PSYS function can be enabled or disabled through SMBus Control1 register Bit<4> as shown in Table 13.

Charger Timeout

The ISL95520 includes a timer to ensure the SMBus master is active and to prevent overcharging the battery. The ISL95520 terminates charging if the charger has not received a write to the MaxChargeVoltage or ChargeCurrent register within 175s. If a timeout occurs, the MaxChargeVoltage or ChargeCurrent register must be written to re-enable charging.

The ISL95520 allows you to disable the charger timeout function through SMBus Control1 register Bit<15> as Table 13 shows.

Trickle Charging

The ISL95520 supports trickle charge to an overly discharged battery. The ISL95520 can activate the trickle charge function when the battery voltage is lower than MinChargeVoltage setting. The VBAT pin is the battery voltage sense point for trickle charge mode.

To enable trickle charge, set the EnableCharging control bit to 1 and set the ChargeCurrent register to a valid non-zero value. To disable trickle charge, either set the EnableCharging control bit to 0 or set the ChargeCurrent register to 0. Table 21 shows the condition to enable the HPB configuration Trickle Charge mode. Table 22 shows the condition to enable the NVDC configuration Trickle Charge mode.

The trickle charging current can be programmed to be 256mA, 128mA, or 64mA through SMBus Control2 register Bit<7> and Bit<12> as shown in Table 14.

In the HPB charger configuration, the ISL95520 charges the battery at 256mA or 128mA in Trickle Charge mode.

In the NVDC charger configuration Trickle Charge mode, the ISL95520 regulates the system voltage at 450mV above the MinChargeVoltage register value. An independent control loop regulates the BGATE FET gate voltage to regulate the battery charging current at 256mA, 128mA, or 64mA.

When the battery voltage is charged to 175mV above the MinChargeVoltage register value, the ISL95520 enters Fast Charging mode by limiting the charging current at the ChargeCurrentLimit register setting.

NVDC Charger System Voltage Regulation

If the battery is absent, the ISL95520 regulates the system bus voltage at the higher value of 7.168V and the MinChargeVoltage register setting.

If the battery is present but BGATE is turned off, the ISL95520 regulates the system bus voltage at the higher value of 7.168V and the MaxChargeVoltage register setting.

The CSON pin sense the system bus voltage.

To prevent system voltage collapse when the battery is absent, the ISL95520 does not limit the adapter current if the system power draw causes the adapter current to exceed the adapter current limit. This function can be enabled or disabled through SMBus Control2 register Bit<4>.

Over-Temperature Protection

The ISL95520 turns off the internal LDO for self-protection when the junction temperature exceeds +155°C. The internal LDO stays off until the junction temperature falls below +128°C.

In the HPB charger configuration, the ISL95520 puts the charger in standby mode after declaring over-temperature protection.

In the NVDC charger configuration, the ISL95520 stops switching after declaring over-temperature protection.

When the temperature falls below 128°C, the ISL95520 enables the internal LDO and the ISL95520 resumes operation.

Battery Overvoltage Protection

The battery overvoltage protection function prevents the battery from being overcharged.

In the HPB charger configuration, the ISL95520 stops switching if the battery voltage is higher than MaxChargeVoltage register setting. If the battery voltage is higher than 4.6V/cell, it stops charging.

In the NVDC charger configuration, the ISL95520 stops switching if the system bus voltage is higher than MaxChargeVoltage register value; if the battery voltage is higher than 4.6V/cell, it turns off BGATE to stop charging.

The MaxChargeVoltage register setting should be less than 4.6V/cell.

System Bus Short Circuit Detection

If the ACIN pin is pulled below 2.63V by the system bus excessive current or short-circuit, the ISL95520 turns off ASGATE to isolate the adapter from the system bus. When the ACIN pin voltage rises above 2.63V again and after the 1.3s or 163ms delay programmed by Control2 register Bit<5>, ASGATE turns on again with soft-start.

An external circuit as shown in Figure 42 can be used to detect the system bus short-circuit. If the system bus short-circuits, the ACIN pin is pulled below 2.63V by diode D1, so ASGATE cannot turn on. While in normal operation, ASGATE can still turn on when the system bus is charged up above 2.63V through D1.

In normal operation, to charge up the system bus above 2.63V through D1 quickly, the ACIN pin voltage divider resistor values need to be small, which in sequence causes larger constant power consumption on the ACIN pin voltage divider resistors. Two optional circuits as shown in Figure 42 can be dedicated to charge up the system bus. Renesas recommends using the option 1 circuit for HPB configuration and the option 2 circuit for NVDC configuration.

For the option 2 circuit, the R3 and R4 voltage divider voltage (the Q1 gate voltage) needs to be 2.63V higher than the Q1 gate source threshold voltage so that Q1 can be turned on and the system bus can be charged up above 2.63V through R2 and Q1. Additionally, the R3 and R4 voltage divider voltage needs to be less than the final system bus voltage so that Q1 can be turned off in normal operation to avoid the leakage current through Q1.

Note: With the option 1 circuit there is leakage current through R1 and D2 when the adapter voltage is higher than the system bus voltage, such as in Learn mode or for the NVDC configuration.

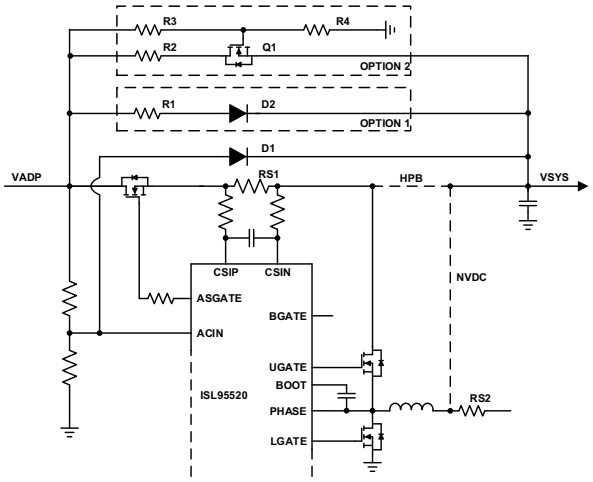


FIGURE 42. EXTERNAL SYSTEM BUS SHORT DETECTION CIRCUIT

Adapter Input Filter

The adapter cable parasitic inductance and capacitance can cause some voltage ring or an overshoot spike at the adapter connector node when adapter is hot plugged in. This voltage spike can damage the ASGATE MOSFET or the ISL95520 pins connecting to the adapter connector node. One low cost solution is to add an R-C snubber circuit at the adapter connector node to clamp the voltage spike as shown in Figure 43. A practical value of the R-C snubber is 2.2Ω to 2.2µF. The appropriate values and power rating should be carefully characterized based on the actual design. Additionally, Renesas does not recommend adding a pure capacitor at the adapter connector node, which can cause an even bigger voltage spike due to the adapter cable or the adapter current path parasitic inductance.

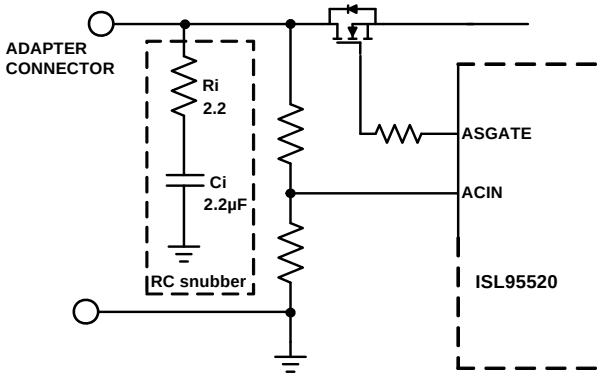


FIGURE 43. ADAPTER INPUT RC SNUBBER CIRCUIT

Test with e-Load Constant Voltage Mode

An electronic load in Constant Voltage mode (e-Load in CV mode) is often used to emulate a battery in testing a battery charger. However, an e-Load in CV mode does not accurately emulate the characteristics of a real battery, particularly the ESR. Such discrepancy may result in much more exaggerated output voltage switching ripple observed by the battery charger and present inaccurate test results. Renesas recommends adding a capacitor, such as 680µF, at the terminal of the e-Load to better match the impedance of a real battery, so that the test result better represents that of a real battery. As a precaution for potentially testing with an e-load with large ESR, Renesas recommends adding an R-C filter at the VBAT pin to smooth the switching ripple observed by the ISL95520. The recommended range of the R-C time constant is 200µs to 1ms.

General Application Information

This design guide provides a high-level explanation of the steps necessary to design a single-phase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced in the following section. In addition to this guide, Renesas provides complete reference designs that include schematics, a bill of materials, and example board layouts.

Select the LC Output Filter

The duty cycle of an ideal buck converter in CCM is a function of the input and the output voltage. This relationship is written by Equation 5:

$$D = \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 5)}$$

The output inductor peak-to-peak ripple current is written by Equation 6:

$$I_{P-P} = \frac{V_{OUT} \cdot (1 - D)}{f_{SW} \cdot L} \quad \text{(EQ. 6)}$$

A typical step-down DC/DC converter has an I_{P-P} of 20% to 40% of the maximum DC output load current for a practical design. The value of I_{P-P} is selected based upon several criteria such as MOSFET switching loss, inductor core loss, and the resistive loss of the inductor winding.

The DC copper loss of the inductor can be estimated by Equation 7:

$$P_{COPPER} = I_{LOAD}^{2} \cdot DCR \quad \text{(EQ. 7)}$$

Where I_{LOAD} is the converter output DC current.

The copper loss can be significant so attention has to be given to the DCR selection. Another factor to consider when choosing the inductor is its saturation characteristics at elevated temperatures. A saturated inductor can destroy circuit components.

A DC/DC buck regulator must have output capacitance C_O into which ripple current I_{P-P} can flow. Current I_{P-P} develops a corresponding ripple voltage V_{P-P} across CO, which is the sum of the voltage drop across the capacitor ESR and of the voltage change stemming from charge moved in and out of the capacitor. These two voltages are written by Equation 8:

$$\Delta V_{ESR} = I_{P-P} \cdot ESR \quad \text{(EQ. 8)}$$

and Equation 9:

$$\Delta V_{C} = \frac{I_{P-P}}{8 \cdot C_O \cdot f_{SW}} \quad \text{(EQ. 9)}$$

If the output of the converter has to support a load with high pulsating current, several capacitors need to be paralleled to reduce the total ESR until the required V_{P-P} is achieved. The inductance of the capacitor can cause a brief voltage dip if the load transient has an extremely high slew rate. Low inductance capacitors should be considered in this scenario. A capacitor dissipates heat as a function of RMS current and frequency. Be sure that I_{P-P} is shared by a sufficient quantity of paralleled capacitors so that they operate below the maximum rated RMS current at f_{SW}. Take into account that the rated value of a capacitor can fade as much as 50% as the DC voltage across it increases.

Select the Input Capacitor

The important parameters for the input capacitance are the voltage rating and the RMS current rating. For reliable operation, select capacitors with voltage and current ratings above the maximum input voltage and capable of supplying the RMS current required by the switching circuit. Their voltage rating should be at least 1.25x greater than the maximum input voltage, while a voltage rating of 1.5x is a preferred rating. Figure 44 is a graph of the input capacitor RMS ripple current, normalized relative to output load current, as a function of duty cycle and adjusted for converter efficiency. The normalized RMS ripple current calculation is written as Equation 10:

$$I_{C_{IN}(RMS,NORMALIZED)} = \frac{I_{MAX} \cdot \sqrt{D \cdot (1-D) + \frac{D \cdot k^2}{12}}}{I_{MAX}} \quad \text{(EQ. 10)}$$

where:

- I_{MAX} is the maximum continuous I_{LOAD} of the converter
- k is a multiplier (0 to 1) corresponding to the inductor peak-to-peak ripple amplitude expressed as a percentage of I_{MAX} (0% to 100%)
- D is the duty cycle that is adjusted to account for the efficiency of the converter, which is written as Equation 11:

$$D = \frac{V_{OUT}}{V_{IN} \cdot EFF} \quad \text{(EQ. 11)}$$

In addition to the capacitance, some low ESL ceramic capacitance is recommended to decouple between the drain of the high-side MOSFET and the source of the low-side MOSFET.

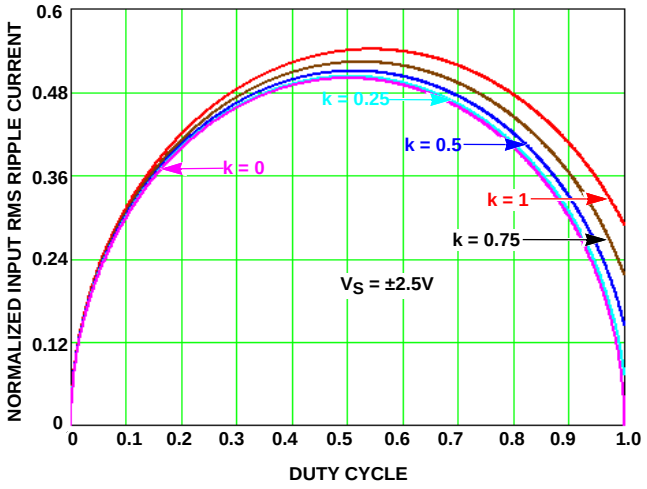


FIGURE 44. NORMALIZED RMS INPUT CURRENT AT EFF = 1

Select the Switching Power MOSFET

Typically, MOSFETs cannot tolerate even brief excursions beyond their maximum drain-to-source voltage rating. The MOSFETs used in the power stage of the converter should have a maximum VDS rating that exceeds the sum of the upper voltage tolerance of the input power source and the voltage spike that occurs when the MOSFET switches off.

Several power MOSFETs are readily available that are optimized for DC/DC converter applications. The preferred high-side MOSFET emphasizes low gate charge so the device spends the least amount of time dissipating power in the linear region. Unlike the low-side MOSFET which has the drain to source voltage clamped by its body diode during turn off, the high-side MOSFET turns off with a VDS of approximately VIN-VOUT, plus the spike across it. The preferred low-side MOSFET emphasizes low $r_{DS(ON)}$ when fully saturated to minimize conduction loss.
Note: This is an optimal configuration of MOSFET selection for low duty cycle applications (D < 50%). For higher output, low input voltage solutions, a more balanced MOSFET selection for high- and low-side devices may be warranted.

For the low-side (LS) MOSFET, the power loss can be assumed to be conductive only and is written as Equation 12:

$$P_{CON\_LS} \approx I_{LOAD}^2 \cdot r_{DS(ON)\_LS} \cdot (1-D) \quad \text{(EQ. 12)}$$

For the high-side (HS) MOSFET, the its conduction loss is written by Equation 13:

$$P_{CON\_HS} = I_{LOAD}^2 \cdot r_{DS(ON)\_HS} \cdot D \quad \text{(EQ. 13)}$$

For the HS MOSFET, the switching loss is written as Equation 14:

$$P_{SW\_HS} = \frac{V_{IN} \cdot I_{VALLEY} \cdot t_{ON} \cdot f_{SW}}{2} + \frac{V_{IN} \cdot I_{PEAK} \cdot t_{OFF} \cdot f_{SW}}{2} \quad \text{(EQ. 14)}$$

where:

- I_{VALLEY} is the difference of the DC component of the inductor current minus 1/2 of the inductor ripple current
- I_{PEAK} is the sum of the DC component of the inductor current plus 1/2 of the inductor ripple current
- t_{ON} is the time required to drive the device into saturation
- t_{OFF} is the time required to drive the device into cut-off

Renesas recommends using a 2.2µF (10V) VDD/VDDP capacitor that has an effective capacitance higher than 0.4µF at 5V and x1.6 effective cap at the BOOT pin at 5V.

Select the Bootstrap Capacitor

The selection of the bootstrap capacitor is written by Equation 15:

$$C_{BOOT} = \frac{Q_g}{\Delta V_{BOOT}} \quad \text{(EQ. 15)}$$

where:

- Q_g is the total gate charge required to turn on the HS MOSFET
- ΔV_{BOOT} is the maximum allowed voltage decay across the boot capacitor each time the HS MOSFET is switched on

As an example, suppose the HS MOSFET has a total gate charge, Q_g, of 25nC at VGS = 5V and a ΔV_{BOOT} of 200mV. The calculated bootstrap capacitance is 0.125µF; for a comfortable margin, select a capacitor that is double the calculated capacitance. In this example, 0.22µF suffices. Use an X7R or X5R ceramic capacitor.

Renesas recommends using a bootstrap capacitor of 0.47µF (25V) that has an effective capacitance higher than 0.25µF at 5V and x50 effective high-side MOSFET gate capacitance.

Select the DCIN Filter

An R-C filter is connected at the DCIN pin. Renesas recommends connecting a 10Ω DCIN resistor between the DCIN pin and the VADP/VSYS diodes, and connecting a 4.7µF (50V) DCIN capacitor with an effective capacitance higher than 0.4µF at 20V to GND.

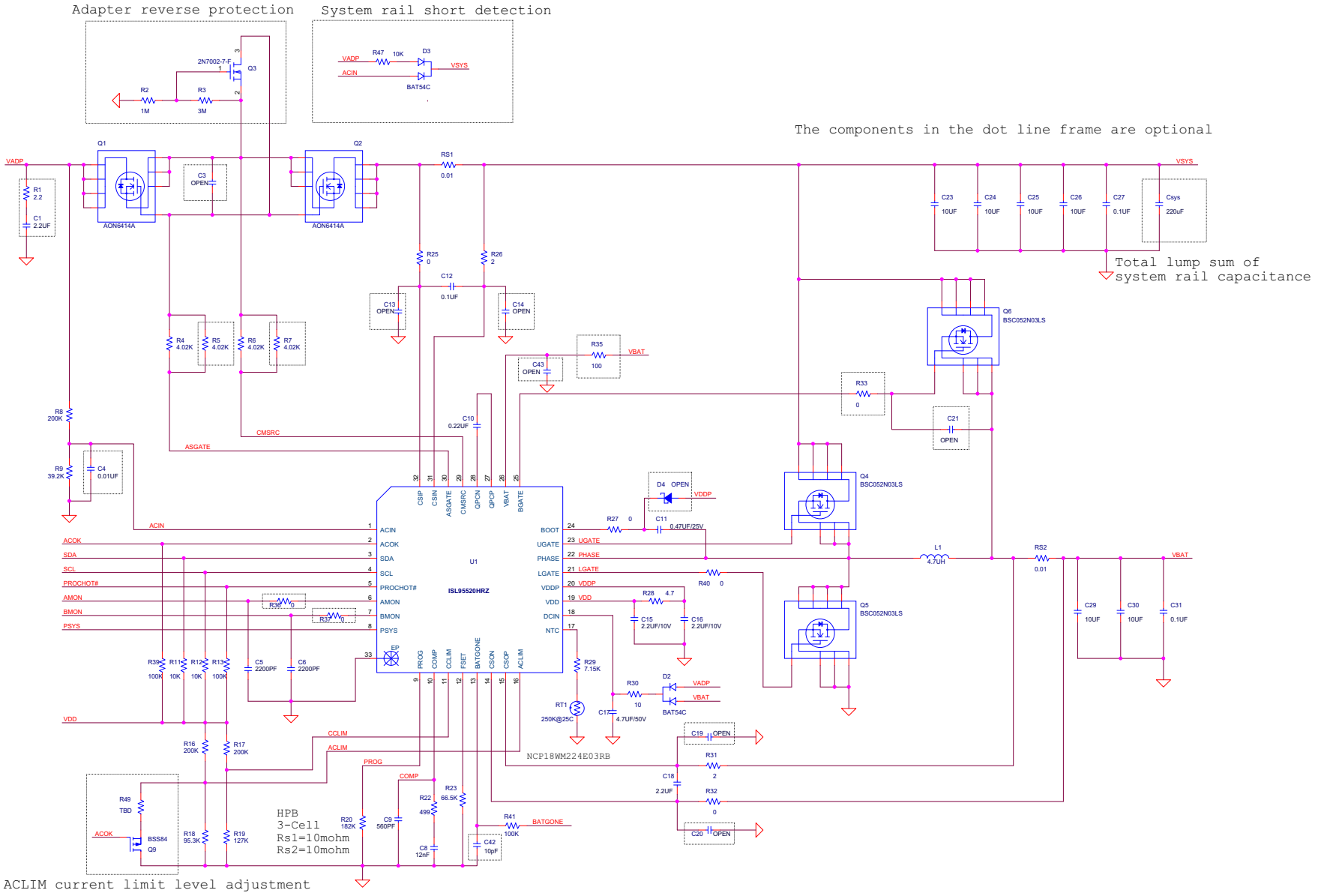


FIGURE 45. ISL95520 HPB CONFIGURATION REFERENCE DESIGN

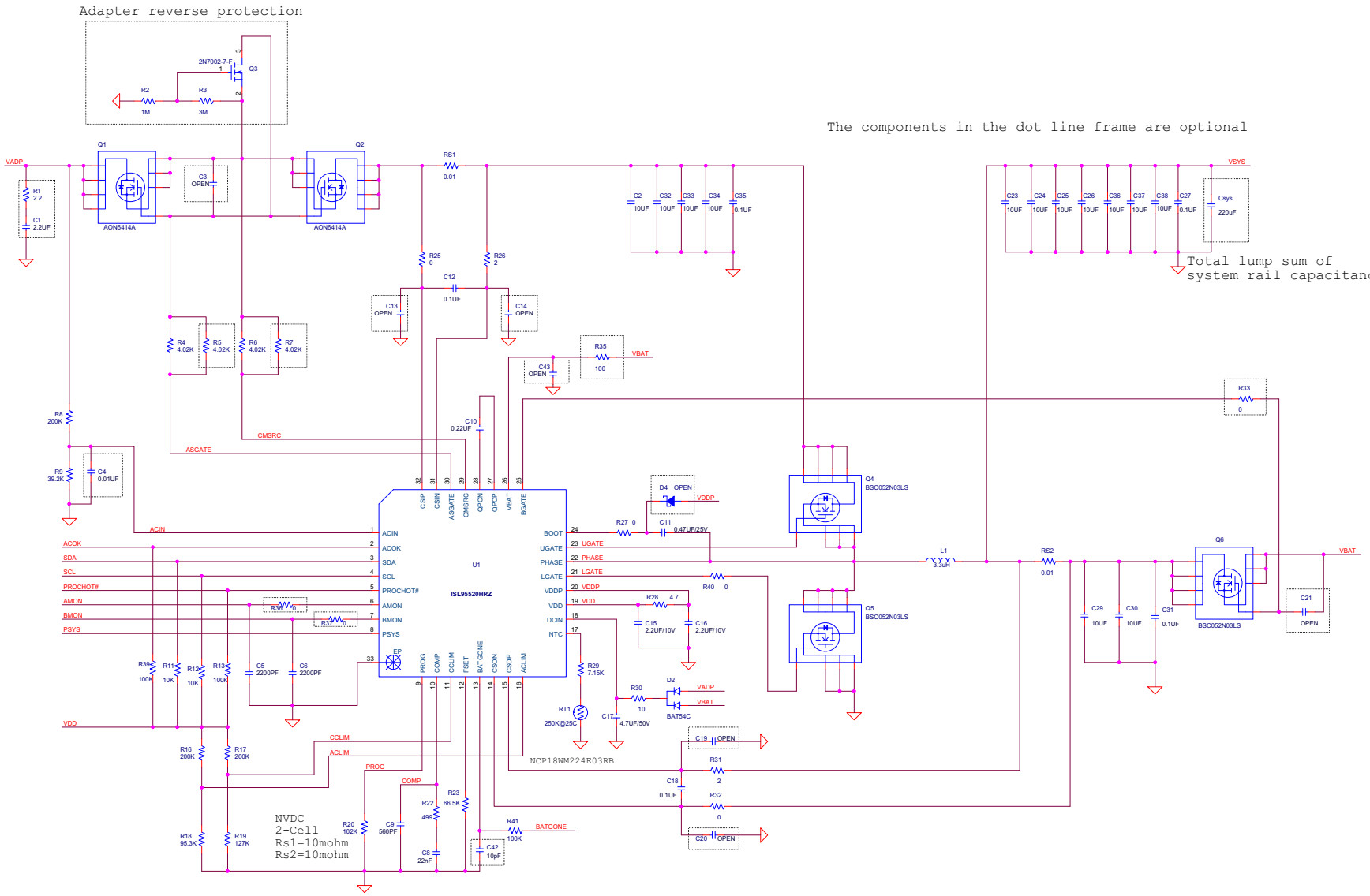
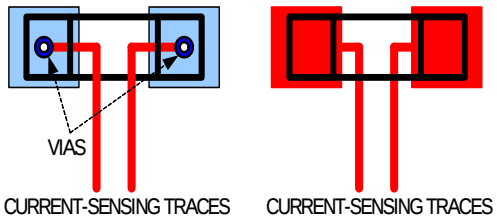
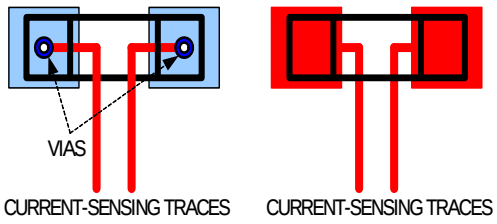


FIGURE 46. ISL95520 NVDC CONFIGURATION REFERENCE DESIGN

Layout Guidelines

ISL95520	SYMBOL	LAYOUT GUIDELINES
BOTTOM PAD	GND	Connect this ground pad to the ground plane through a low impedance path. Renesas recommends using at least five vias to connect to the ground planes in the PCB to ensure sufficient thermal dissipation directly under the IC.
1	ACIN	Place the voltage divider resistors and the optional decoupling capacitor in the general proximity of the controller.
2	ACOK	No special consideration.
3	SDA	No special consideration.
4	SCLK	
5	PROCHOT#	No special consideration.
6	AMON	No special consideration. Place the optional R-C filter in the general proximity of the controller.
7	BMON	
8	PSYS	No special consideration.
9	PROG	Place the PROG programming resistor in the general proximity of the controller.
10	COMP	Place the compensation components in the general proximity of the controller.
11	CCLIM	Place the CCLIM voltage divider resistors in the general proximity of the controller.
12	FSET	Place the FSET programming resistor in the general proximity of the controller.
13	BATGONE	Place the 100kΩ resistor series in the BATGONE signal trace and the optional decoupling capacitor in the general proximity of the controller.
14	CSON	Run two dedicated traces with sufficient width (>20 mil) in parallel (close to each other to minimize the loop area) from the two terminals of the battery current sensing resistor to the IC. Place the differential mode and common mode R-C filter components in the general proximity of the controller. Route the current sensing traces through vias to connect the center of the pads; or route the traces into the pads from the inside of the current sensing resistor. The following drawings show the two preferred ways of routing current sensing traces. 
15	CSOP	
16	ACLIM	Place the ACLIM voltage divider resistors in the general proximity of the controller.
17	NTC	Place the resistor series with the NTC thermistor in general proximity of the controller. Place the NTC thermistor at the point where the temperature is monitored. **Note:** If the NTC thermistor is too close to the switching components, it may couple the switching noise to the NTC pin.
18	DCIN	Place the OR diodes and the R-C filter in the general proximity of the controller.
19	VDD	Place the R-C filter from the VDDP pin in the general proximity of the controller.
20	VDDP	Place the decoupling capacitor in the general proximity of the controller.
21	LGATE	Run the LGATE trace in parallel with the UGATE and PHASE traces on the same PCB layer. Use sufficient width (>30 mil). Avoid any sensitive analog signal trace from crossing over or getting close.

Layout Guidelines

ISL95520	SYMBOL	LAYOUT GUIDELINES (Continued)
22	PHASE	Run these two traces in parallel with sufficient width (>30 mil). Avoid any sensitive analog signal trace from crossing over or getting close. Renesas recommends routing the PHASE trace to the high-side MOSFET source pin instead of general copper. Place the IC close to the switching MOSFET's gate terminals and keep the gate drive signal traces short for a clean MOSFET drive. The IC can be placed on the opposite side of the switching MOSFETs. Place the input capacitors as close as possible to the switching high-side MOSFET drain and the low-side MOSFET source; and use the shortest PCB trace connection. Place these capacitors on the same PCB layer with the MOSFETs instead of on different layers and using vias to make the connection. Place the inductor input terminal to the switching high-side MOSFET drain and low-side MOSFET source terminal as close as possible. Minimize this phase node area to lower the electrical and magnetic field radiation but make this phase node area large enough to carry the current. Place the inductor and the switching MOSFETs on the same layer of the PCB.
23	UGATE	
24	BOOT	Place the bootstrap capacitor in the general proximity of the controller. Use sufficiently wide trace (>30 mil). Avoid any sensitive analog signal trace from crossing over or getting close.
25	BGATE	Use sufficient width (>30 mil) trace from the IC to the BGATE MOSFET gate.
26	VBAT	Place the R-C filter in the general proximity of the controller. Run a dedicated trace from the battery positive connection point to the IC. In the HPB configuration, separate this trace from the trace connecting the CSON pin.
27	QPCP	Place the charge pump flying capacitor in the general proximity of the controller. Route the trace with sufficient width (>30 mil).
28	QPCN	
29	CMSRC	Run these two traces in parallel with sufficient width (>30 mil).
30	ASGATE	
31	CSIN	Place the battery current sensing resistor right next to the inductor output. Run two dedicated trace with decent width (>20 mil) in parallel (close to each other to minimize the loop area) from the two terminals of the adapter current sensing resistor to the IC. Place the differential mode and common mode R-C filter components in the general proximity of the controller. Route the current sensing traces through vias to connect the center of the pads; or route the traces into the pads from the inside of the current sensing resistor. The following drawings show the two preferred ways of routing current sensing traces. 
32	CSIP	

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Jun 17, 2019	FN8694.1	Added related literature section on page 1. Added tape and reel column to ordering information table on page 9. Modified pin descriptions for pins 18, 19, 20, and 24 on page 10. Added information about recommended VDD/VDDP capacitors to the “Select the Switching Power MOSFET” section on page 46. Added information about recommended bootstrap capacitors to the “Select the Bootstrap Capacitor” section on page 46. Added “Select the DCIN Filter” section on page 47. Updated Figure 45 on page 48 and Figure 46 on page 49 Updated package outline drawing from version 3 to version 5. -Changes from version 3 to version 4: Updated the package Width & Length dimensions with tolerance values on the top view from: 4.00 to: 4.00 +/-0.05 -Changes from version 4 to version 5: Side View - Changed "A" to "X" for detail name. Removed "0.050" dimension as it is already listed in Detail X. Corrected arrow with dimension (0.90±0.10) to point to correct dimension line. Bottom View - Removed 'b' next to Note 4 reference. This is no longer needed. Removed diagonal line inside exposed pad. Notes- Removed 'b' from Note 4 no longer needed. Removed About Intersil section. Updated links throughout document. Updated disclaimer.
Feb 18, 2015	FN8694.0	Initial Release

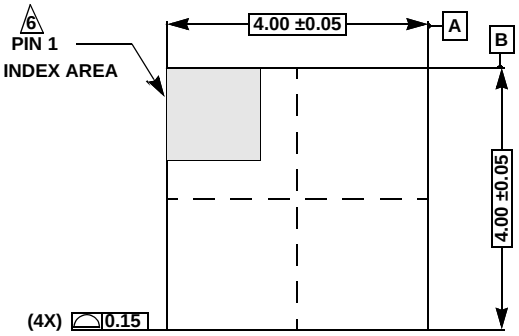
Package Outline Drawing

For the most recent package outline drawing, see L32.4x4A.

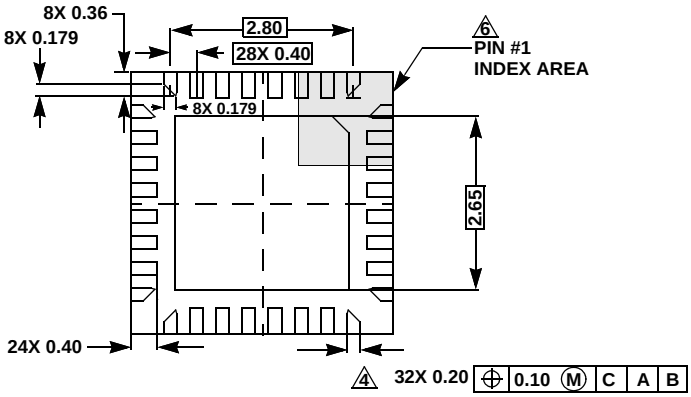
L32.4x4A

32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

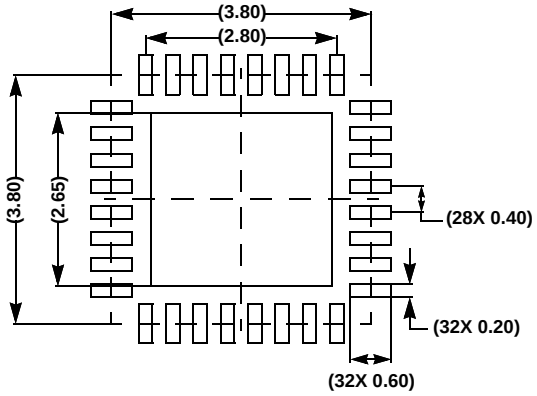
Rev 5, 2/16



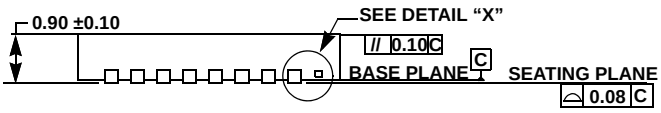
TOP VIEW



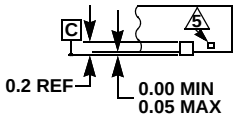
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.25mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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