

ISL88739B

Hybrid Power Boost (HPB) Battery Charger with SMBus Interface

FN8955
Rev.3.00
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The [ISL88739B](#) is a highly versatile battery charger configurable as a Hybrid Power Boost (HPB) charger, supporting 2-, 3-, or 4-cell batteries. The configuration allows the battery to work with the adapter to supply the system load when it exceeds the adapter capability, referred to as Turbo mode. The HPB charger configuration reverse-boosts battery energy to the system bus to help the adapter provide the system power in Turbo mode.

The ISL88739B uses N-channel MOSFETs (NFETs) for all the switches to achieve the best performance and lowest BOM cost. The internal charge pump can turn on all the NFETs quickly or slowly, depending on the circumstance or the need. The ability to quickly turn on NFETs prevents system bus voltage drop when the battery is suddenly removed in Turbo mode or in Battery Learn mode.

The ISL88739B provides many protection features including a PROCHOT# indicator for system low voltage, adapter overcurrent, battery overcurrent, or overheating, with an array of SMBus programmable parameters for maximum flexibility. The ISL88739B also features hardware-based adapter-current limit and battery-current limit in addition to SMBus programmable limits.

The ISL88739B provides a high accuracy adapter current monitor, battery current monitor, and system power monitor outputs. Several configurable current-sense resistor value options provide maximum flexibility for working with high and low power systems, to achieve the best trade-off of current sensing accuracy vs power loss.

Related Literature

For a full list of related documents, visit our website:

- [ISL88739B](#) device page

Features

- Configurable as an HPB charger
- Compliant with Intel PROCHOT# and PSYS requirements
- Adapter current monitor and battery discharging current monitor
- Uses NFET for all switches
 - Supports battery removal during Battery Learn mode
 - Actively controlled inrush current to prevent FET damage
- SMBus programmable settings and high accuracy
- Comprehensive protection features:
 - PROCHOT# indicator for system low voltage, adapter overcurrent, battery overcurrent, or system overheating
 - Hardware-based adapter current and battery current limits
 - Sudden battery removal support in Turbo mode
- 16 switching frequency options from 350kHz to 1MHz
- Low quiescent current
- SMBus and auto-increment I²C compatible
- Robust Ripple Regulator (R3™) modulation scheme provides excellent light-load efficiency and fast dynamic response
- 32 Ld 4mmx4mm QFN package
- Pb-free (RoHS compliant)

Applications

- Devices with rechargeable 2-, 3-, or 4-cell batteries

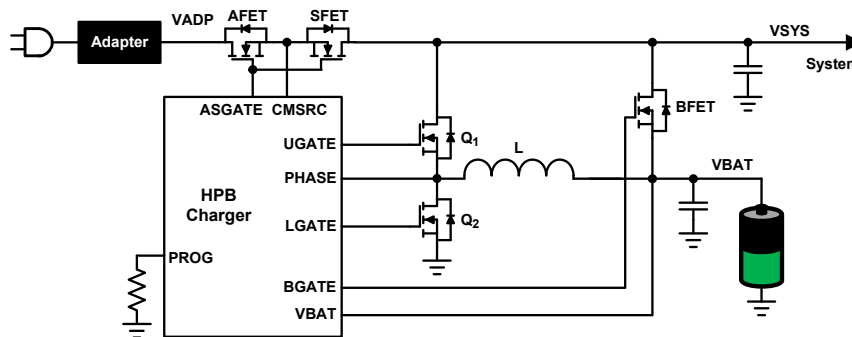


Figure 1. HPB Charger Configuration

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1. Overview

1.1 Block Diagram

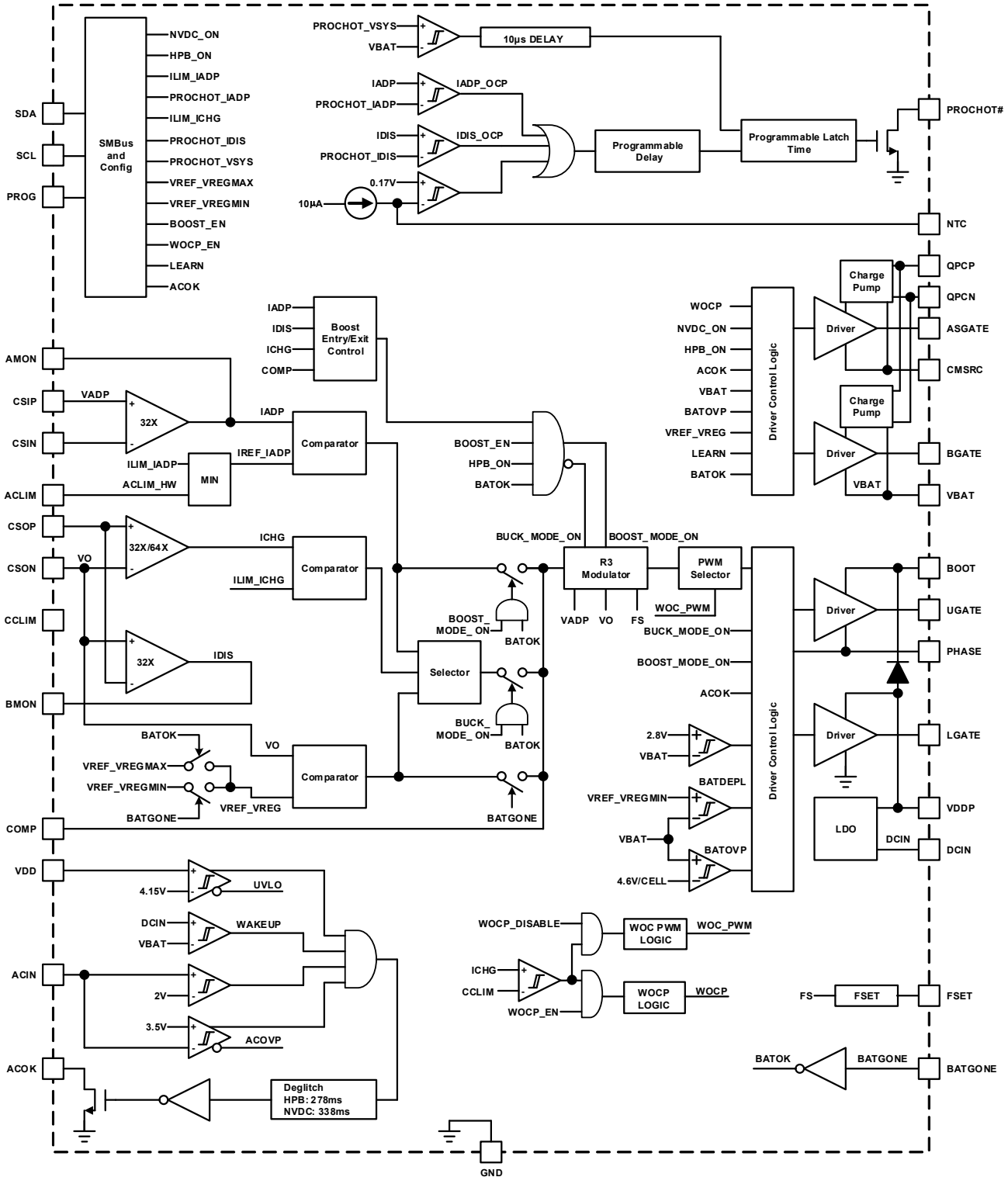


Figure 2. Block Diagram

1.2 Simplified Application Circuits

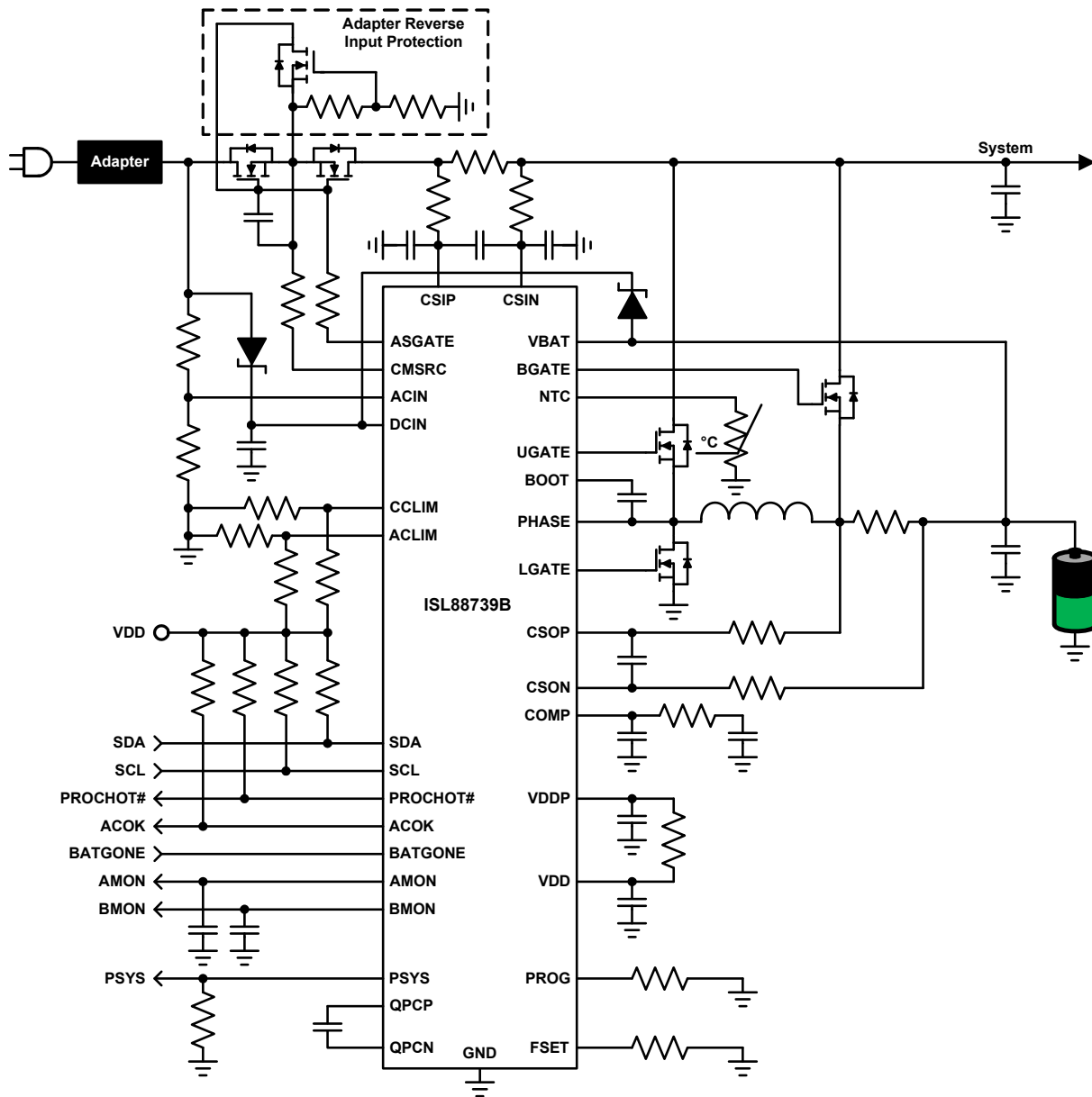


Figure 3. Typical Application Circuit: HPB Charger Configuration with Two NMOS Selectors

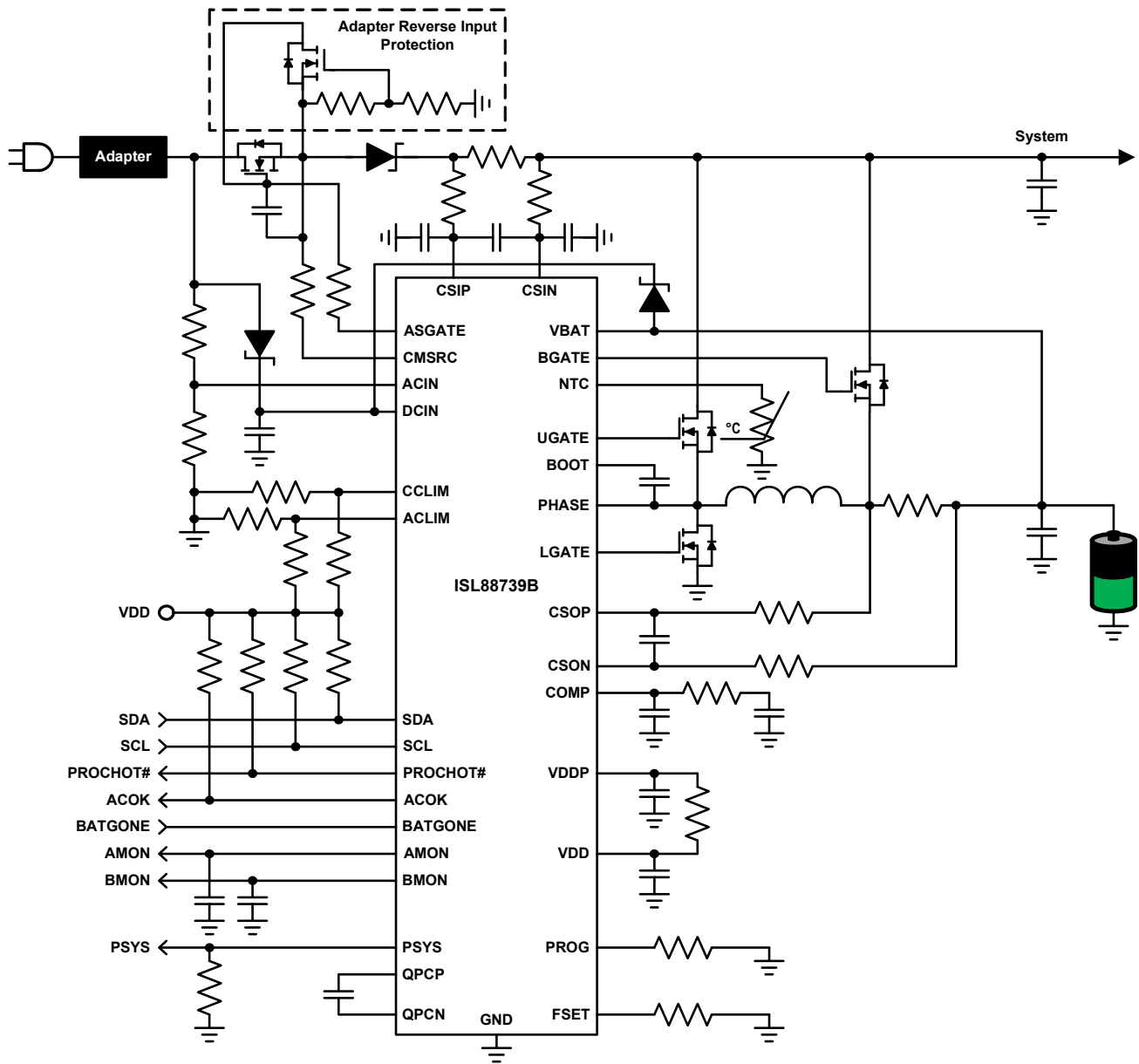


Figure 4. Typical Application Circuit: HPB Charger Configuration with One NMOS Selector and Schottky Diode

1.3 Ordering Information

Part Number (Notes 2, 3)	Part Marking	Temp. Range (°C)	Tape and Reel (Units) (Note 1)	Package (RoHS Compliant)	Pkg. Dwg. #
ISL88739BHRZ	88739B	0 to +85	-	32 Ld 4x4 QFN	L32.4x4A
ISL88739BHRZ-T	88739B	0 to +85	6k	32 Ld 4x4 QFN	L32.4x4A

Notes:

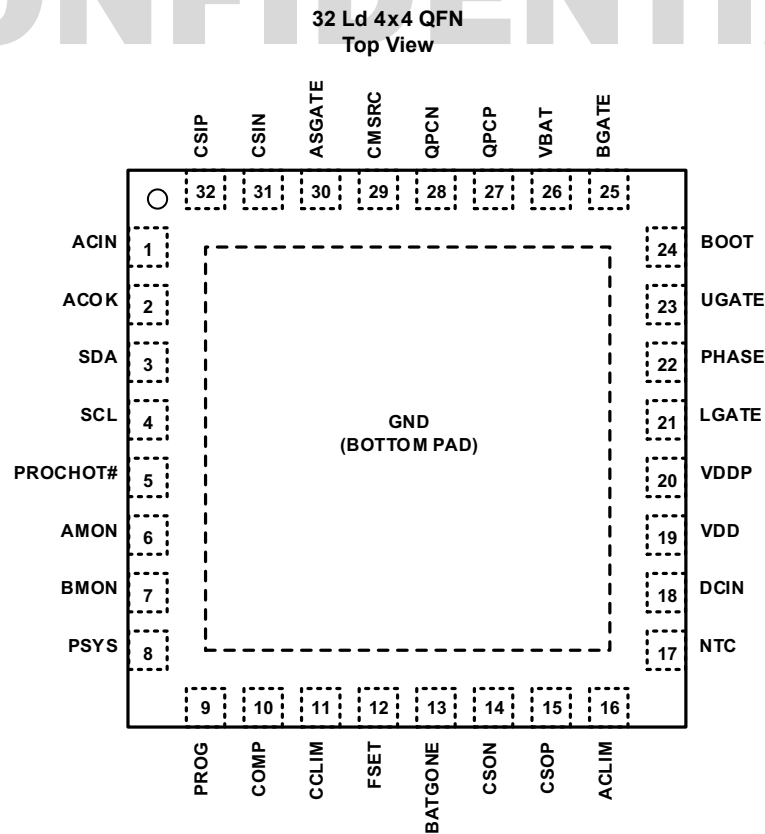
- See [TB347](#) for details about reel specifications.
- These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
- For Moisture Sensitivity Level (MSL), see the [ISL88739B](#) device page. For more information about MSL, see [TB363](#).

Table 1. Key Differences Between Family of Parts

	ISL88739B	ISL88750	ISL95521A	ISL95521B
Charger Type	HPB	NVDC	HPB or NVDC	HPB or NVDC
PSYS	Yes	No	Yes	Yes
PROCHOT# and NTC	Yes	No	Yes	Yes

1.4 Pin Configuration

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1.5 Pin Descriptions

Pin #	Pin Name	Description
Bottom Pad	GND	Signal common of the IC. Unless otherwise stated, signals are referenced to the GND pin. GND should also be used as the thermal pad for heat removal.
1	ACIN	Adapter voltage sense. The adapter voltage is "valid" if the ACIN pin voltage is between 2V and 3.5V. If the ACIN pin voltage exceeds 3.5V, the adapter voltage is in an overvoltage condition and the ISL88739B turns off the ASGATE MOSFETs to isolate the adapter from the system.
2	ACOK	Open-drain output to indicate the adapter voltage is ready. Pulled low if the adapter voltage is not ready.
3	SDA	SMBus data I/O. Connect to the data line from the host controller or smart battery. Connect a 10kΩ pull-up resistor according to the SMBus specification.
4	SCL	SMBus clock I/O. Connect to the clock line from the host controller or smart battery. Connect a 10kΩ pull-up resistor according to the SMBus specification.
5	PROCHOT#	Open-drain output. Pull low with SMBus programmable debounce time if any of the following conditions occur: 1. Adapter current reaches PROCHOT_IADP. 2. Battery discharging current reaches PROCHOT_IDIS. 3. System bus voltage is below the low system voltage detection threshold (programmable through SMBus). 4. NTC pin voltage is below 170mV. When asserted, it latches on for a minimum SMBus programmable time before it can be cleared.
6	AMON	Adapter current monitor output. $V_{AMON} = 32 \times (V_{CSIP} - V_{CSIN})$. Leave the AMON pin floating if not used.
7	BMON	Battery discharging current monitor. $V_{BMON} = 32 \times (V_{CSON} - V_{CSOP})$. Leave the BMON pin floating if not used.
8	PSYS	System power monitor output. Connect the PSYS pin to GND if not used.
9	PROG	A resistor to GND sets the following configurations: 1. HPB charger. 2. Default number of the battery cells in series. 3. Adapter current sense resistor and battery current sense resistor values. See Table 17 on page 39 for programming options. After POR, pulling the PROG pin to 5V enables Learn mode.
10	COMP	Error amplifier output. Connect compensation network externally from COMP to GND.
11	CCLIM	The voltage on this pin sets the WOCP threshold for the current flowing into the battery.
12	FSET	A resistor from this pin to GND programs the default switching frequency. See Table 19 on page 41 for programming options.
13	BATGONE	Battery presence indicator input pin to the ISL88739B. Logic high indicates the battery has been removed. Logic low indicates the battery is present.
14	CSON	Battery current sense negative input.
15	CSOP	Battery current sense positive input.
16	ACLIM	The voltage on this pin sets the hardware-based adapter current limit. The lower value of the hardware-set adapter current limit and the SMBus set adapter current limit is the actual limit of the adapter current. The hardware-based adapter current limit also sets the regulated inrush current level for ASGATE MOSFET protection.
17	NTC	10μA current source output. Connect an NTC thermistor network from this pin to GND. If the NTC pin voltage is below 170mV, the ISL88739B pulls PROCHOT# low. This NTC pin comparator can also be used as a general purpose comparator for the platform to use.
18	DCIN	Internal 5V output LDO input. Renesas recommends connecting a diode-OR from the adapter and battery. The DCIN pin voltage must be higher than the VBAT pin voltage for ASGATE to soft-start turning on. Connect a 10Ω DCIN resistor between the DCIN pin and the VADP/VSYS diodes, and connect a 4.7μF (50V) DCIN capacitor to GND. The capacitor must have an effective capacitance higher than 0.4μF at 20V.
19	VDD	5V power supply input for the ISL88739B control circuitry. Connect a 2.2μF (10V) MLCC capacitor to GND. The capacitor must have an effective capacitance higher than 0.4μF at 5V and x1.6 effective capacitance at the BOOT pin at 5V.

Pin #	Pin Name	Description
20	VDDP	Internal 5V output LDO output. The ISL88739B uses this pin as the FET driver power supply. Connect a 2.2 μ F (10V) MLCC capacitor to GND. The capacitor must have an effective capacitance higher than 0.4 μ F at 5V and x1.6 effective capacitance at the BOOT pin at 5V.
21	LGATE	Low-side switching FET gate drive output. Connect this pin to the gate of the low-side switching FET.
22	PHASE	Current return path for the high-side switching FET gate drive. Connect this pin to the node consisting of the high-side switching FET source, the low-side switch FET drain, and the output inductor.
23	UGATE	High-side switching FET gate drive output. Connect this pin to the gate of the high-side switching FET.
24	BOOT	Connect an MLCC capacitor across the BOOT pin and the PHASE pin. The boot capacitor is charged through an internal bootstrap switch connected from the VDDP pin to the BOOT pin, when the PHASE pin drops below VDDP minus the voltage drop across the internal bootstrap switch. Connect a 0.47 μ F (25V) bootstrap capacitor, which must have an effective capacitance higher than 0.25 μ F at 5V and x50 effective high-side MOSFET gate capacitance.
25	BGATE	Gate drive output for the NFET connecting the system voltage and the battery. The behavior of the BGATE depends on whether the ISL88739B is in HPB charger configuration.
26	VBAT	Current return path for the BGATE gate drive. Also senses battery voltage. Renesas recommends connecting an RC filter at the VBAT pin.
27	QPCP	Internal charge pump positive input. Connect an MLCC capacitor across the QPCP pin and the QPCN pin.
28	QPCN	Internal charge pump negative input. Connect an MLCC capacitor across the QPCP pin and the QPCN pin.
29	CMSRC	Common source node of the two back-to-back ASGATE NFETs.
30	ASGATE	Output of the gate drive for the two back-to-back NFETs.
31	CSIN	Adapter current sense negative input.
32	CSIP	Adapter current sense output input. Also senses input voltage.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
CSIP, CSIN, DCIN, CMSRC, QPCN	-0.3	+28	V
VBAT, CSOP, CSON	-0.3	+28	V
ASGATE, BGATE, QPCP	-0.3	+33	V
VDD, VDDP	-0.3	+7	V
CSIP-CSIN, CSOP-CSON	-0.3	+0.3	V
QPCP-QPCN	-0.3	+7	V
UGATE-PHASE	-0.3	+7	V
BOOT Voltage (BOOT)	-0.3	+33	V
BOOT to PHASE Voltage (BOOT-PHASE)	-0.3	+7 (DC)	V
	-0.3	+9 (<10ns)	V
PHASE Voltage (PHASE)	-0.3	28	V
		-7 (<20ns pulse width, 10 μ J)	V
UGATE Voltage (UGATE)	(PHASE - 0.3) (DC)	BOOT	V
	(PHASE - 5) (<20ns pulse width, 10 μ J)	BOOT	V
LGATE Voltage	-2.5 (<20ns pulse width, 5 μ J)	V _{DDP} + 0.3	V
Open-Drain Outputs, ACOK, PROCHOT#	-0.3	+7	V
All Other Pins	-0.3	V _{DD} + 0.3	V
ESD Rating	Value		Unit
Human Body Model (Tested per JS-001-2014)	2.5		kV
Charged Device Model (Tested per JS-002-2014)	750		V
Latch-Up (Tested per JESD78E; Class 2, Level A)	100		mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
32 Ld QFN Package (Notes 4, 5)	39	3

Notes:

- θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See [TB379](#).
- For θ_{JC} , the "case temp" location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature		+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	see TB493		

2.3 Recommended Operation Conditions

Parameter	Minimum	Maximum	Unit
Ambient Temperature	0	+85	°C
Junction Temperature	0	125	°C

2.4 Electrical Specifications

Operating Conditions: $V_{DD} = 5V$, $T_A = 0^\circ C$ to $+85^\circ C$ unless otherwise noted. **Boldface limits apply across the operating temperature range, $0^\circ C$ to $+85^\circ C$.**

Parameter	Symbol	Test Conditions	Min Note 6	Typ	Max Note 6	Unit
Quiescent Current and POR						
Battery Current	$I_{BAT_BGATE_OFF}$ HPB	Adapter present, BGATE off, $V_{BAT} = 16.8V$, DCIN current does not come from battery, $I_{BAT} = I_{PHASE} + I_{VBAT} + I_{CSOP} + I_{CSON} + I_{CMSRC}$		43	75	μA
	$I_{BAT_BGATE_ON}$ HPB	Battery only, BGATE on, $V_{BAT} = 16.8V$, DCIN current comes from battery, $I_{BAT} = I_{PHASE} + I_{VBAT} + I_{CSOP} + I_{CSON} + I_{DCIN} + I_{CSIP} + I_{CSIN} + I_{CMSRC}$		130	190	μA
Quiescent Current	$I_{DCIN_STANDBY}$ HPB	VADP = 19.2V, AMON, BMON, PSYS all off		160	220	μA
	$I_{DCIN_NOSW_1}$ HPB	VADP = 19.2V, no switching, AMON, BMON, PSYS all off		785	900	μA
	$I_{DCIN_NOSW_2}$ HPB	VADP = 19.2V, no switching, AMON, BMON, PSYS all on		1070	1250	μA
	$I_{DCIN_SW_H}$ HPB	VADP = 19.2V, charge enabled, AMON, BMON, PSYS all off		1.52	1.82	mA
VDD Power-On Reset (POR)	POR V_{DD_R}	VDD rising		4.66	4.75	V
	POR V_{DD_F}	VDD falling	4.35	4.44		mV
Charging Voltage Limit						
Maximum Charging Voltage Accuracy	V_{CHG_MAX}	MaxChargeVoltage = 0x41A0H (16.8V)		16.79		V
			-0.75		0.75	%
		MaxChargeVoltage = 0x3140H (12.608V)		12.6		V
			-0.75		0.75	%
Minimum Charging Voltage Accuracy	V_{CHG_MIN}	MinChargeVoltage = 0x2A00H (10.752V)	11.02	11.20	11.40	V
		MinChargeVoltage = 0x2000H (8.192V)	8.48	8.64	8.84	V
		MinChargeVoltage = 0x1500H (5.376V)	5.680	5.825	6	V
Battery Current Limit						
Battery Current Sense Amplifier Input Differential Voltage Range	V_{IBAT_RGE5}	$R_{s2} = 5m\Omega$, charging current ($V_{CSOP} - V_{CSON}$)	0		40.5	mV
	V_{IBAT_RGE10}	$R_{s2} = 10m\Omega$ or $R_{s2} = 20m\Omega$, charging current ($V_{CSOP} - V_{CSON}$)	0		81	mV
	V_{IBAT_RGED}	Discharging current ($V_{CSOP} - V_{CSON}$)	-81		0	mV

Operating Conditions: $V_{DD} = 5V$, $T_A = 0^{\circ}C$ to $+85^{\circ}C$ unless otherwise noted. **Boldface limits apply across the operating temperature range, $0^{\circ}C$ to $+85^{\circ}C$.** (Continued)

Parameter	Symbol	Test Conditions	Min Note 6	Typ	Max Note 6	Unit	
Charging Current Limit $R_{S2} = 10m\Omega$ $V_{BAT} > 4.5V$	I_{CHG_ACC10}	ChargeCurrentLimit = 0x1F20H (7968mA)		8000		mA	
			-2.1	0.4	3.4	%	
		ChargeCurrentLimit = 0x0FA0H (4000mA)		4025		mA	
			-2.4	0.6	3.8	%	
		ChargeCurrentLimit = 0x07E0H (2016mA)		2030		mA	
			-3.6	0.7	5.4	%	
		ChargeCurrentLimit = 0x03E0H (992mA)		1006		mA	
			-5	1.4	7.9	%	
Charging Current Limit $R_{S2} = 5m\Omega$ $V_{BAT} > 4.5V$	I_{CHG_ACC5}	ChargeCurrentLimit = 0x1F20H (7968mA)		8015		mA	
			-2.4	0.6	3.8	%	
		ChargeCurrentLimit = 0x0FA0H (4000mA)		4030		mA	
			-3.2	0.8	4.3	%	
		ChargeCurrentLimit = 0x07E0H (2016mA)		2035		mA	
			-5	0.9	6.3	%	
		ChargeCurrentLimit = 0x03E0H (992mA)		1008		mA	
			-9.1	1.6	10.3	%	
Trickle Charging Current Limit	$I_{TRKL_ACC10_256}$	$R_{S2} = 10m\Omega$, $V_{BAT} < MinChargeVoltage$	210	265	310	mA	
		$R_{S2} = 10m\Omega$, $V_{BAT} < MinChargeVoltage$	95	135	175	mA	
		$R_{S2} = 5m\Omega$, $V_{BAT} < MinChargeVoltage$	165	255	330	mA	
		$R_{S2} = 5m\Omega$, $V_{BAT} < MinChargeVoltage$; 145mA typical	32	120	208	mA	
	V_{BAT} Trickle Charging Threshold	$V_{TRKL_TH_R}$	MinChargeVoltage = 4.096V, exit Trickle Charging mode		4.39	4.57	V
		$V_{TRKL_TH_F}$	MinChargeVoltage = 4.096V, enter Trickle Charging mode	3.85	4.03		V
	Discharging Current PROCHOT# Threshold $R_{S2} = 5m\Omega$	$I_{DIS_HOT_TH5}$	DCPROCHOT = 0x2A00H (10752mA)		10848		mA
				-3.5	0.9	5.3	%
DCPROCHOT = 0x1500H (5376mA)				5450		mA	
			-6.4	1.4	9.2	%	

Operating Conditions: $V_{DD} = 5V$, $T_A = 0^{\circ}C$ to $+85^{\circ}C$ unless otherwise noted. **Boldface limits apply across the operating temperature range, $0^{\circ}C$ to $+85^{\circ}C$.** (Continued)

Parameter	Symbol	Test Conditions	Min Note 6	Typ	Max Note 6	Unit
Adapter Current Limit						
Adapter Current Sense Amplifier Input Differential Voltage Range	V_{IADP_RGE}	$R_{S1} = 10m\Omega$ or $R_{S1} = 20m\Omega$, adapter current ($V_{CSIP} - V_{CSIN}$)	0		81	mV
Adapter Current Limit $R_{S1} = 10m\Omega$	I_{ADP_10}	AdapterCurrentLimit = 0x1F20H (8064mA)		8115		mA
			-1.2	0.6	2.5	%
		AdapterCurrentLimit = 0x1000H (4096mA)		4140		mA
			-1.3	1.1	3.5	%
		AdapterCurrentLimit = 0x0800H (2048mA)		2075		mA
			-2.5	1.3	5.2	%
		AdapterCurrentLimit = 0x0400H (1024mA)		1055		mA
	-4	3	10	%		
Adapter Current PROCHOT# Threshold $R_{S1} = 10m\Omega$	$I_{ADP_HOT_TH10}$	ACPROCHOT = 0x1500H (5376mA)		5389		mA
			-3.50	0.25	4	%
		ACPROCHOT = 0x0A80H (2688mA)		2728		mA
			-7.0	1.5	10.0	%
Monitor						
AMON Accuracy $V_{AMON} = 32x(V_{CSIP} - V_{CSIN})$ $R_{S1} = 10m\Omega$	V_{AMON}	$V_{CSIP} - V_{CSIN} = 80mV$		2544		mV
			-2.5	-0.6	1.3	%
		$V_{CSIP} - V_{CSIN} = 40mV$		1269		mV
			-3.50	-0.85	1.80	%
		$V_{CSIP} - V_{CSIN} = 20mV$		632		mV
			-6.00	-1.25	3.50	%
		$V_{CSIP} - V_{CSIN} = 10mV$		313		mV
	-10.0	-2.2	6.6	%		
		$V_{CSIP} - V_{CSIN} = 5mV$		154		mV
			-19.50	-3.75	12.50	%
AMON Current Sourcing Capability	$I_{AMON_MAX_SR}$		255	515	800	μA
AMON Current Sinking Capability	$I_{AMON_MAX_SK}$		12	22	32	μA

Operating Conditions: $V_{DD} = 5V$, $T_A = 0^{\circ}C$ to $+85^{\circ}C$ unless otherwise noted. **Boldface limits apply across the operating temperature range, $0^{\circ}C$ to $+85^{\circ}C$.** (Continued)

Parameter	Symbol	Test Conditions	Min Note 6	Typ	Max Note 6	Unit
BMON Accuracy $V_{BMON} = 32 \times (V_{CSOP} - V_{CSOP})$ $R_{S2} = 10m\Omega$	V_{BMON}	$V_{CSOP} - V_{CSOP} = 80mV$		2562		mV
			-3.70	0.08	3.70	%
		$V_{CSOP} - V_{CSOP} = 40mV$		1284		mV
			-4.2	0.3	4.7	%
		$V_{CSOP} - V_{CSOP} = 20mV$		645		mV
			-5.70	0.75	7.40	%
		$V_{CSOP} - V_{CSOP} = 10mV$		325		mV
			-7.5	1.7	11.5	%
BMON Current Sourcing Capability	$I_{BMON_MAX_SR}$		120	285	460	μA
BMON Current Sinking Capability	$I_{BMON_MAX_SK}$		5.5	11.4	17.5	μA
PSYS Output Current $R_{S1} = 10m\Omega$ $R_{S2} = 10m\Omega$ PSYS Current Gain = $1.14\mu A/W$	I_{PSYS}	$V_{CSIP} = 19V, V_{CSIP} - V_{CSIN} = 80mV,$ $V_{BAT} = 12V, V_{CSOP} - V_{CSOP} = 0mV$		174		μA
			-8.3	0.4	9.1	%
		$V_{CSIP} = 19V, V_{CSIP} - V_{CSIN} = 80mV,$ $V_{BAT} = 12V, V_{CSOP} - V_{CSOP} = 20mV$		146.5		μA
			-8.2	0.4	9	%
		$V_{CSIP} = 19V, V_{CSIP} - V_{CSIN} = 80mV,$ $V_{BAT} = 12V, V_{CSOP} - V_{CSOP} = -20mV$		199.5		μA
	-8.4	-0.6	7.2	%		
		$V_{CSIP} = 0V, V_{CSIP} - V_{CSIN} = 0mV,$ $V_{BAT} = 12V, V_{CSOP} - V_{CSOP} = -20mV$		26.2		μA
			-15.2	-4.2	6.8	%
Maximum PSYS Output Voltage	V_{PSYS_MAX}	$I_{PSYS} = 200\mu A$		2.25		V
NTC Source Current	I_{NTC}	NTC = 1V	9.71	10.08	10.44	μA
NTC_PROCHOT# Trip Threshold	V_{NTC_TH}	V_{NTC} falling	161	171	182	mV
NTC_PROCHOT# Hysteresis	V_{NTC_HYS}		18	27	36	mV
ACIN/ACOK Comparator						
ACIN Threshold Rising	$V_{ACIN_TH_R}$	V_{ACIN} rising		2.041	2.070	V
ACIN Threshold Falling	$V_{ACIN_TH_F}$	V_{ACIN} falling	1.995	2.024		V
ACIN OVP Rising	$V_{ACIN_OVP_TH_R}$	V_{ACIN} rising		3.5	3.7	V
ACIN OVP Falling	$V_{ACIN_OVP_TH_F}$	V_{ACIN} falling	3.30	3.45		V
ACIN Input Leakage Current	I_{ACIN_LEAK}		-1		1	μA
ACOK Input Leakage Current	I_{ACOK_LEAK}		-1		1	μA
ACOK Output Low Current	I_{ACOK}	$V_{ACOK} = 0.3V$		240		μA
ACLIM, CCLIM						
ACLIM Current Limit		$V_{ACLIM} = 2.56V, R_{S1} = 10m\Omega$	7970	8075	8175	mA
		$V_{ACLIM} = 1.92V, R_{S1} = 10m\Omega$	5970	6060	6150	mA
		$V_{ACLIM} = 1.28V, R_{S1} = 10m\Omega$	3975	4050	4125	mA

Operating Conditions: $V_{DD} = 5V$, $T_A = 0^{\circ}C$ to $+85^{\circ}C$ unless otherwise noted. **Boldface limits apply across the operating temperature range, $0^{\circ}C$ to $+85^{\circ}C$.** (Continued)

Parameter	Symbol	Test Conditions	Min Note 6	Typ	Max Note 6	Unit
CCLIM Current Limit		$V_{CCLIM} = 2.56V$, $R_{S1} = 10m\Omega$, $R_{S2} = 5m\Omega$	7855	8070	8265	mA
		$V_{CCLIM} = 1.92V$, $R_{S1} = 10m\Omega$, $R_{S2} = 5m\Omega$	5875	6050	6205	mA
		$V_{CCLIM} = 1.28V$, $R_{S1} = 10m\Omega$, $R_{S2} = 5m\Omega$	3900	4035	4155	mA
		$V_{CCLIM} = 2.56V$, $R_{S1} = 10m\Omega$, $R_{S2} = 10m\Omega$	7860	8065	8250	mA
		$V_{CCLIM} = 1.92V$, $R_{S1} = 10m\Omega$, $R_{S2} = 10m\Omega$	5895	6045	6185	mA
		$V_{CCLIM} = 1.28V$, $R_{S1} = 10m\Omega$, $R_{S2} = 10m\Omega$	3930	4035	4135	mA
		$V_{CCLIM} = 2.56V$, $R_{S1} = 20m\Omega$, $R_{S2} = 20m\Omega$	3930	4030	4130	mA
		$V_{CCLIM} = 1.92V$, $R_{S1} = 20m\Omega$, $R_{S2} = 20m\Omega$	2945	3025	3100	mA
$V_{CCLIM} = 1.28V$, $R_{S1} = 20m\Omega$, $R_{S2} = 20m\Omega$	1960	2015	2075	mA		
PROCHOT#						
PROCHOT# Leakage Current	$I_{PROCHOT\#_LEAK}$		-1		1	μA
PROCHOT# Output Low Current	$I_{PROCHOT\#}$	$V_{PROCHOT\#} = 0.3V$		42		mA
Low VSYS PROCHOT# Trip Threshold	$V_{LOW_VSYS_HOT}$	Control1 register Bit<9:8> = 00	5.48	5.62	5.76	V
		Control1 register Bit<9:8> = 01	5.97	6.11	6.25	V
		Control1 register Bit<9:8> = 10	6.44	6.59	6.73	V
		Control1 register Bit<9:8> = 11	6.90	7.05	7.20	V
PROCHOT# Debounce Time		PROCHOT# debounce register Bit<1:0> = 01		102		μs
		PROCHOT# debounce register Bit<1:0> = 10		510		μs
PROCHOT# Duration Time		PROCHOT# duration register Bit<2:0> = 010		15.3		ms
		PROCHOT# duration register Bit<2:0> = 101		1.02		ms
BATGONE Threshold						
BATGONE Threshold Rising	$V_{BATGONE_TH_R}$	$V_{BATGONE}$ rising (battery removal)		2.58	2.75	V
BATGONE Threshold Falling	$V_{BATGONE_TH_F}$	$V_{BATGONE}$ falling (battery insertion)	1.80	2.12		V
LDO						
Output Voltage		$V_{DCIN} = 6V$ to $25V$, $I_{VDDP} = 1mA$	4.80	5.24	5.75	V
		$V_{DCIN} = 6V$, $I_{VDDP} = 30mA$	4.65	5.12	5.65	V
		$V_{DCIN} = 25V$, $I_{VDDP} = 30mA$	4.75	5.22	5.70	V
Gate Driver						
UGATE Pull-up Resistance Note 7	R_{UGPU}	200mA source current		1.0	1.5	Ω
UGATE Source Current	I_{UGSRC}	UGATE - PHASE = 2.5V		2.0		A
UGATE Sink Resistance Note 7	R_{UGPD}	250mA sink current		1.0	1.5	Ω
UGATE Sink Current	I_{UGSNK}	UGATE - PHASE = 2.5V		2.0		A
LGATE Pull-up Resistance Note 7	R_{LGPU}	250mA source current		1.0	1.5	Ω
LGATE Source Current	I_{LGSRC}	LGATE - GND = 2.5V		2.0		A
LGATE Sink Resistance Note 7	R_{LGPD}	250mA sink current		0.5	0.9	Ω
LGATE Sink Current	I_{LGSNK}	LGATE - GND = 2.5V		4.0		A

Operating Conditions: $V_{DD} = 5V$, $T_A = 0^\circ\text{C}$ to $+85^\circ\text{C}$ unless otherwise noted. **Boldface limits apply across the operating temperature range, 0°C to $+85^\circ\text{C}$.** (Continued)

Parameter	Symbol	Test Conditions	Min Note 6	Typ	Max Note 6	Unit
UGATE to LGATE Dead Time	t_{UGFLGR}	UGATE falling to LGATE rising, no load		17		ns
LGATE to UGATE Dead Time	t_{LGFUGR}	LGATE falling to UGATE rising, no load		29		ns
ASGATE Pull-Up Resistance	R_{ASGPU}	1mA source current		500		Ω
ASGATE Sink Resistance	R_{ASGPD}	1mA sink current		1300		Ω
BGATE Pull-Up Resistance	R_{BGPU}	1mA source current		500		Ω
BGATE Sink Resistance	R_{BGPD}	1mA sink current		1300		Ω
Bootstrap Switch						
ON-Resistance	R_F			20		Ω
Reverse Leakage	I_R	$V_R = 25V$		0.2		μA
Amplifiers						
Adapter Current Sense Amplifier Input Offset	V_{ACSNS_OFFSET}			0.4		mV
Battery Charging Current Sense Amplifier Input Offset	$V_{ICHGSNS_OFFSET}$			0.4		mV
Battery Discharging Current Sense Amplifier Input Offset	$V_{IDISSNS_OFFSET}$			0.4		mV
Error Amplifier DC Gain	A_{V0_EA}			80		dB
Error Amp Gain Bandwidth Product	GBW_EA	$C_L = 20\text{pF}$		5		MHz
COMP Lower Clamp	$V_{COMP_L_CLP}$			1.24	1.40	V
COMP Upper Clamp	$V_{COMP_U_CLP}$		4.90	4.99		V
Over-Temperature Protection						
Over-Temperature Threshold	T_{OTP_R}	Temperature rising		155		$^\circ\text{C}$
	T_{OTP_F}	Temperature falling		128		$^\circ\text{C}$
SMBus						
SDA/SCL Input Low Voltage					0.8	V
SDA/SCL Input High Voltage			2			V
SDA/SCL Input Bias Current		SDA, SCL = 0V, 5V	-1		1	μA
SDA, Output Sink Current Note 8		SDA = 0.4V		19		mA
SMBus Frequency	f_{SMB}	Note 8	10		400	kHz
Bus Free Time	t_{BUF}	100kHz, Note 8	4.7			μs
		400kHz, Note 8	1.3			μs
Start Condition Hold Time from SCL	t_{HD_STA}	100kHz, Note 8	4			μs
		400kHz, Note 8	0.6			μs
Start Condition Set-Up Time from SCL	t_{SU_STA}	100kHz, Note 8	4.7			μs
		400kHz, Note 8	0.6			μs
Stop Condition Set-Up Time from SCL	t_{HD_STO}	100kHz, Note 8	4			μs
		400kHz, Note 8	0.6			μs
SDA Hold Time from SCL	t_{HD_DAT}	100kHz, Note 8	300			ns
		400kHz, Note 8	300			ns

Operating Conditions: $V_{DD} = 5V$, $T_A = 0^{\circ}C$ to $+85^{\circ}C$ unless otherwise noted. **Boldface limits apply across the operating temperature range, $0^{\circ}C$ to $+85^{\circ}C$.** (Continued)

Parameter	Symbol	Test Conditions	Min Note 6	Typ	Max Note 6	Unit
SDA Set-Up Time from SCL	t_{SU_DAT}	100kHz, Note 8	250			ns
		400kHz, Note 8	100			ns
SCL Low Period	t_{LOW}	100kHz, Note 8	4.7			μs
		400kHz, Note 8	1.3			μs
SCL High Period	t_{HIGH}	100kHz, Note 8	4			μs
		400kHz, Note 8	0.6			μs
SDA/SCL Rise Time	t_{RISE}	100kHz, 400pF, maximum load, Note 8			1000	ns
		400kHz, 400pF, maximum load, Note 8			300	ns
SDA/SCL Fall Time	t_{FALL}	100kHz, 400pF, maximum load, Note 8			300	ns
		400kHz, 400pF, maximum load, Note 8			300	ns
SMBus Inactivity Time-Out Note 8		Maximum period without a SMBus write to MaxChargeVoltage or ChargeCurrent register		175		s

Notes:

- Parameters with MIN and/or MAX limits are 100% tested at $+25^{\circ}C$, unless otherwise specified. Temperature limits established by characterization and are not production tested.
- Limits established by characterization and are not production tested.
- Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

2.5 Gate Driver Timing Diagram

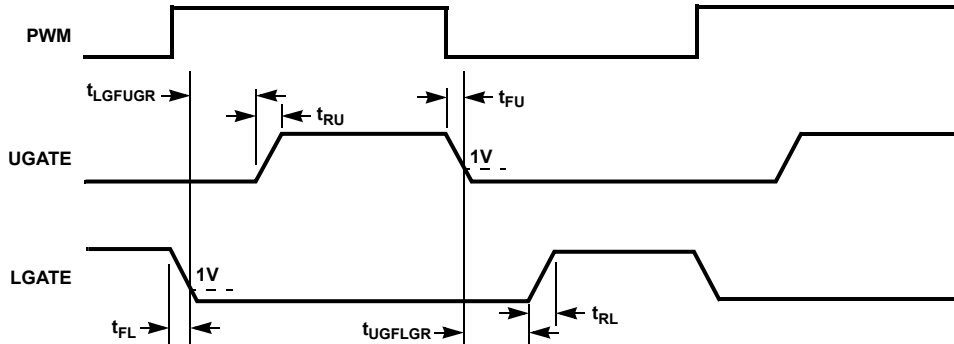


Figure 5. Gate Driver Timing Diagram

3. Typical Performance Curves

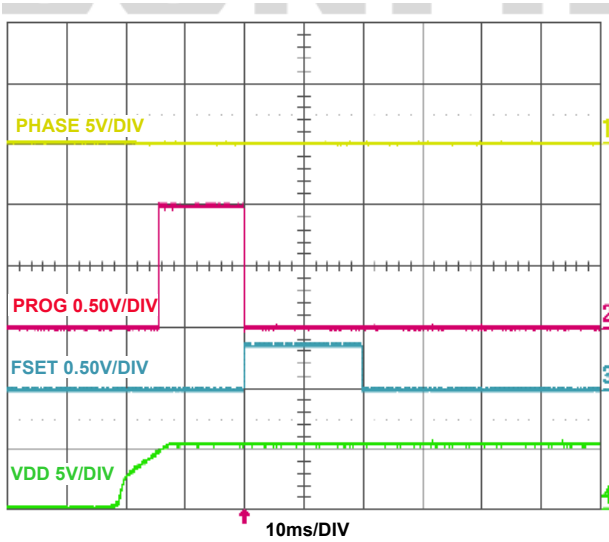


Figure 6. Power-Up, Read Prog, and FSET Resistors

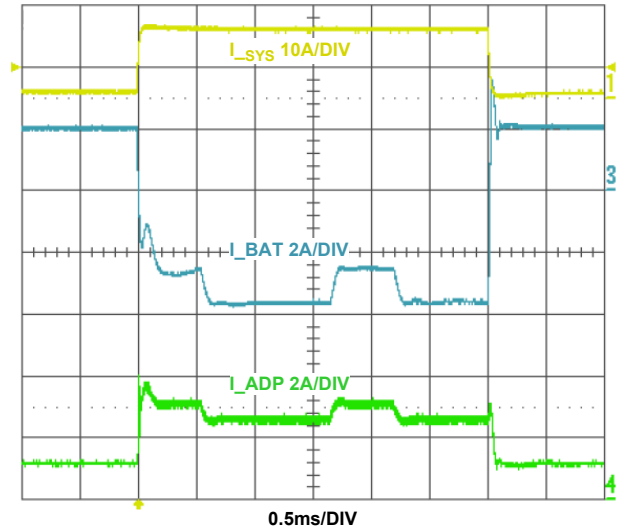


Figure 7. Two Level Adapter Current Limit. VADP = 20V, AdapterCurrentLimit1 = 2.56A, AdapterCurrentLimit2 = 3.072A, T2 = 500µs, T1 = 1ms, V_{BAT} = 7V, MaxChargeVoltage = 8.192V, ChargeCurrent = 2.016A, 1A to 12A System Load Step

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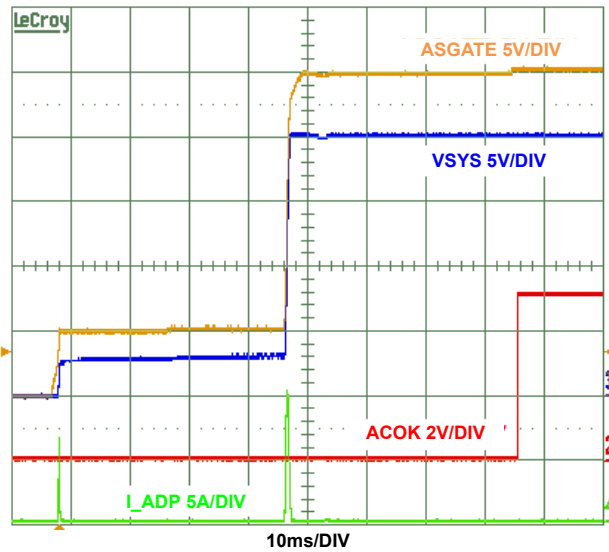


Figure 8. HPB: Adapter Insertion ASGATE Inrush Current Control. No Battery, VADP = 20V, 330µF System Rail Capacitance

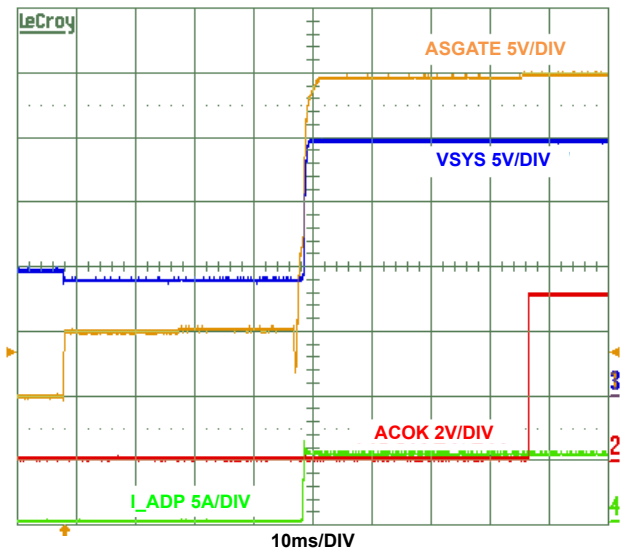


Figure 9. Insertion. V_{BAT} = 10V, VADP = 20V, ACLIM Setting = 5A, System Load = 5.5A

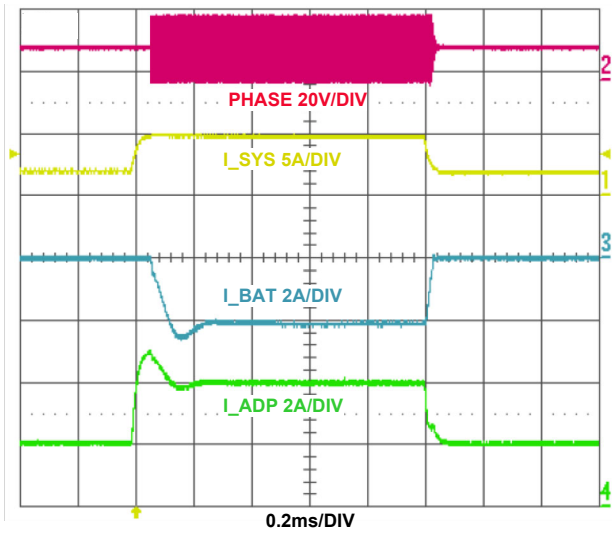


Figure 10. HPB: Charge Disabled, Enter Turbo Mode. VADP = 20V, V_{BAT} = 10V, AdapterCurrentLimit1 = 4.096A, 2A to 5A Load Step

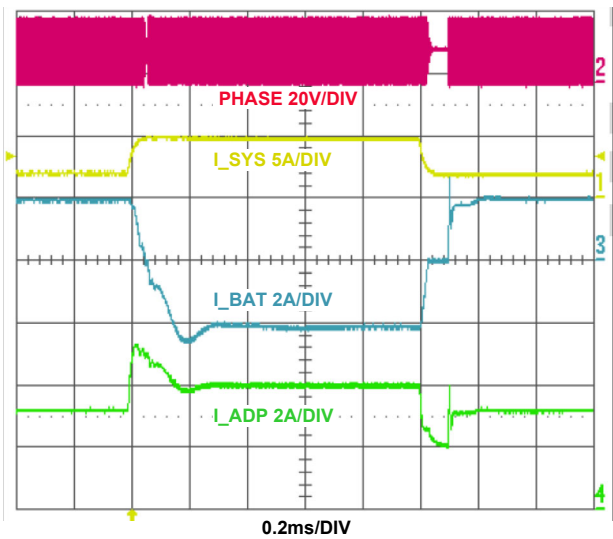


Figure 11. HPB: Charge Enabled, Enter Turbo Mode. VADP = 20V, V_{BAT} = 10V, AdapterCurrentLimit1 = 4.096A, ChargeCurrent = 2.016A, 2A to 5A Load Step

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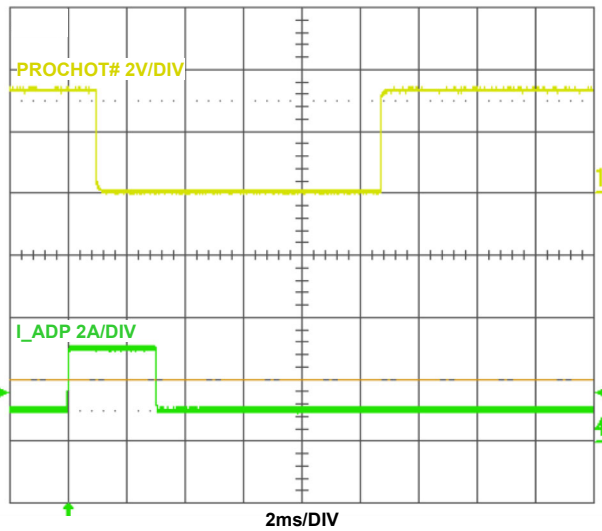


Figure 12. ACPROCHOT# Assertion. ACPROCHOT = 2.048A, PROCHOTDebounce = 1ms, PROCHOTDuration = 10ms

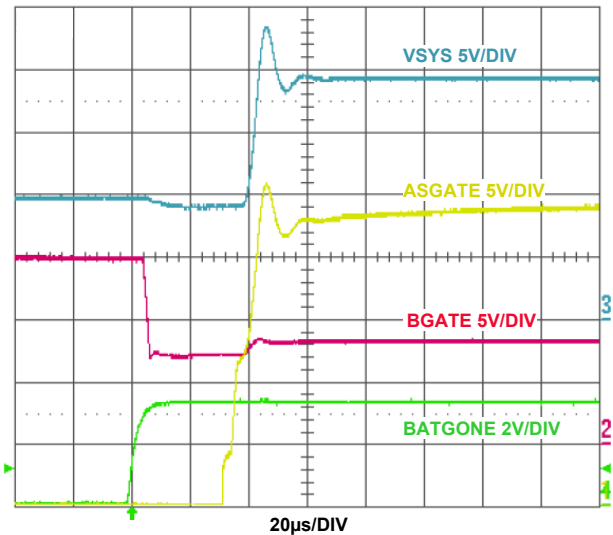


Figure 13. HPB: Battery Sudden Removal in Learn Mode by Pulling BATGONE to High

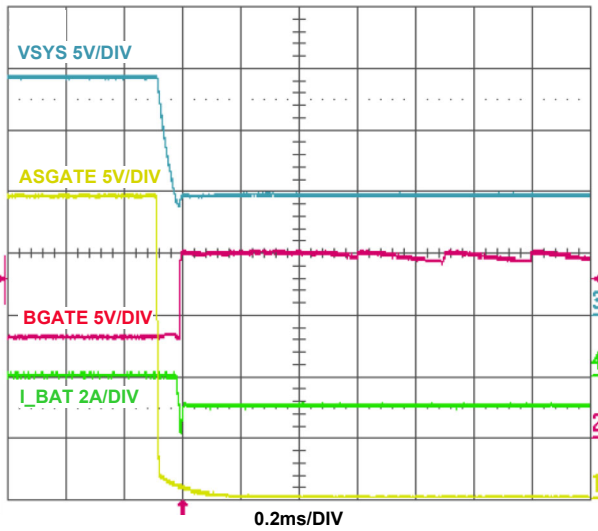


Figure 14. HPB: Enter Learn Mode

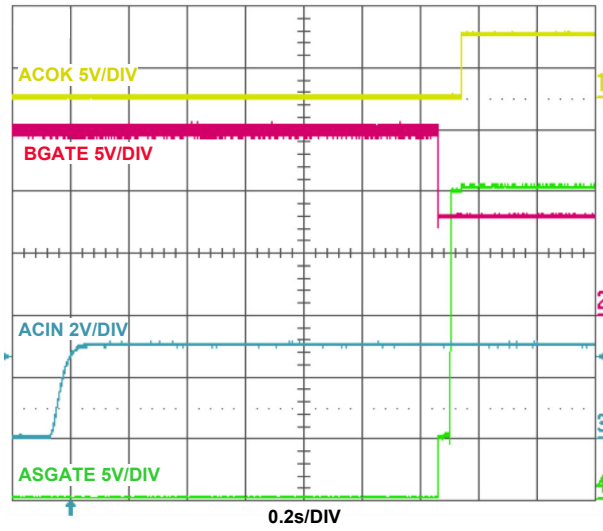


Figure 15. HPB: ASGATE Turning On Delay After Adapter Insertion. $V_{ADP} = 20V$, $V_{BAT} = 10V$, Control2 Register Bit<5> = 0

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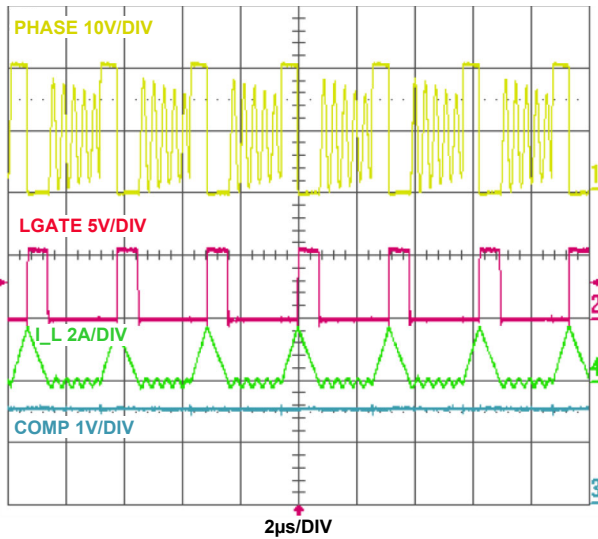


Figure 16. Discontinuous Conduction Mode (DCM) Switching

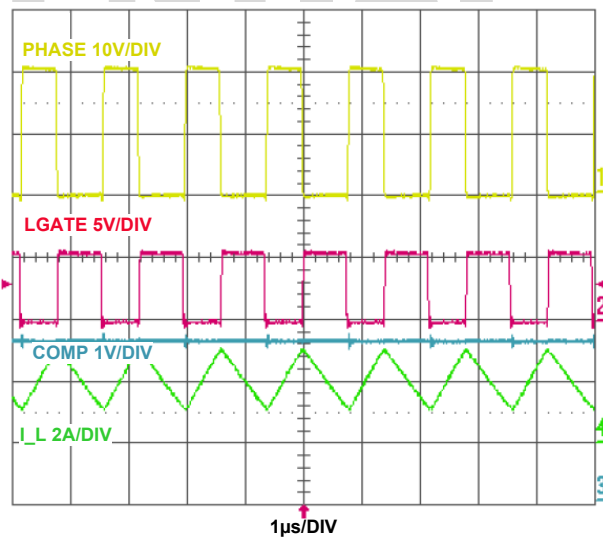


Figure 17. Continuous Conduction Mode (CCM) Switching

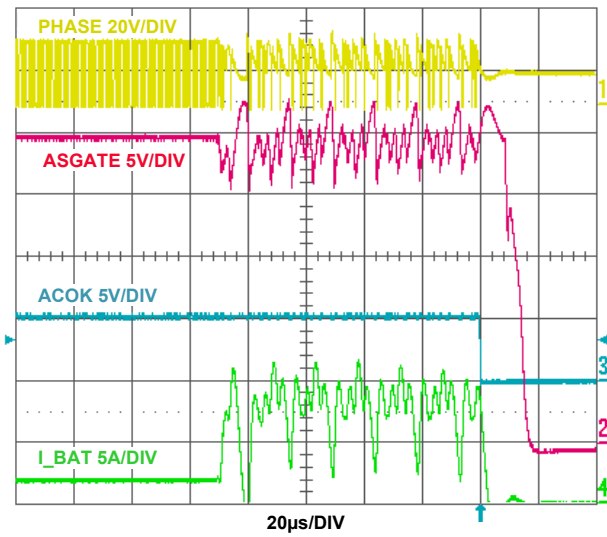


Figure 18. WOCP: Inductor Short During Charging.
 VADP = 20V, V_{BAT} = 10V, ChargeCurrent = 2A,
 CCLIM = 2V

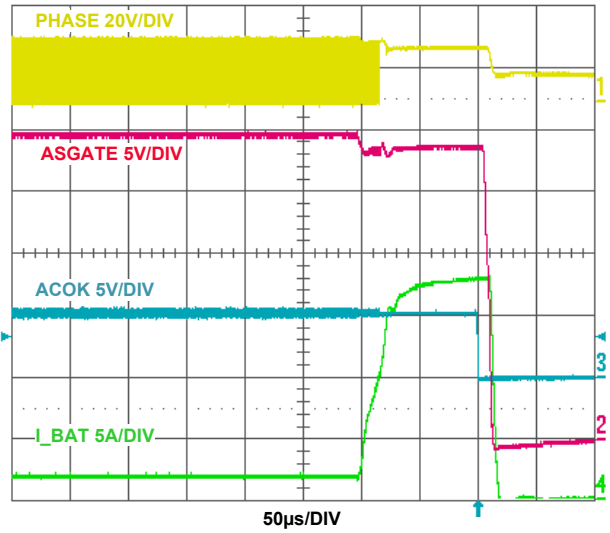


Figure 19. WOCP: High-Side MOSFET Short During Charging. VADP = 20V, V_{BAT} = 10V, ChargeCurrent = 2A,
 CCLIM = 2V

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4. General SMBus Architecture

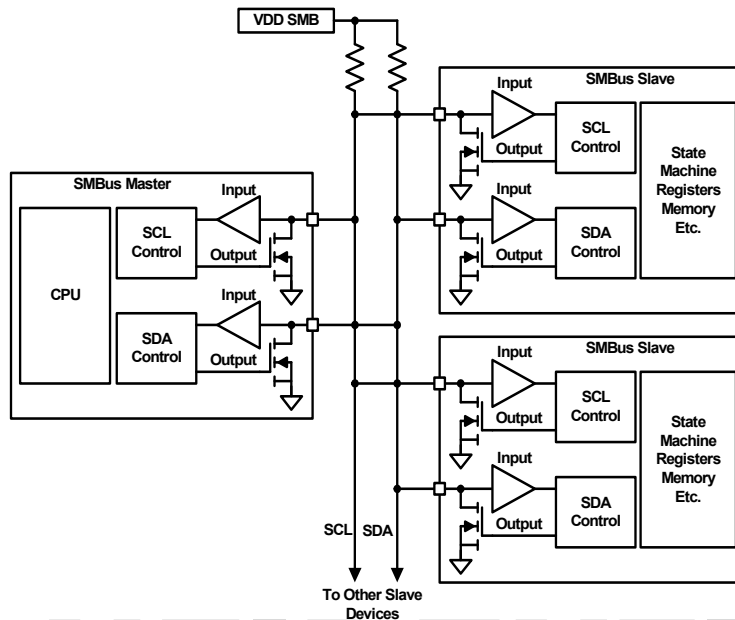


Figure 20. General SMBus Architecture

4.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a Start or Stop condition. The HIGH or LOW state of the data line can change only when the clock signal on the SCL line is LOW. See [Figure 21](#) for an illustration of data validity.

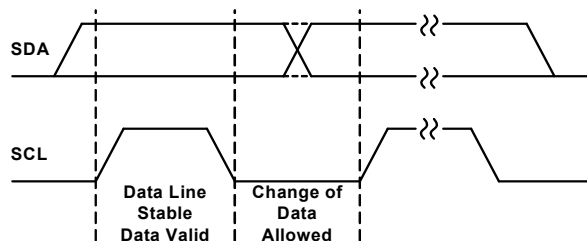


Figure 21. Data Validity

4.2 Start and Stop Conditions

The Start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH, as illustrated in [Figure 22](#). The Stop condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A Stop condition must be sent before each Start condition.

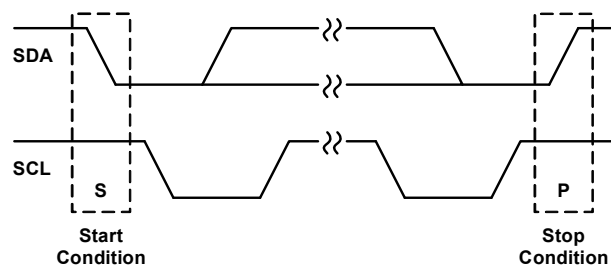


Figure 22. Start and Stop Waveforms

4.3 Acknowledge

Each address and data transmission uses 9-clock pulses. The ninth pulse is the acknowledge bit (ACK). After the start condition, the master sends seven slave address bits and a Read/Write (R/W) bit during the next 8-clock pulses. During the 9-clock pulse, the device that recognizes its own address holds the data line low to acknowledge (as shown in Figure 23). Both the master and the slave use the ACK bit to acknowledge receipt of register addresses and data.

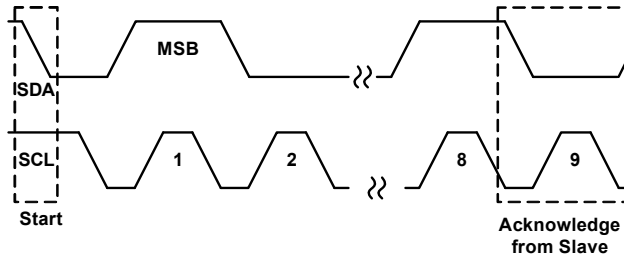


Figure 23. Acknowledge on the SMBus

4.4 SMBus Transactions

All transactions start with a control byte sent from the SMBus master device. The control byte begins with a Start condition, followed by seven bits of slave address (0001001 for the ISL88739B) and the R/W bit. The R/W bit is 0 for a WRITE or 1 for a READ. If any slave device on the SMBus bus recognizes its address, it acknowledges by pulling the Serial Data (SDA) line low for the last clock cycle in the control byte. If no slave exists at that address or it is not ready to communicate, the data line is 1, indicating a Not Acknowledge condition.

After the control byte is sent and the ISL88739B acknowledges it, the second byte sent by the master must be a register address byte, such as 0x14 for the ChargeCurrent register. The register address byte tells the ISL88739B which register the master writes or reads. See Table 2 on page 24 for register details. When the ISL88739B receives a register address byte, it responds with an acknowledge.

4.5 Byte Format

Every byte on the SDA line must be eight bits long and must be followed by an acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first and the Least Significant Bit (LSB) last. The LO BYTE data is transferred before the HI BYTE data. For example, when writing 0x41A0, 0xA0 is sent first and 0x41 is sent second.

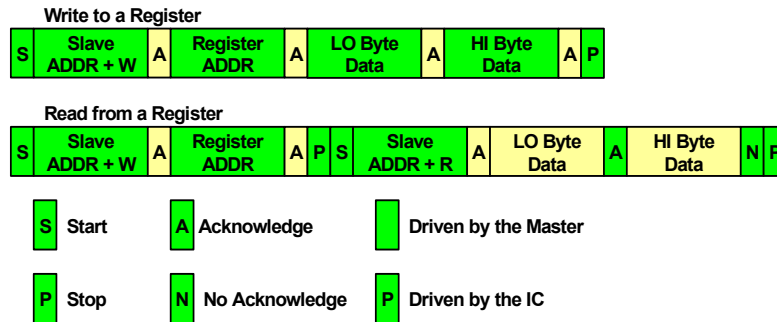


Figure 24. SMBus Read and Write Protocol

4.6 SMBus and I²C Compatibility

The ISL88739B SMBus minimum input logic high voltage is 2V, so it is compatible with an I²C that has a 2V pull-up power supply higher than 2V.

The ISL88739B SMBus registers are 16 bits, so it is compatible with a 16-bit I²C or 8-bit I²C with an auto-increment capability.

5. ISL88739B SMBus Commands

The ISL88739B receives control inputs from the SMBus interface after Power-On Reset (POR). The serial interface complies with the System Management Bus Specification, which can be downloaded from www.smbus.org. The ISL88739B uses the SMBus Read Word and Write Word protocols shown in [Figure 24 on page 23](#) to communicate with the host system and a smart battery. The ISL88739B is an SMBus slave device and does not initiate communication on the bus. It responds to the 7-bit address 0b0001001_:

- Read address = 0b00010011 (0X13H)
- Write address = 0b00010010 (0X12H)

The data (SDA) and clock (SCL) pins have Schmitt-trigger inputs that can accommodate slow edges. Choose pull-up resistors for SDA and SCL to achieve rise times according to the SMBus specifications.

The ISL88739B allows users to change the SMBus registers to change some functions and options, as shown in [Table 2](#).

The illustration in this datasheet is based on current-sensing resistors $R_{s1} = 10\text{m}\Omega$ and $R_{s2} = 10\text{m}\Omega$ unless specified otherwise. For other current-sensing resistor specifications, see [Tables 17](#) and [18](#) on [page 39](#) for more information.

Table 2. Registers Summary ($R_{s1} = 10\text{m}\Omega$ and $R_{s2} = 10\text{m}\Omega$)

Register Names	Register Address	Read/Write	Number of Bits	Description	POR Bit State
ChargeCurrentLimit	0x14H	R/W	8	Bits<12:5> are used. If Bit<0> is interpreted as 1mA, the resolution is 32mA and the POR default value is 0A.	<12:5> 00000000
AdapterCurrentLimit1	0x3FH	R/W	6	Bits<12:7> are used. If Bit<0> is interpreted as 1mA, the resolution is 128mA and the POR default value is 8.064A.	<12:7> 111111
AdapterCurrentLimit2	0x3BH	R/W	6	Bits<12:7> are used. If Bit<0> is interpreted as 1mA, the resolution is 128mA and the POR default value is 8.064A.	<12:7> 111111
T1	0x37H	R/W	3	Bits<2:0> are used. If the 2-level adapter current limit function is enabled and tripped, T1 configures the effective duration of the AdapterCurrentLimit1 register. The POR default value is 500 μ s.	<2:0> 110
T2	0x38H	R/W	3	Bits<2:0> are used. If the 2-level adapter current limit function is enabled and tripped, T2 configures the effective duration of the AdapterCurrentLimit2 register. The POR default value is 100 μ s.	<2:0> 001
MaxChargeVoltage	0x15H	R/W	11	Bits<14:4> are used. If Bit<0> is interpreted as 1mV, resolution is 16mV. The POR default value is based on PROG pin cell number programming: 2-cell: 8.192V 3-cell: 12.288V 4-cell: 16.4V MaxChargeVoltage register should always be programmed higher than MinChargeVoltage register.	

Table 2. Registers Summary ($R_{s1} = 10m\Omega$ and $R_{s2} = 10m\Omega$) (Continued)

Register Names	Register Address	Read/Write	Number of Bits	Description	POR Bit State
MinChargeVoltage	0x3EH	R/W	6	Bits<13:8> are used. If Bit<0> is interpreted as 1mV, resolution is 256mV. The POR default value is based on PROG pin cell number programming: 2-cell: 5.376V 3-cell: 8.064V 4-cell: 10.752V MinChargeVoltage should always be programmed lower than MaxChargeVoltage.	
PROCHOTDebounce	0x39H	R/W	2	Bits<1:0> are used. Set the debounce time before asserting the PROCHOT# signal for NTC_PROCHOT#, ACPROCHOT# and DCPROCHOT#. The POR default value is 100 μ s.	<1:0> 01
PROCHOTDuration	0x3AH	R/W	3	Bits<2:0> are used. Sets the minimum duration of PROCHOT# signal latch-up when it is asserted. The POR default value is 10ms.	<2:0> 011
ACPROCHOT	0x47H	R/W	6	Bits<12:7> are used. Set PROCHOT# threshold for adapter overcurrent condition. If Bit<0> is interpreted as 1mA, resolution is 128mA and POR default value is 6.144A.	<12:7> 110000
DCPROCHOT	0x48H	R/W	6	Sets PROCHOT# threshold for battery over-discharging current condition. Bits<12:7> are used. If Bit<0> is interpreted as 1mA, resolution is 128mA and POR default value is 4.096A.	<12:7> 100000
Control1	0x3DH	R/W	16	See Table 13 , Control1 Register 0x3DH.	
Control2	0x3CH	R/W	12	See Table 14 , Control2 Register 0x3CH.	
Information1	0x46H	R	8	Contains various information reported over SMBus. See Information1 register Table 15 .	
Information2	0x45H	R/W	8	PROG pin resistor reading result report. Also configures the 20m Ω current-sensing resistor option. See Table 16 , Information2 Register 0x45H.	
ManufacturerID	0xFEH	R	8	ASCII for "I".	0x49H
DeviceID	0xFFH	R	8	Device ID register. Read only.	0x09H

5.1 Setting Charging Current Limit

To set the charging current limit, write a 16-bit ChargeCurrentLimit command (0X14H or 0b00010100) using the Write Word protocol shown in [Figure 24 on page 23](#) and the data format shown in [Table 3](#).

The ISL88739B limits the charging current by limiting the $V_{CSOP} - V_{CSOIN}$ voltage. By using the recommended current sense resistor values shown in [Table 17 on page 39](#), the register's LSB always translates to 1mA of charging current. The ChargeCurrentLimit register accepts any charging current command; however, only the valid register bits are written to the register. Do not set the charging current limit lower than 96mA.

After POR, the ChargeCurrentLimit register is reset to 0x0000H. To set the battery charging current value, write a valid, non-zero number to the ChargeCurrentLimit register. The ChargeCurrentLimit register can be read back to verify its content.

[Table 20 on page 46](#) shows the conditions to enable fast charging according to the ChargeCurrentLimit register setting for the HPB configuration.

Table 3. ChargeCurrentLimit Register 0x14H ($R_{S1} = 10m\Omega$ and $R_{S2} = 10m\Omega$).
(See [Table 18 on page 40](#) for other configurations)

Bit	Description
<4:0>	Not used
<5>	0 = Add 0mA of charging current limit. 1 = Add 32mA of charging current limit.
<6>	0 = Add 0mA of charging current limit. 1 = Add 64mA of charging current limit.
<7>	0 = Add 0mA of charging current limit. 1 = Add 128mA of charging current limit.
<8>	0 = Add 0mA of charging current limit. 1 = Add 256mA of charging current limit.
<9>	0 = Add 0mA of charging current limit. 1 = Add 512mA of charging current limit.
<10>	0 = Add 0mA of charging current limit. 1 = Add 1024mA of charging current limit.
<11>	0 = Add 0mA of charging current limit. 1 = Add 2048mA of charging current limit.
<12>	0 = Add 0mA of charging current limit. 1 = Add 4096mA of charging current limit.
<15:13>	Not used

5.2 Setting Adapter Current Limit

To set the adapter current limit, write a 16-bit AdapterCurrentLimit1 command (0x3FH or 0b00111111) and/or AdapterCurrentLimit2 command (0x3BH or 0b00111011) using the Write Word protocol shown in [Figure 24 on page 23](#) and the data format shown in [Table 4 on page 27](#).

The ISL88739B limits the adapter current by limiting the $V_{CSIP} - V_{CSIN}$ voltage. By using the recommended current sense resistor value as [Table 17 on page 39](#) shows, the register's LSB always translates to 1mA adapter current. Any adapter current limit command is accepted; however, only the valid register bits are written to the AdapterCurrentLimit1 and AdapterCurrentLimit2 registers. The minimum adapter current limit command is 128mA and a 0A command is rejected.

After POR, the AdapterCurrentLimit1 and AdapterCurrentLimit2 registers are reset to 0x1F80. The AdapterCurrentLimit1 and AdapterCurrentLimit2 registers can be read back to verify their content.

To set a second level adapter current limit, write a 16-bit AdapterCurrentLimit2 (0x3BH or 0b00111011) command using the Write Word protocol shown in [Figure 24](#) and the data format as shown in [Table 4](#).

The AdapterCurrentLimit2 register has the same specification as the AdapterCurrentLimit1 register. See [“Two-Level Adapter Current Limit” on page 46](#) for detailed operation.

Table 4. AdapterCurrentLimit1 Register 0x3FH and AdapterCurrentLimit2 Register 0x3BH
($R_{s1} = 10m\Omega$ and $R_{s2} = 10m\Omega$)

Bit	Description
<6:0>	Not used
<7>	0 = Add 0mA of adapter current limit. 1 = Add 128mA of adapter current limit.
<8>	0 = Add 0mA of adapter current limit. 1 = Add 256mA of adapter current limit.
<9>	0 = Add 0mA of adapter current limit. 1 = Add 512mA of adapter current limit.
<10>	0 = Add 0mA of adapter current limit. 1 = Add 1024mA of adapter current limit.
<11>	0 = Add 0mA of adapter current limit. 1 = Add 2048mA of adapter current limit.
<12>	0 = Add 0mA of adapter current limit. 1 = Add 4096mA of adapter current limit.
<15:13>	Not used

5.3 Setting Two-Level Adapter Current Limit Duration

For a two-level adapter current limit, write a 16-bit T1 command (0x37H or 0b00110111) using the Write Word protocol shown in [Figure 24 on page 23](#) and the data format shown in [Table 5](#) to set the AdapterCurrentLimit1 duration as the adapter current limit. Write a 16-bit T2 command (0x38H or 0b00111000) to set AdapterCurrentLimit2 duration as the adapter current limit. The T1 register and T2 register accept any command; however, only the valid register bits are written. See [“Two-Level Adapter Current Limit” on page 46](#) for detailed operation.

Table 5. T1 Register 0x37H

Bit	Description
<2:0>	000 = 0ms 001 = 20ms 010 = 15ms 011 = 10ms 100 = 5ms 101 = 1ms 110 = 0.5ms 111 = 0.1ms
<15:3>	Not used

Table 6. T2 Register 0x38H

Bit	Description
<2:0>	000 = 15 μ s 001 = 100 μ s 010 = 500 μ s 011 = 1ms 100 = 300 μ s 101 = 750 μ s 110 = 3ms 111 = 10ms
<15:3>	Not used

5.4 Setting Maximum Charging Voltage

To set the maximum charging voltage, write a 16-bit MaxChargeVoltage command (0X15H or 0b00010101) using the Write Word protocol shown in [Figure 24 on page 23](#) and the data format shown in [Table 7](#).

The maximum charging voltage range is 7.168V to 18.432V. The MaxChargeVoltage register accepts any voltage command; however, only the valid register bits are written to the register.

The MaxChargeVoltage register sets the battery full charging voltage limit. The CSON pin senses the battery voltage for maximum charging voltage regulation.

Table 7. MaxChargeVoltage Register 0x15H

Bit	Description
<3:0>	Not used
<4>	0 = Add 0mV of charging voltage. 1 = Add 16mV of charging voltage.
<5>	0 = Add 0mV of charging voltage. 1 = Add 32mV of charging voltage.
<6>	0 = Add 0mV of charging voltage. 1 = Add 64mV of charging voltage.
<7>	0 = Add 0mV of charging voltage. 1 = Add 128mV of charging voltage.
<8>	0 = Add 0mV of charging voltage. 1 = Add 256mV of charging voltage.
<9>	0 = Add 0mV of charging voltage. 1 = Add 512mV of charging voltage.
<10>	0 = Add 0mV of charging voltage. 1 = Add 1024mV of charging voltage.
<11>	0 = Add 0mV of charging voltage. 1 = Add 2046mV of charging voltage.
<12>	0 = Add 0mV of charging voltage. 1 = Add 4096mV of charging voltage.
<13>	0 = Add 0mV of charging voltage. 1 = Add 8192mV of charging voltage.
<14>	0 = Add 0mV of charging voltage. 1 = Add 16384mV of charging voltage.
<15>	Not used

5.5 Setting Minimum Charging Voltage

To set the minimum charging voltage, write a 16-bit MinChargeVoltage command (0x3EH or 0b00111110) using the Write Word protocol shown in [Figure 24](#) and the data format shown in [Table 8](#).

The minimum charging voltage range is 2.048V to 16.128V. The MinChargeVoltage register accepts any voltage command; however, only the valid register bits are written to the register. The MinChargeVoltage register value should be set lower than the MaxChargeVoltage register value.

The MinChargeVoltage register sets the battery voltage threshold for entry and exit of the Trickle Charge mode. The VBAT pin senses the battery voltage to compare with the MinChargeVoltage register setting. See [“Trickle Charging” on page 47](#) for details.

Table 8. MinChargeVoltage Register 0x3EH

Bit	Description
<7:0>	Not used
<8>	0 = Add 0mV of charging voltage. 1 = Add 256mV of charging voltage.
<9>	0 = Add 0mV of charging voltage. 1 = Add 512mV of charging voltage.
<10>	0 = Add 0mV of charging voltage. 1 = Add 1024mV of charging voltage.
<11>	0 = Add 0mV of charging voltage. 1 = Add 2048mV of charging voltage.
<12>	0 = Add 0mV of charging voltage. 1 = Add 4096mV of charging voltage.
<13>	0 = Add 0mV of charging voltage. 1 = Add 8192mV of charging voltage.
<15:14>	Not used

5.6 Setting PROCHOT# Debounce Time

To set the PROCHOT# signal debounce time before its assertion for ACPROCHOT, DCPROCHOT, and NTC_PROCHOT, write a 16-bit PROCHOT# debounce time (0x39H or 0b00111001) using the Write Word protocol shown in [Figure 24 on page 23](#) and the data format as shown in [Table 9](#). The PROCHOT# Debounce Time register accepts any command; however, only the valid register bits are written.

The low system voltage PROCHOT# has a fixed debounce time of 10 μ s.

Table 9. PROCHOTDebounce Register 0x39H

Bit	Description
<1:0>	00 = 10 μ s 01 = 100 μ s 10 = 500 μ s 11 = 1ms
<15:2>	Not used

5.7 Setting PROCHOT# Duration

To set the PROCHOT# signal latch-up duration when it is asserted for ACPROCHOT, DCPROCHOT, and NTC_PROCHOT and low system voltage PROCHOT, write a 16-bit PROCHOT# Duration command (0x3AH or 0b01111010) using the Write Word protocol shown in [Figure 24 on page 23](#) and the data format shown in [Table 10](#). PROCHOT# Duration register accepts any command; however, only the valid register bits are written.

Table 10. PROCHOT# Duration Register 0x3AH

Bit	Description
<2:0>	000 = 0ms 001 = 20ms 010 = 15ms 011 = 10ms 100 = 5ms 101 = 1ms 110 = 500μs 111 = 100μs
<15:3>	Not used

5.8 Setting PROCHOT# Threshold for Adapter Overcurrent Condition

To set the PROCHOT# assertion threshold for the adapter overcurrent condition, write a 16-bit ACPROCHOT command (0x47H or 0b01000111) using the Write Word protocol shown in [Figure 24 on page 23](#) and the data format shown in [Table 11](#). By using the recommended current sense resistor value as [Table 17 on page 39](#) shows, the register's LSB always translates to a 1mA adapter current. The ACPROCHOT register accepts any command; however, only the valid register bits are written to the register.

After POR, the ACPROCHOT register is reset to 0x1800H. The ACPROCHOT register can be read back to verify its content.

If the adapter current exceeds the ACPROCHOT register setting, the PROCHOT# signal asserts after the debounce time programmed by the PROCHOTDebounce register and latches on for a minimum time programmed by the PROCHOTDuration register.

For the HPB configuration, the ACPROCHOT function is disabled when it is in standby mode. Standby mode turns off the internal comparator reference, which is indicated by Information1 register Bit<8>.

**Table 11. ACPROCHOT Register 0x47H ($R_{s1} = 10m\Omega$ and $R_{s2} = 10m\Omega$).
(See [Table 18 on page 40](#) for other configurations)**

Bit	Description
<6:0>	Not used
<7>	0 = Add 0mA of ACPROCHOT threshold. 1 = Add 128mA of ACPROCHOT threshold.
<8>	0 = Add 0mA of ACPROCHOT threshold. 1 = Add 256mA of ACPROCHOT threshold.
<9>	0 = Add 0mA of ACPROCHOT threshold. 1 = Add 512mA of ACPROCHOT threshold.
<10>	0 = Add 0mA of ACPROCHOT threshold. 1 = Add 1024mA of ACPROCHOT threshold.
<11>	0 = Add 0mA of ACPROCHOT threshold. 1 = Add 2048mA of ACPROCHOT threshold.
<12>	0 = Add 0mA of ACPROCHOT threshold. 1 = Add 4096mA of ACPROCHOT threshold.
<15:13>	Not used

5.9 Setting PROCHOT# Threshold for Battery Over-Discharging Current Condition

To set the PROCHOT# signal assertion threshold for battery over-discharging current condition, write a 16-bit DCPROCHOT command (0x48H or 0b01001000) using the write word protocol shown in [Figure 24 on page 23](#) and the data format shown in [Table 12](#). By using the recommended current sense resistor value as shown [Table 17 on page 39](#), the register's LSB always translates to 1mA adapter current. The DCPROCHOT register accepts any command; however, only the valid register bits are written to the register.

After POR, the DCPROCHOT register is reset to 0x1000H. The DCPROCHOT register can be read back to verify its content.

If the battery discharging current exceeds the DCPROCHOT register setting, the PROCHOT# signal asserts after the debounce time programmed by the PROCHOTDebounce register and latches on for a minimum time programmed by the PROCHOTDuration register.

In Battery Only mode, the DCPROCHOT function works only when PSYS or NTC is enabled, because enabling PSYS or NTC activates the internal comparator reference. The Information1 register Bit<8> indicates whether the internal comparator reference is active.

When the adapter is present, the internal comparator reference is always active unless it is in Standby mode for HPB configuration.

Table 12. DCPROCHOT Register 0x48H ($R_{s1} = 10m\Omega$ and $R_{s2} = 10m\Omega$).
(See [Table 18 on page 40](#) for other configurations)

Bit	Description
<6:0>	Not used
<7>	0 = Add 0mA of DCPROCHOT threshold. 1 = Add 128mA of DCPROCHOT threshold.
<8>	0 = Add 0mA of DCPROCHOT threshold. 1 = Add 256mA of DCPROCHOT threshold.
<9>	0 = Add 0mA of DCPROCHOT threshold. 1 = Add 512mA of DCPROCHOT threshold.
<10>	0 = Add 0mA of DCPROCHOT threshold. 1 = Add 1024mA of DCPROCHOT threshold.
<11>	0 = Add 0mA of DCPROCHOT threshold. 1 = Add 2048mA of DCPROCHOT threshold.
<12>	0 = Add 0mA of DCPROCHOT threshold. 1 = Add 4096mA of DCPROCHOT threshold.
<15:13>	Not used

5.10 Control Registers

To change certain functions or options after POR, write a 16-bit control command to the Control1 register (0x3DH or 0b00111101) or Control2 register (0x3CH or 0b00111100) using the Write Word protocol shown in [Figure 24 on page 23](#) and the data format shown in [Tables 13 and 14](#), respectively.

Table 13. Control1 Register 0x3DH

Bit	Bit Name	Description	POR State
<0>	Standby Mode	<p>1 = The charger enters Standby mode. 0 = The charger exits Standby mode.</p> <p>The Standby mode control bit is valid for HPB configuration only and is valid only when the adapter is present.</p> <p>When the ISL88739B enters Standby mode, it turns off the internal references (indicated by Information1 register Bit<8>) and stops switching to enter a low power consumption mode with minimum quiescent current.</p> <p>If PSYS is already enabled, it cannot enter Standby mode.</p>	0
<1>	Learn Mode	<p>1 = The charger enters Learn mode. 0 = The charger exits Learn mode.</p> <p>The SMBus Learn mode control is valid only when PROG pin is not pulled to 5V after POR.</p>	0
<2>	AMON	<p>1 = Enables the adapter current monitor AMON function. 0 = Disables off the adapter current monitor AMON function.</p>	0
<3>	BMON	<p>1 = Enables the battery discharging current monitor BMON function. 0 = Disables the battery discharging current monitor BMON function.</p> <p>To avoid the battery being overdischarged, the BMON function is disabled if the battery voltage is less than 3.5V.</p>	0
<4>	PSYS	<p>1 = Enables the system power monitor PSYS function. 0 = Disables the system power monitor PSYS function.</p> <p>The PSYS function does not include the power provided by battery if battery voltage is less than 3.5V.</p> <p>PSYS cannot be turned on for the HPB configuration if an adapter has already entered Standby mode.</p>	0
<5>	Low System Voltage Detection	<p>1 = Enables the low system voltage detect function. 0 = Disables the low system voltage detect function.</p> <p>Bit<5> is valid only when the internal comparator reference is active, which is indicated by Information1 register Bit<8>.</p> <p>In Battery Only mode, the low system voltage detection function works only when PSYS or NTC is enabled, because enabling PSYS or NTC activates the internal comparator reference.</p> <p>When an adapter is present, the internal comparator reference is always active unless it is in Standby mode for the HPB configuration.</p> <p>For the HPB configuration, ISL88739B senses the system voltage through the CSIP pin.</p>	0

Table 13. Control1 Register 0x3DH (Continued)

Bit	Bit Name	Description	POR State
<6>	NTC	<p>1 = Enables the NTC function. 0 = Disables the NTC function.</p> <p>When the NTC function is turned on, if the NTC pin voltage is less than 170mV, the PROCHOT# signal asserts after the debounce time programmed by the PROCHOTDebounce register and latches on for a minimum time programmed by the PROCHOTDuration register.</p> <p>For NTC function to work, the internal reference indicated by Information1 register Bit<8> needs to be active.</p> <p>When an adapter is present, the NTC function is always turned on unless it is in Standby mode, in which case Bit<6> is invalid.</p> <p>In Battery Only mode, Bit<6> is valid to turn on or off the NTC function only when PSYS is turned off; the NTC function is always turned on automatically if PSYS is turned on.</p>	0
<7>	Fast Learn Mode Exit	<p>1 = Fast Learn Mode Exit. 0 = Slow Learn Mode Exit.</p> <p>Fast Learn Mode Exit turns on the ASGATE MOSFETs instantly without going through the ASGATE soft-start turning on procedure when BATGONE pin voltage goes from logic LOW to HIGH.</p> <p>Slow Learn Mode Exit goes through the ASGATE soft-start turning on procedure 163ms after the BATGONE pin voltage goes from logic LOW to HIGH.</p> <p>The Fast Learn Mode Exit control bit is valid only when the battery is removed during Learn mode and it only works for the HPB configuration.</p>	0
<9:8>	Threshold for Low System Voltage Detection	<p>If the Control register Bit<5> = 1, Bits<9:8> programs the low system voltage detection threshold. If the system voltage is below this threshold, the PROCHOT# signal asserts after a fixed 10μs debounce time and latches on for a minimum time programmed by the PROCHOTDuration register.</p> <p>00 = 5.6V threshold. 01 = 6.06V threshold. 10 = 6.53V threshold. 11 = 7V threshold.</p> <p>Valid only when Control1 register Bit<5> = 1.</p>	00
<10>	Turbo/Boost Mode	<p>1 = Disables Turbo/Boost mode. 0 = Enables Turbo/Boost mode.</p>	1
<11>	Charging Current WOCP	<p>1 = Disables charging current way overcurrent protection function. 0 = Enables charging current way overcurrent protection function.</p>	0
<12>	Enable Charging	<p>0 = Disables charging. 1 = Enables charging.</p>	1

Table 13. Control1 Register 0x3DH (Continued)

Bit	Bit Name	Description	POR State
<14:13>	Force The Number Of Battery Cells In Series	<p>Bits<14:13> can overwrite the number of battery cells in series that are programmed by the PROG pin. When Bit<14:13> is written, only the POR default MaxChargeVoltage register value and MinChargeVoltage register value change according to the cell number. The battery 4.6V/cell overvoltage protection threshold also changes according to the cell number.</p> <p>The MaxChargeVoltage register setting should always be smaller than battery overvoltage threshold $4.6V * cell\#$.</p> <p>Bits<14:13> if not used, keep its POR code based on the PROG pin cell# setting.</p> <p>00 = Not available and is ignored if written. 01 = 2-cell. 10 = 3-cell. 11 = 4-cell.</p>	PROG cell#
<15>	SMBus Timeout	<p>The ISL88739B includes a timer to ensure the SMBus master is active and to prevent overcharging the battery. If the adapter is present and if the ISL88739B does not receive a write to the MaxChargeVoltage or ChargeCurrentLimit register within 175s, the ISL88739B terminates charging. If a timeout occurs, writing the MaxChargeVoltage or ChargeCurrentLimit register re-enables charging.</p> <p>0 = Enable the SMBus timeout function. 1 = Disable the SMBus timeout function.</p>	0

Table 14. Control2 Register 0x3CH

Bit	Bit Name	Description	POR State
<3:0>	Frequency Setting	<p>Overwrites the switching frequency set by the FSET pin. See the default CCM switching frequency programming Table 19 on page 41 for the correlation.</p> <p>1111 = 992kHz (equivalent to R_FSET = 0Ω) 1110 = 838kHz 1101 = 729kHz 1100 = 642kHz 1011 = 678kHz 1010 = 614kHz 1001 = 561kHz 1000 = 517kHz 0111 = 513kHz 0110 = 477kHz 0101 = 449kHz 0100 = 421kHz 0011 = 417kHz 0010 = 395kHz 0001 = 375kHz 0000 = Switching frequency set by FSET pin</p> <p>To keep the switching frequency set by the PROG pin resistor, leave Bit<3:0> as it is or write code 0000, which sets the same frequency that the PROG pin resistor does.</p>	0000
<4>		Not used	0
<5>	ASGATE Turn-On Delay	<p>0 = Sets the restart ASGATE turn on delay to 1.3s. 1 = Sets the restart ASGATE turn on delay to 163ms.</p> <p>Bit<5> configures the ASGATE restart delay only in a fault condition (adapter OVP and WOCP). In normal operation after adapter plugged in, the ASGATE turn on delay is always 163ms, regardless of the Bit<5> setting.</p>	0

Table 14. Control2 Register 0x3CH (Continued)

Bit	Bit Name	Description	POR State
<6>	Two-level Adapter Current Limit Function	0 = Disables the two-level adapter current limit function. 1 = Enables the two-level adapter current limit function.	1
<7> <12>	Trickle Charging Current	Bit <12> and Bit <7> can be combined together to change the trickle charging current value. Bit <12>:<7> configuration: <0>:<0> = 256mA trickle charging current. <0>:<1> = 128mA trickle charging current. <1>:<0> = 128mA trickle charging current. <1>:<1> = 64mA trickle charging current. The 64mA trickle charging current option is valid only for "R _{s1} = 10mΩ, R _{s2} = 10mΩ" and "R _{s1} = 20mΩ, R _{s2} = 20mΩ" configurations for the HPB charger.	0:1
<8>	Adapter OVP	0 = Enables the adapter OVP function; 1 = Disables the adapter OVP function. If the adapter OVP function is enabled, the ISL88739B turns off ASGATE and pulls down ACOK when ACIN >3.5V.	0
<9>	PSYS Current Gain	For the "R _{s1} = 10mΩ, R _{s2} = 5mΩ" and "R _{s1} = 10mΩ, R _{s2} = 10mΩ" configuration: 0 = 1.14μA/W 1 = 0.285μA/W For the "R _{s1} = 20mΩ, R _{s2} = 10mΩ" and "R _{s1} = 20mΩ, R _{s2} = 20mΩ" configuration: 0 = 2.28μA/W 1 = 0.57μA/W	0
<10>	ACLIM Inrush Current Limit Time	0 = Sets the soft-start ACLIM inrush current limit period as 1ms when an adapter is plugged in. 1 = Sets the soft-start ACLIM inrush current limit period as 4ms when an adapter is plugged in.	0
<11>	BGATE Off Timing	Bit<11> is valid for the HPB configuration only. It changes the BGATE FET turning off timing when an adapter is plugged in. 0 = Turn off BGATE FET according to battery voltage (see " Soft-Start " on page 42 for details). 1 = Turn off BGATE FET before turning on ASGATE FETs.	0
<13>	ACLIM Function	Bit<13> configures ACLIM to be functional all the time or only during ASGATE turning on procedure to limit the inrush current. 0 = The ACLIM function is on all the time. 1 = The ACLIM function is off after ACOK assertion.	0
<15:14>	DCM LGATE Turning Off Timing	Bit<15:14> adjusts the LGATE turning off timing when the buck switcher is in DCM operation to minimize the MOSFETs body diode conduction time. By default, LGATE turns off when the inductor current is positive (from PHASE node to output). 00 = Earliest LGATE turning off when the PHASE pin voltage is about -6mV. 01 = Earlier LGATE turning off when the PHASE pin voltage is about -4mV. 10 = Early LGATE turning off when the PHASE pin voltage is about -2mV. 11 = Late LGATE turning off when the PHASE pin voltage is about 0mV.	00

5.11 Information Registers

To read the information register, write a 16-bit Information1 command (0x46H or 0b01000110) or Information2 command (0x45H or 0b01000101) using the Read Word protocol shown in [Figure 24 on page 23](#) and the data format shown in [Tables 15](#) and [16](#), respectively.

Table 15. Information1 Register 0x46H

Bit	Bit Name	W/R	Description
<0>	Adapter Present	R	0 = The adapter is not present. 1 = The adapter is present.

Table 15. Information1 Register 0x46H (Continued)

Bit	Bit Name	W/R	Description
<1>	ASGATE ON	R	0 = ASGATE is off. 1 = ASGATE is on.
<2>	VBAT<MinChargeVoltage	R	0 = VBAT>MinChargeVoltage. 1 = VBAT<MinChargeVoltage. Valid only when Information1 register Bit<8> = 1.
<3>	VSYS<Low System Voltage Setting	R	0 = VSYS>Low System Voltage Setting programmed by Control1 register Bit<9:8>. 1 = VSYS<Low System Voltage Setting programmed by Control1 register Bit<9:8>. Valid only when Information1 register Bit<8> = 1.
<4>	NTC_PROCHOT#	R	0 = NTC_PROCHOT# not asserted. 1 = NTC_PROCHOT# asserted. Valid only when Information1 register Bit<8> = 1.
<5>		R	Not used
<6>	In Turbo/Boost Mode	R	0 = Not in Turbo/Boost mode. 1 = In Turbo/Boost mode.
<7>	ACPROCHOT	R	0 = ACPROCHOT# not asserted. 1 = ACPROCHOT# asserted.
<8>	Reference Active	R	0 = Reference is not active. 1 = Reference is active. When Bit<8> = 1, Information Register Bits <4:2> are valid. When an adapter is present, the internal comparator reference is always active unless it is in Standby mode for the HPB charger configuration. In Battery Only mode, the default internal reference is not active unless PSYS or NTC is enabled.

Table 16. Information2 Register 0x45H

Bit	Bit Name	W/R	Description	POR State
<0> <8>	R _{S1}	W/R	If R _{S1} = 20mΩ (R _{S1} = 20mΩ and R _{S2} = 10mΩ or R _{S1} = 20mΩ and R _{S2} = 20mΩ), both Bit<8> and Bit<0> need to be programmed to 1 to have correct internal current-sensing scaling. Bit<8>:<0>: <0>:<0> = R _{S1} = 10mΩ. <0>:<1> = R _{S1} = 10mΩ. <1>:<0> = R _{S1} = 10mΩ. <1>:<1> = R _{S1} = 20mΩ.	0:0
<3:1>			Not used Internally hardwired as <3:1> = 010.	
<5:4>	Cell Number	R	00 = Not available. 01 = 2-cell. 10 = 3-cell. 11 = 4-cell.	
<6>	Current-Sensing Resistor	R	0 = "R _{S1} :R _{S2} = 2:1" (R _{S1} = 10mΩ and R _{S2} = 5mΩ or R _{S1} = 20mΩ and R _{S2} = 10mΩ) 1 = "R _{S1} :R _{S2} = 1:1" (R _{S1} = 10mΩ and R _{S2} = 10mΩ or R _{S1} = 20mΩ and R _{S2} = 20mΩ) Together with Bit<8> and Bit<0> R _{S1} setting, it can be calculated that R _{S1} = 10mΩ or R _{S1} = 20mΩ.	
<7>		R	0 by default.	
<15:9>			Not used	

6. Application Information

6.1 R3 Modulator

The ISL88739B uses the Renesas Robust Ripple Regulator R3 modulation scheme. The R3 modulator combines the best features of fixed frequency Pulse-Width Modulation (PWM) and hysteretic PWM while eliminating many of their shortcomings. [Figure 25](#) conceptually shows the R3 modulator circuit and [Figure 26](#) shows the operation principles in steady state.

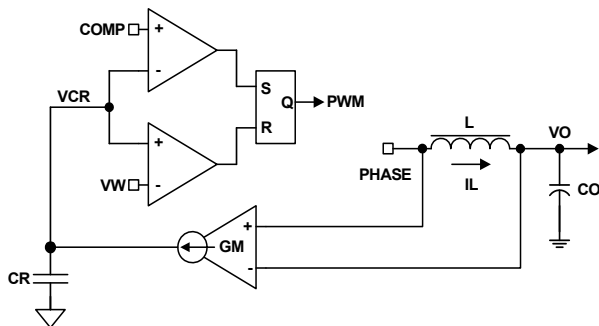


Figure 25. R3 Modulator

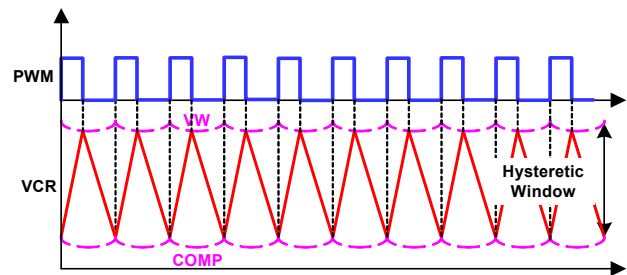


Figure 26. R3 Modulator Operation Principles in Steady State

A fixed voltage window (VW window) exists between VW and COMP. The modulator charges the ripple capacitor C_r with a current source equal to $g_m(V_{IN} - V_o)$ during PWM on-time and discharges the ripple capacitor C_r with a current source equal to $g_m V_o$ during PWM off-time, where g_m is a gain factor. The C_r voltage, V_{cr} , therefore emulates the inductor current waveform. The modulator turns off the PWM pulse when V_{cr} reaches VW and turns on the PWM pulse when it reaches COMP.

Because the modulator works with V_{cr} , which is a large amplitude and noise free synthesized signal, it achieves lower phase jitter than conventional hysteretic mode modulators.

[Figure 27](#) shows the operation principles during dynamic response. The COMP voltage rises during dynamic response, turning on PWM pulses earlier and more frequently. This operation temporarily allows for higher control loop bandwidth than conventional fixed frequency PWM modulators at the same steady-state switching frequency.

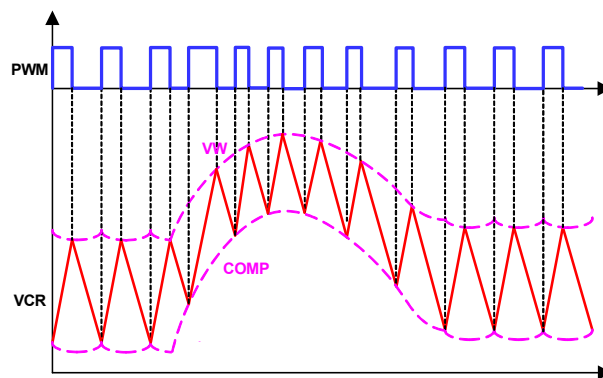


Figure 27. R3 Modulator Operation Principles in Dynamic Response

The R3 modulator can operate in Diode Emulation (DE) mode to increase light-load efficiency. In DE mode, the low-side MOSFET conducts when the current is flowing from source-to-drain and does not allow reverse current, emulating a diode. As shown in [Figure 28](#), when LGATE is on, the low-side MOSFET carries current, creating negative voltage on the phase node due to the voltage drop across the ON-resistance. The IC monitors the current by monitoring the phase node voltage. It turns off LGATE when the phase node voltage reaches zero to prevent the inductor current from reversing the direction and creating unnecessary power loss.

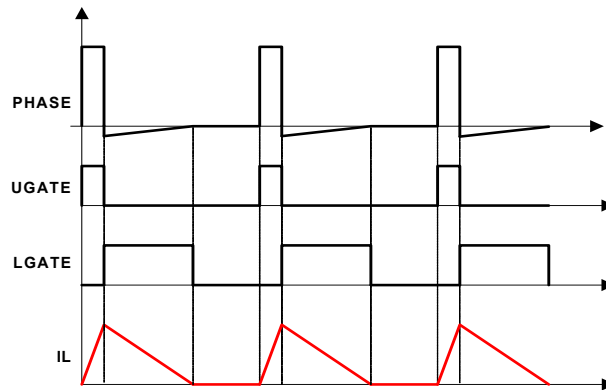


Figure 28. Diode Emulation

If the load current is light enough, as [Figure 28](#) shows, the inductor current reaches and stays at zero before the next phase node pulse and the regulator is in Discontinuous Conduction Mode (DCM). If the load current is heavy enough, the inductor current never reaches 0A and therefore, the regulator is in CCM although the controller is in DE mode.

To turn off LGATE when inductor current reaches near zero in DCM, use the Control2 register Bit<15:14> to adjust the LGATE turning off timing. The default timing purposely turns off LGATE slightly earlier than the inductor current zero crossing. The SMBus bit can adjust the timing more aggressively towards the precise zero-crossing point to minimize the MOSFET's body diode conduction time for higher efficiency at light load. However, it is not recommended to turn off LGATE after the inductor current zero crossing, which can feed energy back to the adapter side.

[Figure 29 on page 39](#) shows the operation principle in Diode Emulation mode at light load. The load gets incrementally lighter in the three cases from top to bottom. The PWM on-time is determined by the VW window size, therefore is the same, making the inductor current triangle the same in the three cases. The R3 modulator clamps the ripple capacitor voltage V_{cr} in DE mode to make it mimic the inductor current. It takes the COMP voltage longer to hit V_{cr} , naturally stretching the switching period. The inductor current triangles move further apart from each other so that the inductor current average value is equal to the load current. The reduced switching frequency helps increase light-load efficiency.

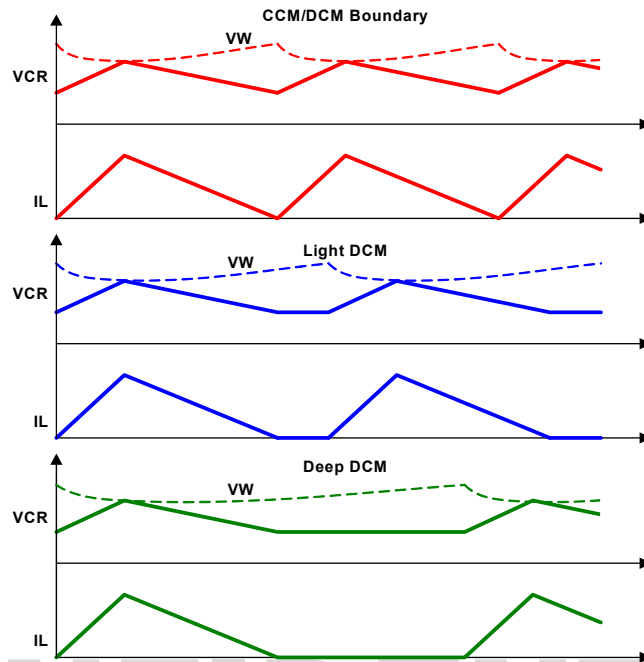


Figure 29. Period Stretching

6.2 Programming Charger Options

The resistor from the PROG pin to GND programs the configuration of the ISL88739B as an HPB charger, as well as the default number of battery cells in series and the default values of the adapter and battery current sense resistors R_{s1} and R_{s2} . [Table 17](#) shows the programming options.

Table 17. PROG Pin Programming Options

PROG-GND Resistance (kΩ)	Charger Type	Current Sense Resistor Value	Default Number of Battery Cells in Series
Typical (1% Standard Resistor)			
150	HPB	$R_{s1}:R_{s2} = 1:1$ $R_{s1} = 10m\Omega$ $R_{s2} = 10m\Omega$ or $R_{s1} = 20m\Omega$ $R_{s2} = 20m\Omega$	4
165			2
182			3
215		$R_{s1}:R_{s2} = 2:1$ $R_{s1} = 10m\Omega$ $R_{s2} = 5m\Omega$ or $R_{s1} = 20m\Omega$ $R_{s2} = 10m\Omega$	4
237			2
255			3

Before soft-start and when V_{DD} voltage reaches its POR value, the ISL88739B sources $10\mu A$ current out of the PROG pin and reads the PROG pin voltage to determine the resistor value. However, application environmental noise may pollute the PROG pin voltage and cause an incorrect reading. If noise is a concern, connect a capacitor from the PROG pin to GND to provide filtering. The resistor and the capacitor RC time constant should be less than $40\mu s$, so the PROG pin voltage can rise to steady state before the ISL88739B reads it.

[Figure 1 on page 1](#) shows the typical application circuit for an HPB charger. In this configuration, the ISL88739B connects the system voltage rail to either the adapter or the battery. In Turbo mode, which means the system is

drawing more power than the adapter's power rating, the ISL88739B operates as a boost converter to reverse-boost the battery energy to the system voltage rail, so the battery works with the adapter to supply the system power.

The PROG pin resistor programs the ratio of the current-sensing resistor values R_{S1} and R_{S2} as 2:1 or 1:1. Therefore, four sets of R_{S1} and R_{S2} current-sensing resistor values can be used, for example:

- $R_{S1} = 10\text{m}\Omega$, $R_{S2} = 5\text{m}\Omega$
- $R_{S1} = 10\text{m}\Omega$, $R_{S2} = 10\text{m}\Omega$
- $R_{S1} = 20\text{m}\Omega$, $R_{S2} = 10\text{m}\Omega$
- $R_{S1} = 20\text{m}\Omega$, $R_{S2} = 20\text{m}\Omega$

If $20\text{m}\Omega$ R_{S1} is used, the SMBus Information2 register Bit<0> and Bit<8> both need to be set as 1 for the appropriate internal current-sensing scaling.

Smaller current sense resistor values reduce power loss, while larger current sense resistor values provide better accuracy.

The PROG pin resistor configures the internal current sense gain automatically for different R_{S1} and R_{S2} , so that the SMBus command remains the same for $20\text{m}\Omega$ or $10\text{m}\Omega$ R_{S1} and for $10\text{m}\Omega$ or $5\text{m}\Omega$ R_{S2} . For example, the AdapterCurrentLimit1 register, AdapterCurrentLimit2 register, and the ACPROCHOT register can be programmed with the same SMBus command value, regardless of whether R_{S1} is $20\text{m}\Omega$ or $10\text{m}\Omega$, to obtain the same current. The ChargeCurrent register and DCPROCHOT register can be programmed with the same SMBus command value, regardless of whether R_{S2} is $10\text{m}\Omega$ or $5\text{m}\Omega$, to obtain the same current. Using any option would result in 1mA/LSB correlation in the SMBus commands.

If R_{S1} and R_{S2} values are different from the PROG pin programming table, the SMBus command needs to be scaled accordingly to obtain the correct current.

Upon POR, the ISL88739B uses the default number of cells in series as [Table 17](#) shows and sets the default MaxChargeVoltage register value and default MinChargeVoltage register value accordingly. When SMBus communication is established, the SMBus can program a different number of battery cells in series through SMBus Control1 register Bit<14:13>.

[Table 18 on page 40](#) shows the adapter current and battery current related settings according to different R_{S1} and R_{S2} options.

Table 18. Current-Sensing Resistor Configurations

Current-Sensing Resistors	Registers			K_{PSYS} ($\mu\text{A/W}$)	
	ChargeCurrent	DCPROCHOT	AdapterCurrentLimit1* AdapterCurrentLimit2* ACPROCHOT**	Control2 Bit<9> = 0	Control2 Bit<9> = 1
1 $R_{S1} = 10\text{m}\Omega$ $R_{S2} = 5\text{m}\Omega$	Bit<12:5> Max = 1FE0h, 8.160A Min = 0020h, 32mA Default = 0000h, 0A	Bit<13:8> Max = 3F00h, 16.128A Min = 0100h, 256mA Default = 2000h, 8.192A	Bit<12:7> Max = 1F80h, 8.064A Min = 0080h, 128mA *Default = 1F80h, 8.064A **Default = 1800h, 6.144A	1.14	0.285
2 $R_{S1} = 10\text{m}\Omega$ $R_{S2} = 10\text{m}\Omega$	Bit<12:5> Max = 1FE0h, 8.160A Min = 0020h, 32mA Default = 0000h, 0A	Bit<12:7> Max = 1F80h, 8.064A Min = 0080h, 128mA Default = 1000h, 4.096A	Bit<12:7> Max = 1F80h, 8.064A Min = 0080h, 128mA *Default = 1F80h, 8.064A **Default = 1800h, 6.144A	1.14	0.285
3 $R_{S1} = 20\text{m}\Omega$ $R_{S2} = 10\text{m}\Omega$	Bit<11:4> Max = 0FF0, 4.080A Min = 0010, 16mA Default = 0000h, 0A	Bit<12:7> Max = 1F80h, 8.064A Min = 0080h, 128mA Default = 1000h, 4.096A	Bit<11:6> Max = 0FC0h, 4.032A Min = 0040h, 64mA *Default = 0FC0h, 4.032A **Default = 0C00h, 3.072A	2.28	0.57

Table 18. Current-Sensing Resistor Configurations (Continued)

Current-Sensing Resistors	Registers			K _{PSYS} (μA/W)	
	ChargeCurrent	DCPROCHOT	AdapterCurrentLimit1* AdapterCurrentLimit2* ACPROCHOT**	Control2 Bit<9> = 0	Control2 Bit<9> = 1
4 R _{S1} = 20mΩ R _{S2} = 20mΩ	Bit<11:4> Max = 0FF0, 4.080A Min = 0010, 16mA Default = 0000h, 0A	Bit<11:6> Max = 0FC0h, 4.032A Min = 0040h, 64mA Default = 0800h, 2.048A	Bit<11:6> Max = 0FC0h, 4.032A Min = 0040h, 64mA *Default = 0FC0h, 4.032A **Default = 0C00h, 3.072A	2.28	0.57

6.3 Programming Switching Frequency

The resistor from the FSET pin to GND programs the default CCM switching frequency, as shown in [Table 19](#). Before soft-start, the ISL88739B sources 10μA current out of the FSET pin and reads the FSET pin voltage to determine the resistor value. However, application environmental noise can pollute the FSET pin voltage and cause an incorrect reading. If noise is a concern, connect a capacitor from the FSET pin to GND to provide filtering. The resistor and the capacitor RC time constant should be less than 40μs, so the FSET pin voltage can rise to steady state before the ISL88739B reads it.

Table 19. Default CCM Switching Frequency Options

FSET-GND Resistance (kΩ)	Switching Frequency (kHz)	
	Typical (±15%)	4-Cell With Period Stretch
0	992	500
22.6	838	430
38.3	729	375
54.9	642	335
69.8	678	460
86.6	614	420
102	561	390
118	517	360
133	513	420
150	477	390
165	449	370
182	421	350
200	417	360
215	395	340
237	375	330
255	350	310

In DE mode, the ISL88739B's phase comparator monitors the PHASE node voltage during low-side switching FET on-time to detect the inductor current zero crossing. The phase comparator needs a minimum on-time of the low-side switching FET for it to recognize inductor current zero crossing. If the low-side switching FET on-time is too short for the phase comparator to successfully recognize the inductor zero crossing, the ISL88739B can lose diode emulation ability. To prevent such a scenario, the ISL88739B employs a minimum low-side switching FET on-time. When the intended low-side switching FET on-time is shorter than the minimum value, the ISL88739B stretches the switching period to keep the low-side switching FET on-time at the minimum value, which causes the CCM switching frequency to drop below the set point. This effect is pronounced only in applications using a 4-cell battery and high switching frequency setting.

The switching frequency can be changed through SMBus Control2 register Bit<3:0> after POR. See the SMBus Control2 register programming table for a detailed description.

6.4 Soft-Start

When the DCIN pin voltage is higher than 5V, an internal LDO starts to regulate and output 5V on the VDDP pin, which is the power supply for the gate drives.

The VDD pin is the 5V power supply for the ISL88739B control circuitry. Use an R-C filter to generate the VDD pin voltage from the VDDP pin voltage. When the VDD pin voltage exceeds its POR, the ISL88739B sources 10 μ A current out of the PROG pin and reads the pin voltage to determine the PROG resistor value; it then sources 10 μ A current out of the FSET pin and reads the pin voltage to determine the FSET resistor value. The PROG resistor and the FSET resistor values program the configurations of the ISL88739B.

Soft-start, turning on ASGATE FETs, begins 163ms after:

- VDD pin voltage exceeds its POR
- ACIN pin voltage exceeds 2V
- DCIN voltage is higher than VBAT pin voltage

ASGATE FETs turn off when ACIN pin voltage is lower than 2V. ASGATE turn-off does not depend on the DCIN and VBAT comparison.

Note: after the adapter is plugged in, the ASGATE turn-on delay is always 163ms, regardless of the Control2 register Bit<5> setting. Control2 register Bit<5> only sets the ASGATE turn-on delay during restart in a fault condition.

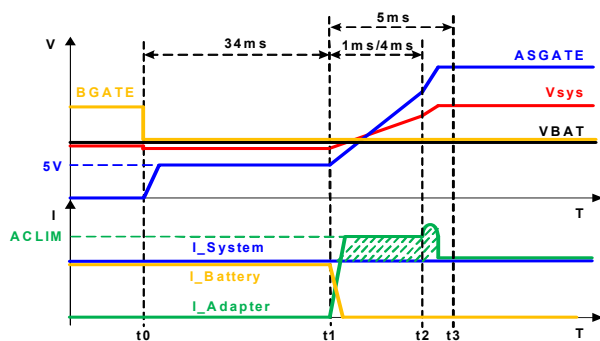


Figure 30. Soft-Start with $V_{BAT} < 4.5V$ or $V_{BAT} > 7V$

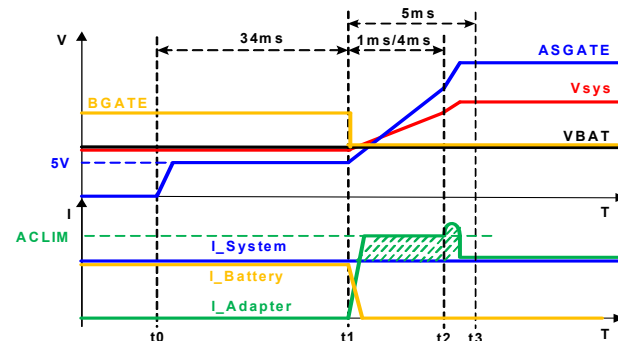


Figure 31. Soft-Start with $4.5V < V_{BAT} < 7V$

During soft-start in the HPB charger configuration, the ISL88739B limits the adapter current in several steps. As shown in [Figure 30](#), at t_0 , the ISL88739B outputs 20 μ A current source to charge the ASGATE pin voltage to 5V and then holds the ASGATE pin voltage at 5V for 34ms until t_1 . From t_1 to t_2 , the ISL88739B limits the adapter current at the value set by the ACLIM pin voltage for the next 1ms (the default is 1ms; a 4ms option is available through SMBus Control2 register Bit<10>). From t_2 to t_3 , the ISL88739B outputs 20 μ A for another 4ms (or 1ms) to fully turn on ASGATE without actively limiting the adapter current. ACOK is asserted high after the ASGATE is fully turned on. The stepped soft-start scheme carefully bias up the system and protects the back-to-back ASGATE FETs against potential damage caused by the inrush current.

[Figure 32 on page 43](#) shows the HPB configuration without battery soft-start waveform when the system load is less than the ACLIM-set current level. During t_1 through t_2 , the ISL88739B charges the system bus capacitor with (ACLIM - system load) current and reaches the adapter voltage by t_2 . There is no inrush current after t_2 .

[Figure 33 on page 43](#) shows the HPB configuration without battery soft-start waveform when the system load is greater than the ACLIM-set current level, which is not a recommended mode of operation. During t_2 through t_3 , the ISL88739B fully turns on the ASGATE and lets the adapter charge the system bus capacitor without current limit.

In the HPB charger configuration, the ISL88739B can determine when to turn off the BGATE MOSFET to prevent system voltage disturbance. BGATE MOSFET turns off at t_0 before ASGATE ramps up if $V_{BAT} < 4.5V$ or $V_{BAT} > 7V$ as shown in [Figure 30 on page 42](#) and remains on until t_2 if $4.5V < V_{BAT} < 7V$ as shown in [Figure 31 on page 42](#). Such a scheme prevents the system bus voltage from dropping by the MOSFET body-diode voltage drop caused by the BGATE MOSFET turning off early. This should not pose any danger to the battery. However, if this scheme is not desired, Control2 register Bit<11> can turn off BGATE before ASGATE ramps up regardless of the battery voltage.

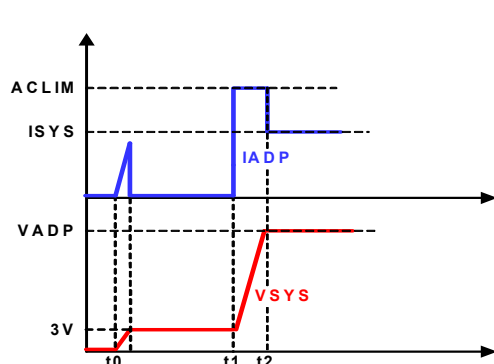


Figure 32. No Battery Soft-Start with $I_{SYS} < ACLIM$

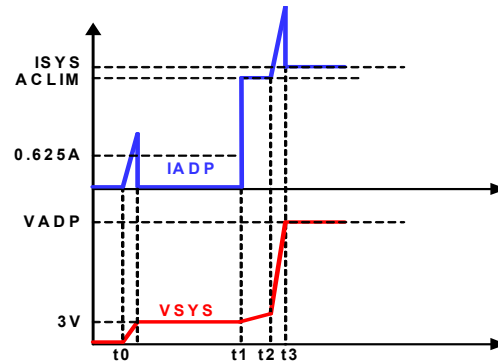


Figure 33. No Battery Soft-Start with $I_{SYS} > ACLIM$

6.5 Adapter Presence Detection and ACOK

ACOK is an open-drain output pin indicating the presence of the adapter and readiness of the adapter to supply power to the system bus. The ISL88739B actively pulls ACOK low in the absence of the adapter.

Use a voltage divider from the adapter voltage to set the ACIN pin voltage. ISL88739B allows the external circuit to pull up the ACOK pin after:

- ACIN pin voltage exceeds 2V
- DCIN voltage is higher than VBAT pin voltage
- ASGATE FETs are fully turned on

ISL88739B pulls down the ACOK pin to GND only when the ACIN pin voltage is lower than 2V. ACOK go-low does not depend on the DCIN and VBAT comparison.

For the buck converter to properly charge the battery, the ACIN pin voltage divider should be selected so that the minimum adapter voltage set by the ACIN pin voltage divider is higher than the maximum battery voltage. There is a delay of 163ms between the ACIN pin voltage rising above 2V and ASGATE starting to turn on.

Depending on different operation scenarios, the total deglitch time varies from the ACIN pin voltage rising above 2V to ACOK asserted high. For the HPB configuration, this deglitch time is about 278ms with PROG pin resistor reading and about 247ms without PROG pin resistor reading. These typical numbers can have an 11% variation.

6.6 Adapter Overvoltage Protection

If the ACIN voltage exceeds 3.5V, an adapter overvoltage condition has occurred. The ISL88739B turns off the ASGATE MOSFETs to isolate the adapter from the system and deasserts the ACOK signal by pulling it low.

When the ACIN voltage drops below 3.5V, after the 1.3s or 163ms debounce time set by Control2 register Bit<5>, it goes through the ASGATE soft-start to turn on ASGATE.

The adapter OVP function can be disabled through the SMBus Control2 register Bit<8>.

6.7 Power Source Selection

The ISL88739B automatically selects the adapter and/or the battery as the source for system power.

The BGATE pin drives an NFET that connects and disconnects the battery from the system and the switcher.

The ASGATE pin drives a pair of back-to-back common source NFETs to connect and disconnect the adapter from the system and the battery.

If the adapter is present, the ISL88739B turns on ASGATE to connect the adapter to the system. In the HPB charger configuration, it also turns off BGATE to disconnect the battery from the system when it turns on ASGATE.

If the adapter is absent, the ISL88739B turns off ASGATE and turns on BGATE to connect the battery to the system. If system bus voltage is higher than the battery voltage, the ISL88739B waits until the system bus voltage decays to battery voltage before turning on BGATE to avoid inrush current into the battery.

6.8 Battery Learn Mode

The ISL88739B supports Battery Learn mode. The ISL88739B enters Battery Learn mode when it receives the SMBus Control command (see [Table 13 on page 32](#)), or when the PROG pin voltage is externally pulled to 5V after POR. It is not possible to pull up the PROG pin to 5V if the PROG pin to GND resistor value is set to 0Ω. The ISL88739B exits Battery Learn mode when it receives the SMBus control command as shown in [Table 13](#), or when the PROG pin voltage is no longer pulled to 5V.

6.9 HPB Charger Battery Learn Mode Entry/Exit

In the HPB charger configuration Battery Learn mode, the ISL88739B turns off ASGATE and turns on BGATE regardless of whether the adapter is present. This mode of operation supplies the system power from the battery, even when the adapter is plugged in, such as calibration of the battery fuel gauge. The Information1 register Bit<1> indicates ASGATE on or off.

Upon entering Battery Learn mode, the ISL88739B only turns on BGATE when the system bus voltage decays to battery voltage to avoid inrush current from system bus to battery.

There are three ways of exiting HPB charger configuration Battery Learn mode:

- Receive the Battery Learn Mode Exit command through SMBus.
- The PROG pin voltage drops below 5V.
- BATGONE pin voltage goes from logic LOW to HIGH.

In cases 1 and 2, after the ASGATE turn on delay of 163ms, the ISL88739B goes through the soft-start process to turn on ASGATE and turn off BGATE as described in [“Soft-Start” on page 42](#).

In case 3, the ISL88739B uses its maximum gate drive strength to turn on ASGATE quickly to prevent system voltage collapse. This action can be completed within ~35μs after the BATGONE pin voltage level goes to logic high. If the soft-start process is still preferred in this case, use SMBus Control1 register Bit<7> to configure the preference.

6.10 Hardware-Based Adapter Current Limit

The ACLIM pin voltage set hardware-based adapter current limit provides an extra level of protection in the unlikely event of SMBus communication failure.

[Equation 1](#) gives the relationship between the ACLIM pin voltage and the hardware-based adapter current limit, where $V_{ACLIMHW}$ is the ACLIM pin voltage in volts and $I_{ACLIMHW}$ is the hardware-based adapter current limit in amperes.

$$(EQ. 1) \quad I_{ACLIMHW} = \frac{V_{ACLIMHW}}{32 \times R_{s1}}$$

[Equation 1](#) is true for all current-sensing resistor configurations.

The ISL88739B uses the lower value of the hardware-set adapter current limit and the SMBus programmed adapter current limit as the actual adapter current limit.

The ACLIM pin voltage also sets the ASGATE soft-start current limit level from t2 to t3. The ACLIM current limit function can be disabled through SMBus Control2 register Bit<13> after ACOK assertion, so that the ACLIM pin is only used for ASGATE soft-start current limit from t2 to t3 as shown in [“Soft-Start” on page 42](#).

6.11 HPB Charger Turbo Mode Support

In Turbo mode, the system draws more power than the adapter’s power rating. It prompts the need for the switcher to change from Forward Buck mode of operation to Reverse-Boost mode of operation to reverse the energy flow. This mode of operation enables the battery to help the adapter provide the required system power. This operation has been widely used in many systems, such as “Sun mode” and “Eclipse mode” for bidirectional battery charger/dischargers used on satellites with solar panels as the power source acting as the adapter. See “A zero voltage switching bidirectional battery charger/discharger for the NASA EOS Satellite”, Dan M. Sable, Fred C. Lee and Bo H. Cho, APEC 1992 Conference Proceedings.

In the HPB charger configuration, the ISL88739B normally operates the switcher as a synchronous buck converter with diode emulation. When the buck converter is in light-load condition, it enters DCM operation with reduced switching frequency to increase efficiency. From the description of the R3 modulator operational principle, the COMP pin voltage is lower at lighter load and can reach the low clamp.

In Turbo mode, the ISL88739B operates the switcher in reverse-boost mode to boost energy from the battery to the adapter voltage rail, so that the adapter current is limited at the adapter current limit set point while the battery supplies the additional power required by the system.

The Control1 register Bit<10> enables/disables the Turbo/Boost function. See [Table 13 on page 32](#) for details.

The ISL88739B enters Turbo mode when all of the following three criteria are met:

- Adapter current is within 80mA of AdapterCurrentLimit1 (or AdapterCurrentLimit2 if two-level adapter current limit function is enabled) register setting.
- Battery charging current is less than 150mA.
- COMP pin voltage is lower than 1.4V.

Meeting these three criteria means that the ISL88739B enters Turbo mode only when it is absolutely necessary. For example, assume the adapter voltage is 20V, the adapter current limit is 4A (80W rating) and the ISL88739B is charging an 8V battery at a 5A rate (40W charging power). If the system load increases from 0W to 79W instantaneously, the adapter current increases from 2A to 5.95A instantaneously, exceeding the 4A current limit level. However, the adapter current loop takes control and decreases the charging current to limit the adapter current at 4A, eventually providing 79W of system power and 1W of battery charging power. In this case, the ISL88739B does not need to enter Turbo mode for the adapter to conserve battery energy. In the same example, if the system load increases from 0W to 81W instantaneously, the adapter current increases from 2A to 6.05A instantaneously, exceeding the 4A current limit level. The adapter current loop takes control and decreases the charging current to limit the adapter current at 4A. Thus, the ISL88739B eventually determines that it needs to enter Turbo mode so the adapter provides 80W and the battery provides 1W, to provide 81W to the system.

The interaction of the control loops within the ISL88739B, including the adapter current loop, the charging current loop, and the battery full charging voltage loop, determines the timing of the Turbo mode entry. The timing strongly depends on the control loop compensation design and the interaction among the loops. In the previous example, compared with system power instantaneously increasing from 0W to 81W, instantaneously increasing system power from 0W to 160W causes the ISL88739B to enter Turbo mode much faster because the loops drive the circuit parameters to meet the three Turbo mode entry criteria much quicker when the adapter is more severely overloaded.

The ISL88739B exits Turbo mode when one of the following three criteria are met:

- Battery charging current exceeds 150mA ($R_{s2} = 10m\Omega$).
- Adapter current is less than AdapterCurrentLimit register setting and COMP voltage is lower than 1.4V.
- Battery discharging current is less than 140mA (for $R_{s2} = 10m\Omega$) for 140ms.

[Table 20 on page 46](#) shows the ISL88739B HPB configuration charge function and Turbo/Boost function control truth table.

Table 20. HPB Charger Behavior Truth Table

Turbo/Boost Mode Control Bit	EnableCharging Control Bit	ChargeCurrent Register		
0 = Enable Boost 1 = Disable Boost	0 = Disable Charging 1 = Enable Charging	0 = 0A Command 1 = Non-Zero Valid Command	Charge?	Boost?
0	0	0	No	Yes
0	0	1	No	Yes
0	1	0	No	Yes
0	1	1	Yes (Fast charge and trickle charge enabled)	Yes
1	0	0	No	No
1	0	1	No	No
1	1	0	No	No
1	1	1	Yes (Fast charge and trickle charge enabled)	No

6.12 Two-Level Adapter Current Limit

In a real system, a Turbo event usually does not last very long. It is often no longer than milliseconds, a time length during which the adapter can supply current higher than its DC rating. The ISL88739B employs two-level adapter current limit to take full advantage of adapter's surge capability and minimize the power draw from the battery.

[Figure 34 on page 47](#) shows the two SMBus-programmable adapter current limit levels, AdapterCurrentLimit1 and AdapterCurrentLimit2, as well as the durations t1 and t2. The two-level adapter current limit function is initiated when the adapter current reaches the AdapterCurrentLimit1 register setting and it starts at AdapterCurrentLimit2 for t2 duration and then changes to AdapterCurrentLimit1 for t1 duration before repeating the pattern. These parameters can set adapter current limit with an envelope that allows the adapter to temporarily output surge current without requiring the charger to enter Turbo mode. Such operation maximizes battery life.

AdapterCurrentLimit1 register value can be higher or lower than AdapterCurrentLimit2 value.

The two-level adapter current limit function can be enabled and disabled through SMBus Control2 register Bit<6>. When the two-level adapter current limit function is disabled, only AdapterCurrentLimit1 value is used as the adapter current limit and AdapterCurrentLimit2 value is ignored.

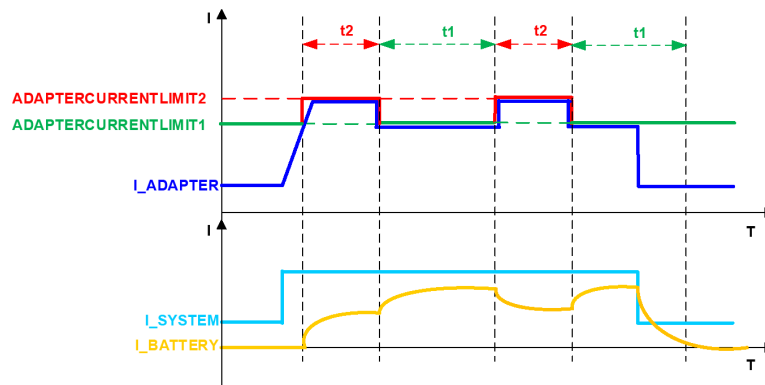


Figure 34. Two-Level Adapter Current Limit

6.13 Current Monitor

The ISL88739B provides an adapter current monitor through the AMON pin and a battery discharging current monitor through BMON pin. The AMON pin voltage is 32x the ($V_{CSIP} - V_{CSIN}$) voltage and the BMON pin voltage is 32x the ($V_{CSOP} - V_{CSOP}$) voltage.

AMON and BMON function can be enabled or disabled through SMBus Control1 register Bit<2> and Bit<3> respectively, as [Table 13 on page 32](#) shows.

6.14 PSYS Monitor

The ISL88739B PSYS pin provides a measure of the instantaneous power consumption of the entire platform. The PSYS pin outputs a current source described by [Equation 2](#).

$$(EQ. 2) \quad I_{PSYS} = K_{PSYS} \times (V_{ADP} \times I_{ADP} + V_{BAT} \times I_{BAT})$$

K_{PSYS} is based on the current-sensing resistors R_{S1} and R_{S2} configuration and is selectable through SMBus Control2 register Bit<9>. See [Table 18 on page 40](#) for details. V_{ADP} is the adapter voltage in volts, I_{ADP} is the adapter current in amperes, V_{BAT} is the battery voltage, and I_{BAT} is the battery discharging current. When the battery is discharging, I_{BAT} is a positive value; when the battery is being charged, I_{BAT} is a negative value.

The PSYS information includes the power loss of the charger circuit and the actual power delivered to the system. Resistor R_{PSYS} connected between the PSYS pin and GND, convert the PSYS information from current to voltage.

The PSYS function can be enabled or disabled using SMBus Control1 register Bit<4> as [Table 13 on page 32](#) shows.

6.15 Charger Timeout

The ISL88739B's timer ensures the SMBus master is active and to prevent overcharging the battery. The ISL88739B terminates charging if the charger has not received a write to the MaxChargeVoltage or ChargeCurrent register within 175s. If a time-out occurs, MaxChargeVoltage or ChargeCurrent register must be written to re-enable charging.

The ISL88739B allows users to disable the charger timeout function through SMBus Control1 register Bit<15> as shown in [Table 13 on page 32](#).

6.16 Trickle Charging

The ISL88739B supports trickle charge to an overly discharged battery. It can activate the trickle charge function when the battery voltage is lower than MinChargeVoltage setting. The VBAT pin is the battery voltage sense point for Trickle Charge mode.

To enable trickle charge, set the EnableCharging control bit to 1 and set the ChargeCurrent register to a valid non-zero value. To disable trickle charge, either set the EnableCharging control bit to 0 or set the ChargeCurrent register to 0. [Table 20 on page 46](#) shows the condition to enable HPB configuration Trickle Charge mode.

The trickle charging current can be programmed to be 256mA, 128mA, or 64mA through SMBus Control2 register Bit<7> and Bit<12> as shown in [Table 14 on page 34](#).

In the HPB charger configuration, the ISL88739B charges the battery at 256mA, 128mA, or 64mA in Trickle Charge mode.

When the battery voltage is charged to 175mV above MinChargeVoltage register value, the ISL88739B enters fast charging mode by limiting the charging current at the ChargeCurrentLimit register setting.

The ISL88739B CSON pin sinks about 20μA current and the CSOP pin sinks about 35μA current to provide the bias power for the battery current-sensing amplifier. If there is a resistor series in CSON pin, the voltage drop on this resistor creates a small offset so that the actual battery charging current becomes slightly smaller. If there is a resistor series in CSOP pin, the voltage drop on this resistor creates a small offset so that the actual battery charging current becomes slightly larger. These two resistors can slightly tweak the actual battery charging current.

6.17 Charging Current WOCP

The ISL88739B provides the WOCP (Way-Overcurrent Protection) function for the current flowing into to the battery against the high-side MOSFET short and inductor short scenarios. It employs the CCLIM pin to set the WOCP threshold. ISL88739B monitors the CSOP-CSON voltage and compares it with the WOCP threshold. When the WOC comparator is tripped, it either terminates the PWM switching pulse, or turns off ASGATE and deassert ACOK, configurable through SMBus Control11 register Bit<11>.

When the WOCP function is enabled through Control11 register Bit<11>, if the WOC comparator is tripped, the ISL88739B counts when within every 20μs. Whenever the ISL88739B counts to seven times in 656ms, it turns off ASGATE and deasserts ACOK immediately. After the 1.3s or 163ms debounce time set by Control2 register Bit<5>, it goes through the ASGATE soft-start to retry.

When the WOCP function is disabled through Control11 register Bit<11>, as long as the WOC comparator is tripped within every 20μs, it terminates the PWM switching pulse immediately for the rest of the time of the 20μs.

The CCLIM pin voltage sets the charging current WOCP threshold. [Equations 3](#) and [4](#) give the relationship between the CCLIM pin voltage and the WOCP threshold, where $V_{CCLIMHW}$ is the CCLIM pin voltage in volts and I_{WOCP} is the WOCP threshold in amperes.

$$(EQ. 3) \quad I_{WOCP} = 1.23 \times \frac{V_{CCLIMHW}}{64 \times R_{s2}}$$

[Equation 3](#) is true for $R_{s1} : R_{s2} = 2:1$ ($R_{s1} = 10m\Omega$ and $R_{s2} = 5m\Omega$ or $R_{s1} = 20m\Omega$ and $R_{s2} = 10m\Omega$).

$$(EQ. 4) \quad I_{WOCP} = \frac{V_{CCLIMHW}}{32 \times R_{s2}}$$

[Equation 4](#) is true for $R_{s1} : R_{s2} = 1:1$ ($R_{s1} = 10m\Omega$ and $R_{s2} = 10m\Omega$ or $R_{s1} = 20m\Omega$ and $R_{s2} = 20m\Omega$).

The WOC comparator monitors the peak current crossing the battery current-sensing resistor R_{s2} , so the WOCP threshold needs to be set at least half of the inductor ripple current higher than the SMBus-programmed charging current command, to avoid false tripping in normal charging.

For the WOCP function to work properly, it needs to connect an RC filter from the CSON pin to ground to increase the overcurrent detection sensitivity. This RC filter time constant should be selected carefully and cannot be too large, otherwise the WOCP could be falsely tripped by the current overshoot flowing into the battery when ISL88739B exits Turbo mode after system bus load release. Meanwhile, the WOCP threshold should be set high enough to avoid the false trip by the current overshoot flowing into the battery.

The current spike flowing into the battery could cause a voltage spike at the battery connector due to the battery current path impedance. Adding an RC filter at VBAT is recommended in this scenario.

6.18 Over-Temperature Protection

The ISL88739B turns off the internal LDO for self-protection when the junction temperature exceeds +155°C. The internal LDO stays off until the junction temperature falls below +128°C.

In the HPB charger configuration, the ISL88739B puts the charger in Standby mode after declaring over-temperature protection.

When the temperature falls below +128°C, the ISL88739B enables the internal LDO and ISL88739B resumes operation.

6.19 Battery Overvoltage Protection

The battery overvoltage protection function prevents the battery from being overcharged.

In the HPB charger configuration, the ISL88739B stops switching if the battery voltage is higher than the MaxChargeVoltage register setting. If the battery voltage is higher than 4.6V/cell, it stops charging.

The MaxChargeVoltage register setting should be less than 4.6V/cell.

6.20 System Bus Short-Circuit Detection

If the ACIN pin is pulled below 2V by the system bus excessive current or short-circuit, the ISL88739B turns off ASGATE to isolate the adapter from the system bus. When the ACIN pin voltage rises above 2V again and after 163ms delay, ASGATE turns on again with soft-start.

An external circuit, as shown in [Figure 35](#), can detect the system bus short-circuit. If the system bus short-circuits, the ACIN pin is pulled below 2V by diode D₁, so ASGATE cannot turn on. While in normal operation, ASGATE still can turn on when the system bus is charged up above 2V through D₁.

In normal operation, to charge up the system bus above 2V through D₁ quickly, the ACIN pin voltage divider resistor values need to be small, which in sequence causes a larger constant power consumption on the ACIN pin voltage divider resistors. Two optional circuits as shown in [Figure 35](#) can be dedicated to charge up the system bus. It is recommended to use Option 1 circuit for HPB configuration.

For the Option 2 circuit, the R₃ and R₄ voltage divider voltage, for example, the Q₁ gate voltage, needs to be 2V higher than the Q₁ gate source threshold voltage so that Q₁ can be turned on and the system bus can be charged up above 2V through R₂ and Q₁. Meanwhile, the R₃ and R₄ voltage divider voltage needs to be less than the final system bus voltage so that Q₁ can be turned off in normal operation to avoid the leakage current through Q₁. D₃ can block the leakage current from the system bus to the adapter side through the Q₁ body diode in Battery Only mode.

Note that leakage current occurs through R₁ and D₂ in the Option 1 circuit when the adapter voltage is higher than the system bus voltage, such as in Learn mode.

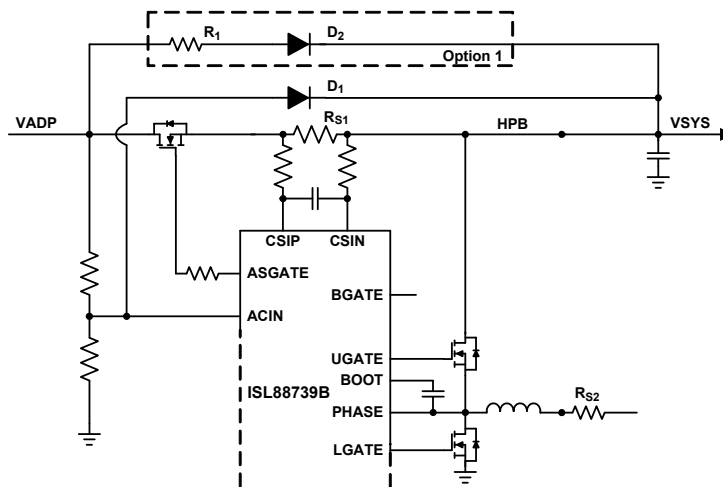


Figure 35. External System Bus Short Detection Circuit

6.21 Adapter Input Filter

The adapter cable parasitic inductance and capacitance can cause some voltage ring or overshoot spike at the adapter connector node when the adapter is hot plugged in. This voltage spike can damage the ASGATE MOSFET or the ISL88739B pins connecting to the adapter connector node. One low cost solution is to add an RC snubber circuit at the adapter connector node to clamp the voltage spike as shown in [Figure 36](#). A practical value of the RC snubber is 2.2Ω to $2.2\mu\text{F}$ while the appropriate values and power rating should be carefully characterized based on the actual design. Do not add a pure capacitor at the adapter connector node, which can cause an even bigger voltage spike due to the adapter cable or the adapter current path parasitic inductance.

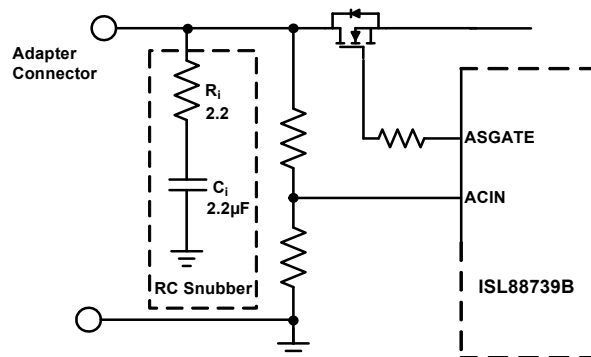


Figure 36. Adapter Input RC Snubber Circuit

6.22 Testing with e-Load Constant Voltage Mode

An electronic load in Constant Voltage mode (e-Load in CV mode) often emulates a battery in testing a battery charger. However, an e-Load in CV mode does not accurately emulate the characteristics of a real battery, particularly the ESR. Such a discrepancy can result in a much more exaggerated output voltage switching ripple observed by the battery charger and present inaccurate test results. Adding a capacitor, such as $680\mu\text{F}$, is recommended at the terminal of the e-Load to better match the impedance of a real battery, so that the test result better represents that with a real battery. As a precaution for potentially testing with an e-load with large ESR, adding an R-C filter at the VBAT pin is recommended to smooth the switching ripple observed by the ISL88739B. The recommended range of the R-C time constant is $200\mu\text{s}$ to 1ms .

7. Design Guide

This design guide provides a high-level explanation of how to design a single-phase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced in the following section. In addition to this guide, Renesas provides complete reference designs that include schematics, bill of materials, and example board layouts.

7.1 Selecting the LC Output Filter

The duty cycle of an ideal buck converter in CCM is a function of the input and the output voltage. This relationship is written by [Equation 5](#):

$$(EQ. 5) \quad D = \frac{V_{OUT}}{V_{IN}}$$

The output inductor peak-to-peak ripple current is written by [Equation 6](#):

$$(EQ. 6) \quad I_{P-P} = \frac{V_{OUT} \cdot (1 - D)}{f_{SW} \cdot L}$$

A typical step-down DC/DC converter has an I_{P-P} of 20% to 40% of the maximum DC output load current for a practical design. The value of I_{P-P} is selected based upon several criteria such as MOSFET switching loss, inductor core loss and the resistive loss of the inductor winding.

The DC copper loss of the inductor can be estimated by [Equation 7](#):

$$(EQ. 7) \quad P_{COPPER} = I_{LOAD}^2 \cdot DCR$$

where I_{LOAD} is the converter output DC current.

The copper loss can be significant so attention has to be given to the DCR selection. Another factor to consider when choosing the inductor is its saturation characteristics at elevated temperatures. A saturated inductor could cause destruction of circuit components.

A DC/DC buck regulator must have output capacitance C_O into which ripple current I_{P-P} can flow. Current I_{P-P} develops a corresponding ripple voltage V_{P-P} across C_O , which is the sum of the voltage drop across the capacitor ESR and of the voltage change stemming from charge moved in and out of the capacitor.

These two voltages are written by [Equations 8](#) and [9](#):

$$(EQ. 8) \quad \Delta V_{ESR} = I_{P-P} \cdot ESR$$

$$(EQ. 9) \quad \Delta V_C = \frac{I_{P-P}}{8 \cdot C_O \cdot f_{SW}}$$

If the output of the converter has to support a load with high pulsating current, several capacitors need to be paralleled to reduce the total ESR until the required V_{P-P} is achieved. The inductance of the capacitor can cause a brief voltage dip if the load transient has an extremely high slew rate. Low inductance capacitors should be considered in this scenario. A capacitor dissipates heat as a function of RMS current and frequency. Be sure that I_{P-P} is shared by a sufficient quantity of paralleled capacitors so that they operate below the maximum rated RMS current at f_{SW} . Take into account that the rated value of a capacitor can fade as much as 50% as the DC voltage across it increases.

7.2 Selecting the Input Capacitor

The important parameters for the input capacitance are the voltage rating and the RMS current rating. For reliable operation, select capacitors with voltage and current ratings above the maximum input voltage that are capable of supplying the RMS current required by the switching circuit. Their voltage rating should be at least 1.25 times greater than the maximum input voltage, while a voltage rating of 1.5 times is a preferred rating. [Figure 37 on page 52](#) is a graph of the input capacitor RMS ripple current, normalized relative to output load current, as a function

of duty cycle and is adjusted for converter efficiency. The normalized RMS ripple current calculation is written as [Equation 10](#):

$$(EQ. 10) \quad I_{C_{IN}(RMS,NORMALIZED)} = \frac{I_{MAX} \cdot \sqrt{D \cdot (1-D) + \frac{D \cdot k^2}{12}}}{I_{MAX}}$$

where:

- I_{MAX} is the maximum continuous I_{LOAD} of the converter
- k is a multiplier (0 to 1) corresponding to the inductor peak-to-peak ripple amplitude expressed as a percentage of I_{MAX} (0% to 100%)
- D is the duty cycle that is adjusted to take into account the efficiency of the converter, which is written as [Equation 11](#):

$$(EQ. 11) \quad D = \frac{V_{OUT}}{V_{IN} \cdot EFF}$$

In addition to the capacitance, some low ESL ceramic capacitance is recommended to decouple between the drain of the high-side MOSFET and the source of the low-side MOSFET.

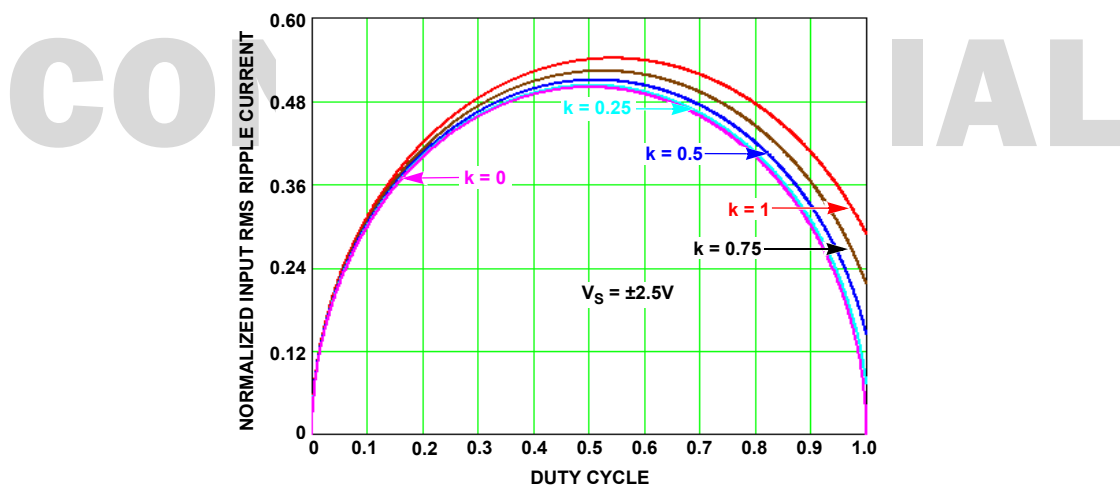


Figure 37. Normalized RMS Input Current at EFF = 1

7.3 Selecting the Switching Power MOSFET

Typically, a MOSFET cannot tolerate even brief excursions beyond its maximum drain-to-source voltage rating. The MOSFETs used in the power stage of the converter should have a maximum VDS rating that exceeds the sum of the upper voltage tolerance of the input power source and the voltage spike that occurs when the MOSFET switches off.

There are several power MOSFETs readily available that are optimized for DC/DC converter applications. The preferred high-side MOSFET emphasizes low gate charge so that the device spends the least amount of time dissipating power in the linear region. Unlike the low-side MOSFET, which has the drain-to-source voltage clamped by its body diode during turn off, the high-side MOSFET turns off with a VDS of approximately $V_{IN} - V_{OUT}$, plus the spike across it. The preferred low-side MOSFET emphasizes low $r_{DS(ON)}$ when fully saturated to minimize conduction loss. Note: that this is an optimal configuration of MOSFET selection for low duty cycle applications ($D < 50\%$). For higher output, low input voltage solutions, a more balanced MOSFET selection for high-side and low-side devices may be warranted.

For the Low-Side (LS) MOSFET, the power loss can be assumed to be conductive only and is written as [Equation 12](#):

$$(EQ. 12) \quad P_{CON_LS} \approx I_{LOAD}^2 \cdot r_{DS(ON)_LS} \cdot (1 - D)$$

For the High-Side (HS) MOSFET, conduction loss is written by [Equation 13](#):

$$(EQ. 13) \quad P_{CON_HS} = I_{LOAD}^2 \cdot r_{DS(ON)_HS} \cdot D$$

For the high-side MOSFET, the switching loss is written as [Equation 14](#):

$$(EQ. 14) \quad P_{SW_HS} = \frac{V_{IN} \cdot I_{VALLEY} \cdot t_{ON} \cdot f_{SW}}{2} + \frac{V_{IN} \cdot I_{PEAK} \cdot t_{OFF} \cdot f_{SW}}{2}$$

where:

- I_{VALLEY} is the difference of the DC component of the inductor current minus 1/2 of the inductor ripple current
- I_{PEAK} is the sum of the DC component of the inductor current plus 1/2 of the inductor ripple current
- t_{ON} is the time required to drive the device into saturation
- t_{OFF} is the time required to drive the device into cut-off

Renesas recommends using a 2.2 μ F (10V) VDD/VDDP capacitor, which has an effective capacitance higher than 0.4 μ F at 5V and x1.6 effective capacitance at the BOOT pin at 5V.

7.4 Selecting the Bootstrap Capacitor

The selection of the bootstrap capacitor is written by [Equation 15](#):

$$(EQ. 15) \quad C_{BOOT} = \frac{Q_g}{\Delta V_{BOOT}}$$

where:

- Q_g is the total gate charge required to turn on the high-side MOSFET
- ΔV_{BOOT} is the maximum allowed voltage decay across the boot capacitor each time the high-side MOSFET is switched on

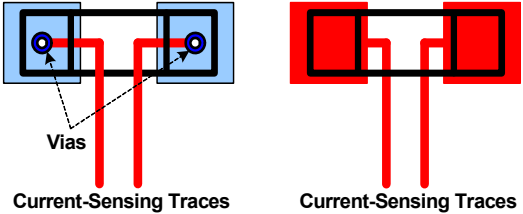
As an example, suppose the high-side MOSFET has a total gate charge Q_g of 25nC at $V_{GS} = 5V$ and a ΔV_{BOOT} of 200mV. The calculated bootstrap capacitance is 0.125 μ F; for a comfortable margin, select a capacitor that is double the calculated capacitance. In this example, 0.22 μ F will suffice. Use an X7R or X5R ceramic capacitor.

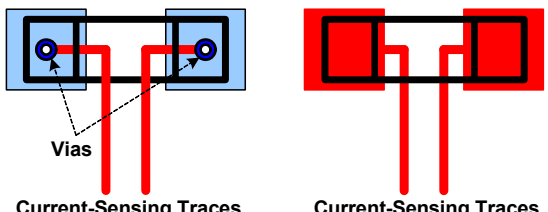
Renesas recommends using a bootstrap capacitor of 0.47 μ F (25V), which has an effective capacitance higher than 0.25 μ F at 5V and x50 effective high-side MOSFET gate capacitance.

7.5 Selecting the DCIN Filter

An RC filter is connected at the DCIN pin. Renesas recommends connecting a 10 Ω DCIN resistor between the DCIN pin and the VADP/VSYS diodes, and connecting a 4.7 μ F (50V) DCIN capacitor to GND, which has an effective capacitance higher than 0.4 μ F at 20V.

8. Layout Guidelines

Pin #	Symbol	Layout Guidelines
Bottom Pad	GND	Connect this ground pad to the ground plane through the low impedance path. Renesas recommends using at least five vias to connect to ground planes in PCB to ensure there is sufficient thermal dissipation directly under the IC.
1	ACIN	Place the voltage divider resistors and the optional decoupling capacitor in the general proximity of the controller.
2	ACOK	No special consideration.
3	SDA	
4	SCLK	
5	PROCHOT#	
6	AMON	
7	BMON	No special consideration.
8	PSYS	
9	PROG	Place the PROG programming resistor in the general proximity of the controller.
10	COMP	Place the compensation components in the general proximity of the controller.
11	CCLIM	Place the CCLIM voltage divider resistors in the general proximity of the controller.
12	FSET	Place the FSET programming resistor in the general proximity of the controller.
13	BATGONE	Place the 100kΩ resistor series in the BATGONE signal trace and the optional decoupling capacitor in the general proximity of the controller.
14	CSON	<p>Run two dedicated traces with sufficient width in parallel (close to each other to minimize the loop area) from the two terminals of the battery current-sensing resistor to the IC. Place the differential-mode and common-mode RC filter components in the general proximity of the controller.</p> <p>Route the current-sensing traces through vias to connect the center of the pads; or route the traces into the pads from the inside of the current-sensing resistor. The following drawings show the two preferred ways of routing current-sensing traces.</p> <div style="text-align: center;">  <p style="text-align: center;">Current-Sensing Traces Current-Sensing Traces</p> </div>
15	CSOP	
16	ACLIM	Place the ACLIM voltage divider resistors in the general proximity of the controller.
17	NTC	Place the resistor series with the NTC thermistor in the general proximity of the controller. Place the NTC thermistor at the point where the temperature is to be monitored. Note: if the NTC thermistor is too close to the switching components, it can couple the switching noise to the NTC pin.
18	DCIN	Place the OR diodes and the RC filter in the general proximity of the controller.
19	VDD	Place the RC filter from VDDP pin in the general proximity of the controller.
20	VDDP	Place the decoupling capacitor in the general proximity of the controller.
21	LGATE	Run LGATE trace in parallel with UGATE and PHASE traces on the same PCB layer. Use sufficient width. Avoid any sensitive analog signal trace from crossing over or getting close.

Pin #	Symbol	Layout Guidelines
22	PHASE	Run these two traces in a parallel fashion with sufficient width. Avoid any sensitive analog signal trace from crossing over or getting close. Route the PHASE trace to the high-side MOSFET source pin instead of general copper.
23	UGATE	<p>Place the IC close to the switching MOSFET's gate terminals and the gate drive signal traces short for a clean MOSFET drive. The IC can be placed on the opposite side of the switching MOSFETs.</p> <p>Place the input capacitors as close as possible to the switching high-side MOSFET drain and the low-side MOSFET source; and use shortest PCB trace connection. Place these capacitors on the same PCB layer with the MOSFETs instead of on different layers and using vias to make the connection.</p> <p>Place the inductor input terminal to the switching high-side MOSFET drain and low-side MOSFET source terminal as close as possible. Minimize this phase node area to lower the electrical and magnetic field radiation but make this phase node area big enough to carry the current. Place the inductor and the switching MOSFETs on the same layer of the PCB.</p>
24	BOOT	Place the bootstrap capacitor in the general proximity of the controller. Use sufficient wide trace. Avoid any sensitive analog signal trace from crossing over or getting close.
25	BGATE	Use sufficient width trace from the IC to the BGATE MOSFET gate.
26	VBAT	Place the RC filter in the general proximity of the controller. Run a dedicated trace from the battery positive connection point to the IC. In HPB configuration, separate this trace with the trace connecting the CSON pin.
27	QPCP	Place the charge pump flying capacitor in the general proximity of the controller. Route trace with sufficient width.
28	QPCN	
29	CMSRC	Run these two traces in parallel fashion with sufficient width.
30	ASGATE	
31	CSIN	<p>Place the battery current-sensing resistor right next to the inductor output. Run two dedicated trace with decent width in parallel (close to each other to minimize the loop area) from the two terminals of the adapter current-sensing resistor to the IC. Place the differential-mode and common-mode RC filter components in general proximity of the controller.</p> <p>Route the current-sensing traces through vias to connect the center of the pads; or route the traces into the pads from the inside of the current -sensing resistor. The following drawings show the two preferred ways of routing current-sensing traces.</p> <div style="text-align: center;">  <p>The left diagram shows a current-sensing resistor with two pads. Red traces connect the center of each pad through vias to the controller. The right diagram shows a similar setup, but the red traces connect to the pads from the inside of the resistor pads.</p> </div>
32	CSIP	

9. Revision History

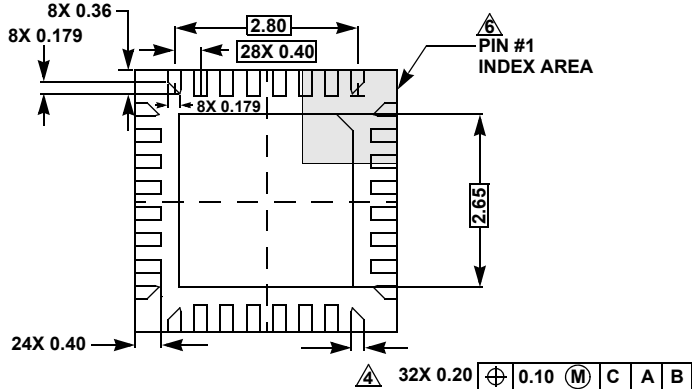
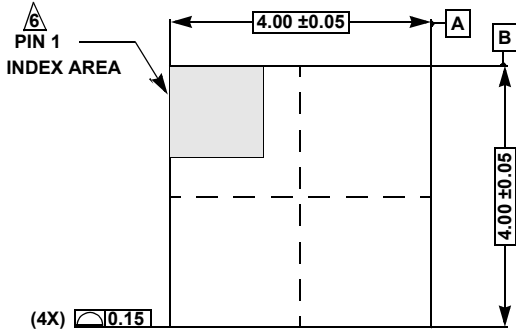
Rev.	Date	Change
3.00	Jul 12, 2019	Added Related Literature section. Updated ACIN, DCIN, VDD, VDDP, and BOOT pin descriptions. Added the last sentence to the Selecting the Switching Power MOSFET and Selecting the Bootstrap Capacitor sections on page 53. Added the DCIN Filter section on page 53. Updated Figures 2 and 38. Updated disclaimer.
2.00	Oct 12, 2018	Updated Ordering Information table to add tape and reel version to table and updated Notes 1 and 3. Corrected test reference used for ESD and Latch-up testing that was used on part. Updated verbiage in Sections 6.4 3rd paragraph and 6.5 2nd paragraph.
1.00	Feb 14, 2018	Removed ISL88739A from Table 1 on page 7. Removed About Intersil section. Updated Disclaimer.
0.00	Sep 7, 2017	Initial release

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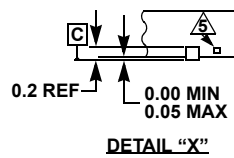
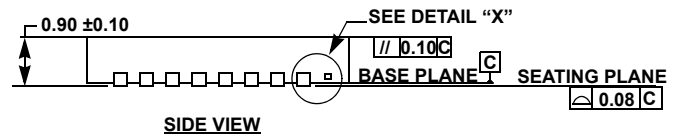
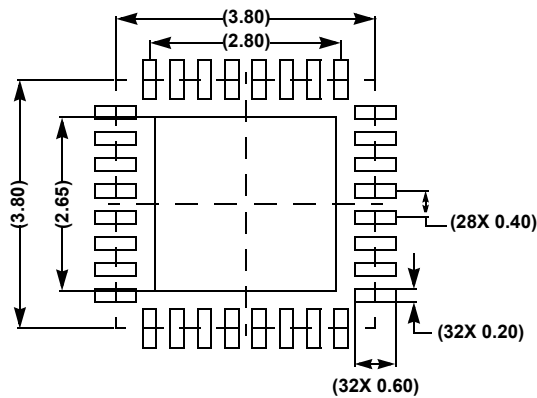
10. Package Outline Drawing

For the most recent package outline drawing, see [L32.4x4A](#).

L32.4x4A
 32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
 Rev 5, 2/16



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NOTES:

1. Dimensions are in millimeters.
 Dimensions in () for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.25mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
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