ISL80410

40V, Low Quiescent Current, High Accuracy, 150mA Linear Regulator

The ISL80410 is a high voltage, adjustable V_{OUT}, low quiescent current linear regulator ideally suited for "always-on" and "keep alive" applications. The ISL80410 operates from an input voltage of +6V to +40V under normal operating conditions and consumes only 18µA of quiescent current at no load.

The ISL80410 features an EN pin that can be used to put the device into a low-quiescent current shutdown mode in which it draws only 2µA of supply current. The device features over-temperature shutdown and current limit protection.

The ISL80410 is rated to operate across the -40°C to +125°C temperature range and is available in an 8 Ld Small Outline Exposed Pad Plastic Package (EPSOIC).

Applications

- Industrial
- Telecommunications

Features

- Wide V_{IN} range of 6V to 40V
- Adjustable output voltage from 2.5V to 12V
- Ensured 150mA output current
- Ultra low 18µA typical quiescent current
- Low 2µA of typical shutdown current
- ±1% accurate voltage reference (over temperature, load)
- Low dropout voltage of 295mV at 150mA
- Low 26µV_{RMS} noise
- 40V tolerant logic level (TTL/CMOS) enable input
- Stable operation with 10µF output capacitor
- 5kV ESD HBM rated
- Thermal shutdown and current limit protection
- 8 Ld exposed pad EPSOIC package

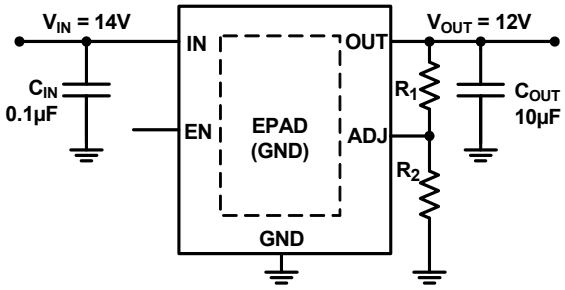

Figure 1. Typical Application

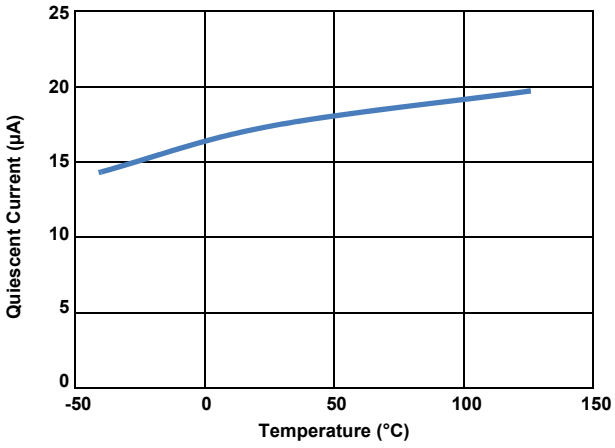

Figure 2. Quiescent Current vs Temperature (at Unity Gain), V_{IN} = 14V

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1. Overview

1.1 Block Diagram

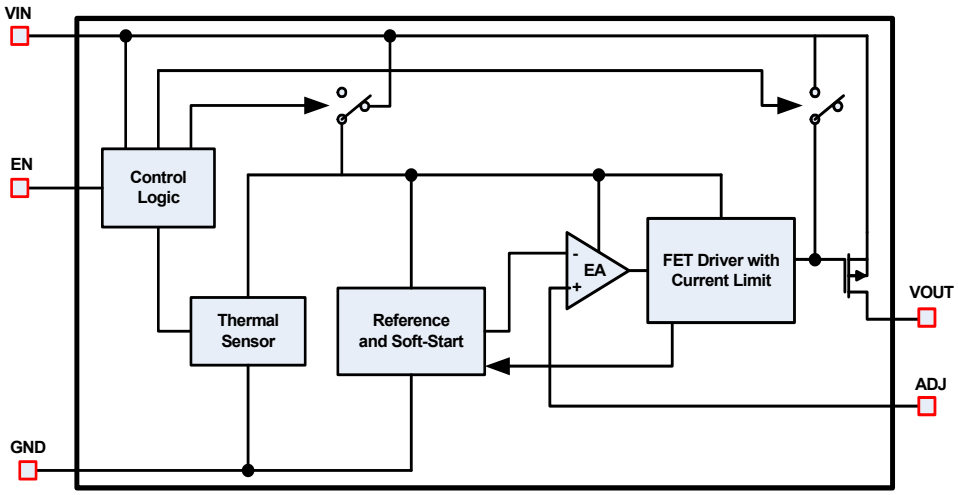


Figure 3. Block Diagram

1.2 Ordering Information

Part Number (Notes 2, 3)	Part Marking	Enable Pin	Output Voltage (V)	Package (RoHS Compliant)	Pkg. Dwg. #	Carrier Type (Note 1)	Temp. Range (°C)
ISL80410IBEZ	80410 IBEZ	Yes	ADJ	8 Ld EPSOIC	M8.15B	Tube	-40 to +125
ISL80410IBEZ-T						Reel, 2.5k	
ISL80410IBEZ-T7A						Reel, 250	
ISL80410EVAL1Z	Evaluation Platform						

Notes:

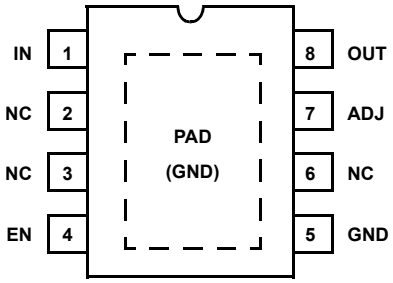
1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL80410 device page. For more information about MSL, see TB363.

Table 1. Key Differences in Family of 40V LDO Parts

Part Number	Minimum I_{OUT}	IC Package
ISL80410	150mA	8 Ld EPSOIC
ISL80136	50mA	8 Ld EPSOIC
ISL80138	150mA	14 LD HTSSOP

1.3 Pin Configuration

8 Ld EPSOIC
Top View



1.4 Pin Descriptions

Pin Number	Pin Name	Description
1	IN	Input voltage pin. A minimum 0.1µF X5R/X7R capacitor is required for proper operation. Range: 6V to 40V
2, 3, 6	NC	These pins have internal termination and can be left unconnected. Connection to ground is optional.
4	EN	Set this pin high to enable the device. Range: 0V to V_{IN}
5	GND	Ground pin.
7	ADJ	This pin is connected to the external feedback resistor divider, which sets the LDO output voltage.
8	OUT	Regulated output voltage. A 10µF X5R/X7R output capacitor is required for stability. Range: 0V to 12V
-	PAD	It is recommended to solder the PAD to the ground plane.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
IN Pin to GND Voltage	GND - 0.3	45	V
OUT Pin to GND Voltage	GND - 0.3	16	V
ADJ Pin to GND Voltage	GND - 0.3	3	V
EN Pin to GND Voltage	GND - 0.3	VIN	V
Output Short-Circuit Duration	Indefinite		-
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per JESD22-A114E)		5	kV
Machine Model (Tested per JESD-A115-A)		200	V
Charge Device Model (Tested per JESD22-C101C)		2.2	kV
Latch-up (Tested per JESD78B; Class II, Level A)		100	mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld EPSOIC Package (Notes 4, 5)	50	9

Notes:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. See TB379 for more information.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature		+150	°C
Maximum Storage Temperature Range	-65	+175	°C
Pb-Free Reflow Profile	See TB493		

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Ambient Temperature Range	-40	+125	°C
IN pin to GND Voltage	+6	+40	V
OUT pin to GND Voltage	+2.5	12	V
EN pin to GND Voltage	0	40	V

2.4 Electrical Specifications

Recommended Operating Conditions, unless otherwise noted. V_{IN} = 14V, I_{OUT} = 1mA, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical specifications are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
Input Voltage Range	V_{IN}		**6**		**40**	V
Guaranteed Output Current	I_{OUT}	V_{IN} = V_{OUT} + V_{DO}	**150**			mA
ADJ Reference Voltage	V_{OUT}	EN = High, V_{IN} = 14V, I_{OUT} = 0.1mA to 150mA	**1.211**	1.223	**1.235**	V
Line Regulation	(V_{OUT} low line - V_{OUT} high line) /V_{OUT} low line	6V < V_{IN} < 40V, I_{OUT} = 1mA		0.04	**0.15**	%
Load Regulation	(V_{OUT} no load - V_{OUT} high load) /V_{OUT} no load	V_{IN} = 14V, I_{OUT} = 100µA to 150mA		0.3	**0.6**	%
Dropout Voltage (Note 6)	ΔV_{DO}	I_{OUT} = 1mA, V_{OUT} = 2.5V		7	**33**	mV
		I_{OUT} = 150mA, V_{OUT} = 2.5V		380	**610**	mV
		I_{OUT} = 1mA, V_{OUT} = 5V		7	**33**	mV
		I_{OUT} = 150mA, V_{OUT} = 5V		295	**545**	mV
Shutdown Current	I_{SHDN}	EN = LOW		2	**3.64**	µA
Quiescent Current	IQ	EN = HIGH, I_{OUT} = 0mA		18	**24**	µA
		EN = HIGH, I_{OUT} = 1mA		22	**42**	µA
		EN = HIGH, I_{OUT} = 10mA		34	**60**	µA
		EN = HIGH, I_{OUT} = 150mA		90	**125**	µA
Power Supply Rejection Ratio	PSRR	f = 100Hz; V_{IN_RIPPLE} = 500mV_{P-P}; Load = 150mA		66		dB
Output Voltage Noise		V_{IN} = 14V, V_{OUT} = 3.3V, C_{OUT} = 10µF, I_{OUT} = 10mA, BW = 100Hz to 100kHz		26		µV_{RMS}
EN Function						
EN Threshold Voltage	V_{EN_H}	V_{OUT} = Off to On			**1.485**	V
	V_{EN_L}	V_{OUT} = On to Off	**0.975**			V
EN Pin Current	I_{EN}	V_{OUT} = 0V		0.026		µA
EN to Regulation Time (Note 7)	t_{EN}			1.65	**1.93**	ms
Protection Features						
Output Current Limit	I_{LIMIT}	V_{OUT} = 0V	**175**	410		mA
Thermal Shutdown	T_{SHDN}	Junction Temperature Rising		+165		°C
Thermal Shutdown Hysteresis	T_{HYST}			+20		°C

Notes:

6. Dropout voltage is defined as (V_{IN} - V_{OUT}) when V_{OUT} is 2% below the value of V_{OUT}.
7. Enable to Regulation Time is the time the output takes to reach 95% of its final value with V_{IN} = 14V. EN is taken from V_{IL} to V_{IH} in 5ns. For the adjustable versions, the output voltage is set at 5V.
8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

3. Typical Performance Curves

V_{IN} = 14V, I_{OUT} = 1mA, V_{OUT} = 5V, T_J = +25°C, unless otherwise specified.

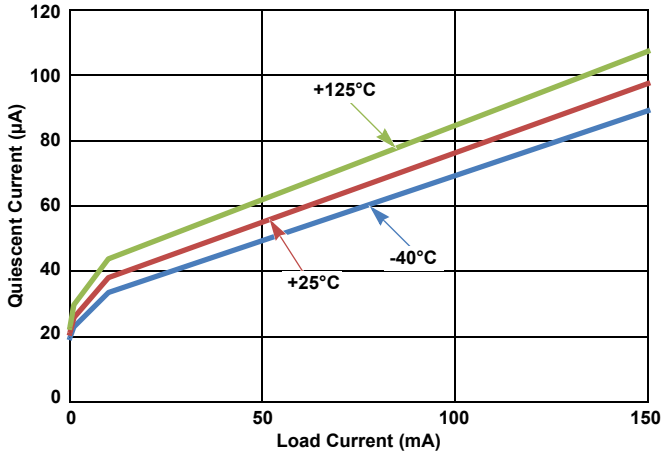


Figure 4. Quiescent Current vs Load Current

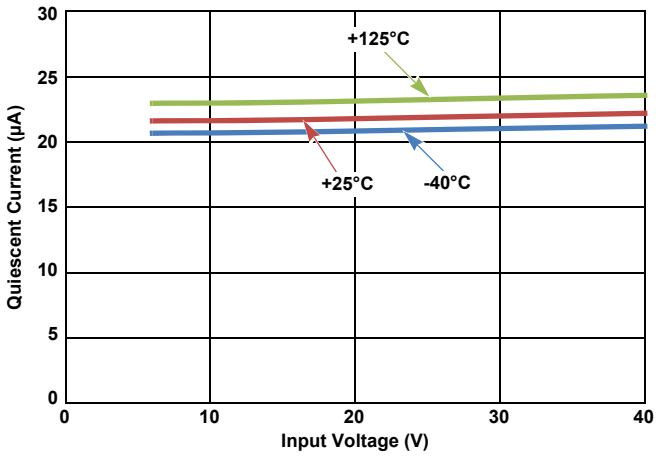


Figure 5. Quiescent Current vs Input Voltage (No Load)

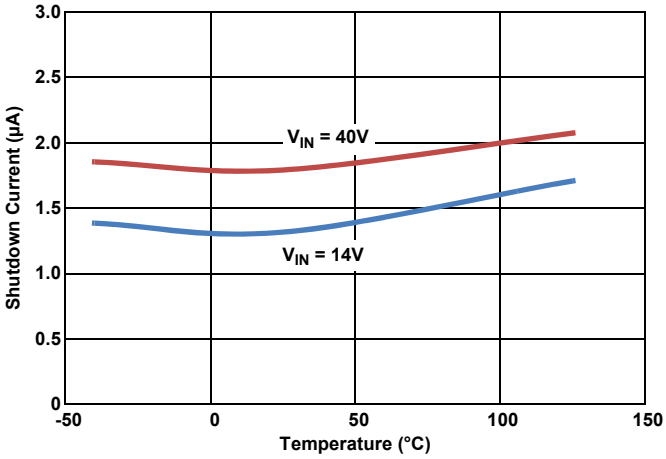


Figure 6. Shutdown Current vs Temperature (EN = 0)

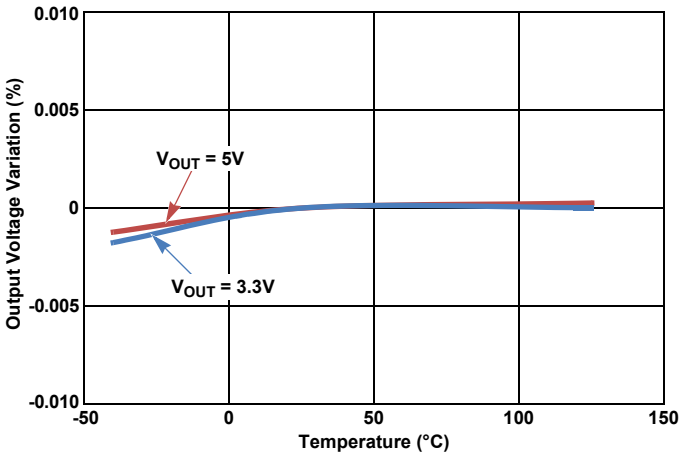


Figure 7. Output Voltage vs Temperature (Load = 50mA)

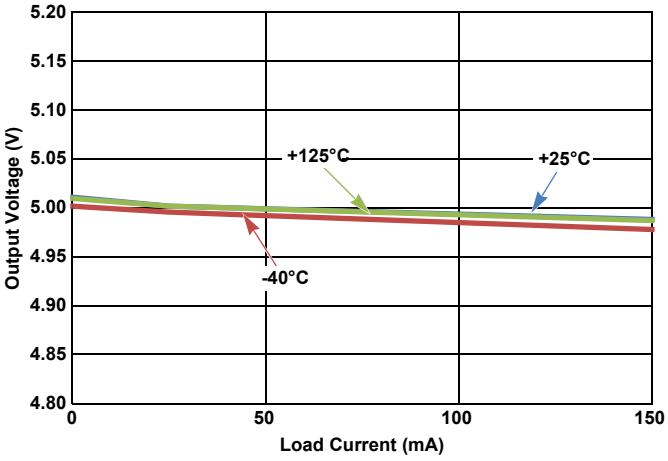


Figure 8. Output Voltage vs Load Current

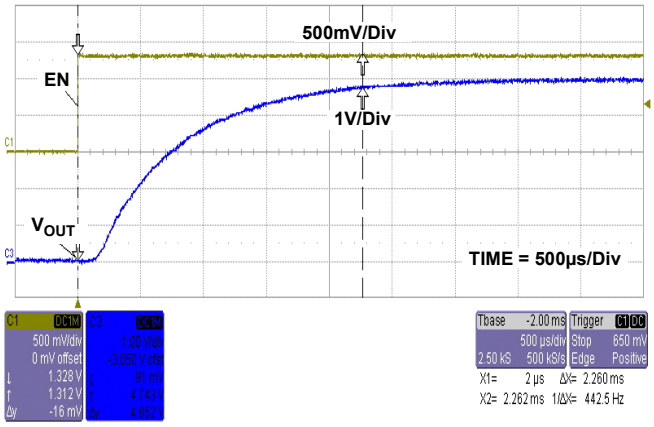


Figure 9. Start-Up Waveform

V_{IN} = 14V, I_{OUT} = 1mA, V_{OUT} = 5V, T_J = +25°C, unless otherwise specified. (Continued)

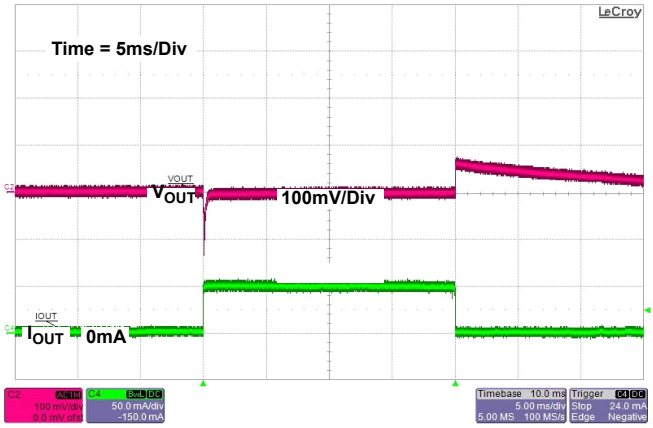


Figure 10. Load Transient Response

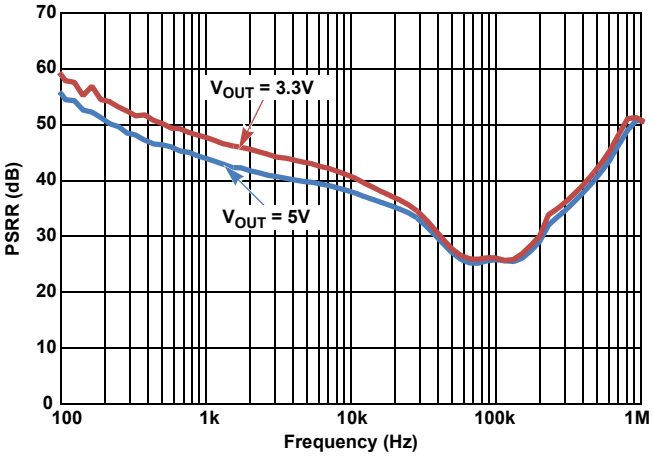


Figure 11. PSRR vs Frequency for Various Output Voltages, (Load = 150mA)

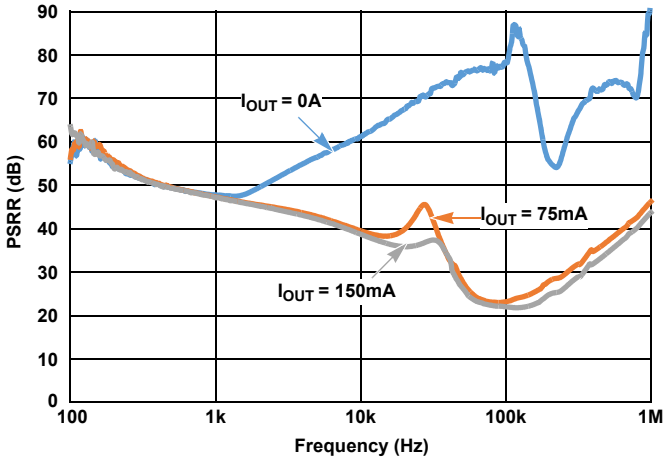


Figure 12. PSRR vs Frequency for Various Load Currents, V_{OUT} = 3.3V

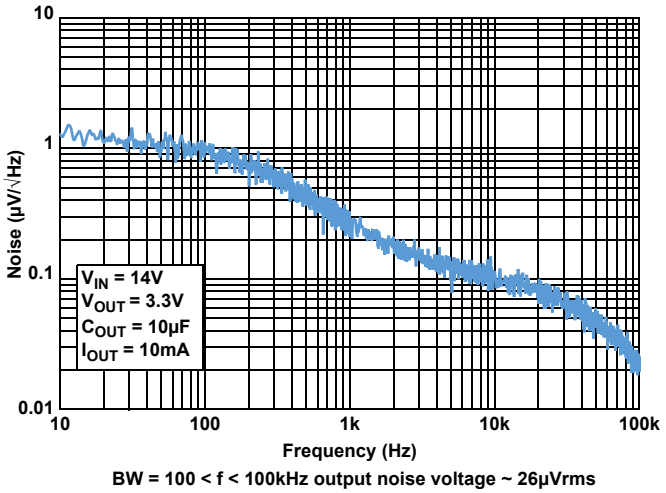


Figure 13. Output Noise Spectral Density, I_{OUT} = 10mA

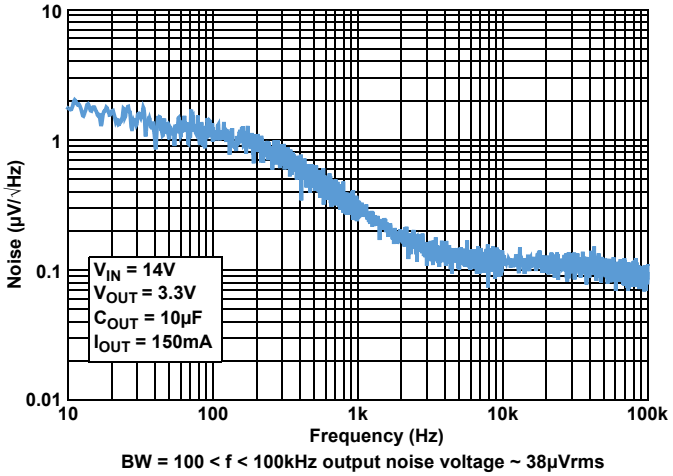


Figure 14. Output Noise Spectral Density, I_{OUT} = 150mA

4. Functional Description

4.1 Functional Overview

The ISL80410 is a high performance, high voltage, Low-Dropout regulator (LDO) with 150mA sourcing capability. The part is rated to operate across the -40°C to +125°C temperature range. Its ultra low quiescent current makes it an ideal choice for “always-on” applications. It works well under a “load dump condition” in which the input voltage could rise up to 40V. This LDO device also features current limit and thermal shutdown protection.

4.2 Enable Control

The ISL80410 has an enable pin, which turns the device on when pulled high. When EN is low, the IC goes into shutdown mode and draws less than 2µA of current. Tie the EN pin directly to IN for “always-on” operation.

4.3 Current Limit Protection

The ISL80410 has internal current limiting functionality to protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current largely independent of the output voltage. If the short or overload is removed from V_{OUT}, the output returns to normal voltage regulation mode.

4.4 Thermal Fault Protection

If the die temperature exceeds a typical value of +165°C, the output of the LDO shuts down until the die temperature cools to a typical value of +145°C. The level of power dissipated, combined with the ambient temperature and the thermal impedance of the package, determines if the junction temperature exceeds the thermal shutdown temperature. See “Power Dissipation” on page 9 for more details.

5. Application Information

5.1 Input and Output Capacitors

A minimum 0.1µF ceramic capacitor is recommended at the input for proper operation. For the output, a ceramic capacitor with a capacitance of 10µF is recommended for the ISL80410 to maintain stability. Route the ground connection of the output capacitor directly to the GND pin of the device and place it close to the IC.

5.2 Output Voltage Setting

The ISL80410 output voltage is programmed using an external resistor divider as shown in Figure 15.

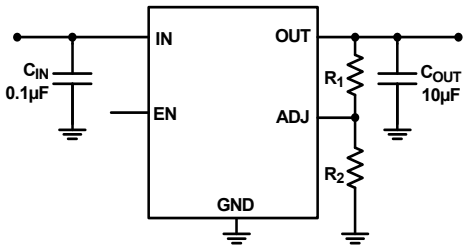


Figure 15. Output Voltage Setting

The output voltage is calculated using Equation 1:

(EQ. 1) $$V_{OUT} = 1.223V \times \left(\frac{R_1}{R_2} + 1\right)$$

5.3 Power Dissipation

The junction temperature must not exceed the range specified in "Recommended Operating Conditions" on page 4. The power dissipation can be calculated using Equation 2:

(EQ. 2) $$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND}$$

The maximum allowable junction temperature, $T_{J(MAX)}$, and the maximum expected ambient temperature, $T_{A(MAX)}$, determine the maximum allowable junction temperature rise (ΔT_J), as shown in Equation 3:

(EQ. 3) $$\Delta T_J = T_{J(MAX)} - T_{A(MAX)}$$

To calculate the maximum ambient operating temperature, use the junction-to-ambient thermal resistance (θ_{JA}) as shown in Equation 4:

(EQ. 4) $$T_{J(MAX)} = P_{D(MAX)} \times \theta_{JA} + T_A$$

5.4 Board Layout Recommendations

A good Printed Circuit Board (PCB) layout is important to achieve expected performance. When placing the components and routing the trace, minimize the ground impedance and keep the parasitic inductance low. The input and output capacitors should have a good ground connection and be placed as close to the IC as possible. The feedback trace in the adjustable version should be away from other noisy traces. Connect the exposed pad to the ground plane using as many vias as possible within the pad for the best thermal relief.

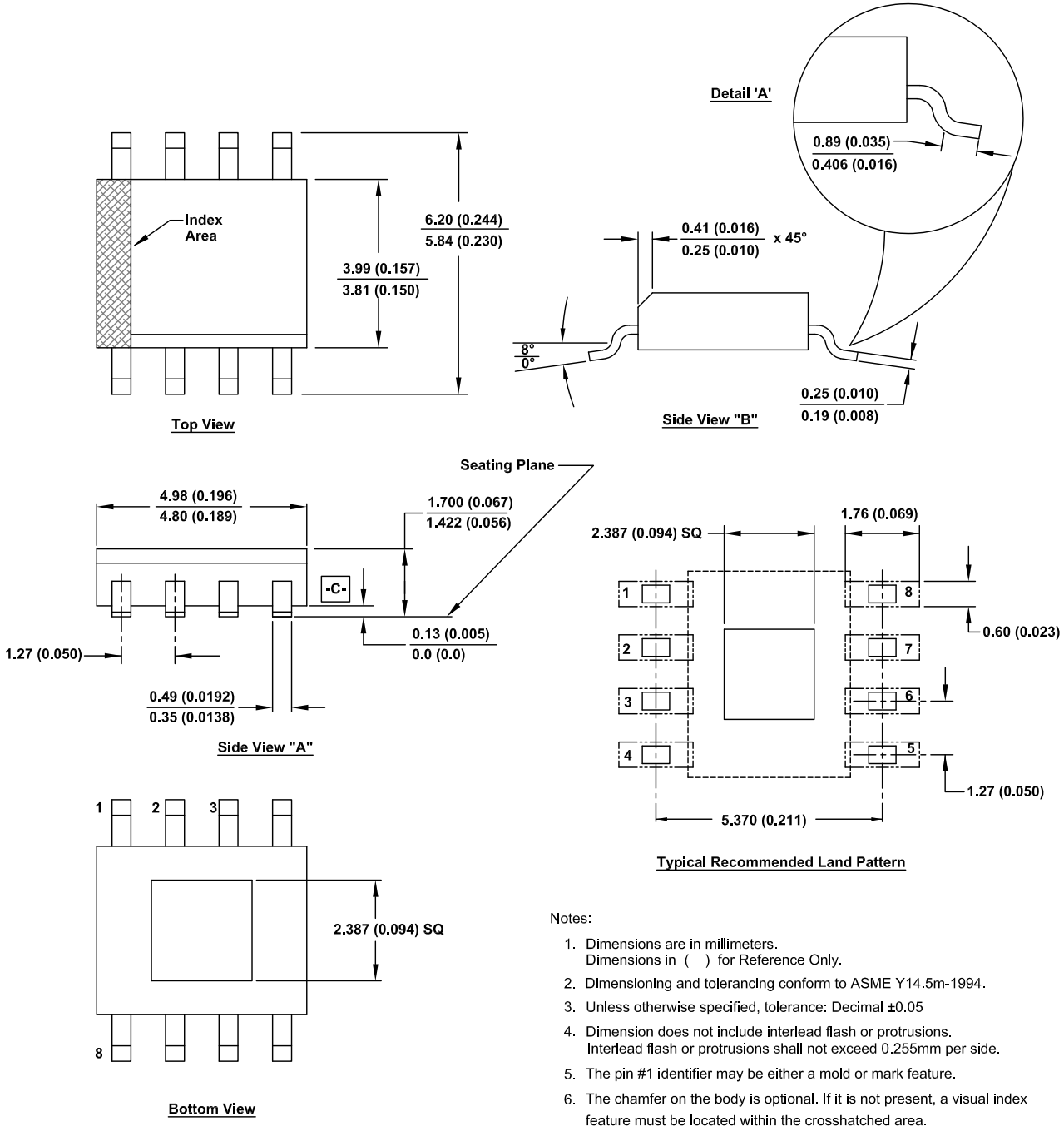
6. Revision History

Rev.	Date	Description
2.01	Oct 2, 2023	Updated M8.15B POD to the latest revision (corrected typo).
2.00	Aug 8, 2019	Updated POD to the latest revision. Changes are as follows: -Updated L Millimeter minimum in detail A from 0.41 to 0.406. -Updated the following in the Side View: -Changed total package height Millimeter MIN and MAX values from: 1.43 MIN and 1.68 MAX to: 1.422 MIN and 1.700 MAX and Inches max from 0.066 to 0.067. -Changed A1 Inches MIN from: 0.001 to 0.0, and A1 Millimeters MIN from 0.03 to 0.0
1.00	Feb 8, 2019	Updated title Updated the 6th bullet and added the 8th bullet in the features list. Updated Related Literature section. Updated ordering information table with tape and reel information and updated notes. Added Output Voltage Noise specification.
0.00	Jan 24, 2018	Initial release.

7. Package Outline Drawing

For the most recent package outline drawing, see M8.15B.

M8.15B
8 Lead Narrow Body Small Outline Exposed Pad Plastic Package
Rev 8, 9/2023



Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.255mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.

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