ISL80083

2.5MHz Integrated Power Management IC with I^{2}C Compatible Interface

FN7886
Rev 1.00
May 15, 2013

ISL80083 is an integrated mini Power Management IC (mini-PMIC) for powering low-voltage microprocessor, or applications using a single Li-Ion or Li-Polymer cell battery to power multiple voltage rails. ISL80083 integrates a high-efficiency 2.5MHz synchronous step-down converter, a low-input low-dropout linear regulator, 33MHz oscillator, level shift, and input supply select.

The 2.5MHz PWM switching frequency allows for the use of very small external inductors and capacitors. The step-down converter can enter skip mode under light load conditions to further improve the efficiency and maximize the battery life. For noise sensitive applications, it can also be programmed through I^{2}C interface to operate in forced PWM mode, regardless of the load current condition. The I^{2}C interface supports on-the-fly control of the output voltage from 0.625V to 2.225V at 25mV/step size for dynamic power saving. The step-down converter can supply up to 800mA load current. ISL80083 also provides a 300mA low dropout (LDO) regulator. The input voltage range is from 2.6V to 5.5V allowing it to be powered from one of the on-chip step-down converters or directly from the battery. The default LDO output comes with factory pre-set fixed output voltage options between 0.9V to 3.6V.

ISL80083 is available in a 2.11mm x 2.13mm 25 Ball CSP package.

Features

- 800mA synchronous step-down converter and 300mA, general-purpose LDO
- 400kb/s I^{2}C-bus series interface transfers the control data between the host controller and the ISL80083
- Fixed SMPS output voltage I^{2}C programmability
  - At 25mV/step . . . . . 0.625V to 2.225V
- LDO output voltage I^{2}C programmability
  - At 50mV/step . . . . . 0.9V to 3.6V
- 33MHz oscillator
- Level shift from 1.8V to 3V with enable
- Input select
- Switcher I^{2}C programmable skip mode under light load or forced fixed switching frequency PWM mode

Applications

- Power cable

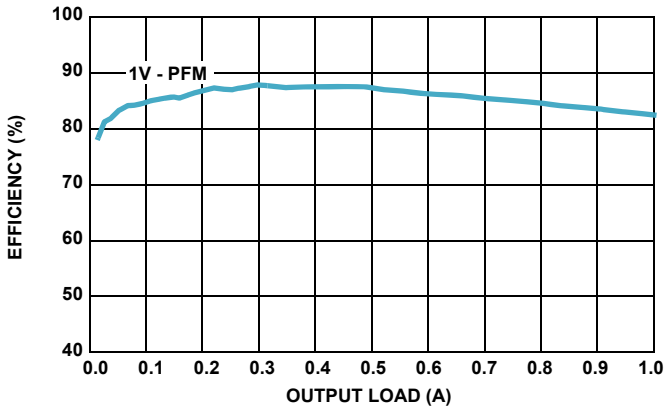
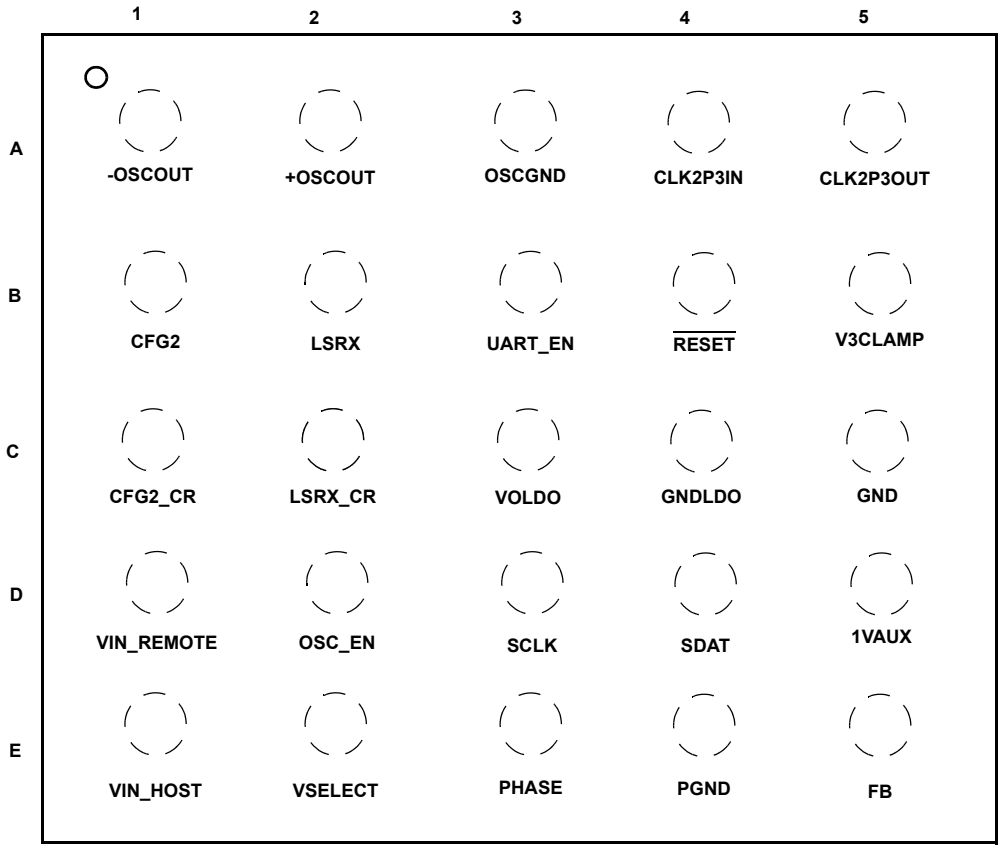


FIGURE 1. EFFICIENCY vs LOAD (3.3V$_{IN}$, T$_{A}$ = +25°C)

Pin Configuration

ISL80083
(25 BALL CSP 2.11 x 2.13mm)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
A1	-OSCOUT	Negative terminal of the precision 33MHz oscillator differential output.
A2	+OSCOUT	Positive terminal of the precision 33MHz oscillator differential output.
A3	OSCGND	Isolated ground for the internal 33MHz oscillator.
A4	CLK2P3IN	2.3V input for the 33MHz oscillator. Connect a 220nF capacitor from CLK2P3OUT to OSCGND.
A5	CLK2P3OUT	2.3V internal LDO output for the 33MHz oscillator. Connect CLK2P3IN to CLK2P3OUT along with a 220nF capacitor for low noise performance.
B1	CFG2	This is the output of the level shifter from the CFG2_CR rail control signal shifting from 1.8V to 3V.
B2	LSRX	This is the output of the level shifter from the LSRX_CR rail control signal shifting from 1.8V to 3V.
B3	UART_EN	Level shift of LSRX logic enable control. The output LSRX is in high Z state when UART_EN is pulled low. There is a 125kΩ pull-down resistor from this pin to GND.
B4	$\overline{\text{RESET}}$	This is a totem pole output to indicate a fault mode. The output is low if any of the fault is detected. The output is high during normal operation.
B5	V3CLAMP	This rail is a 3V LDO sourcing from VSELECT.
C1	CFG2_CR	This is the input to the level shifter for the CONFIG2 rail control signal shifting from 3V to 1.8V.
C2	LSRX_CR	This is the input to the level shifter from the LSRX rail control signal.
C3	VOLDO	Output of the LDO.

Pin Descriptions (Continued)

PIN NUMBER	PIN NAME	DESCRIPTION
C4	GNDLDO	Power ground for LDO.
C5	GND	System ground for analog and digital circuitry.
D1	VIN_REMOTE	Input voltage secondary for cases where VIN_HOST is valid, VIN_REMOTE is held off IC. If there is 2.6V present and VIN host is not valid, then the pass MOSFET turns on. If this voltage is greater than 4.5V, then its pass MOSFET turn off.
D2	OSC_EN	Oscillator control pin. Connect to logic high will allow all outputs to operate normally and SMPS in PWM. Connecting to logic low will disable the 33MHz oscillator, 1VAUX, and allow the SMPS to operate in high light load efficiency PFM. There is a 125kΩ pull-up resistor from this pin to 1.8V.
D3	SCLK	I^2C interface clock pin.
D4	SDAT	I^2C interface data pin.
D5	1VAUX	This rail is a low impedance pass PFET switch sourcing from switcher's output thru the VFB pin.
E1	VIN_HOST	Input voltage primary for the IC. If there is 2.6V present, then the pass MOSFET turns on. If this voltage is greater than 4.5V, then its pass MOSFET turn off.
E2	VSELECT	Input voltage for buck converter switcher, V3CLAMP, LDO, and it also serves as the power supply pin for the whole internal digital/analog circuits.
E3	PHASE	Switching node for DC to DC converter; connect to one terminal of the inductor.
E4	PGND	Power ground for switcher.
E5	FB	Feedback pin for switcher; connect external voltage divider resistors between switcher output, this pin and ground. For fixed output versions, connect this pin directly to the switcher output.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	FB (V)	SLV LDO (V)	TEMP. RANGE (°C)	PACKAGE Tape & Reel (Pb-free)	PKG. DWG. #
ISL80083IIZ-T	80083	Adj	3.3	-40 to +85	25 Ball WLCSP	W5x5.25B
ISL80083IIZ-TK	80083	Adj	3.3	-40 to +85	25 Ball WLCSP	W5x5.25B
ISL80083IIZ-TS	80083	Adj	3.3	-40 to +85	25 Ball WLCSP	W5x5.25B

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free WLCSP and BGA packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu - e1 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free WLCSP and BGA packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL80083. For more information on MSL please see Tech Brief TB363.

Block Diagram

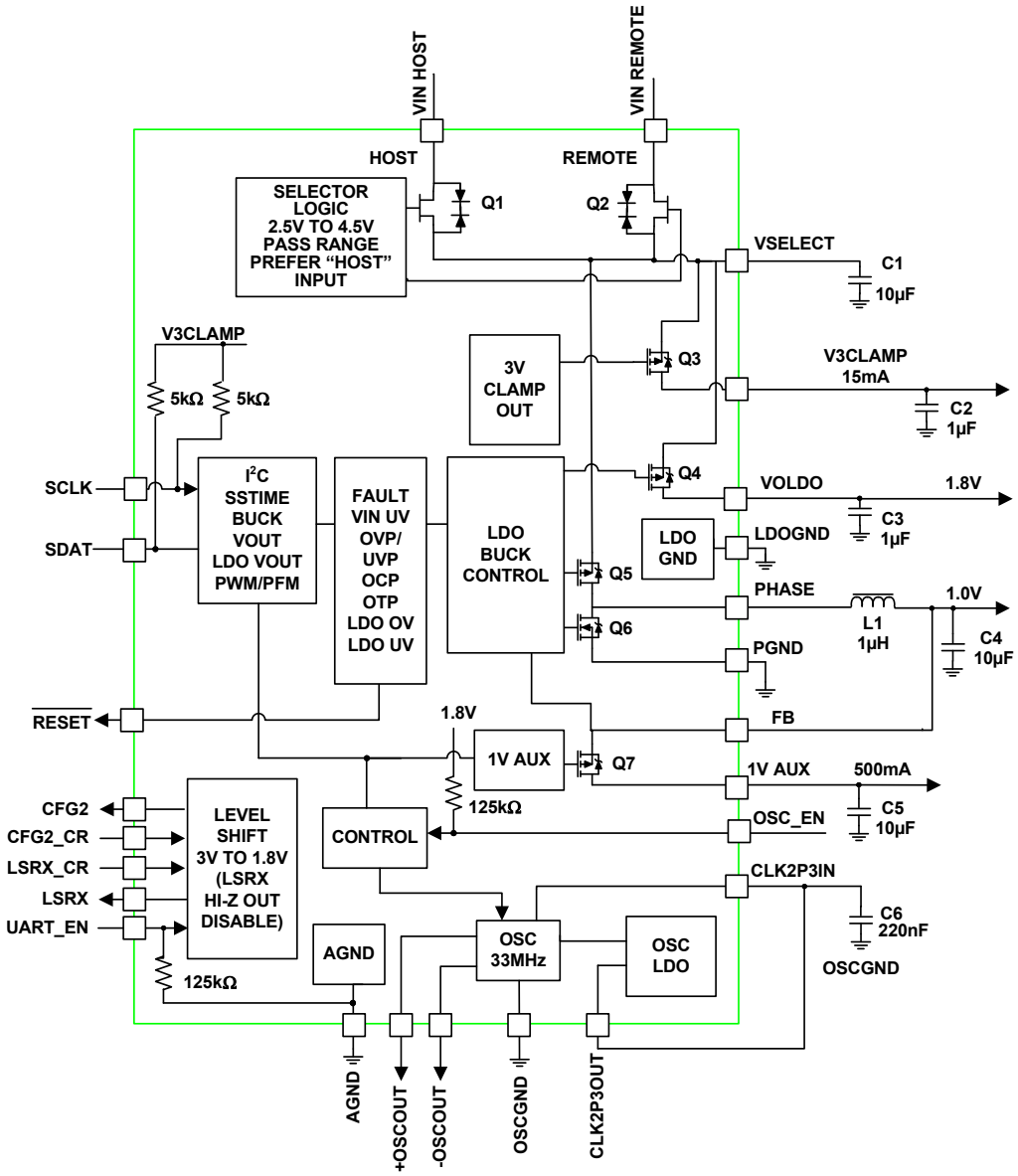


TABLE 1. TYPICAL APPLICATION PART LIST

PARTS	DESCRIPTION	MANUFACTURER	PART NUMBER	SPECIFICATIONS	SIZE
L1	Inductor	TDK	VSF302512T-1R0	1.0µH/1.8A/33mΩ	3.0mmx2.5mmx1.2mm
C1, C4, C5	Input and output capacitor	Murata	GRM21BR60J106KE19L	10µF/6.3V	0402
C2, C3	Output capacitor	Murata	GRM185R60J105KE26D	1µF/6.3V	0201
C6	Bias Capacitor	Various	GRM185R60J224KE26D	220nF/6.3V	0201

Absolute Maximum Ratings (Refer to ground)

VIN_HOST, VIN_REMOTE ..... –0.3V (DC) to 22V (DC)
VSELECT ..... –0.3V (DC) to 6.5V (DC) or 7V (20ms)
PHASE ..... -1.5V (100ns)/-0.3V (DC) to 6.5V (DC) or 7V (20ms)
V3PCLAMP ..... -0.3V to 6.5V
AGND, OSCGND, PGND, GNDLDO ..... -0.3V to 0.3V
1VAUX, CFG2, CFG2_CR, LSRX, LSRX_CR ..... -0.3V to 3.6V
$\overline{\text{RESET}}$, SDAT, SCLK, UART_EN, VOLDO ..... -0.3V to 3.6V
All other pins ..... -0.3V to 2.9V
ESD Ratings
Human Body Model (Tested per JESD22-A114F) 2kV
Machine Model (Tested per JESD22-A115-A) 200V
Charged Device Model (Tested per JESD22-C101D) 1kV
Latch Up (Tested per JESD78B, Class II, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CSP Package (Notes 4, 5)	70	0.9

Maximum Junction Temperature Range ..... -40°C to +150°C
Recommended Junction Temperature Range ..... 0°C to +125°C
Storage Temperature Range ..... -40°C to +150°C
Pb-free Reflow Profile ..... see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

VIN_HOST, VIN_REMOTE ..... 2.7V to 20V
SMPS Output Current ..... 0A to 800mA
LDO Output Current ..... 0mA to 300mA
Operating Ambient Temperature ..... 0°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications

Unless otherwise noted, all parameter limits are guaranteed over the recommended operating conditions and the typical specifications are measured at the following conditions: T_A = +25°C, VIN_HOST or VIN_REMOTE = 3.3V. For LDO, VSELECT = VOLDO + 0.5V to 5.5V, L1 = 1.0µH, C1 = C4 = C5 = 10µF, C2 = C3 = C6 = 1µF, I_{OUT} = 0A for SMPS and LDO (see Figure 1 for more details). **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
VIN_HOST or VIN_REMOTE Voltage Range			**2.7**		**20**	V
VSELECT Undervoltage Lockout Threshold	V_{UVLO}	Rising, I_{OUT} = 0A for both SMPS and LDO	**2.40**	2.56	**2.62**	V
		Falling	**2.30**	2.46	**2.57**	V
Quiescent Supply Current on VSELECT	$I_{VSELECT}$	All outputs no loading		150	**500**	µA
Thermal Shutdown				155		°C
Thermal Shutdown Hysteresis				30		°C
INPUT SELECTOR						
VIN_HOST P-Channel MOSFET ON-resistance	Q1	VSELECT = 3.3V, I_O = 200mA		0.20		Ω
VIN_REMOTE P-Channel MOSFET ON-resistance	Q2	VSELECT = 3.3V, I_O = 200mA		0.20		Ω
Minimum Pass Range Voltage	V_{IN_MIN}			2.2	**2.7**	V
Maximum Pass Range Voltage	V_{IN_Max}			4.5	**5.52**	V
SMPS						
Output Start Up Voltage		VSELECT = 3.3V, PWM	**0.950**	1.000	**1.050**	V
Line Regulation		VSELECT = V_O + 0.5V to 5.5V (minimal 2.5V)		0.1		%/V
P-Channel MOSFET ON-resistance	Q5	VSELECT = 3.3V, I_O = 200mA		0.14	**0.18**	Ω
N-Channel MOSFET ON-resistance	Q6	VSELECT = 3.3V, I_O = 200mA		0.05	**0.08**	Ω
P-Channel MOSFET Peak Current Limit	I_{PK}		**1**	1.4	**1.7**	A
PWM Switching Frequency	f_S	f_{OSC}/13		2.5		MHz
SW Minimum ON-time		V_{FB} = 2V		70		ns

Electrical Specifications Unless otherwise noted, all parameter limits are guaranteed over the recommended operating conditions and the typical specifications are measured at the following conditions: T_A = +25°C, VIN_HOST or VIN_REMOTE = 3.3V. For LDO, VSELECT = VOLDO + 0.5V to 5.5V, L1 = 1.0µH, C1 = C4 = C5 = 10µF, C2 = C3 = C6 = 1µF, I_{OUT} = 0A for SMPS and LDO (see Figure 1 for more details). **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
SS Time		VOUT Rise Time		1		ms
Soft-Discharge Resistor		Resistor from PHASE to PGND		115		Ω
1VAUX						
P-Channel MOSFET ON-resistance	Q7	I_O = 200mA		0.07		Ω
Shutdown Delay Time		Sleep Mode From OSC_EN < 0.45V		1.5		ms
LDOs						
Internal Peak Current Limit			**200**	425	**540**	mA
VOLDO Output Start-Up Voltage		VSELECT = 3.3V	**1.71**	1.80	**1.89**	V
V3CLAMP Output Voltage		I_{3P3V} = 15mA, VSELECT = 3.3V	**2.7**	3.0	**3.3**	V
VOLDO Power Supply Rejection Ratio		I_O = 300mA @ 1kHz, VSELECT = 3.3V, V_O = 2.6V, T_A = +25°C		55		dB
VOLDO Output Voltage Noise		VSELECT = 3.3V, I_O = 10mA, T_A = +25°C, BW = 10Hz to 100kHz		45		μV_{RMS}
LEVEL SHFT						
CFG2_CR Logic High Input			**1.4**			V
CFG2_CR Logic Low Input					**0.4**	V
LSRX_CR Logic High Input		UART_EN > 1.2V	**1.4**			V
LSRX_CR Logic Low Input		UART_EN > 1.2V			**0.4**	V
CFG2 Logic High Output		CFG2_CR > 1.2V, 3.3kΩ Pull-down	**2.8**		**3.3**	V
CFG2 Logic Low Output		CFG2_CR < 0.4V, 3.3kΩ Pull-down			**0.4**	V
LSRX Logic High Output		UART_EN > 1.2V, LSRX_CR > 1.2V, 1MΩ Pull-down	**2.4**		**3.2**	V
LSRX Logic Low Output		UART_EN > 1.2V, LSRX_CR < 0.4V, 1MkΩ Pull-down			**0.4**	V
CFG2 Low-to-High Prop Delay		CFG2_CR > 1.2V		50		ns
CFG2 High-to-Low Prop Delay		CFG2_CR < 0.4V		50		ns
LSRX Low-to-High Prop Delay		UART_EN > 1.2V, LSRX_CR > 1.2V		50		ns
LSRX High-to-Low Prop Delay		UART_EN > 1.2V, LSRX_CR < 0.4V		50		ns
LSRX Output Impedance	High Z	UART_EN < 0.6V		10		MΩ
OSCILLATOR						
CLK2P3OUT Voltage		I_{2P2V} = 15mA, VSELECT = 2.8V to 5.5V	**2.25**	2.30	**2.35**	V
Output Voltage	V_{OH}	Single-ended (+OSCOUT or -OSCOUT)	**700**			mV
Output Voltage	V_{OL}	Single-ended (+OSCOUT or -OSCOUT)			**100**	mV
Frequency		Measured from +OSCOUT to -OSCOUT, VSELECT = 3.3V		33.00		MHz
Jitter		Measured from +OSCOUT to -OSCOUT, VSELECT = 3.3V		6		ps RMS/ Cycle
CLK_OSC Disable Time - Sleep Mode		Delay from OSC_EN < 0.45V		1		ms
CLK_OSC Start Time From Sleep		From CLK_EN > 1.2V		100		µs

I^2C Interface Timing Specifications For SCL and SDA pins, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
C_{pin}	Pin Capacitance				**15**	pF
f_{SCL}	SCL Frequency				**400**	kHz
t_{sp}	Pulse Width Suppression Time at SDA and SCL Inputs	Any pulse narrower than the max spec is suppressed			**50**	ns
t_{AA}	SCL Falling Edge to SDA Output Data Valid	SCL falling edge crossing V_{IL}, until SDA exits the V_{IL} to V_{IH} window			**900**	ns
t_{BUF}	Time the Bus Must be Free Before the Start of a New Transmission	SDA crossing V_{IH} during a STOP condition, to SDA crossing V_{IH} during the following START condition	**1300**			ns
t_{LOW}	Clock LOW Time	Measured at the V_{IL} crossings	**1300**			ns
t_{HIGH}	Clock HIGH Time	Measured at the V_{IH} crossings	**600**			ns
$t_{SU:STA}$	START Condition Set-up Time	SCL rising edge to SDA falling edge; both crossing V_{IH}	**600**			ns
$t_{HD:STA}$	START Condition Hold Time	From SDA falling edge crossing V_{IL} to SCL falling edge crossing V_{IH}	**600**			ns
$t_{SU:DAT}$	Input Data Set-up Time	From SDA exiting the V_{IL} to V_{IH} window, to SCL rising edge crossing V_{IL}	**100**			ns
$t_{HD:DAT}$	Input Data Hold Time	From SCL rising edge crossing V_{IH} to SDA entering the V_{IL} to V_{IH} window	**0**			ns
$t_{SU:STO}$	STOP Condition Set-up Time	From SCL rising edge crossing V_{IH}, to SDA rising edge crossing V_{IL}	**600**			ns
$t_{HD:STO}$	STOP Condition Hold Time for Read, or Volatile Only Write	From SDA rising edge to SCL falling edge; both crossing V_{IH}	**1300**			ns
t_{DH}	Output Data Hold Time	From SCL falling edge crossing V_{IL}, until SDA enters the V_{IL} to V_{IH} window	**0**			ns
t_R	SDA and SCL Rise Time	From V_{IL} to V_{IH}	**20 + 0.1 x Cb**		**250**	ns
t_F	SDA and SCL Fall Time	From V_{IH} to V_{IL}	**20 + 0.1 x Cb**		**250**	ns
Cb	Capacitive Loading of SDA or SCL	Total on-chip and off-chip	**10**		**400**	pF
Rpu	SDA and SCL Bus Pull-up Resistor Off-Chip	Maximum is determined by t_R and t_F For Cb = 400pF, max is about 2kΩ~2.5kΩ For Cb = 40pF, max is about 15kΩ~20kΩ	**1**			kΩ

NOTE:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves and Waveforms

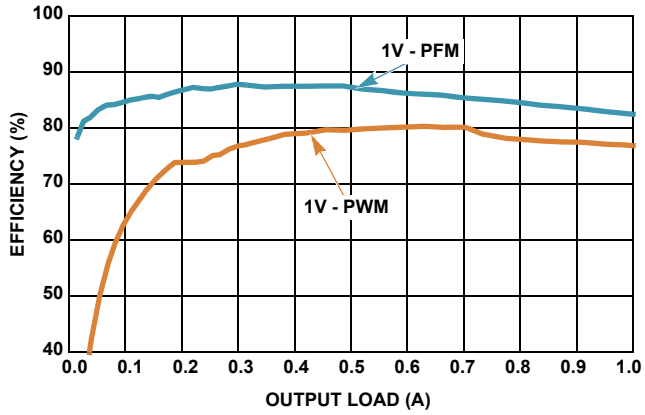


FIGURE 2. EFFICIENCY vs LOAD ($3.3V_{IN}$, $T_{A=}$ +25°C)

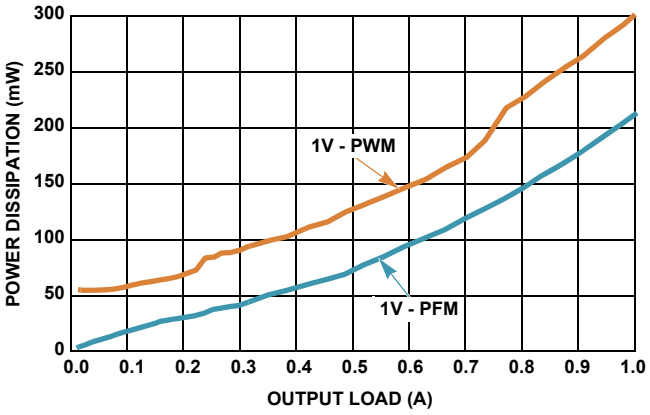


FIGURE 3. POWER DISSIPATION vs LOAD ($3.3V_{IN}$, $T_{A=}$ +25°C)

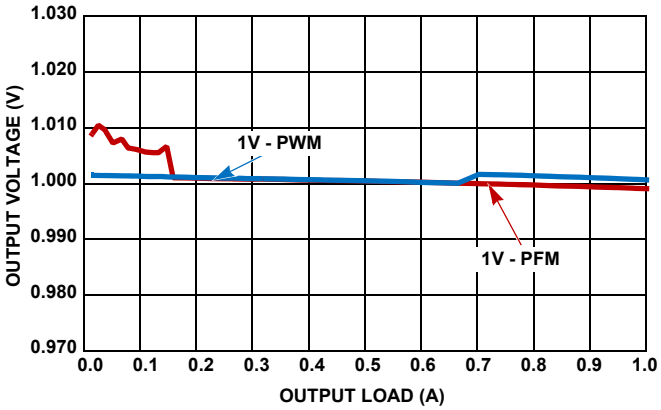


FIGURE 4. VOUT REGULATION vs LOAD ($3.3V_{IN}$, $T_{A=}$ +25°C)

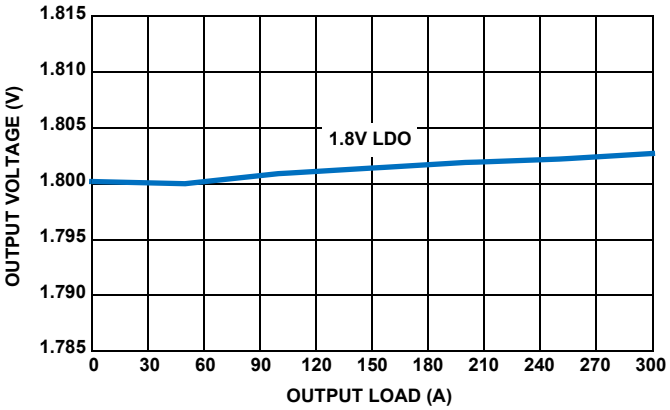


FIGURE 5. VOUT REGULATION vs LOAD ($3.3V_{IN}$, $T_{A=}$ +25°C)

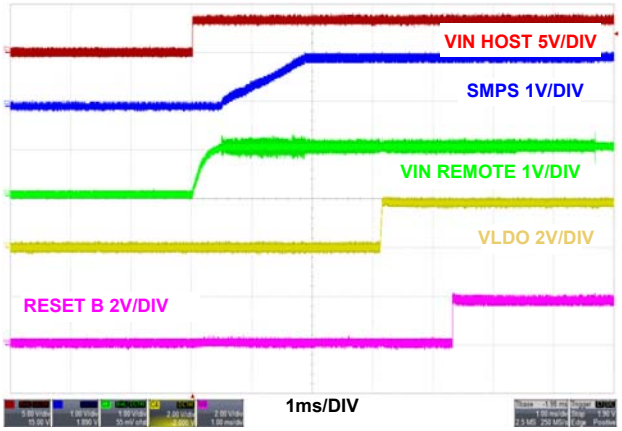


FIGURE 6. START-UP WITH VIN HOST = 3.3V AT NO LOAD (PFM)

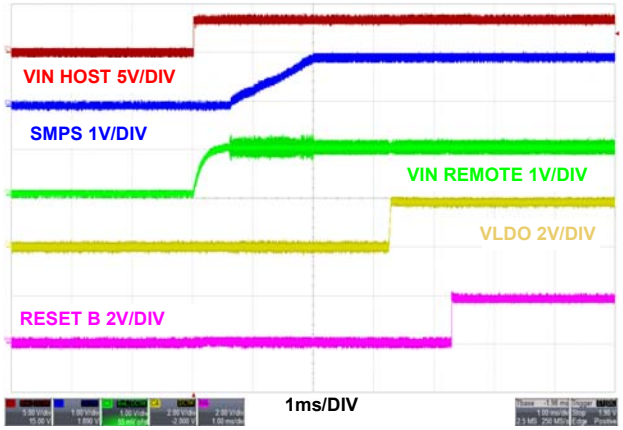


FIGURE 7. START-UP WITH VIN HOST = 3.3V AT NO LOAD (PWM)

Typical Performance Curves and Waveforms (Continued)

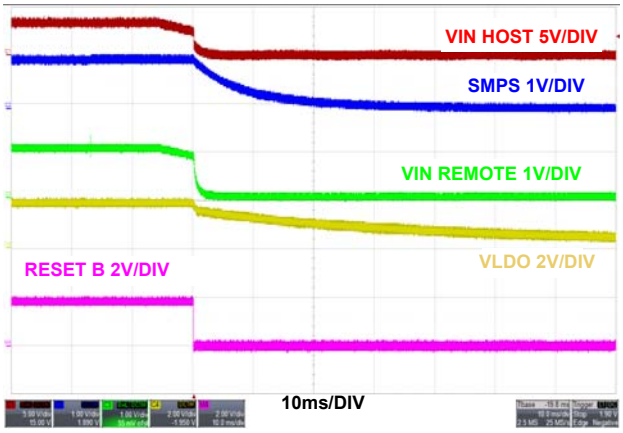


FIGURE 8. SHUT DOWN VIN HOST = 3.3V AT NO LOAD (PFM)

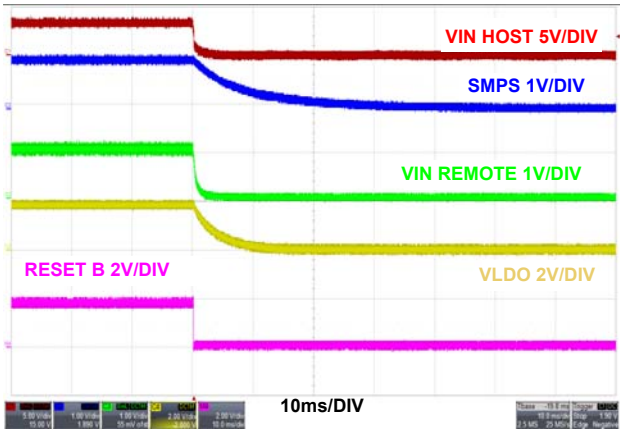


FIGURE 9. SHUT DOWN VIN HOST = 3.3V AT NO LOAD (PWM)

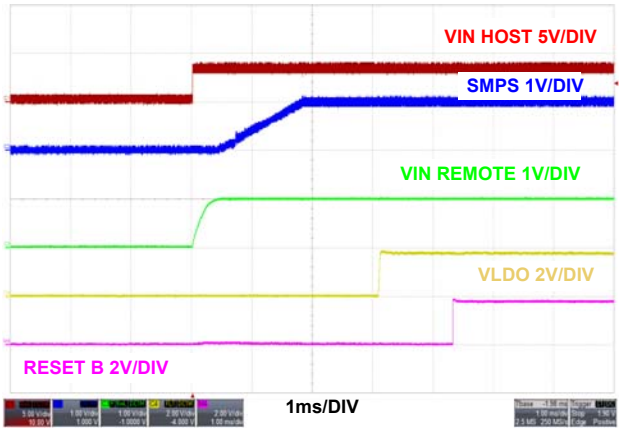


FIGURE 10. START-UP VIN HOST = 3.3V AT 0.8A LOAD (PWM)

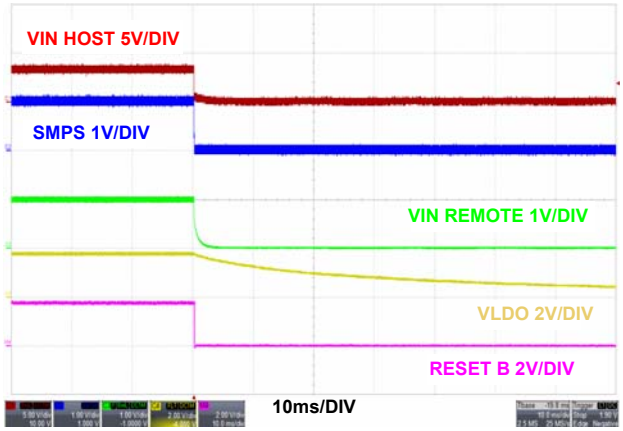


FIGURE 11. SHUTDOWN VIN HOST = 3.3V AT 0.8A LOAD (PWM)

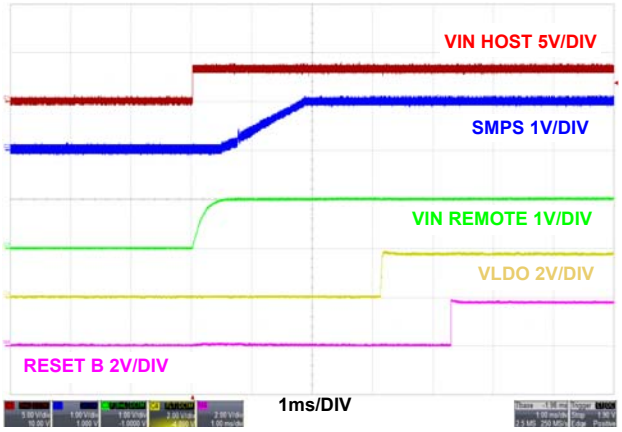


FIGURE 12. START-UP VIN HOST = 3.3V AT 0.8A LOAD (PFM)

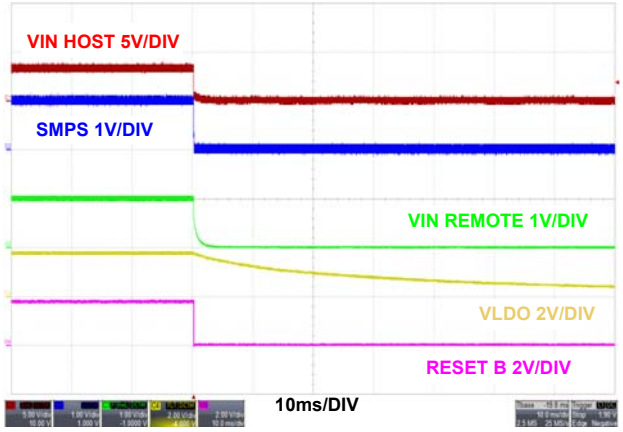


FIGURE 13. SHUTDOWN VIN HOST = 3.3V AT 0.8A LOAD (PFM)

Typical Performance Curves and Waveforms (Continued)

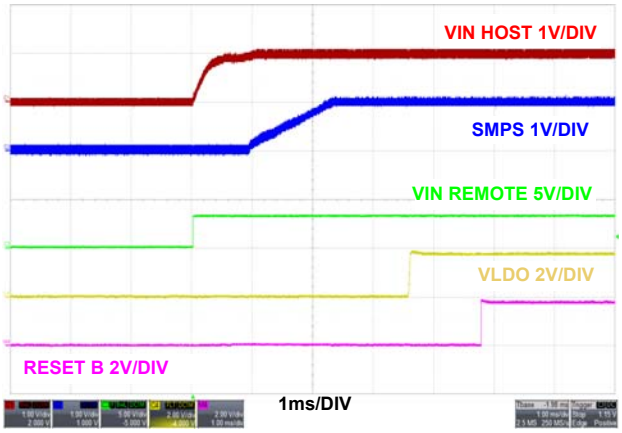


FIGURE 14. START-UP VIN REMOTE = 3.3V AT NO LOAD (PWM)

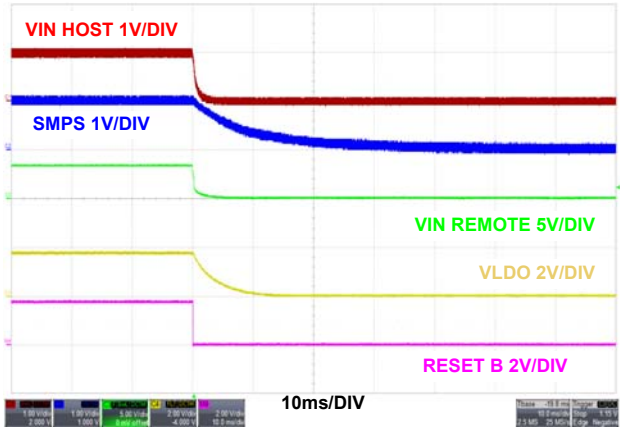


FIGURE 15. SHUTDOWN VIN REMOTE = 3.3V AT NO LOAD (PWM)

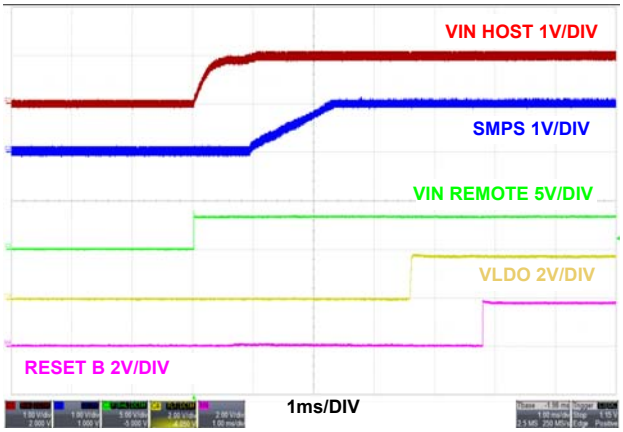


FIGURE 16. START-UP VIN REMOTE = 3.3V AT NO LOAD (PFM)

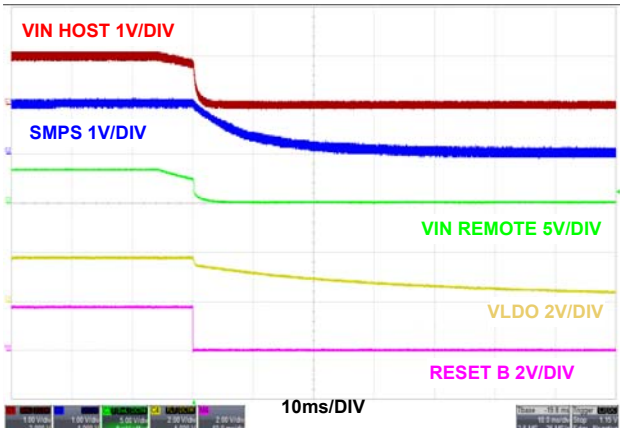


FIGURE 17. SHUTDOWN VIN REMOTE = 3.3V AT NO LOAD (PFM)

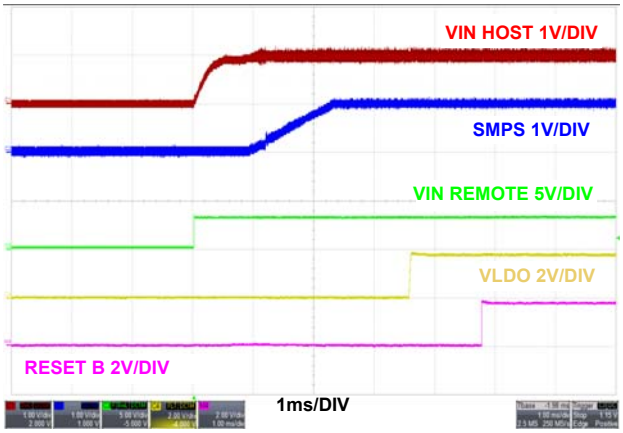


FIGURE 18. START-UP VIN REMOTE = 3.3V AT 0.8A LOAD (PFM)

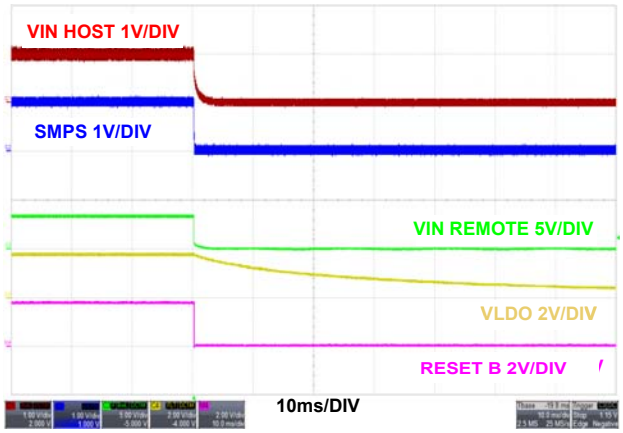


FIGURE 19. SHUTDOWN VIN REMOTE = 3.3V AT 0.8A LOAD (PFM)

Typical Performance Curves and Waveforms (Continued)

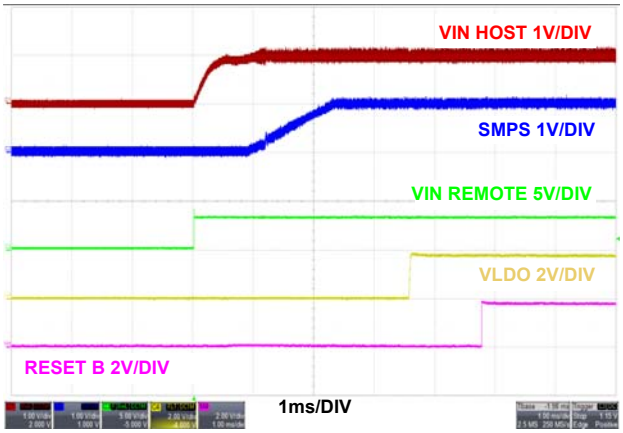


FIGURE 20. START-UP VIN REMOTE = 3.3V AT 0.8A LOAD (PWM)

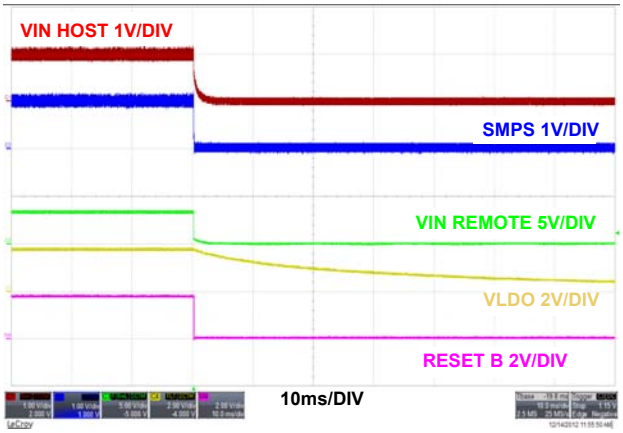


FIGURE 21. SHUTDOWN VIN REMOTE = 3.3V AT 0.8A LOAD (PWM)

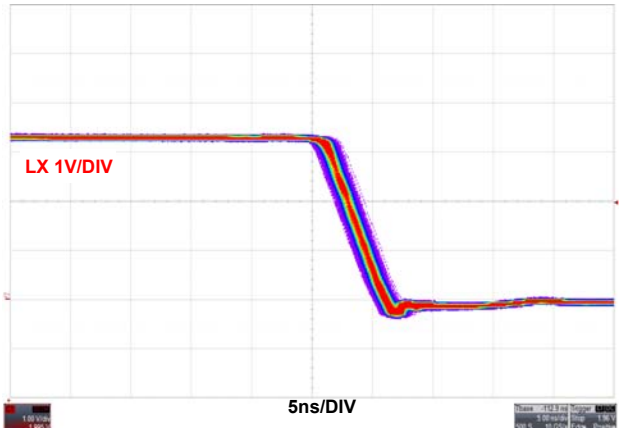


FIGURE 22. JITTER AT NO LOAD (PWM), VIN = 3.3V

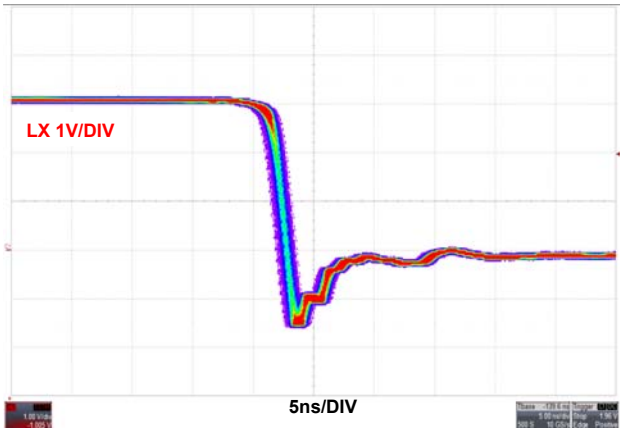


FIGURE 23. JITTER AT FULL LOAD (PWM), VIN = 3.3V

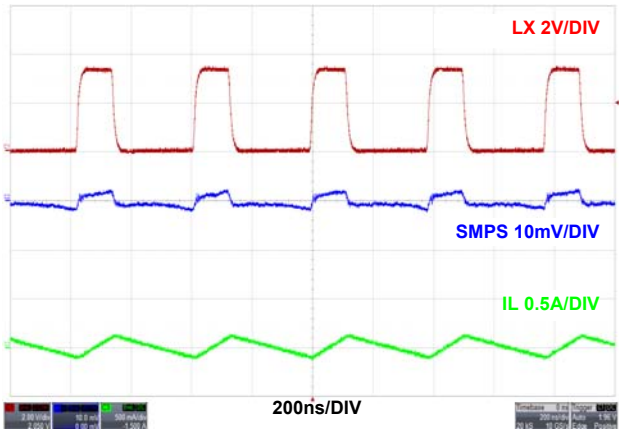


FIGURE 24. STEADY STATE AT NO LOAD (PWM), VIN = 3.3V

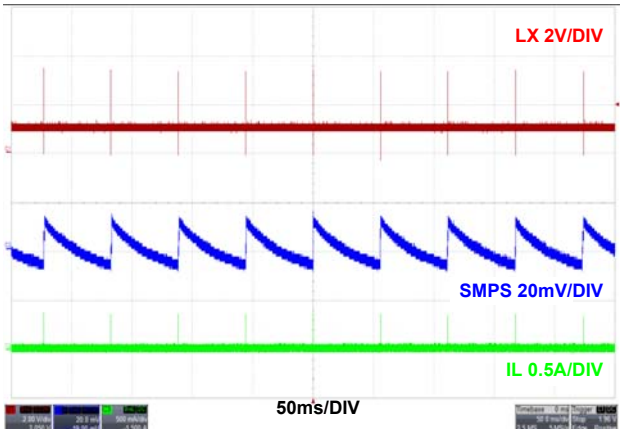


FIGURE 25. STEADY STATE AT NO LOAD (PFM), VIN = 3.3V

Typical Performance Curves and Waveforms (Continued)

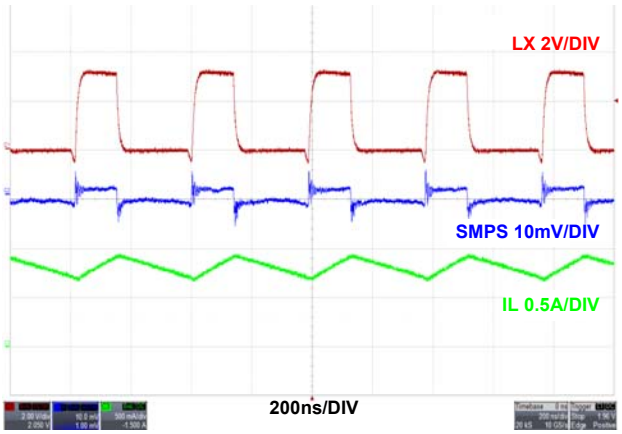


FIGURE 26. STEADY STATE AT 0.8A LOAD (PWM), VIN = 3.3V

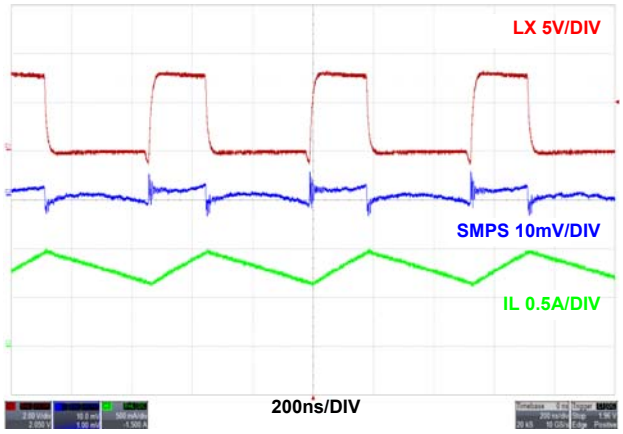


FIGURE 27. STEADY STATE AT 0.8A LOAD (PFM), VIN = 3.3V

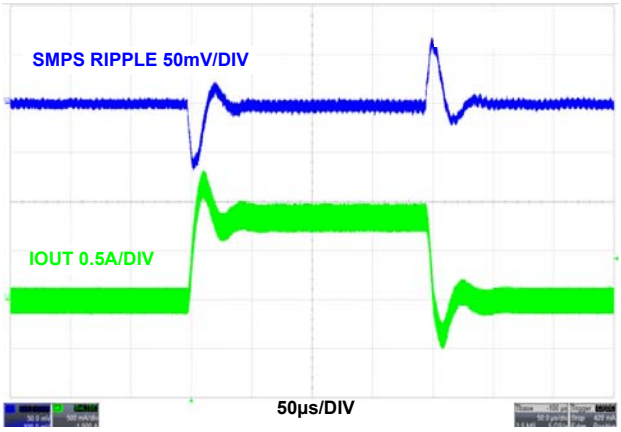


FIGURE 28. LOAD TRANSIENT (PWM), VIN = 3.3V

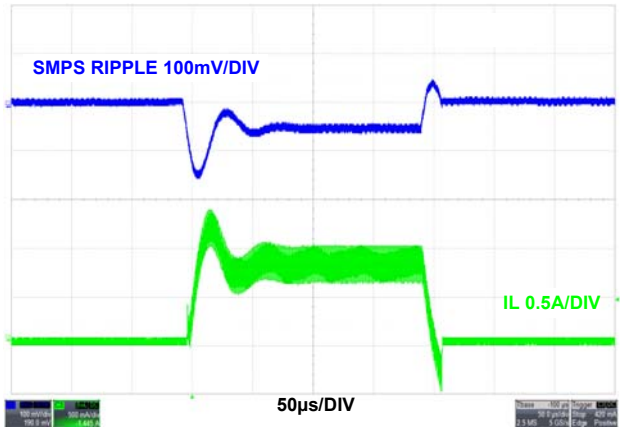


FIGURE 29. LOAD TRANSIENT (PFM), VIN = 3.3V

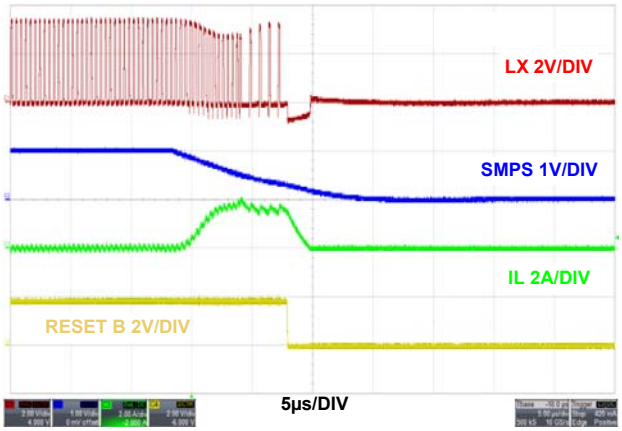


FIGURE 30. OUTPUT SHORT CIRCUIT, VIN = 3.3V

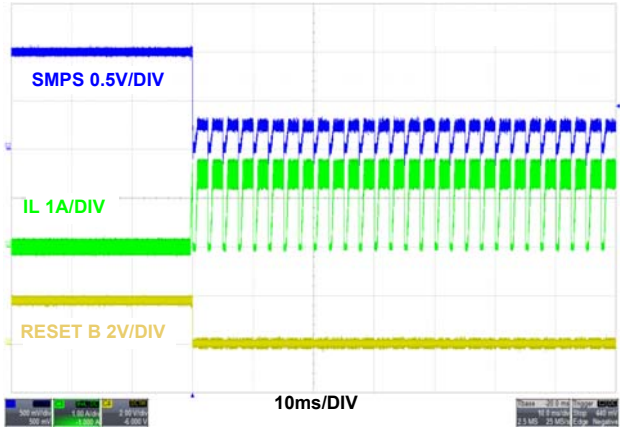


FIGURE 31. OVERCURRENT PROTECTION, VIN = 3.3V

Typical Performance Curves and Waveforms (Continued)

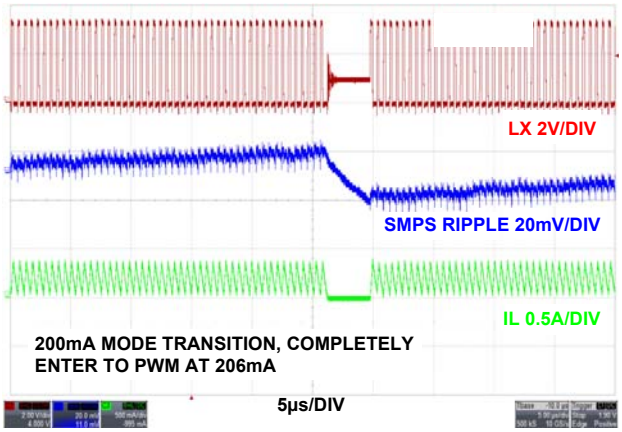


FIGURE 32. PFM TO PWM TRANSITION, VIN = 3.3V

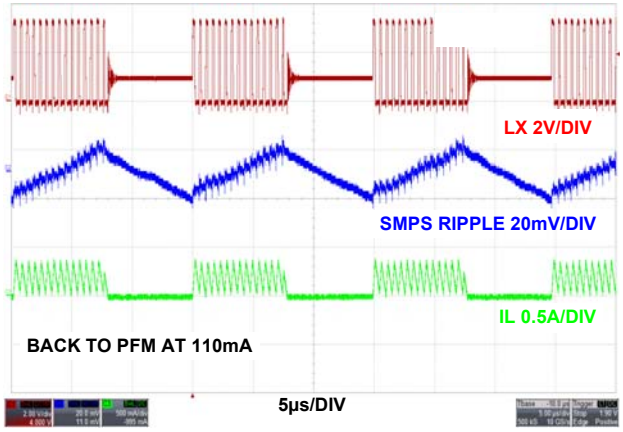


FIGURE 33. PWM TO PFM TRANSITION, VIN = 3.3V

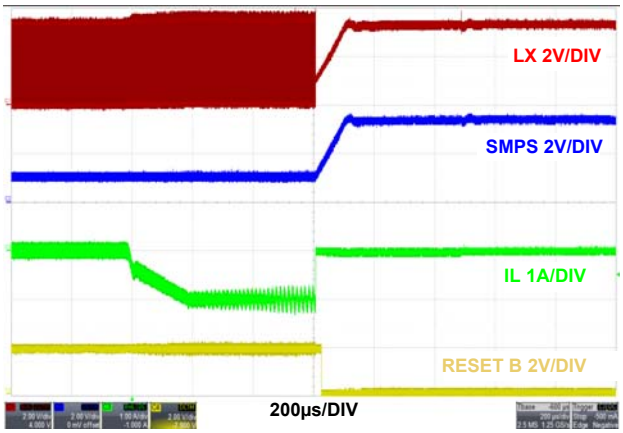


FIGURE 34. OVERVOLTAGE PROTECTION, VIN = 3.3V

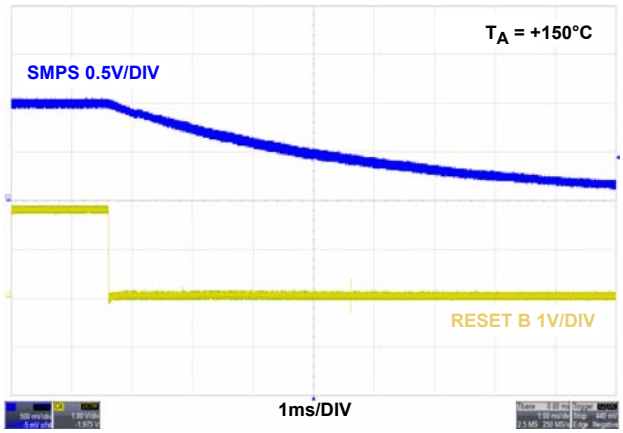


FIGURE 35. OVER-TEMPERATURE PROTECTION, VIN = 3.3V

Input Selector Operation

Input power for the ISL80083 is automatically selected from one of two source pins; VIN_HOST or VIN_REMOTE. The rising slew rate of VIN_HOST or VIN_REMOTE is assumed to be 120V/ms or less. The selector output is VSELECT and should be de-coupled with a 10µF or greater MLCC. In addition to choosing which input will provide power, the selector provides de-bounce, a soft-start to limit inrush current and it protects other circuit blocks of the ISL80083 against overvoltage.

Typically, when either input pin exceeds 2.2V, it is considered “in range” and its switch is activated over approximately 300µs, which limits the surge to the VSELECT capacitor. Once complete, the selector provides typically a 200mΩ path between the selected input and VSELECT. The un-selected input is isolated from VSELECT and <5µA will flow in or out of the input.

In the case that both inputs enter the selectable range at the same moment, the VIN_HOST will be selected. Otherwise, the selector will simply choose the first input that comes in range.

Typically, overvoltage is considered to be greater than 4.5V. If this condition occurs, the selector will disconnect this input within 5µs. In the case that neither input is considered in range, the selector will isolate both inputs from VSELECT and the ISL80083 will remain in an un-powered state until an input comes in range.

SMPS Introduction

The SMPS converter on ISL80083 uses the peak-current-mode pulse-width modulation (PWM) control scheme for fast transient response and pulse-by-pulse current limiting. The converter is able to supply up to 800mA load current. The default output voltage is 1V upon start-up and can be programmed via the I^2C interface in the range of 0.625V to 2.225V at 25mV/step with a programmable slew rate using the register SMPS_OUT. When OSC_EN is pulled low, the I^2C register 03H switches over. The default output is still 1V and will operate in PFM. Optionally, the SMPS can be programmed to be actively discharged via an on-chip bleeding resistor (typical 115Ω) when the converter is disabled.

Soft-Start

Upon VSELECT engaged, the output is defaulted to 1V with a rise time of about 1ms to reduce the in-rush. Then 1ms of delay later, the LDO will rise to 1.8V in 20ms. See Figure 36, start-up sequence for more details.

$\overline{\text{RESET}}$

$\overline{\text{RESET}}$ is the totem pole window comparator output that continuously monitors the buck regulator output voltage via the FB pin. $\overline{\text{RESET}}$ is actively held low when disabled and during the buck regulator soft-start period. $\overline{\text{RESET}}$ goes high after 1ms or 8.4ms delay as long as the output voltages of the switcher and LDO are above 95% of the nominal regulation voltage. The delay time is controlled via the I^2C interface. The default delay time is 1ms. When V_{OUT} drops 10% below the nominal regulation voltage, the ISL80083 pulls $\overline{\text{RESET}}$ low. Any fault condition forces $\overline{\text{RESET}}$ low until the fault condition is cleared by attempts to soft-start.

Overcurrent Protection

The overcurrent protection is realized by monitoring the current through the PFET, Q5 in the block diagram. Upon detection of overcurrent condition, the upper MOSFET will be immediately turned off and will not be turned on again until the next switching cycle. Upon detection of the initial overcurrent condition, the overcurrent fault counter is set to 1. If, on the subsequent cycle, another overcurrent condition is detected, the OC fault counter will be incremented. If there are 17 sequential OC fault detections, the regulator will be shut down under an overcurrent fault condition. An overcurrent fault condition will result in the switcher and LDO attempting to restart in a hiccup mode within the delay of 600µs. At the end of the wait period, the fault counters are reset and soft-start is attempted again.

Likewise, an overcurrent on the LDO output still results in the switcher and LDO attempting to restart in a hiccup mode within the delay of 600µs. The 1V SMPS and 1VAUX will soft-start first, then the LDO will attempt to start 1ms later. The LDO output may not reach regulation unless an overcurrent condition is removed. Once an overcurrent fault is removed, $\overline{\text{RESET}}$ will transition high after the delay time when the LDO voltage reaches regulation.

Negative Current Protection

Similar to the overcurrent, the negative current protection is realized by monitoring the current across the lowside N-FET, as shown in the “Block Diagram” on page 4. When the valley point of the inductor current reaches -1A for 2 consecutive cycles, both P-FET and N-FET are off. The 115Ω parallel to the N-FET will activate discharging the output into regulation. The control will begin to switch when output is within regulation. The regulator will be in PFM for 20µs before switching to PWM if necessary.

Undervoltage Lockout (UVLO)

An undervoltage lockout (UVLO) circuit is provided on the ISL80083. The UVLO circuit block can prevent abnormal operation in the event that the supply voltage is too low to guarantee proper operation. The UVLO on VSELECT is set for a typical 2.49V with 100mV hysteresis. When the input voltage is sensed to be lower than the UVLO threshold, all the related channels are disabled.

Low Dropout Operation

The SMPS converter features low dropout operation, which maximizes the battery life. When the input voltage drops to a level that the converter can no longer operate under switching regulation to maintain the output voltage, the P-Channel MOSFET is completely turned on (100% duty cycle). The dropout voltage under such conditions is the product of the load current and the ON-resistance of the P-Channel MOSFET. Minimum required input voltage VSELECT under such conditions is the sum of the output voltage plus the voltage drop across the inductor and the P-Channel MOSFET switch.

Active Output Voltage Discharge For SMPS

The ISL80083 offers a feature to actively discharge the output voltage of SMPS via an internal bleeding resistor (typically 115Ω) when the channel is disabled. This feature is enabled by default, but the output can be disabled through programming the control bit in SMPS_PARAMETER register.

3.0V Clamp Output

The V3CLAMP is a 3V LDO sourced from VSELECT capable of providing up to 15mA. There is an internal clamp to prevent this output from exceeding 3.3V.

1V Auxiliary Output

The 1V AUX is an auxiliary output sourced from the 1V switcher. The 50mΩ PFET is controlled by using I^2C. There is approximately 5ms delay time from the enable to the output start-up. Soft-start rise time is approximately 20µs to prevent a switcher glitch. Pulling OSC_EN low can also disable the 1VAUX output.

Thermal Shutdown

When the die temperature of ISL80083 reaches +150°C, the regulator is completely shut down and as the temperature drops to +120°C (typical), the device resumes normal operation after initiate its soft-start cycle.

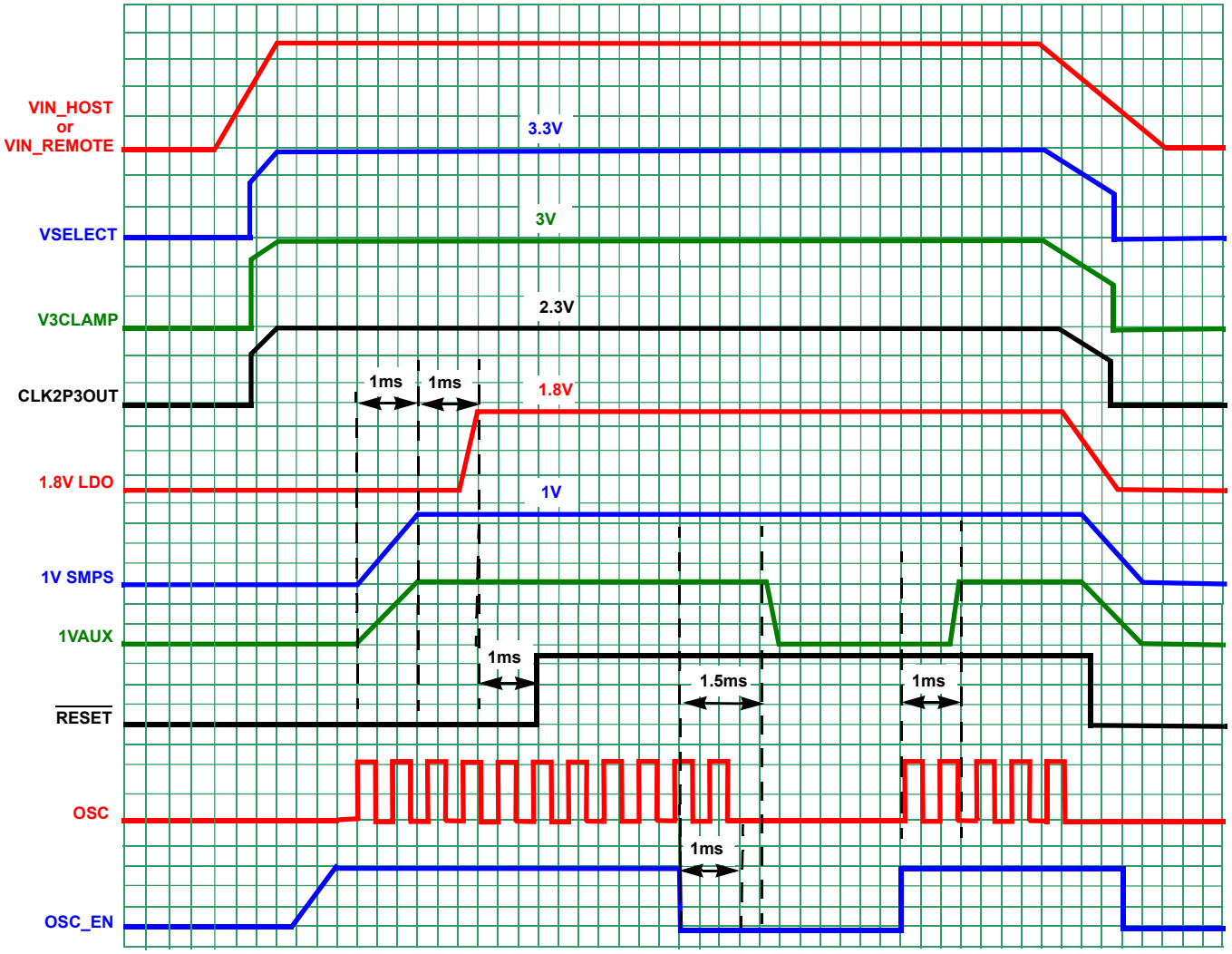


FIGURE 36. START-UP AND SHUTDOWN SEQUENCE

I²C Compatible Interface

The ISL80083 offers an I²C compatible interface, using two pins: SCLK for the serial clock and SDAT for serial data respectively. According to the I²C specifications, there are internal 5kΩ pull-up resistors for the clock and data signals connected to V3PCLAMP.

Signal timing specifications should satisfy the standard I²C bus specification. The maximum bit rate is 400kb/s and more details regarding the I²C specifications can be found from Philips.

I²C Slave Address

The ISL80083 serves as a slave device and the 7-bit default chip address is 1101100, as shown in Figure 37. According to the I²C specifications, here the value of Bit 0 determines the direction of the message ("0" means "write" and "1" means "read").

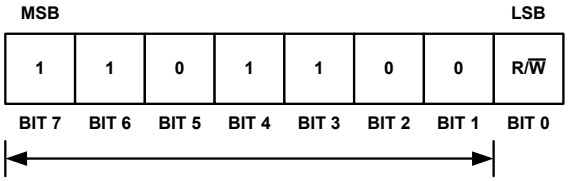


FIGURE 37. I²C SLAVE ADDRESS

I²C Protocol

Figure 38 shows typical I²C-bus transaction protocols.

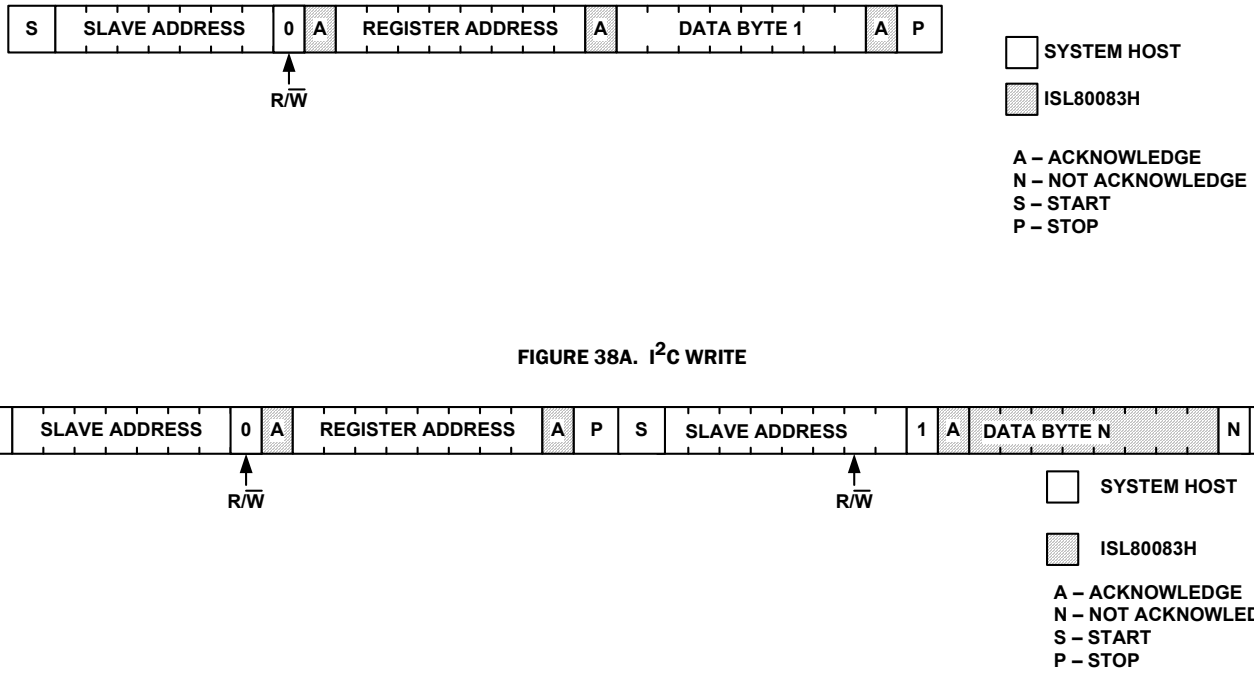


FIGURE 38A. I²C WRITE

FIGURE 38B. I²C READ

FIGURE 38.

I²C Control Registers

All the registers are reset at initial start-up.

CONTROL REGISTER

PARAMETERS, address 0x00h

TABLE 2. REAL TIME OSC ADJUSTMENT REGISTER

BIT	NAME	ACCESS	RESET	DESCRIPTION	
B7	OSC_TRIM	R/W	0	Reg00h Value	Adjustment
B6	OSC_TRIM	R/W	0	0111 1111	+127
B5	OSC_TRIM	R/W	0	0111 1110	+126
B4	OSC_TRIM	R/W	0	|	
B3	OSC_TRIM	R/W	0	|	
B2	OSC_TRIM	R/W	0	0000 0001	+1
B1	OSC_TRIM	R/W	0	0000 0000	0
B0	OSC_TRIM	R/W	0	1111 1111	-1
				|	-2
				|	
				1000 0001	-127
				1000 0000	-128

LDO OUTPUT VOLTAGE CONTROL REGISTER

LDO_OUT, address 0x01h.

TABLE 3. LDO OUTPUT VOLTAGE CONTROL REGISTERS

BIT	NAME	ACCESS	RESET	DESCRIPTION
B7	1VAUX_EN	R/W	1	1VAUX enable selection. 0-enable, 1-disable
B6	RESERVED	R/W	1	
B5	LDO_OUT-5	R/W	0	Refer to Table 4 for LDO output voltage settings
B4	LDO_OUT-4	R/W	1	
B3	LDO_OUT-3	R/W	0	
B2	LDO_OUT-2	R/W	0	
B1	LDO_OUT-1	R/W	1	
B0	LDO_OUT-0	R/W	0	

TABLE 4. LDO OUTPUT VOLTAGE SETTINGS

LDOOUT <5:0>	LDO OUTPUT VOLTAGE (V)	LDOOUT <5:0>	LDO OUTPUT VOLTAGE (V)	LDOOUT <5:0>	LDO OUTPUT VOLTAGE (V)	LDOOUT <5:0>	LDO OUTPUT VOLTAGE (V)
00H	0.9	10H	1.70	20H	2.50	30H	3.30
01H	0.95	11H	1.75	21H	2.55	31H	3.35
02H	1.00	12H	1.80	22H	2.60	32H	3.40
03H	1.05	13H	1.85	23H	2.65	33H	3.45
04H	1.1	14H	1.90	24H	2.70	34H	3.50
05H	1.15	15H	1.95	25H	2.75	35H	3.55
06H	1.20	16H	2.00	26H	2.80	36H	3.60
07H	1.25	17H	2.05	27H	2.85		
08H	1.30	18H	2.10	28H	2.90		
09H	1.35	19H	2.15	29H	2.95		
0AH	1.40	1AH	2.20	2AH	3.00		
0BH	1.45	1BH	2.25	2BH	3.05		
0CH	1.50	1CH	2.30	2CH	3.10		
0DH	1.55	1DH	2.35	2DH	3.15		
0EH	1.60	1EH	2.40	2EH	3.20		

SMPS OUTPUT VOLTAGE CONTROL REGISTER

SMPS_OUT, address 0x02h

Caution: Disable SMPS prior to changing from fixed output voltage to adjustable output voltage or from adjustable output voltage to fixed output voltage using I^2C.

TABLE 5. BUCK CONVERTER OUTPUT VOLTAGE CONTROL REGISTER

BIT	NAME	ACCESS	RESET	DESCRIPTION
B7	OSC_CONTROL	R/W	1	33MHz oscillator control selection. 0-off, 1-on
B6	SMPS_EN	R/W	1	SMPS enable selection. 0-disable, 1-enable
B5	SMPS_pwm-5	R/W	0	Refer to Table 6 for SMPS output voltage setting
B4	SMPS_pwm-4	R/W	0	
B3	SMPS_pwm-3	R/W	1	
B2	SMPS_pwm-2	R/W	1	
B1	SMPS_pwm-1	R/W	1	
B0	SMPS_pwm-0	R/W	1	

TABLE 6. SMPS OUTPUT VOLTAGE SETTING

SMPSOUT <5:0>	SMPS OUTPUT VOLTAGE (V)	SMPSOUT <5:0>	SMPS OUTPUT VOLTAGE (V)	SMPSOUT <5:0>	SMPS OUTPUT VOLTAGE (V)
00H	0.625	1DH	1.375	3BH	2.125
01H	0.650	1EH	1.400	3CH	2.150
02H	0.675	1FH	1.425	3DH	2.175
03H	0.700	20H	1.450	3EH	2.200
04H	0.725	21H	1.475	3FH	2.225
05H	0.750	22H	1.500		
06H	0.775	23H	1.525		
07H	0.800	24H	1.550		
08H	0.825	25H	1.575		
09H	0.850	26H	1.600		
0AH	0.875	27H	1.625		
0BH	0.900	28H	1.650		
0CH	0.925	29H	1.675		
0DH	0.950	2AH	1.700		
0EH	0.975	2BH	1.725		
0FH	1.000	2CH	1.750		
10H	1.025	2DH	1.775		
11H	1.050	2EH	1.800		
12H	1.075	2FH	1.825		
13H	1.100	30H	1.850		
14H	1.125	31H	1.875		
15H	1.150	32H	1.900		
16H	1.175	33H	1.925		
17H	1.200	34H	1.950		
18H	1.225	35H	1.975		
19H	1.250	36H	2.000		
19H	1.275	37H	2.025		
1AH	1.300	38H	2.050		
1BH	1.325	39H	2.075		
1CH	1.350	3AH	2.100		

SMPS OUTPUT VOLTAGE CONTROL REGISTER

SMPS_SLEEP, address 0x03h

Caution: Disable SMPS prior to changing from fixed output voltage to adjustable output voltage or from adjustable output voltage to fixed output voltage using I^2C.

TABLE 7. BUCK CONVERTER OUTPUT VOLTAGE CONTROL REGISTER

BIT	NAME	ACCESS	RESET	DESCRIPTION
B7	$\overline{\text{RESET}}$_DY	R/W	0	RESET Delay Time, 00 to 1.07ms 01 to 8.4ms
B6	SMPSSR	R/W	0	SMPS Slew Rate Setting, 0 to 0.19mV/µs 1 to 0.38mV/µs
B5	SMPS_pfm-5	R/W	0	Refer to Table 8 for SMPS output voltage setting.
B4	SMPS_pfm-4	R/W	0	
B3	SMPS_pfm-3	R/W	1	
B2	SMPS_pfm-2	R/W	1	
B1	SMPS_pfm-1	R/W	1	
B0	SMPS_pfm-0	R/W	1	

TABLE 8. SMPS OUTPUT VOLTAGE SETTING

SMPSOUT <5:0>	SMPS OUTPUT VOLTAGE (V)	SMPSOUT <5:0>	SMPS OUTPUT VOLTAGE (V)	SMPSOUT <5:0>	SMPS OUTPUT VOLTAGE (V)
00H	0.625	1CH	1.350	39H	2.075
01H	0.650	1DH	1.375	3AH	2.100
02H	0.675	1EH	1.400	3BH	2.125
03H	0.700	1FH	1.425	3CH	2.150
04H	0.725	20H	1.450	3DH	2.175
05H	0.750	21H	1.475	3EH	2.200
06H	0.775	22H	1.500	3FH	2.225
07H	0.800	23H	1.525		
08H	0.825	24H	1.550		
09H	0.850	25H	1.575		
0AH	0.875	26H	1.600		
0BH	0.900	27H	1.625		
0CH	0.925	28H	1.650		
0DH	0.950	29H	1.675		
0EH	0.975	2AH	1.700		
0FH	1.000	2BH	1.725		
10H	1.025	2CH	1.750		
11H	1.050	2DH	1.775		
12H	1.075	2EH	1.800		
13H	1.100	2FH	1.825		
14H	1.125	30H	1.850		
15H	1.150	31H	1.875		
16H	1.175	32H	1.900		
17H	1.200	33H	1.925		
18H	1.225	34H	1.950		
19H	1.250	35H	1.975		
19H	1.275	36H	2.000		
1AH	1.300	37H	2.025		
1BH	1.325	38H	2.050		

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
May 15, 2013	FN7886.1	Initial Release

About Intersil

Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the largest markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil, visit our website at www.intersil.com.

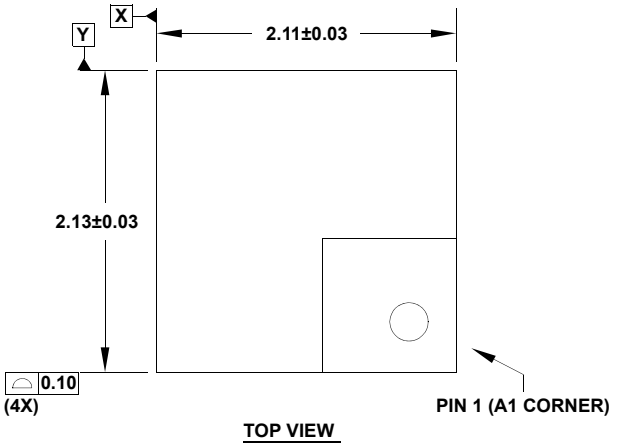
For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com. You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/en/support/ask-an-expert.html. Reliability reports are also available from our website at http://www.intersil.com/en/support/qualandreliability.html#reliability

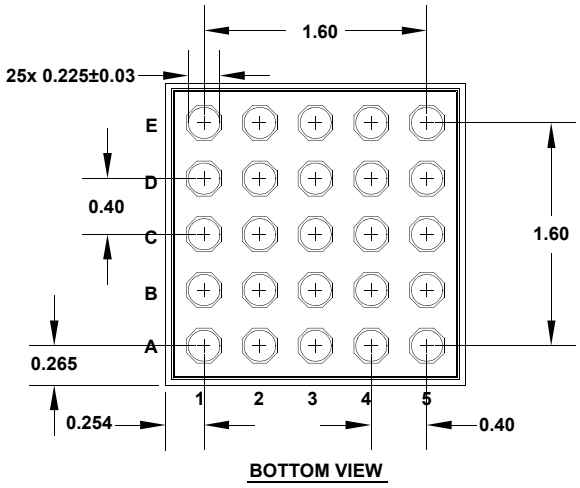
Package Outline Drawing

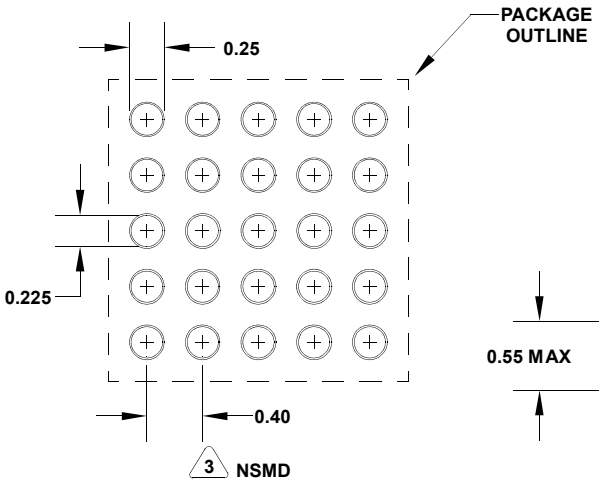
W5x5.25B

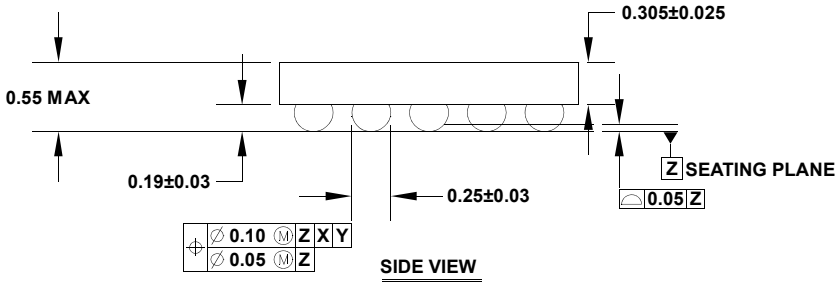
5X5 ARRAY 25 BALL WITH 0.40 PITCH WAFER LEVEL CHIP SCALE PACKAGE (WLCSP)

Rev 2, 12/11









NOTES:

1. **All dimensions are in millimeters.**
2. **Dimension and tolerance per ASMEY 14.5M-1994, and JESD 95-1 SPP-010.**
3. **NSMD refers to Non-Solder Mask Defined pad design per Intersil Tech Brief TB451 located at: http://www.intersil.com/data/tb/tb451.pdf.**