ISL8002B

Compact Synchronous Buck Regulator

FN8690
Rev 3.00
October 28, 2016

The ISL8002B is a highly efficient, monolithic, synchronous step-down DC/DC converter that can deliver up to 2A of continuous output current from a 2.7V to 5.5V input supply. It uses peak current mode control architecture to allow very low duty cycle operation. ISL8002B operates at a 2MHz switching frequency, thereby providing superior transient response and allowing for the use of a small inductor. ISL8002B also has excellent stability.

The ISL8002B integrates very low $r_{DS(ON)}$ MOSFETs in order to maximize efficiency. In addition, since the high-side MOSFET is a PMOS, the need for a boot capacitor is eliminated, thereby reducing external component count.

The device can be configured for either PFM (discontinuous conduction) or PWM (continuous conduction) operation at light load. PFM provides high efficiency by reducing switching losses at light loads and PWM for fast transient response, which helps reduce the output noise and RF interference.

The device is offered in a space saving 8 Ld 2mmx2mm TDFN Pb-free package with exposed pad for improved thermal performance. The complete converter occupies less than $64mm^2$ area.

Features

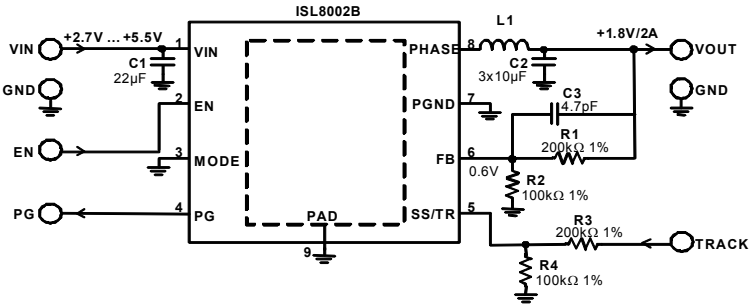
- V_{IN} range 2.7V to 5.5V
- I_{OUT} maximum is 2A
- External soft-start programmable
- Output tracking and sequencing
- Switching frequency is 2MHz
- Selectable PFM or PWM operation option
- Overcurrent and short-circuit protection
- Over-temperature/thermal protection
- V_{IN} undervoltage lockout and V_{OUT} overvoltage protection
- Up to 95% peak efficiency

Applications

- General purpose POL
- Industrial, instrumentation and medical equipment
- FPGAs
- Telecom and networking equipment
- Game console

Related Literature

- For a full list of related documents, visit our website
  - ISL8002B product page



$$R_1 = R_2\left(\frac{V_O}{VFB} - 1\right) \quad \text{(EQ. 1)}$$

FIGURE 1. TYPICAL APPLICATION CIRCUIT CONFIGURATION (INTERNAL COMPENSATION OPTION)

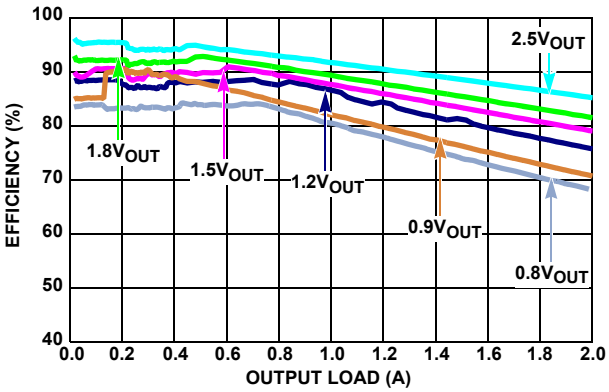


FIGURE 2. EFFICIENCY vs LOAD (f_{SW} = 2MHz, V_{IN} = 3.3V), MODE = PFM, T_A = +25°C

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TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

PART NUMBER	INTERNAL/ EXTERNAL COMP	TRACKING/EXTERNAL SOFT- START	OUTPUT CURRENT (A)	PG RISING/FALLING DELAY TIME	NOMINAL SWITCHING FREQUENCY (MHz)
ISL8002/A	Yes	No	2	1ms/15µs	1/2
ISL80019/A	Yes	No	1.5	1ms/15µs	1/2
ISL8002B	No	Yes	2	0.1ms/15µs	2

TABLE 2. RECOMMENDED COMPONENT VALUE SELECTION TABLE

V_{OUT} (V)	C_1 (µF)	C_2 MINIMUM (µF)	C_3 (pF)	L_1 (µH)	R_1, R_3 (Note 1) (kΩ)	R_2, R_4 (Note 1) (kΩ)
0.8	22	3 X10	4.7	0.82	33	100
1.2	22	3 X10	4.7	1.0	100	100
1.5	22	3 X10	4.7	1.0	150	100
1.8	22	3 X10	4.7	1.2	200	100
2.5	22	3 X10	4.7	1.8	316	100
3.3	22	3 X10	4.7	2.2	450	100

NOTE:

1. Populate R_3 and R_4 if Tracking feature is used. Ratio between R_1/R_2 should equal R_3/R_4. Otherwise connect SS/TR to V_{IN} for internal soft-start.

Ordering Information

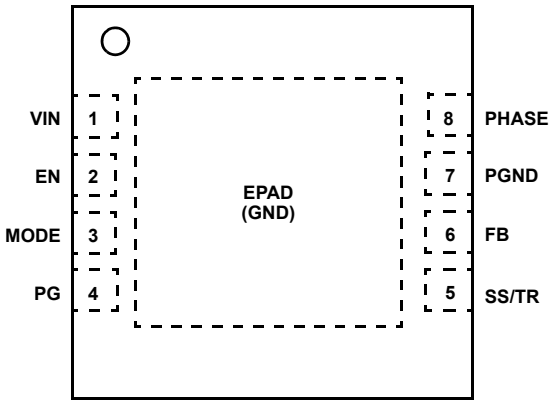
PART NUMBER (Notes 2, 3, 4)	PART MARKING	TAPE AND REEL (UNITS)	TECHNICAL SPECIFICATIONS	TEMPERATURE RANGE (°C)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ISL8002BIRZ-T	02B	1000	2A, 2MHz	-40 to +85	8 Ld TDFN	L8.2x2C
ISL8002BIRZ-T7A	02B	250	2A, 2MHz	-40 to +85	8 Ld TDFN	L8.2x2C
ISL8002BFRZ-T	2BF	1000	2A, 2MHz	-40 to +125	8 Ld TDFN	L8.2x2C
ISL8002BFRZ-T7A	2BF	250	2A, 2MHz	-40 to +125	8 Ld TDFN	L8.2x2C
ISL8002BDEMO1Z	Demonstration Board					

NOTES:

2. Please refer to TB347 for details on reel specifications.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), please see device information page for ISL8002B. For more information on MSL please see techbrief TB363.

Pin Configuration

ISL8002B
(8 LD 2x2 TDFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	SYMBOL	PIN DESCRIPTION
1	VIN	The input supply for the power stage of the PWM regulator and the source for the internal linear regulator that provides bias for the IC. Place a minimum of 10µF ceramic capacitance from VIN to GND and as close as possible to the IC for decoupling.
2	EN	Device enable input. When the voltage on this pin rises above 1.4V, the device is enabled. The device is disabled when the pin is pulled to ground. When the device is disabled, a 100Ω resistor discharges the output through the PHASE pin. See Figure 3, "FUNCTIONAL BLOCK DIAGRAM" on page 5 for details.
3	MODE	Mode selection pin. Connect to logic high or input voltage VIN for PWM mode. Connect to logic low or ground for PFM mode. There is an internal 1MΩ pull-down resistor to prevent an undefined logic state in case the MODE pin is left floating, however, it is not recommended to leave this pin floating.
4	PG	Power-good output is pulled to ground during the soft-start interval and also when the output voltage is below regulation limits. There is an internal 5MΩ internal pull-up resistor on this pin.
5	SS/TR	Soft-start pins for regulator. If SS/TR pin is tied to VIN, an internal soft-start of 1ms will be used. A resistor divider from VIN to SS/TR and a capacitor from the SS/TR pin to ground determines the output ramp rate. Adding a resistive divider across SS/TR can be used for output tracking. See "Output Tracking and Sequencing" on page 18 for soft-start and output tracking/sequencing details. Maximum C_{SS} value is 1µF.
6	FB	Feedback pin for the regulator. FB is the negative input to the voltage loop error amplifier. The output voltage is set by an external resistor divider connected to FB. In addition, the power-good PWM regulator's power-good and undervoltage protection circuits use FB to monitor the output voltage.
7	PGND	Power and analog ground connections. Connect directly to the board GND plane.
8	PHASE	Power stage switching node for output voltage regulation. Connect to the output inductor. This pin is discharged by a 100Ω resistor when the device is disabled. See Figure 3, "FUNCTIONAL BLOCK DIAGRAM" on page 5 for details.
-	EPAD	The exposed pad must be connected to the PGND pin for proper electrical performance. Place as many vias as possible under the pad connecting to the PGND plane for optimal thermal performance.

Functional Block Diagram

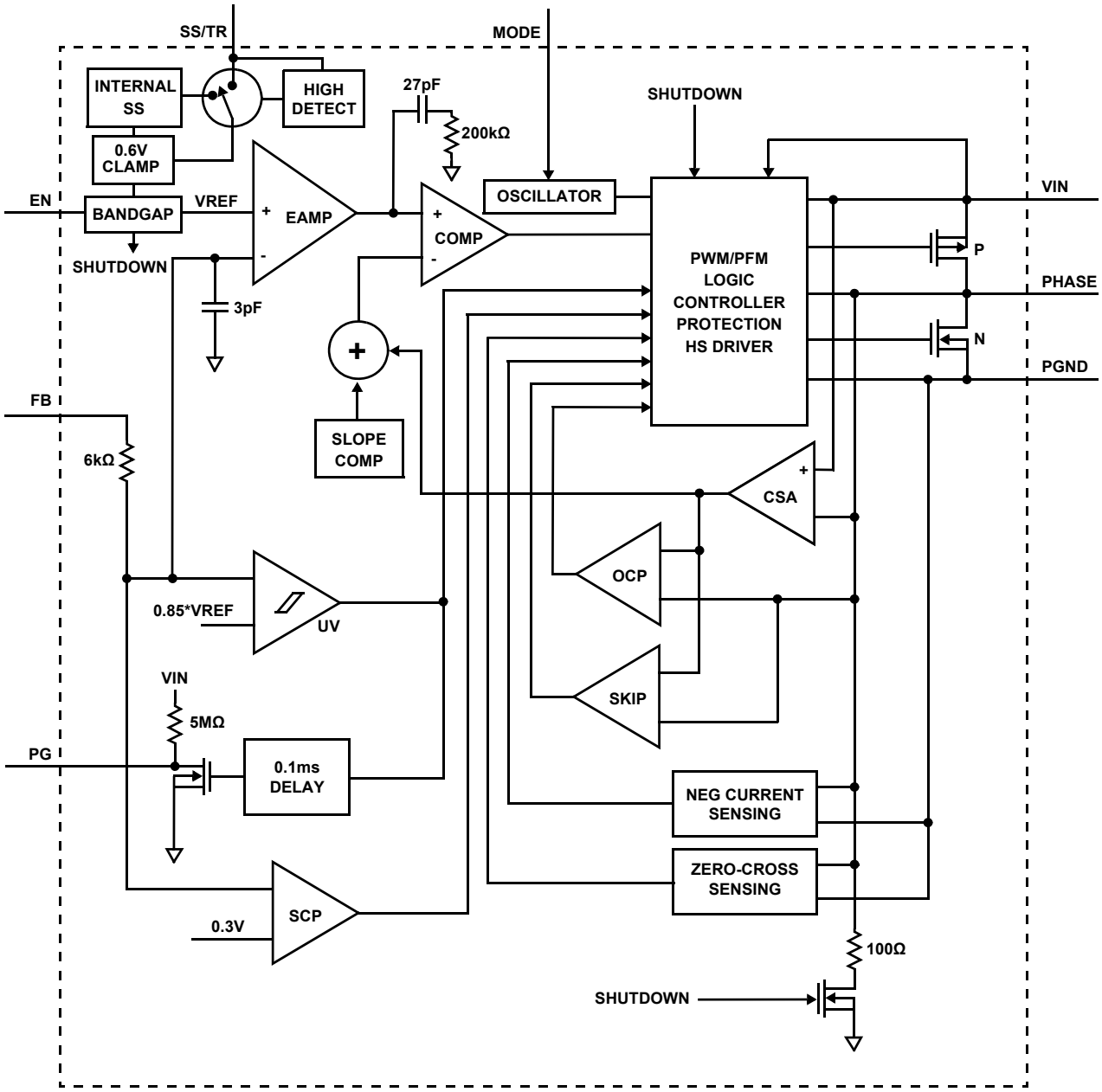


FIGURE 3. FUNCTIONAL BLOCK DIAGRAM

Absolute Maximum Ratings

VIN . . . . . -0.3V to 6V (DC) or 7V (20ms)
PHASE . . . . . -1.5V (100ns)/-0.3V (DC) to 6V (DC) or 7V (20ms)
EN, COMP, PG, MODE . . . . . -0.3V to VIN + 0.3V
FB . . . . . -0.3V to 2.7V
ESD Rating
Human Body Model (Tested per JESD22-JS-001) 4kV
Charged Device Model (Tested per JESD22-C101D) 2kV
Latch-Up (Tested per JESD78D, Class 2, Level A) . . . . ±100mA at +125°C

Thermal Information

Thermal Resistance (Typical, Notes 5, 6)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
2x2 TDFN Package	71	7

Junction Temperature Range . . . . . -55°C to +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493
Junction Temperature Range at 0A . . . . . +150°C

Recommended Operating Conditions

V_{IN} Supply Voltage Range . . . . . 2.7V to 5.5V
Load Current Range . . . . . 0A to 2A
Junction Temperature Range . . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379 for details.
6. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

T_J = -40°C to +125°C, V_{IN} = 2.7V to 5.5V, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range,-40°C to +85°C (IRZ) or -40°C to +125°C (FRZ).**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
INPUT SUPPLY						
V_{IN} Undervoltage Lockout Threshold	V_{UVLO}	Rising, no load		2.5	**2.7**	V
		Falling, no load	**2.2**	2.4		V
Quiescent Supply Current	I_{VIN}	MODE = PFM (GND), no load at the output		35	**60**	µA
		MODE = PWM (V_{IN}), no load at the output		8	**15**	mA
Shutdown Supply Current	I_{SD}	MODE = PFM (GND), V_{IN} = 5.5V, EN = low		20	**30**	µA
OUTPUT REGULATION						
Feedback Voltage	V_{FB}	T_J = -40°C to +85°C	**0.595**	0.600	**0.605**	V
		T_J = -40°C to +125°C	**0.589**	0.6	**0.605**	V
		SS/TR = 100mV	**0.08**	0.100	**0.12**	V
		SS/TR = 500mV	**0.490**	0.500	**0.510**	V
VFB Bias Current	I_{VFB}	V_{FB} = 2.7V. T_J = -40°C to +125°C	**-120**	50	**350**	nA
Line Regulation		V_{IN} = V_O + 0.5V to 5.5V, nominal = 3.6V T_J = -40°C to +125°C	**-0.32**	-0.05	**0.28**	%/V
Load Regulation		(Note 8)		< -0.2		%/A
Soft-Start Ramp Time Cycle		SS/TR = V_{IN}		1		ms
PROTECTIONS						
Positive Peak Current Limit	IPLIMIT		**2.7**	3.2	**3.7**	A
Peak Skip Limit	I_{SKIP}	V_{IN} = 3.6V, V_{OUT} = 1.8V (see "Applications Information" on page 19 for more detail)		450		mA
Zero Cross Threshold			**-170**	-70	**30**	mA
Negative Current Limit	INLIMIT		**-2.37**	-1.8	**-1**	A
Thermal Shutdown		Temperature rising		150		°C
Thermal Shutdown Hysteresis		Temperature falling		25		°C

Electrical Specifications

T_J = -40°C to +125°C, V_{IN} = 2.7V to 5.5V, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range,-40°C to +85°C (IRZ) or -40°C to +125°C (FRZ). (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
COMPENSATION						
Error Amplifier Transconductance				80		µA/V
Transresistance	RT		**0.24**	0.3	**0.40**	Ω
PHASE						
P-Channel MOSFET ON-Resistance		V_{IN} = 5V, I_O = 200mA		117		mΩ
N-Channel MOSFET ON-Resistance		V_{IN} = 5V, I_O = 200mA		86		mΩ
OSCILLATOR						
Nominal Switching Frequency	f_{SW}		**1700**	2000	**2300**	kHz
PG						
Output Low Voltage		1mA sinking current			**0.3**	V
Delay Time (Rising Edge)				0.1	**0.2**	ms
PGOOD Delay Time (Falling Edge)				5		µs
PG Pin Leakage Current		PG = VIN		0.01	**0.1**	µA
UVP PG Rising Threshold			**80**	85	**90**	%
UVP PG Hysteresis				5		%
EN AND MODE LOGIC						
EN Logic Input Low					**1**	V
EN Logic Input High			**1.4**			V
MODE Logic Input Low					**0.4**	V
MODE Logic Input High			**1.4**			V
Logic Input Leakage Current	I_{MODE}	Pulled up to 5.5V		5.5	**8**	µA

NOTES:

7. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
8. Not tested in production. Characterized using evaluation board. Refer to Figures 10 through 12 load regulation diagrams. T_A +105°C represents near worst case operating point.

Typical Performance Curves

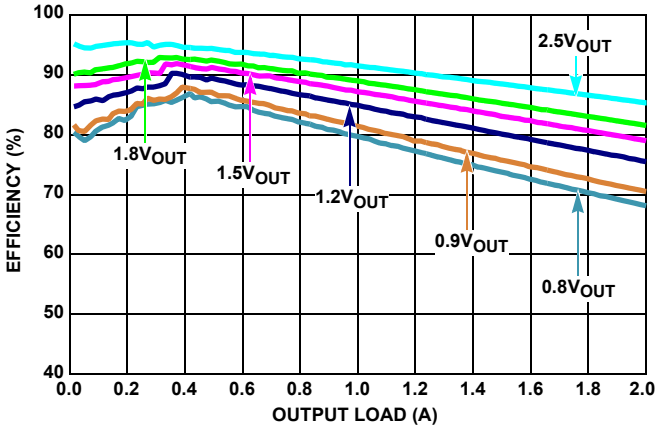


FIGURE 4. EFFICIENCY vs LOAD f_{SW} = 2MHz, V_{IN} = 3.3V, MODE = PFM, T_A = +25°C

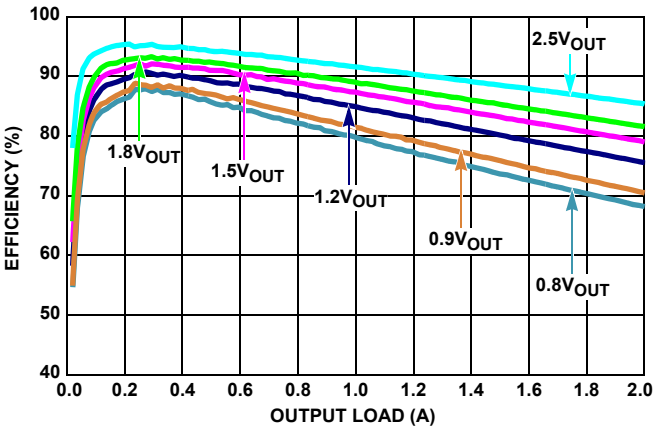


FIGURE 5. EFFICIENCY vs LOAD f_{SW} = 2MHz, V_{IN} = 3.3V, MODE = PWM, T_A = +25°C

Typical Performance Curves (Continued)

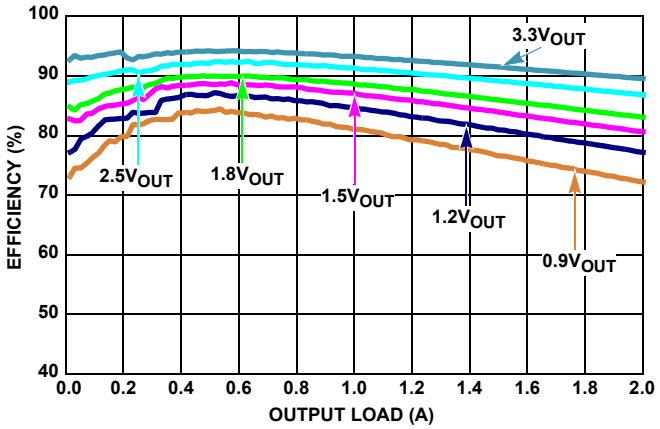


FIGURE 6. EFFICIENCY vs LOAD f_{SW} = 2MHz, V_{IN} = 5V, MODE = PFM, T_A = +25°C

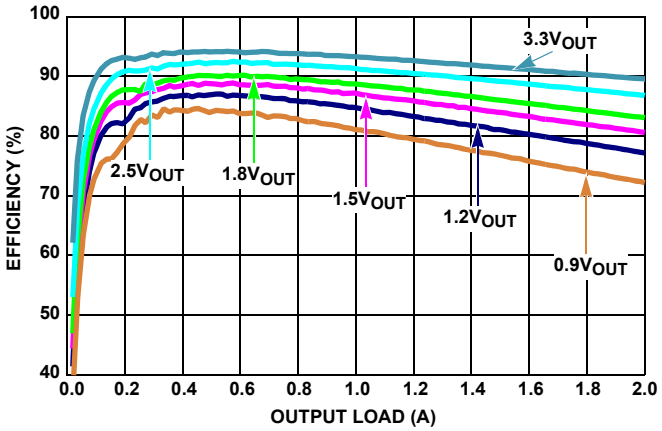


FIGURE 7. EFFICIENCY vs LOAD f_{SW} = 2MHz, V_{IN} = 5V, MODE = PWM, T_A = +25°C

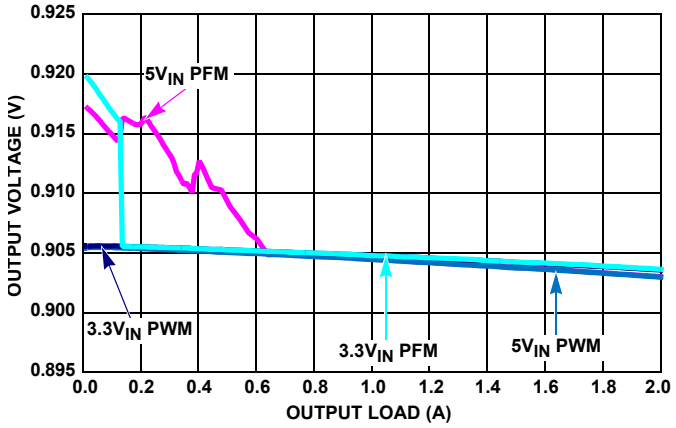


FIGURE 8. V_{OUT} REGULATION vs LOAD, f_{SW} = 2MHz, V_{OUT} = 0.9V, T_A = +25°C

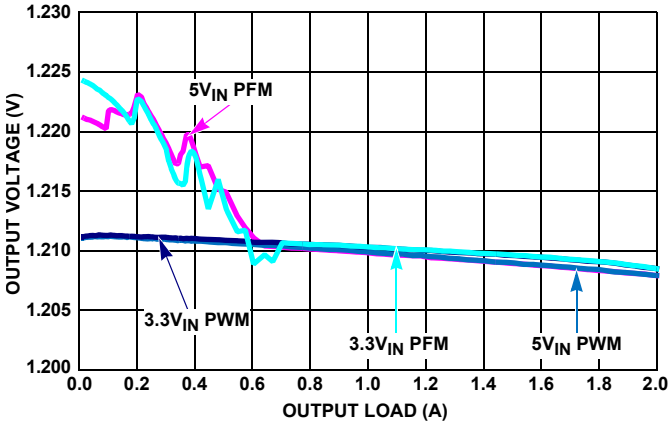


FIGURE 9. V_{OUT} REGULATION vs LOAD, f_{SW} = 2MHz, V_{OUT} = 1.2V, T_A = +25°C

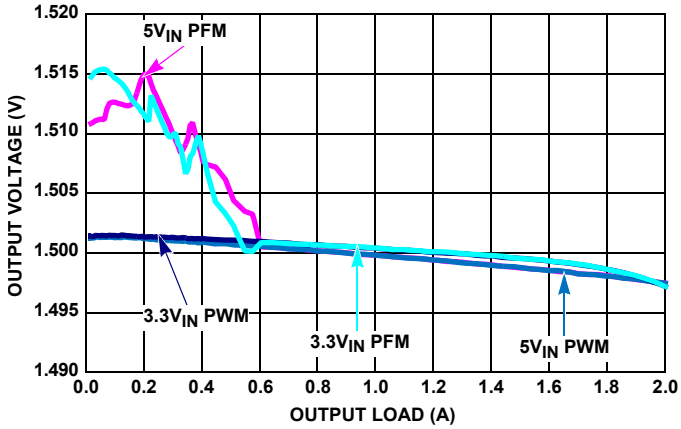


FIGURE 10. V_{OUT} REGULATION vs LOAD, f_{SW} = 2MHz, V_{OUT} = 1.5V, T_A = +25°C

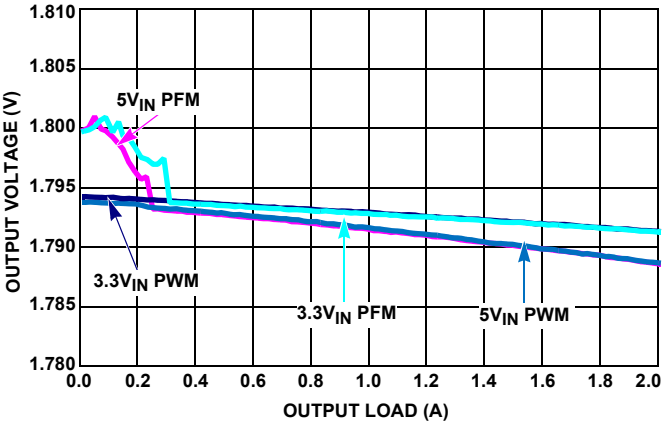


FIGURE 11. V_{OUT} REGULATION vs LOAD, f_{SW} = 2MHz, V_{OUT} = 1.8V, T_A = +25°C

Typical Performance Curves (Continued)

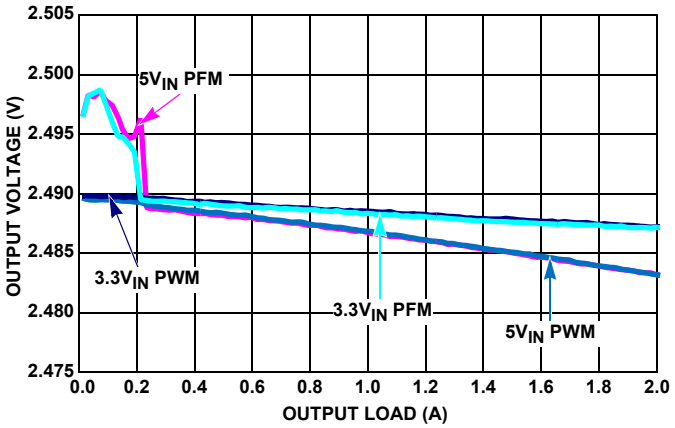


FIGURE 12. V_{OUT} REGULATION vs LOAD, f_{SW} = 2MHz, V_{OUT} = 2.5V, T_A = +25°C

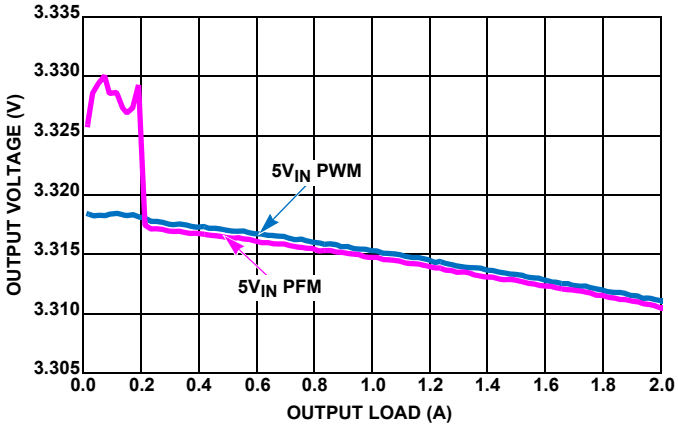


FIGURE 13. V_{OUT} REGULATION vs LOAD, f_{SW} = 2MHz, V_{OUT} = 3.3V, T_A = +25°C

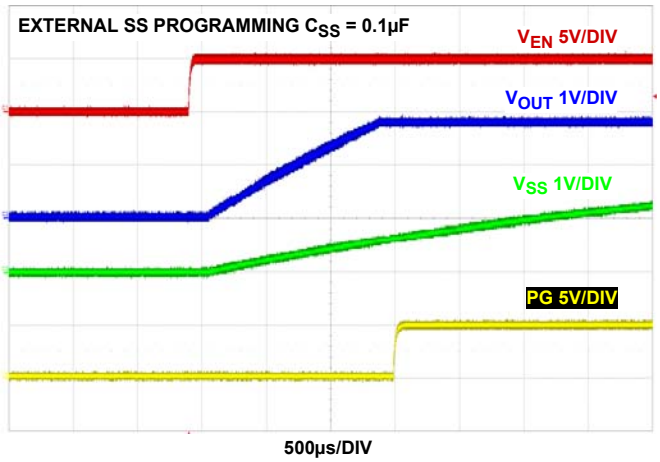


FIGURE 14. START-UP AT NO LOAD f_{SW} = 2MHz, V_{IN} = 5V, MODE = PWM, T_A = +25°C

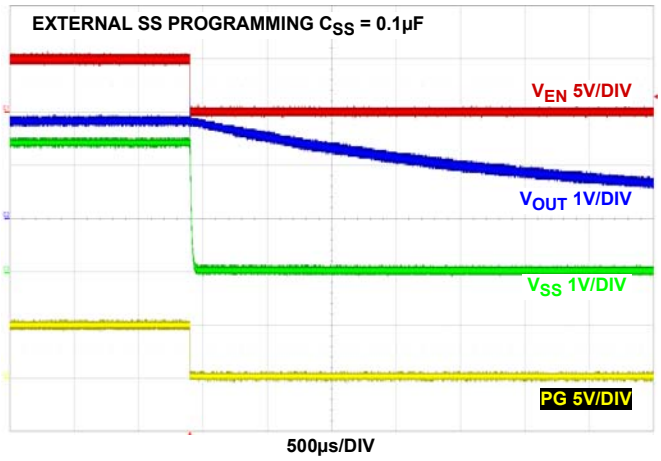


FIGURE 15. SHUTDOWN AT NO LOAD f_{SW} = 2MHz, V_{IN} = 5V, MODE = PWM, T_A = +25°C

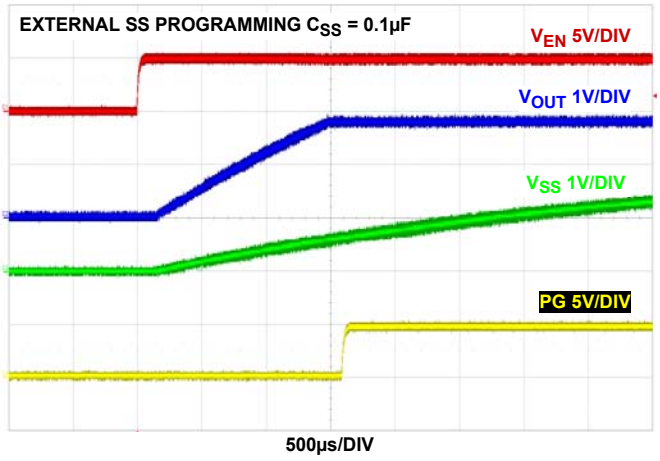


FIGURE 16. START-UP AT 2A LOAD f_{SW} = 2MHz, V_{IN} = 5V, MODE = PWM, T_A = +25°C

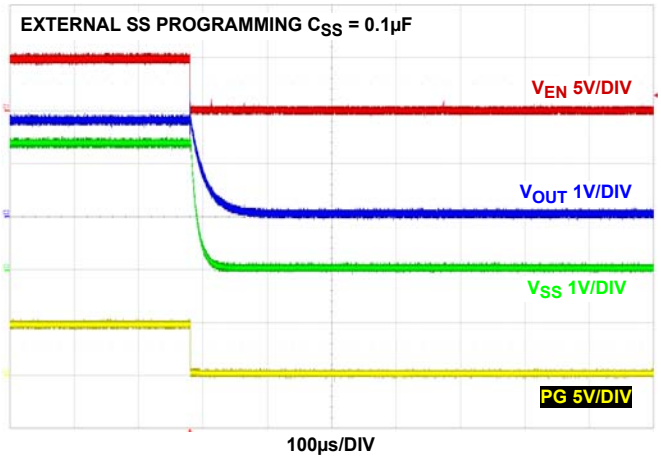


FIGURE 17. SHUTDOWN AT 2A LOAD f_{SW} = 2MHz, V_{IN} = 5V, MODE = PWM, T_A = +25°C

Typical Performance Curves (Continued)

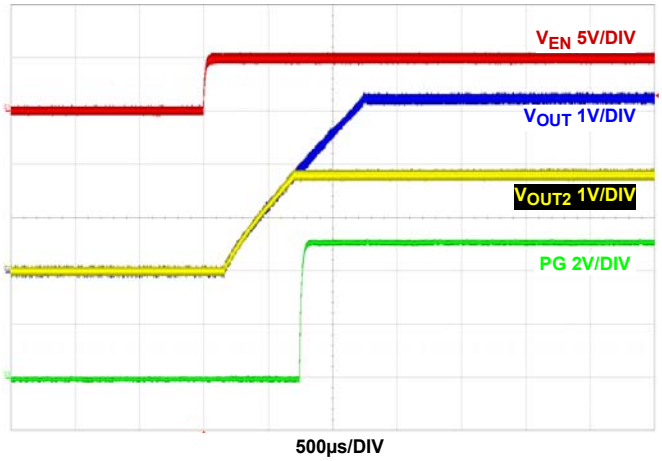


FIGURE 18. COINCIDENTAL VOLTAGE TRACKING START-UP AT NO LOAD, V_{IN} = 5V, MODE = PWM, T_A = +25°C

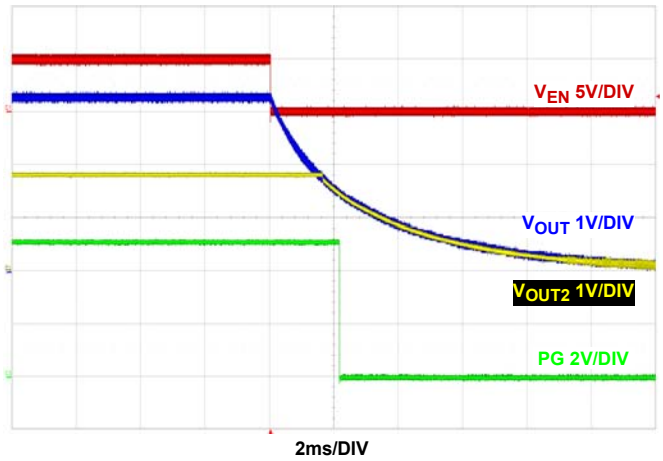


FIGURE 19. COINCIDENTAL VOLTAGE TRACKING SHUTDOWN AT NO LOAD, V_{IN} = 5V, MODE = PWM, T_A = +25°C

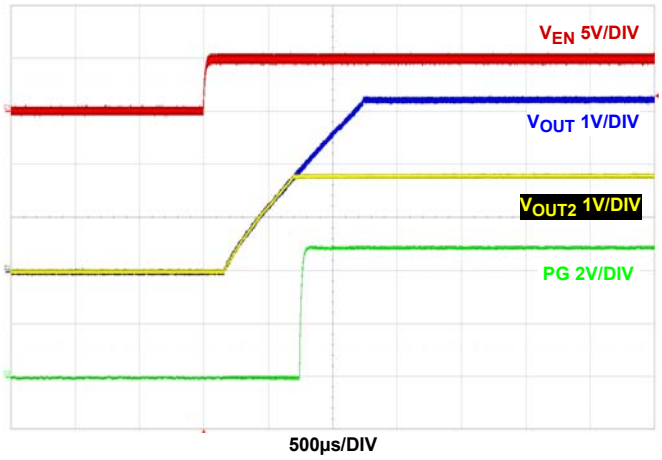


FIGURE 20. COINCIDENTAL VOLTAGE TRACKING START-UP AT FULL LOAD, V_{IN} = 5V, MODE = PWM, T_A = +25°C

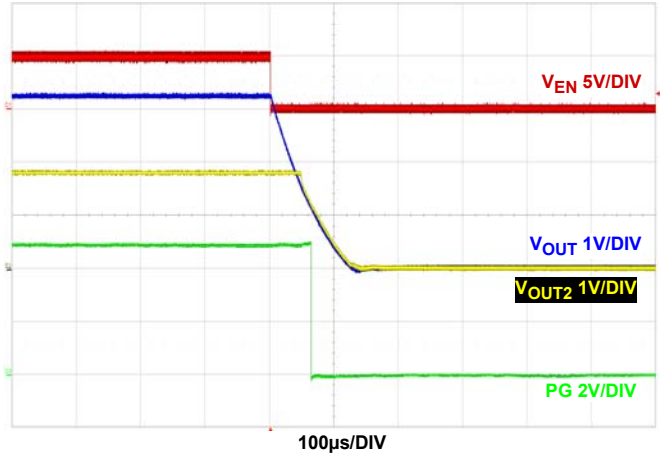


FIGURE 21. COINCIDENTAL VOLTAGE TRACKING SHUTDOWN AT FULL LOAD, V_{IN} = 5V, MODE = PWM, T_A = +25°C

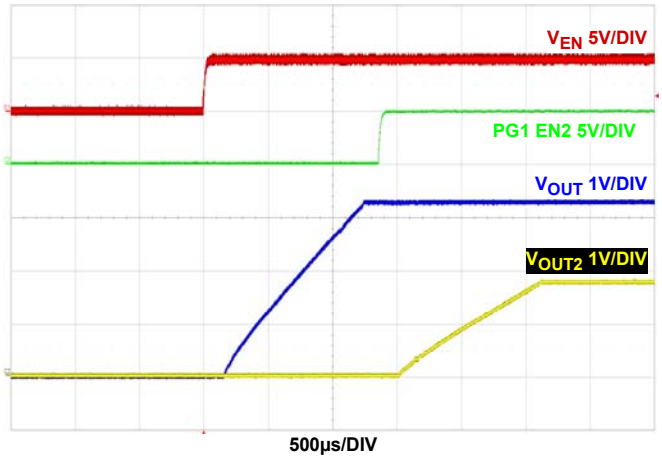


FIGURE 22. SEQUENTIAL START-UP USING EN AND PG AT NO LOAD, V_{IN} = 5V, MODE = PWM, T_A = +25°C

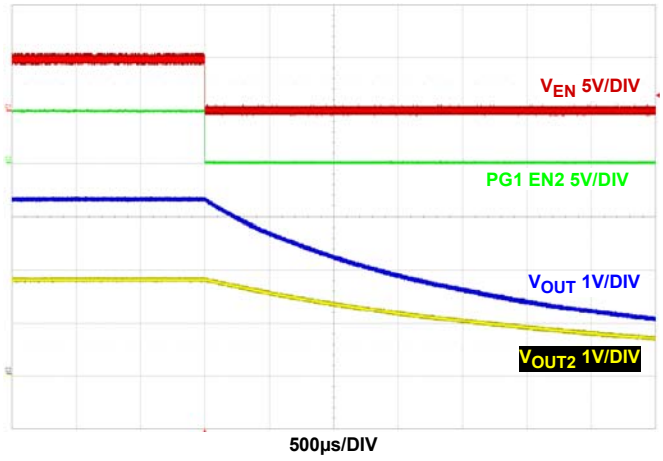


FIGURE 23. SEQUENTIAL SHUTDOWN USING EN AND PG AT NO LOAD, V_{IN} = 5V, MODE = PWM, T_A = +25°C

Typical Performance Curves (Continued)

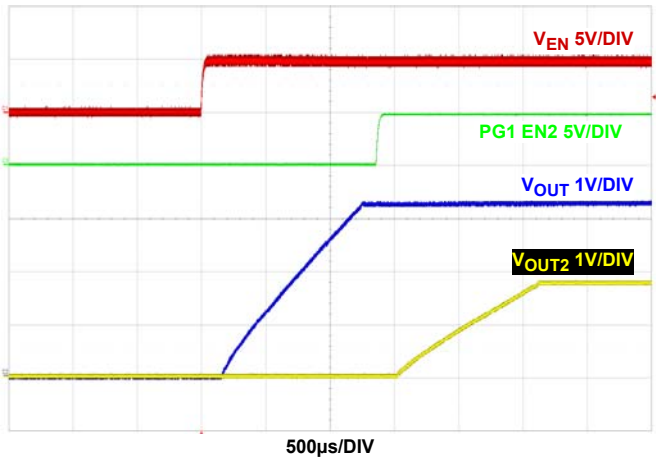


FIGURE 24. SEQUENTIAL START-UP USING EN AND PG AT FULL LOAD, V_{IN} = 5V, MODE = PWM, T_A = +25°C

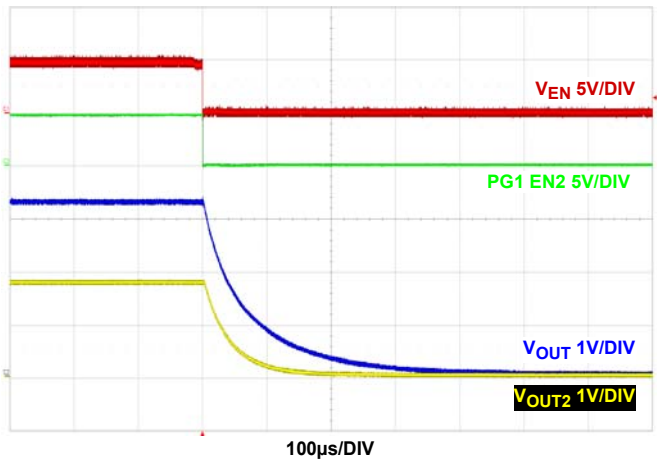


FIGURE 25. SEQUENTIAL SHUTDOWN USING EN AND PG AT FULL LOAD, V_{IN} = 5V, MODE = PWM, T_A = +25°C

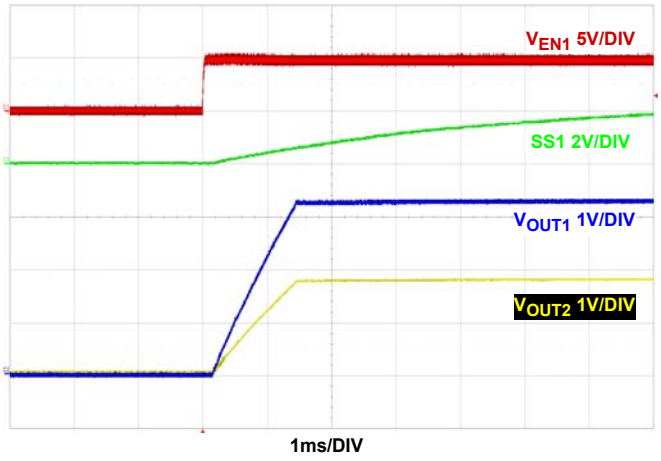


FIGURE 26. RATIOMETRIC START-UP WITH V_{OUT1} LEADING V_{OUT2} AT NO LOAD, V_{IN} = 5V, MODE = PWM, T_A = +25°C

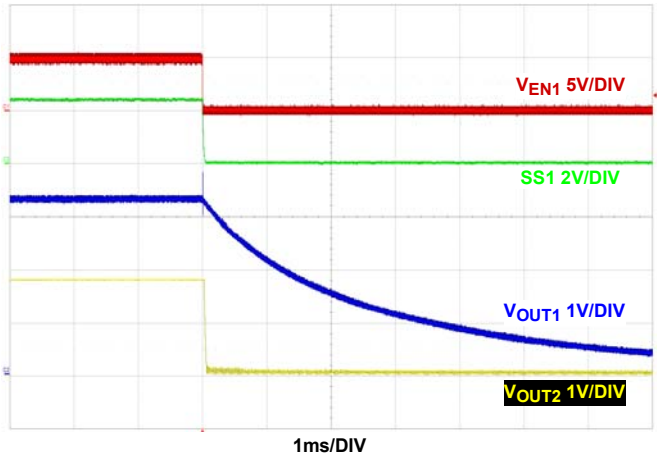


FIGURE 27. RATIOMETRIC SHUTDOWN WITH V_{OUT1} LEADING V_{OUT2} AT NO LOAD, V_{IN} = 5V, MODE = PWM, T_A = +25°C

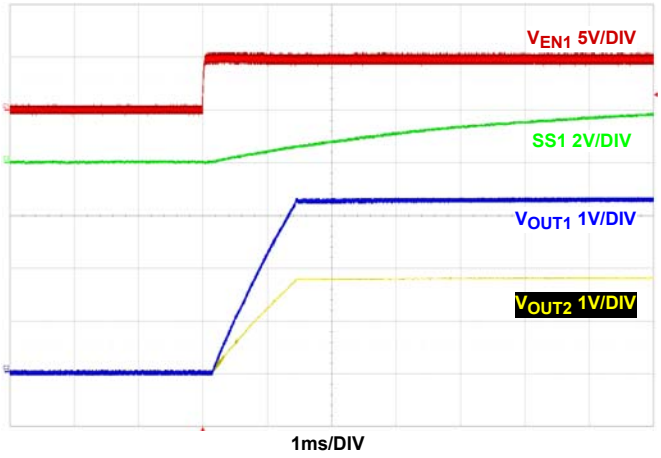


FIGURE 28. RATIOMETRIC START-UP WITH V_{OUT1} LEADING V_{OUT2} AT FULL LOAD, V_{IN} = 5V, MODE = PWM, T_A = +25°C

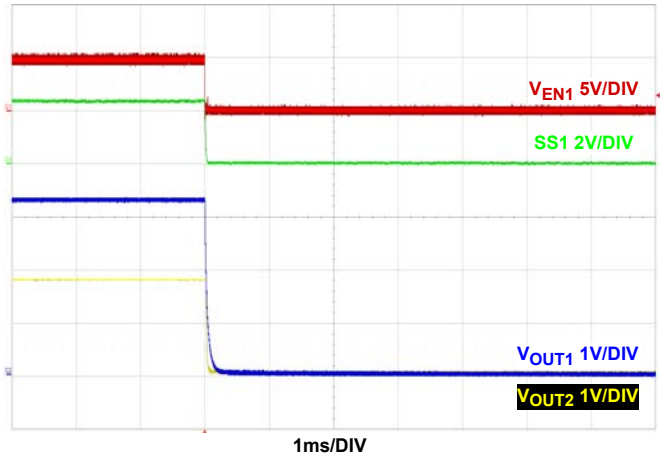


FIGURE 29. RATIOMETRIC SHUTDOWN WITH V_{OUT1} LEADING V_{OUT2} AT FULL LOAD, V_{IN} = 5V, MODE = PWM, T_A = +25°C

Typical Performance Curves (Continued)

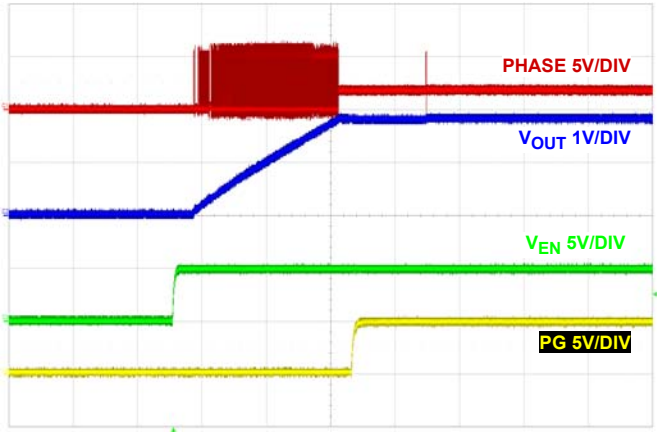


FIGURE 30. START-UP AT NO LOAD, V_{IN} = 5V, MODE = PFM, T_A = +25°C

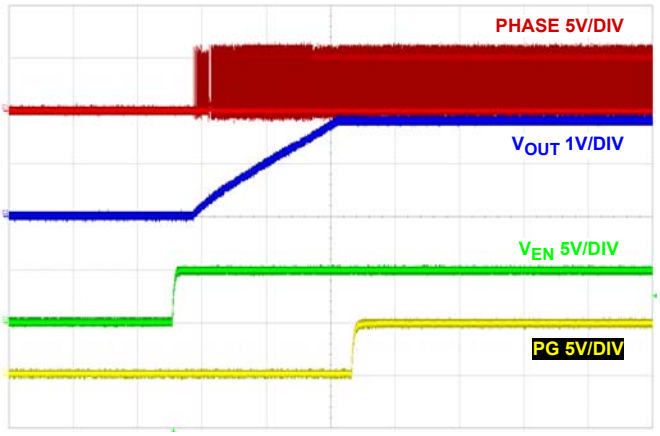


FIGURE 31. START-UP AT NO LOAD, V_{IN} = 5V, MODE = PWM, T_A = +25°C

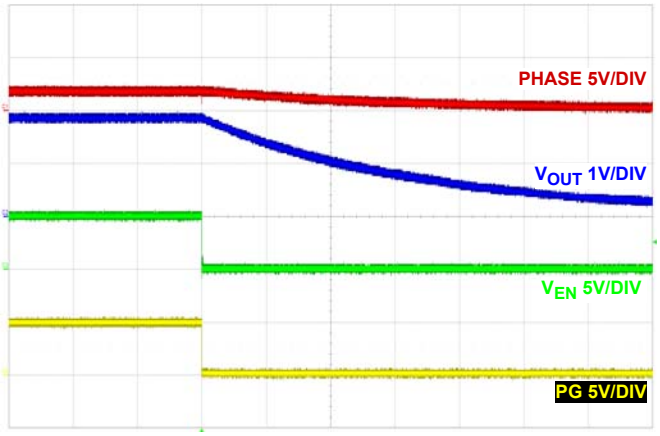


FIGURE 32. SHUTDOWN AT NO LOAD, V_{IN} = 5V, MODE = PFM, T_A = +25°C

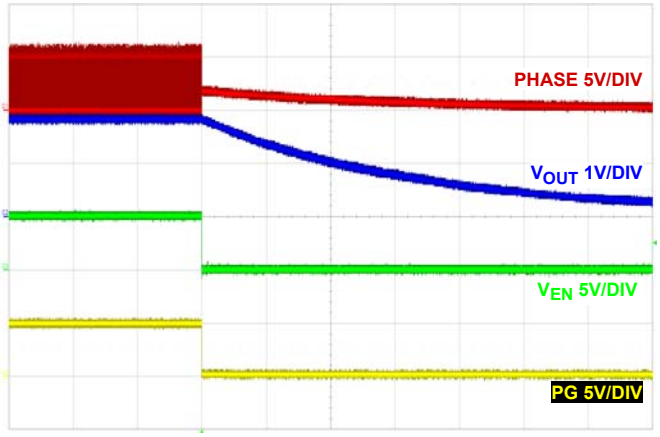


FIGURE 33. SHUTDOWN AT NO LOAD, V_{IN} = 5V, MODE = PWM, T_A = +25°C

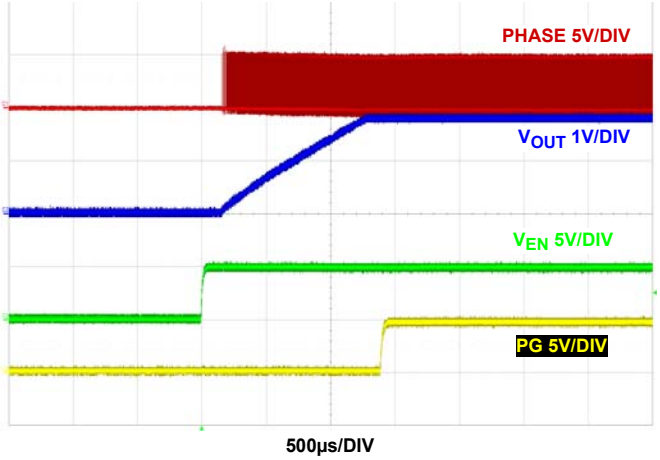


FIGURE 34. START-UP AT 2A LOAD, V_{IN} = 5V, MODE = PWM, T_A = +25°C

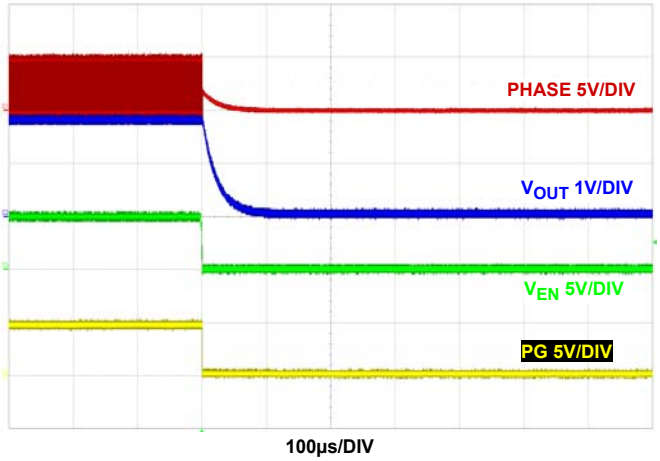


FIGURE 35. SHUTDOWN AT 2A LOAD, V_{IN} = 5V, MODE = PWM, T_A = +25°C

Typical Performance Curves (Continued)

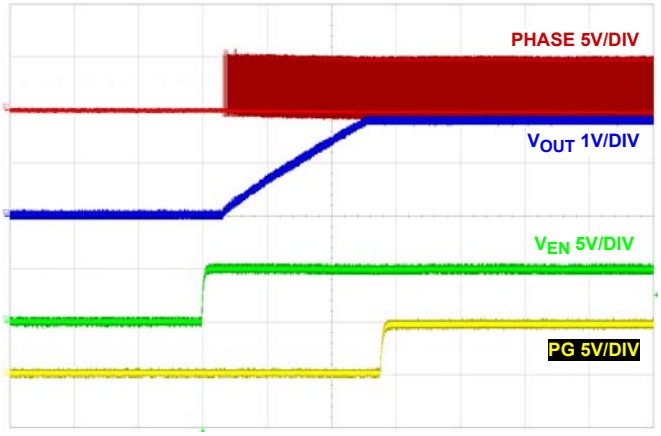


FIGURE 36. START-UP AT 2A LOAD, V_{IN} = 5V, MODE = PFM, T_A = +25°C

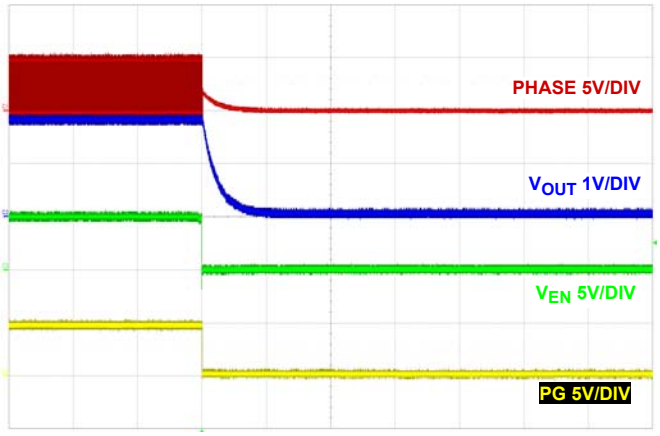


FIGURE 37. SHUTDOWN AT 2A LOAD, V_{IN} = 5V, MODE = PFM, T_A = +25°C

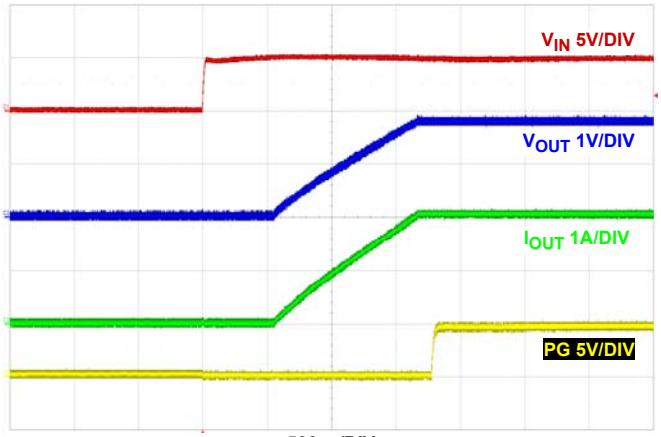


FIGURE 38. START-UP V_{IN} AT 2A LOAD, V_{IN} = 5V, MODE = PFM, T_A = +25°C

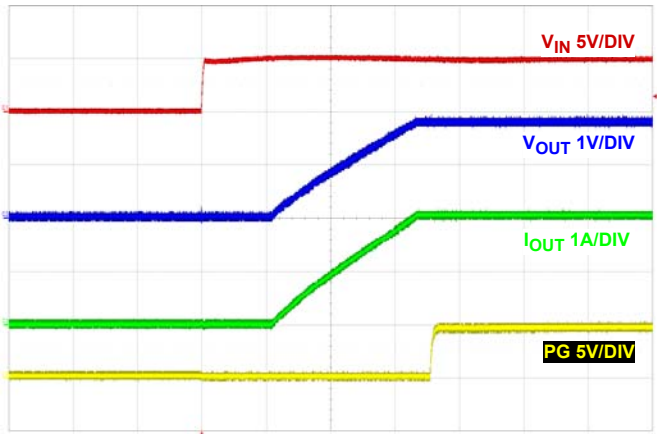


FIGURE 39. START-UP V_{IN} AT 2A LOAD, V_{IN} = 5V, MODE = PWM, T_A = +25°C

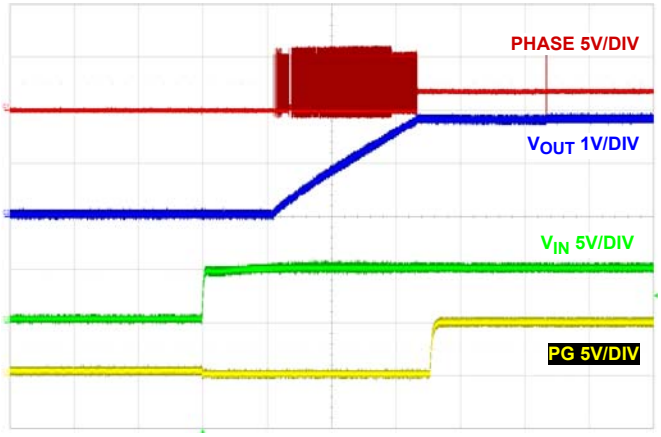


FIGURE 40. START-UP V_{IN} AT NO LOAD, V_{IN} = 5V, MODE = PFM, T_A = +25°C

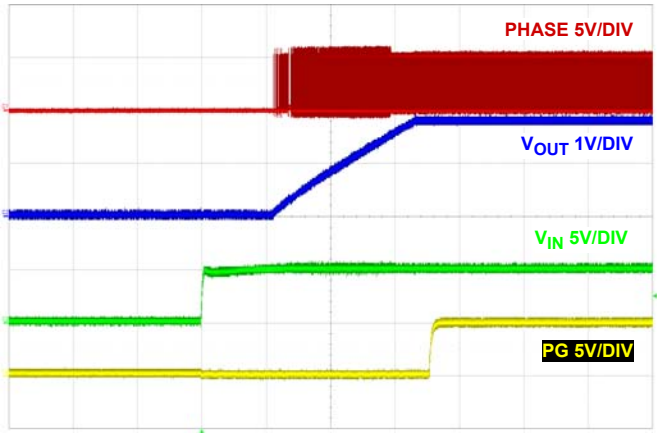


FIGURE 41. START-UP V_{IN} AT NO LOAD, V_{IN} = 5V, MODE = PWM, T_A = +25°C

Typical Performance Curves (Continued)

FIGURE 42. JITTER AT NO LOAD PWM, V_{IN} = 5V, MODE = PWM, T_A = +25°C

FIGURE 43. JITTER AT FULL LOAD PWM, V_{IN} = 5V, MODE = PWM, T_A = +25°C

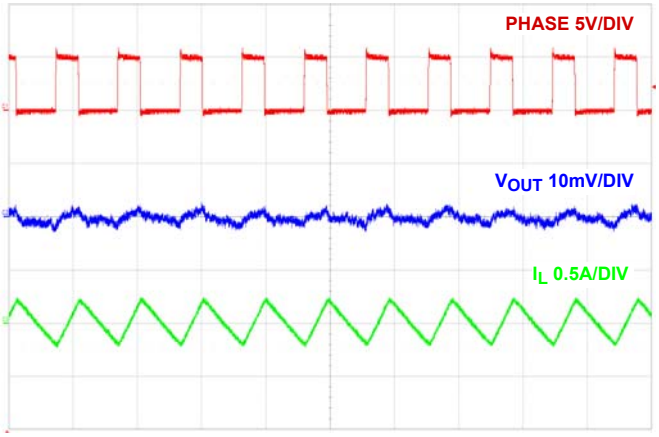


FIGURE 44. STEADY STATE AT NO LOAD, V_{IN} = 5V, MODE = PWM, T_A = +25°C

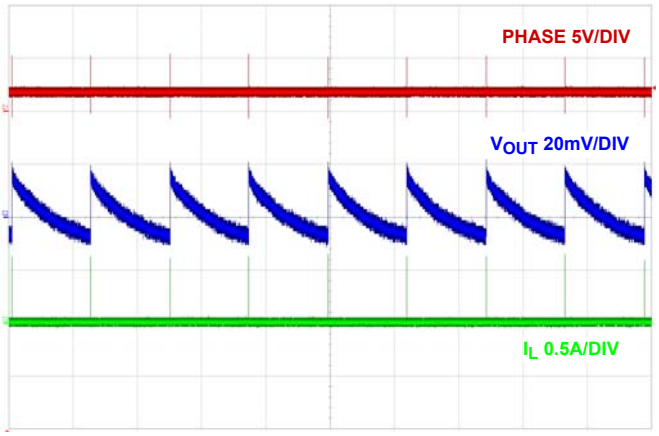


FIGURE 45. STEADY STATE AT NO LOAD, V_{IN} = 5V, MODE = PFM, T_A = +25°C

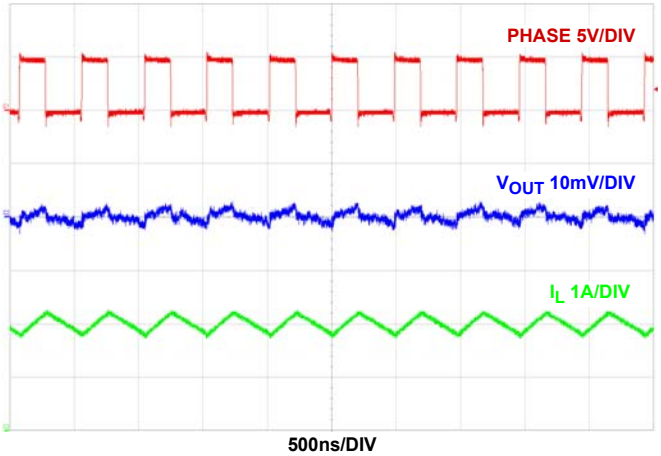


FIGURE 46. STEADY STATE AT 2A LOAD, V_{IN} = 5V, MODE = PWM, T_A = +25°C

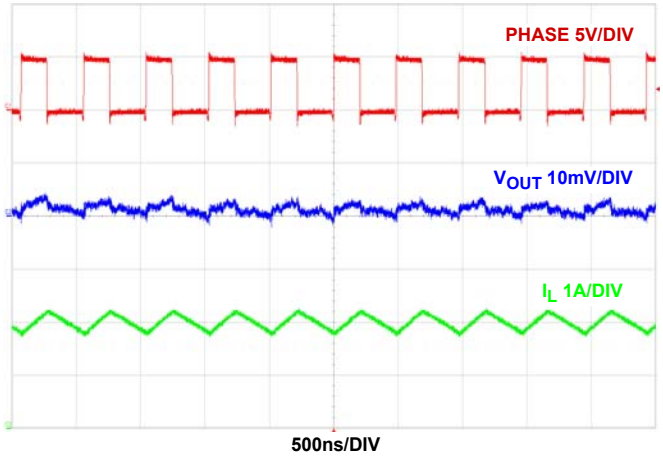


FIGURE 47. STEADY STATE AT 2A LOAD, V_{IN} = 5V, MODE = PFM, T_A = +25°C

Typical Performance Curves (Continued)

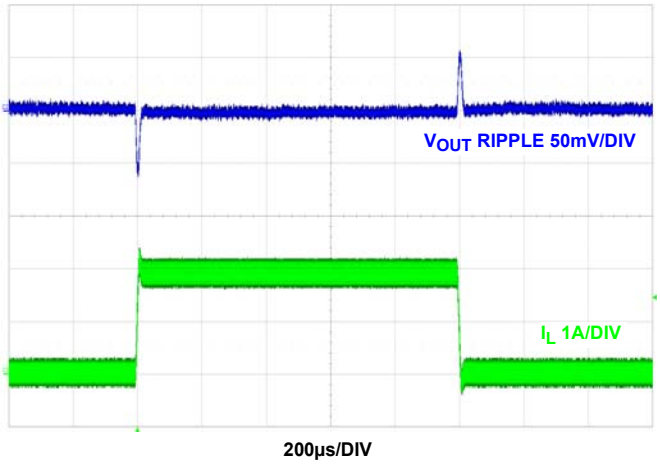


FIGURE 48. LOAD TRANSIENT, V_{IN} = 5V, MODE = PWM, T_A = +25°C

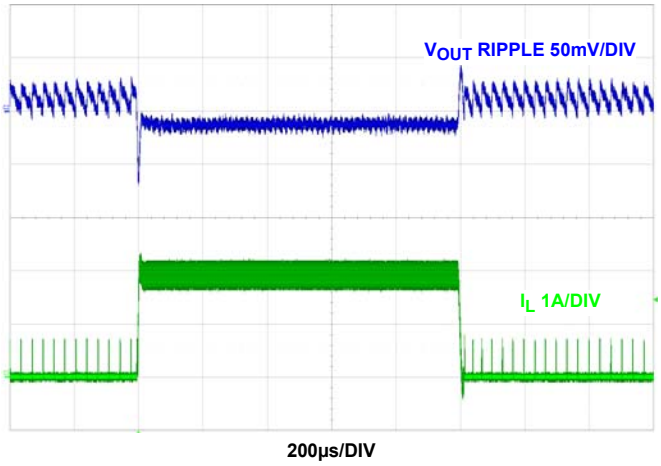


FIGURE 49. LOAD TRANSIENT, V_{IN} = 5V, MODE = PFM, T_A = +25°C

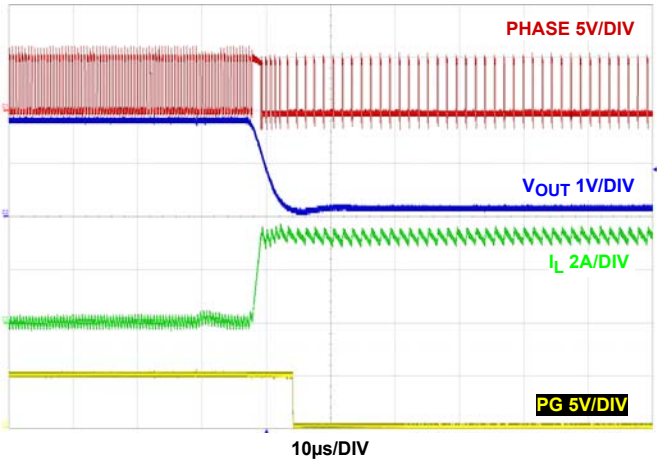


FIGURE 50. OUTPUT SHORT CIRCUIT, V_{IN} = 5V, MODE = PWM, T_A = +25°C

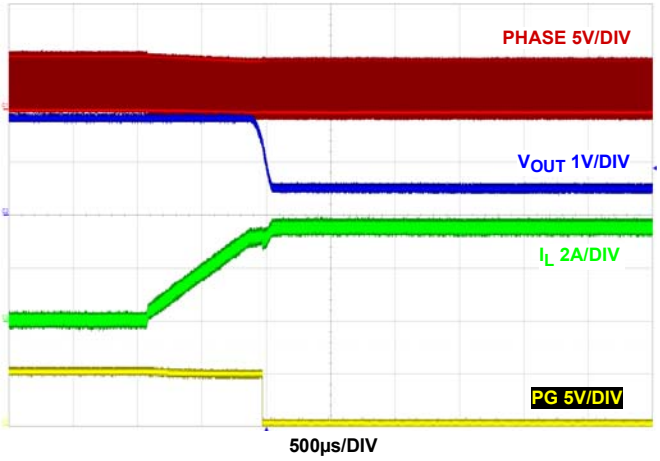


FIGURE 51. OVERCURRENT PROTECTION, V_{IN} = 5V, MODE = PWM, T_A = +25°C

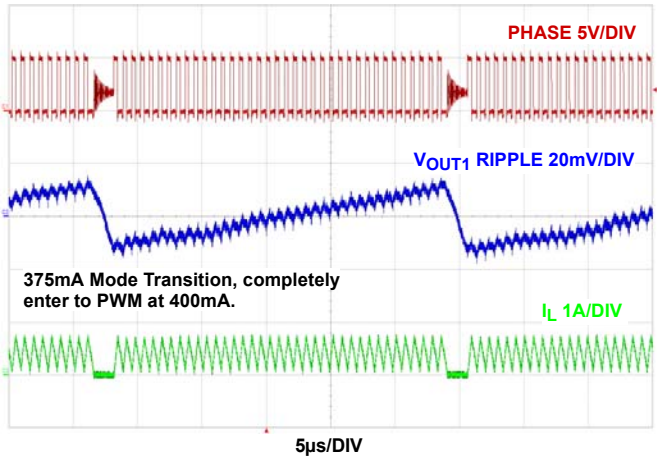


FIGURE 52. PFM TO PWM TRANSITION, V_{IN} = 5V, MODE = PFM, T_A = +25°C

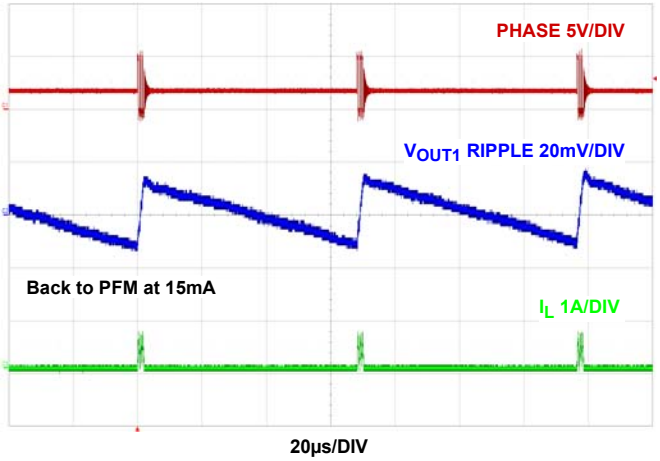


FIGURE 53. PWM TO PFM TRANSITION, V_{IN} = 5V, MODE = PFM, T_A = +25°C

Typical Performance Curves (Continued)

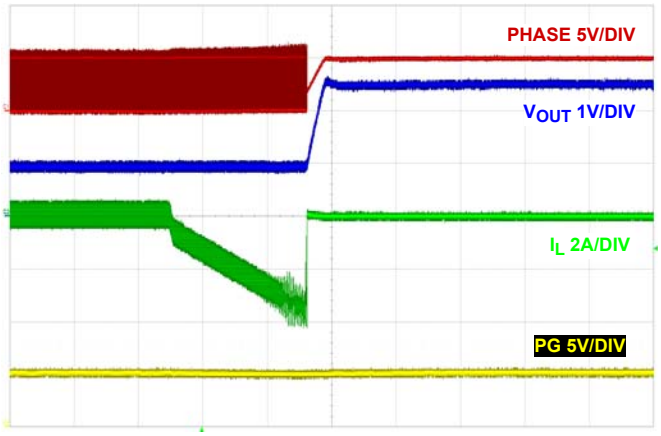


FIGURE 54. OVERVOLTAGE PROTECTION, V_{IN} = 5V, MODE = PWM, T_A = +25°C

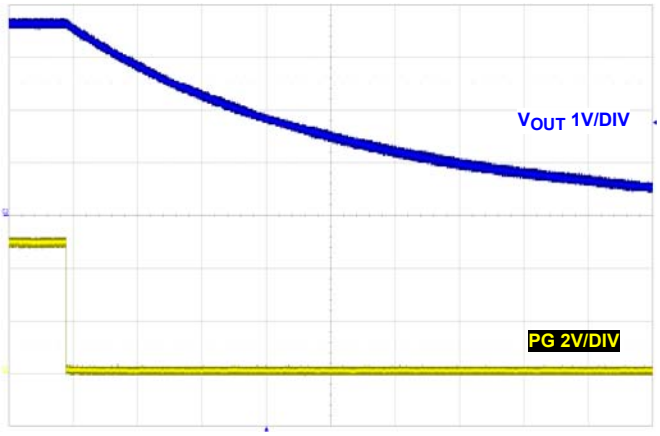


FIGURE 55. OVER-TEMPERATURE PROTECTION, V_{IN} = 5V, MODE = PWM, T_A = +159°C

Theory of Operation

The device is a step-down switching regulator optimized for battery powered applications. It operates at a high switching frequency, which enables the use of smaller inductors resulting in small form factor, while also providing excellent efficiency. Further, at light loads while in PFM mode, the regulator reduces the switching frequency, thereby minimizing the switching loss and maximizing battery life. The quiescent current, when the output is not loaded, is typically only 35µA. The supply current is typically only 20µA when the regulator is shut down.

PWM Control Scheme

Pulling the MODE pin HI (>2.5V) forces the converter into PWM mode, regardless of output current. The device employs the current-mode Pulse-Width Modulation (PWM) control scheme for fast transient response and pulse-by-pulse current limiting. Refer to the "Functional Block Diagram" on page 5. The current loop consists of the oscillator, the PWM comparator, current sensing circuit and the slope compensation for the current loop stability. The slope compensation is 900mV/Ts, which changes with frequency. The gain for the current sensing circuit is typically 300mV/A. The control reference for the current loops comes from the error amplifier's (EAMP) output.

The PWM operation is initialized by the clock from the oscillator. The P-channel MOSFET is turned on at the beginning of a PWM cycle and the current in the MOSFET starts to ramp-up. When the sum of the current amplifier, CSA, and the slope compensation reaches the control reference of the current loop, the PWM comparator COMP sends a signal to the PWM logic to turn off the P-FET and turn on the N-channel MOSFET. The N-FET stays on until the end of the PWM cycle. Figure 56 shows the typical operating waveforms during the PWM operation. The dotted lines illustrate the sum of the slope compensation ramp and the current-sense amplifier's CSA output. To ensure proper PWM control, minimum on time need to be greater than 90ns.

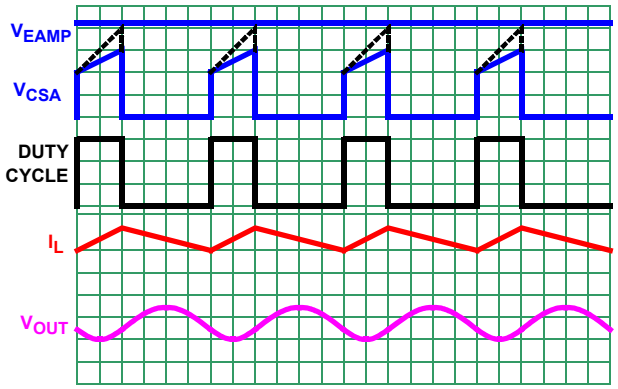


FIGURE 56. PWM OPERATION WAVEFORMS

The reference voltage is 0.6V, which is used by feedback to adjust the output of the error amplifier, V_{EAMP}. The error amplifier is a transconductance amplifier that converts the voltage error signal to a current output. The voltage loop is internally compensated with the 27pF and 200kΩ RC network. The maximum EAMP voltage output is precisely clamped to 1.6V.

PFM Mode

Pulling the MODE pin LO (<0.4V) forces the converter into PFM mode. The device enters a Pulse-skipping mode at light load to minimize the switching loss by reducing the switching frequency. Figure 57 illustrates the Skip mode operation. A zero-cross sensing circuit shown in Figure 57 monitors the N-FET current for zero crossing. When 16 consecutive cycles of the inductor current crossing zero are detected, the regulator enters the Skip mode. During the sixteen detecting cycles, the current in the inductor is allowed to become negative. The counter is reset to zero when the current in any cycle does not cross zero.

Once the Skip mode is entered, the pulse modulation starts being controlled by the SKIP comparator shown in the "Functional Block Diagram" on page 5. Each pulse cycle is still synchronized by the PWM clock. The P-FET is turned on at the clock's rising edge and turned off when the output is higher than 1.5% of the nominal regulation or when its current reaches the peak skip current limit value. Then the inductor current is discharging to 0A and stays at zero. The internal clock is disabled. The output voltage reduces gradually due to the load current discharging the output capacitor. When the output voltage drops to the nominal voltage, the P-FET will be turned on again at the rising edge of the internal clock as it repeats the previous operations.

The regulator resumes normal PWM mode operation when the output voltage drops 1.5% below the nominal voltage.

Overcurrent Protection

The overcurrent protection is realized by monitoring the CSA output with the OCP comparator, as shown in the "Functional Block Diagram" on page 5. The current sensing circuit has a gain of 300mV/A, from the P-FET current to the CSA output. When the CSA output reaches a threshold, the OCP comparator is tripped to turn off the P-FET immediately. The overcurrent function protects the switching converter from a shorted output by monitoring the current flowing through the upper MOSFET.

Upon detection of an overcurrent condition, the upper MOSFET will be immediately turned off and will not be turned on again until the next switching cycle. If the overcurrent condition goes away, the output will resume back into regulation point.

Short-Circuit Protection

The Short-Circuit Protection (SCP) comparator monitors the VFB pin voltage for output short-circuit protection. When the VFB is lower than 0.3V, the SCP comparator forces the PWM oscillator frequency to drop to 1/3 of the normal operation value. This comparator is effective during start-up or an output short-circuit event.

Negative Current Protection

Similar to the overcurrent, the negative current protection is realized by monitoring the current across the low-side N-FET, as shown in the "Functional Block Diagram" on page 5. When the valley point of the inductor current reaches -1.8A for 2 consecutive cycles, both P-FET and N-FET shut off. The 100Ω in parallel to the N-FET will activate discharging the output into regulation. The control will begin to switch when output is within regulation. The regulator will be in PFM for 20µs before switching to PWM if necessary.

PG

PG is an output of a comparator that continuously monitors the buck regulator output voltage. PG is actively held low when EN is low and during the buck regulator soft-start period. After 0.1ms delay of the soft-start period, PG becomes high impedance as long as the output voltage is within nominal regulation voltage set by VFB. When VFB drops 15% below the nominal regulation voltage, the device pulls PG low. Any fault condition forces PG low until the fault condition is cleared by attempts to soft-start. There is an internal 5MΩ pull-up resistor to fit most applications. An external resistor can be added from PG to VIN for more pull-up strength.

UVLO

When the input voltage is below the Undervoltage Lockout (UVLO) threshold, the regulator is disabled.

Enable, Disable and Soft Start-Up

After the VIN pin exceeds its rising POR trip point (nominal 2.7V), the device begins operation. If the EN pin is held low externally, nothing happens until this pin is released. Once the EN is released and above the logic threshold, the internal default soft-start time is 1ms if SS/TR is tied high above 0.6V.

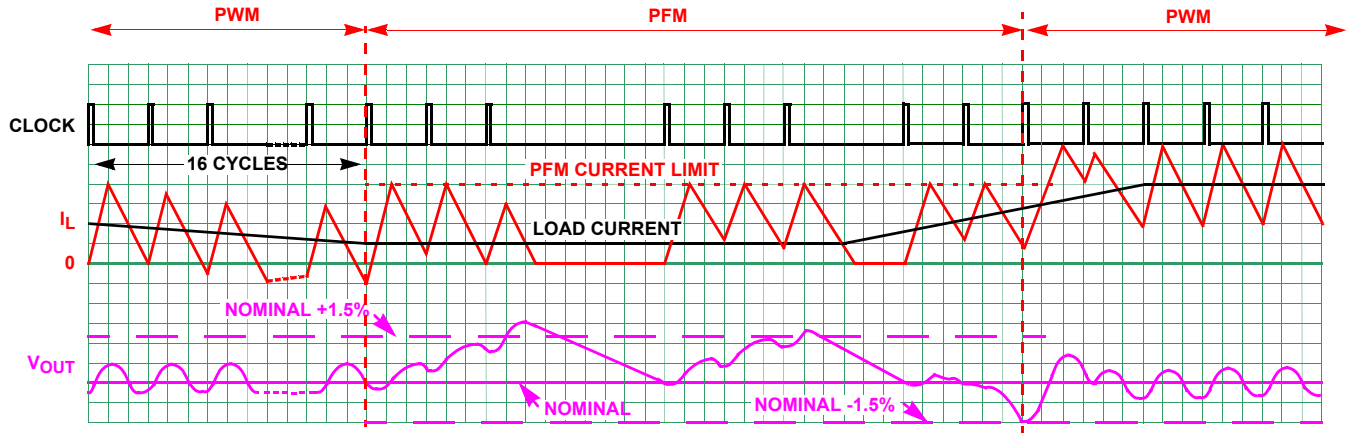


FIGURE 57. SKIP MODE OPERATION WAVEFORMS

Output Tracking and Sequencing

Output soft-start programming, tracking and sequencing between multiple regulators can be implemented by using the SS/TR pin. Independent programming soft-start for each channel is shown in Figure 58. The output ramp time for each channel (t_{SS}) is set by the soft-start capacitor (C_{SS}). Maximum C_{SS} value is 1µF and the SS time should be greater than 1ms.

Figures 59, 60, and 61 show several configurations for output tracking/sequencing for a 3.3V and 1.8V application.

Ratiometric tracking is achieved in Figure 59 by connecting SS/TR on each channel. The measurement is shown in Figures 26 through 29.

By connecting a feedback network from V_{OUT1} to the SS/TR2 pin with the same ratio that sets V_{OUT2} voltage, absolute tracking shown in Figure 60 is implemented. The measurement is shown in Figures 18 through 21. If the output of Channel 1 is shorted to GND, it will enter overcurrent mode, SS/TR2 will be pulled low through the added resistor between V_{OUT1} and SS2 and this will force Channel 2 into being low as well.

Figure 61 illustrates output sequencing. When EN1 is transitioned high, VOUT1 comes up first and V_{OUT2} won't start until OUT1 > 85% of its regulation point. The measurement is shown in Figures 22 through 25.

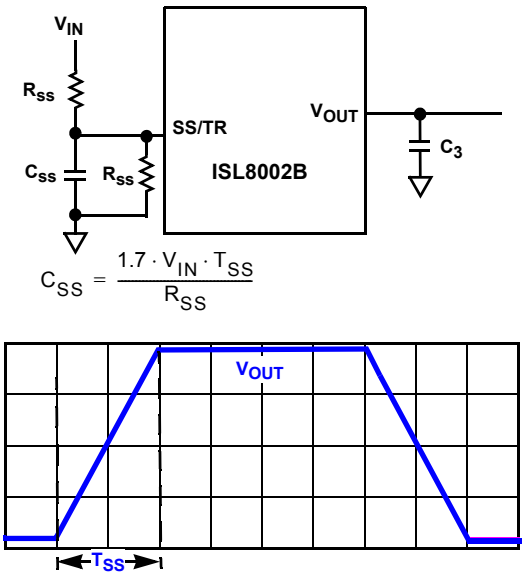


FIGURE 58. PROGRAMMING SOFT-START

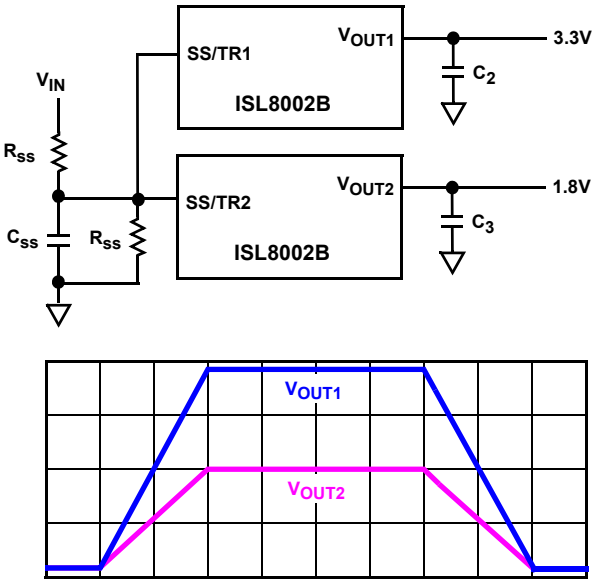


FIGURE 59. RATIOMETRIC START-UP

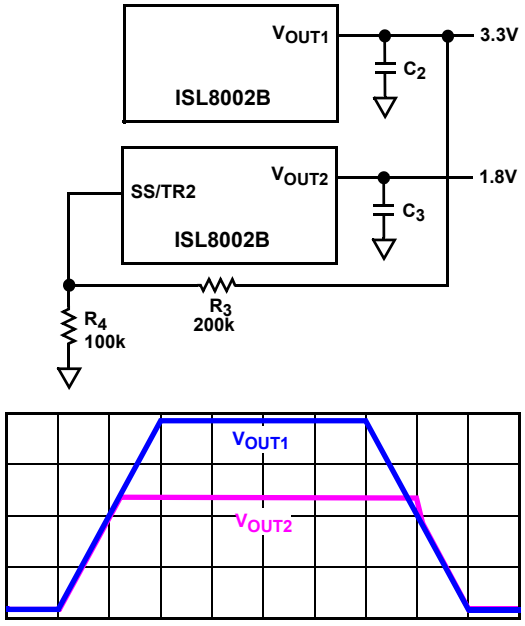


FIGURE 60. COINCIDENTAL VOLTAGE TRACKING

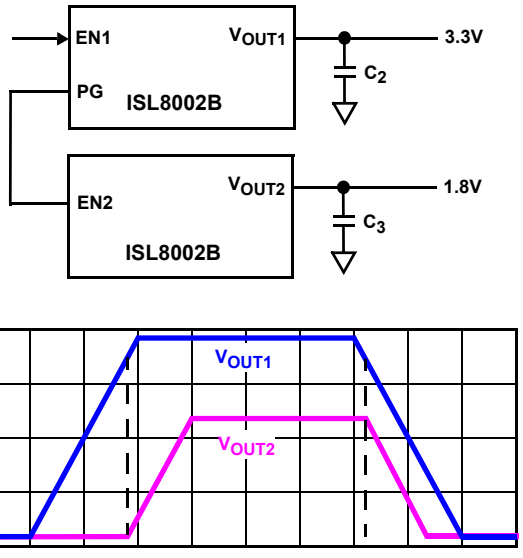


FIGURE 61. OUTPUT SEQUENCING

Discharge Mode (Soft-Stop)

When a transition to shutdown mode occurs or the V_{IN} UVLO is set, the outputs discharge to GND through an internal 100Ω switch.

Thermal Shutdown

The device has built-in thermal protection. When the internal temperature reaches +150°C, the regulator is completely shut down. As the temperature drops to +125°C, the device resumes operation by stepping through the soft-start.

Power Derating Characteristics

To prevent the ISL8002B from exceeding the maximum junction temperature, some thermal analysis is required. The temperature rise is given by Equation 2:

$$T_{RISE} = (PD)(\theta_{JA}) \quad \text{(EQ. 2)}$$

where PD is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature. The junction temperature, T_J, is given by Equation 3:

$$T_J = (T_A + T_{RISE}) \quad \text{(EQ. 3)}$$

where T_A is the ambient temperature. For the DFN package, the θ_{JA} is +71°C/W.

The actual junction temperature should not exceed the absolute maximum junction temperature of +125°C when considering the thermal design.

The ISL8002B delivers full current at ambient temperatures up to +85°C. If the thermal impedance from the thermal pad maintains the junction temperature below the thermal shutdown level, (depending on the input voltage/output voltage combination and the switching frequency) the device power dissipation must be reduced to maintain the junction temperature at or below the thermal shutdown level. Figure 62 illustrates the approximate output current derating versus ambient temperature for the ISL8002DEMO1Z kit.

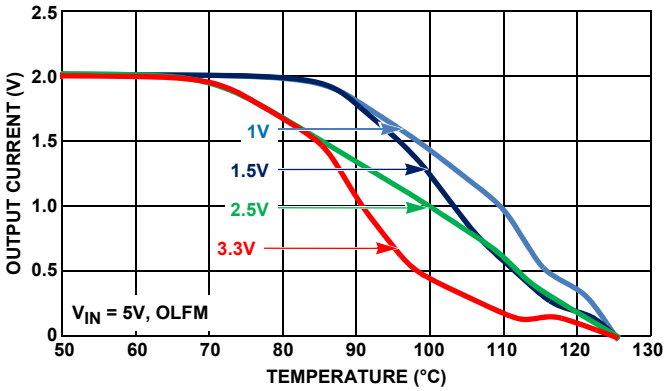


FIGURE 62. DERATING CURVE vs TEMPERATURE

Applications Information

Output Inductor and Capacitor Selection

To consider steady state and transient operations, the ISL8002B typically requires a 1.2µH inductor. Higher or lower inductor value can be used to optimize the total converter system performance. For example, for higher output voltage 3.3V application, in order to decrease the inductor ripple current and output voltage ripple, the output inductor value can be increased. It is recommended to set the inductor ripple current to be approximately 30% of the maximum output current for optimized performance. The inductor ripple current can be expressed as shown in Equation 4:

$$\Delta I = \frac{V_O \bullet \left(1 - \frac{V_O}{V_{IN}}\right)}{L \bullet f_{SW}} \quad \text{(EQ. 4)}$$

The inductor's saturation current rating needs to be at least larger than the peak current.

The device uses an internal compensation network and the output capacitor value is dependent on the output voltage. The ceramic capacitor is recommended to be X5R or X7R.

Output Voltage Selection

The output voltage of the regulator can be programmed (from 0.6V up to 80% of V_{IN}) via an external resistor divider that is used to scale the output voltage relative to the internal reference voltage and feed it back to the inverting input of the error amplifier.

The output voltage programming resistor, R_2, will depend on the value chosen for the feedback resistor and the desired output voltage of the regulator. The value for the feedback resistor is typically between 10kΩ and 100kΩ, as shown in Equation 5.

$$R_1 = R_2\left(\frac{V_O}{VFB} - 1\right) \quad \text{(EQ. 5)}$$

If the output voltage desired is 0.6V, then R_2 is left unpopulated and R_1 is shorted. There is a leakage current from VIN to PHASE. It is recommended to preload the output with 10µA minimum. For better performance, add 4.7pF in parallel with R_1. Check loop analysis before use in application.

Input Capacitor Selection

The main functions for the input capacitor are to provide decoupling of the parasitic inductance and to provide filtering function to prevent the switching current flowing back to the battery rail. At least two 22µF X5R or X7R ceramic capacitors are a good starting point for the input capacitor selection.

Output Capacitor Selection

An output capacitor is required to filter the inductor current. Output ripple voltage and transient response are two critical factors when considering output capacitance choice. The current mode control loop allows for the use of low ESR ceramic capacitors and thus smaller board layout. Electrolytic and polymer capacitors may also be used.

Additional consideration applies to ceramic capacitors. While they offer excellent overall performance and reliability, the actual in-circuit capacitance must be considered. Ceramic capacitors are rated using large peak-to-peak voltage swings and with no DC bias. In the DC/DC converter application, these conditions do not reflect reality. As a result, the actual capacitance may be considerably lower than the advertised value. Consult the manufacturers datasheet to determine the actual in-application capacitance. Most manufacturers publish capacitance vs DC bias so that this effect can be easily accommodated. The effects of AC voltage are not frequently published, but an assumption of ~20% further reduction will generally suffice. The result of these considerations can easily result in an effective capacitance 50% lower than the rated value. Nonetheless, they are a very good choice in many applications due to their reliability and extremely low ESR.

Equations 6 and 7 allow calculation of the required capacitance to meet a desired ripple voltage level. Additional capacitance may be used.

For the ceramic capacitors (low ESR) =

$$V_{OUTripple} = \frac{\Delta I}{8 * f_{SW} * C_{OUT}} \quad \text{(EQ. 6)}$$

where ΔI is the inductor's peak-to-peak ripple current, f_{SW} is the switching frequency and C_{OUT} is the output capacitor.

If using electrolytic capacitors then:

$$V_{OUTripple} = \Delta I * ESR \quad \text{(EQ. 7)}$$

Regarding transient response needs, a good starting point is to determine the allowable overshoot in V_{OUT} if the load is suddenly removed. In this case, energy stored in the inductor will be transferred to C_{OUT} causing its voltage to rise. After calculating capacitance required for both ripple and transient needs, choose the larger of the calculated values. Equation 8 determines the required output capacitor value in order to achieve a desired overshoot relative to the regulated voltage.

$$C_{OUT} = \frac{I_{OUT}^2 * L}{V_{OUT}^2 * ((V_{OUTMAX}/V_{OUT})^2 - 1)} \quad \text{(EQ. 8)}$$

where V_{OUTMAX}/V_{OUT} is the relative maximum overshoot allowed during the removal of the load. For an overshoot of 5%, Equation 8 becomes Equation 9

$$C_{OUT} = \frac{I_{OUT}^2 * L}{V_{OUT}^2 * (1.05^2 - 1)} \quad \text{(EQ. 9)}$$

Layout Considerations

The PCB layout is a very important converter design step to make sure the designed converter works well. The power loop is composed of the output inductor L's, the output capacitor C_{OUT}, the PHASE's pins and the PGND pin. It is necessary to make the power loop as small as possible and the connecting traces among them should be direct, short, and wide. The switching node of the converter, the PHASE pins, and the traces connected to the node are very noisy, so keep the voltage feedback trace away from these noisy traces. The input capacitor should be placed as close as possible to the VIN pin and the ground of the input and output capacitors should be connected as close as possible. The heat of the IC is mainly dissipated through the thermal pad. Maximizing the copper area connected to the thermal pad is preferable. In addition, a solid ground plane is helpful for better EMI performance. It is recommended to add at least four vias ground connection within the pad for the best thermal relief.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
October 28, 2016	FN8690.3	Updated Related Literature section on page 1. Added ISL8002BFRZ-T and ISL8002BFRZ-T7A information to ordering information table on page 3. Updated EC table boldface statement. Added Test condition for 1st line of Feedback Voltage specification. Bolded the -40°C to +125°C min/max values.
June 5, 2015	FN8690.2	Figure 13 on page 9 changed the color of the curve: blue changed to pink and pink one changed to blue. POD on page 22 updated, changes since rev0: Tiebar Note updated From: Tiebar shown (if present) is a non-functional feature. To: Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
February 20, 2015	FN8690.1	Added ISL8002BIRZ-T7A to Ordering Information table on page 3. Added ESD Ratings and Latch-up on page 6. Clarified Application section on page 19.
November 10, 2014	FN8690.0	Initial Release.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

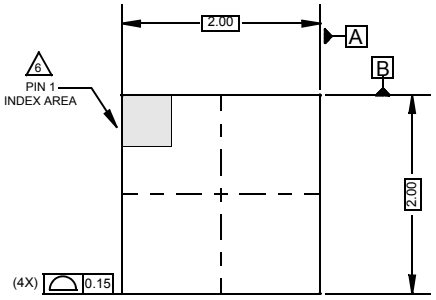
Package Outline Drawing

For the most recent package outline drawing, see L8.2x2C.

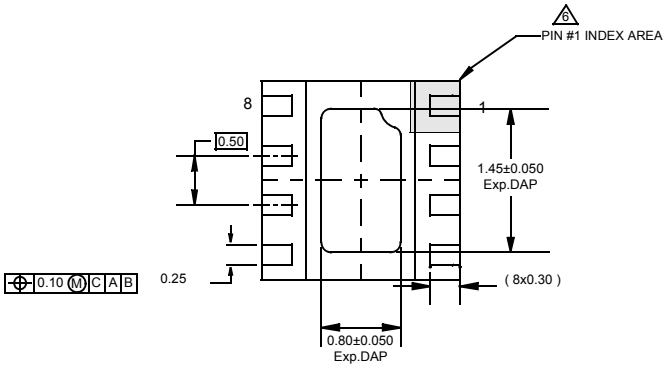
L8.2x2C

8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE (TDFN) WITH E-PAD

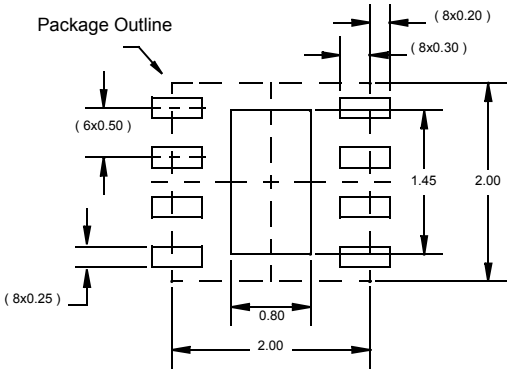
Rev 1, 5/15



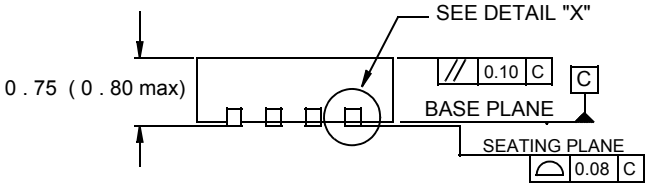
TOP VIEW



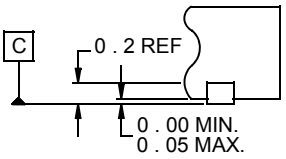
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.