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Datasheet

ISL75055SLH

Radiation Hardened 3A Source and Sink DDR Terminator/LDO with Buffered Reference

Description

The ISL75055SLH is a radiation hardened 0.75V to 5.5V input, 3A sourcing and sinking low-dropout linear regulator designed for powering the VTT termination rail of DDR memory modules. A buffered reference amplifier provides an accurate VREF reference supply for the DDR. Individual adjustable overcurrent protection (OCP) for sourcing and sinking allows the current limit of the LDO to be configured down to 300mA.

The ISL75055SLH features external error amplifier inputs to set VDDQ/2 as the reference voltage in DDR applications. It also features an internal 0.5V reference for standard LDO applications.

Separate VCC bias and LDO VIN pins, combined with a very low dropout allows minimal internal losses while maintaining highly accurate output regulation.

The ISL75055SLH is offered in an 18 Lead Ceramic Metal Seal Flatpack Package with Two Bottom Heat Slugs (CDFP) and operates across the full military temperature range of -55°C to +125°C.

Applications

- DDR, DDR2, DDR3 and DDR4 memory VTT termination rail and buffered VREF reference
- Low noise supply rail for FPGA, DSP and ASIC
- General purpose LDO rails
- Two quadrant supply for sourcing or sinking up to 3A of current

Features

- Qualified to Renesas Rad Hard QML-V Equivalent Screening and QCI Flow (R34TB0001EU)
  - All screening and QCI is in accordance with MIL-PRF-38535 Class-V
- Separate 2.7V to 5.5V bias rail and 0.75V to 5.5V LDO input rail
- 3A sourcing and sinking low dropout regulator with 600µV dead band crossover
- Internal buffered reference amplifier provides VREF = VDDQ/2 for DDR applications
- Internal 0.5V voltage reference for standard LDO applications
- Low 142mV typical dropout at 3A sourcing in DDR4 configuration
- Individual OCP setting for source and sink from 300mA to 3A
- Optional LDO and buffer output discharge function
- Externally adjustable soft-start
- TID Rad Hard Assurance (RHA) testing
  - LDR (<10mrad(Si)/s): 75krad(Si)
- SEE Characterization
  - No DSEE for VIN = 6.2V, VCC = 6.2V at 86MeV•cm^2/mg
  - VOUT and BUF-OUT SET < 2% at 86MeV•cm^2/mg
  - |VOUT - BUF-OUT| SET < 40mV at 86MeV•cm^2/mg
  - SEFI < 0.18µm^2 at 86MeV•cm^2/mg

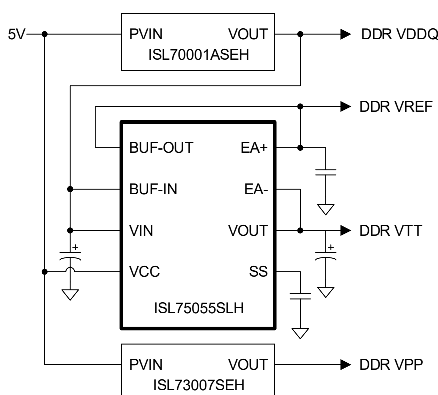

Figure 1. DDR4 Power Management Block Diagram

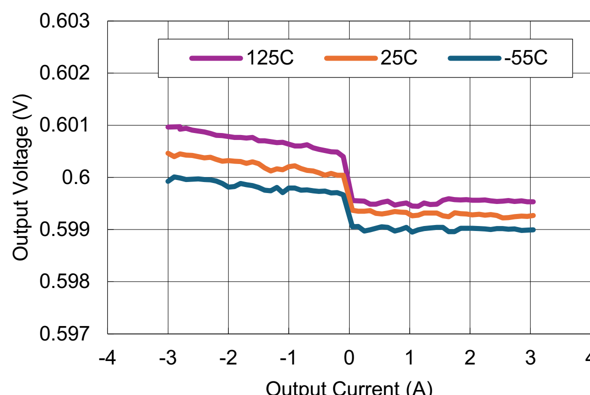

Figure 2. DDR4 Output Voltage Regulation

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1. Overview

1.1 Typical Applications

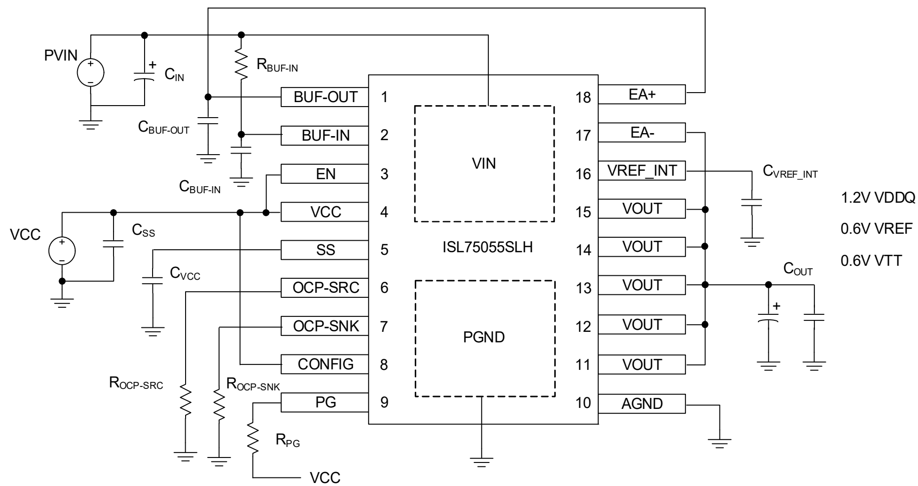


Figure 3. CDFP Typical Application Circuit: VTT Rail for DDR4 Memory Module

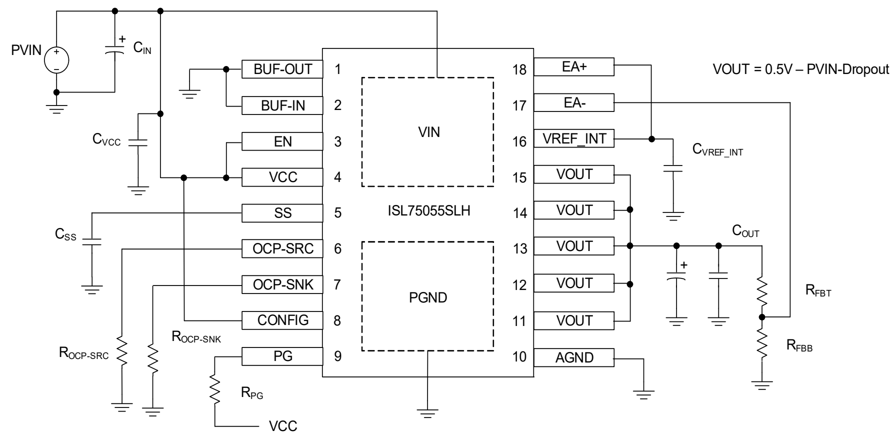


Figure 4. CDFP Typical Application Circuit: Standard LDO Output Applications

1.2 Block Diagram

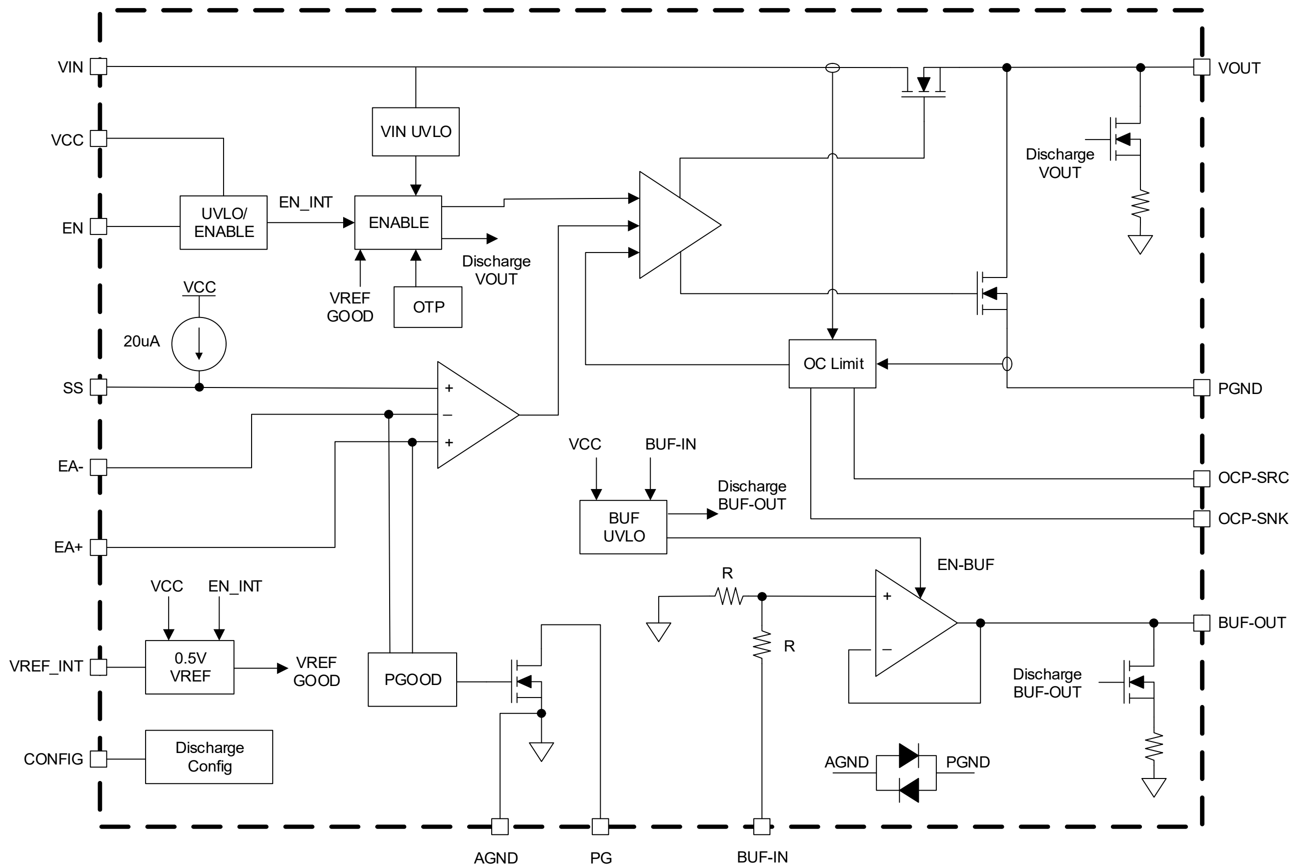
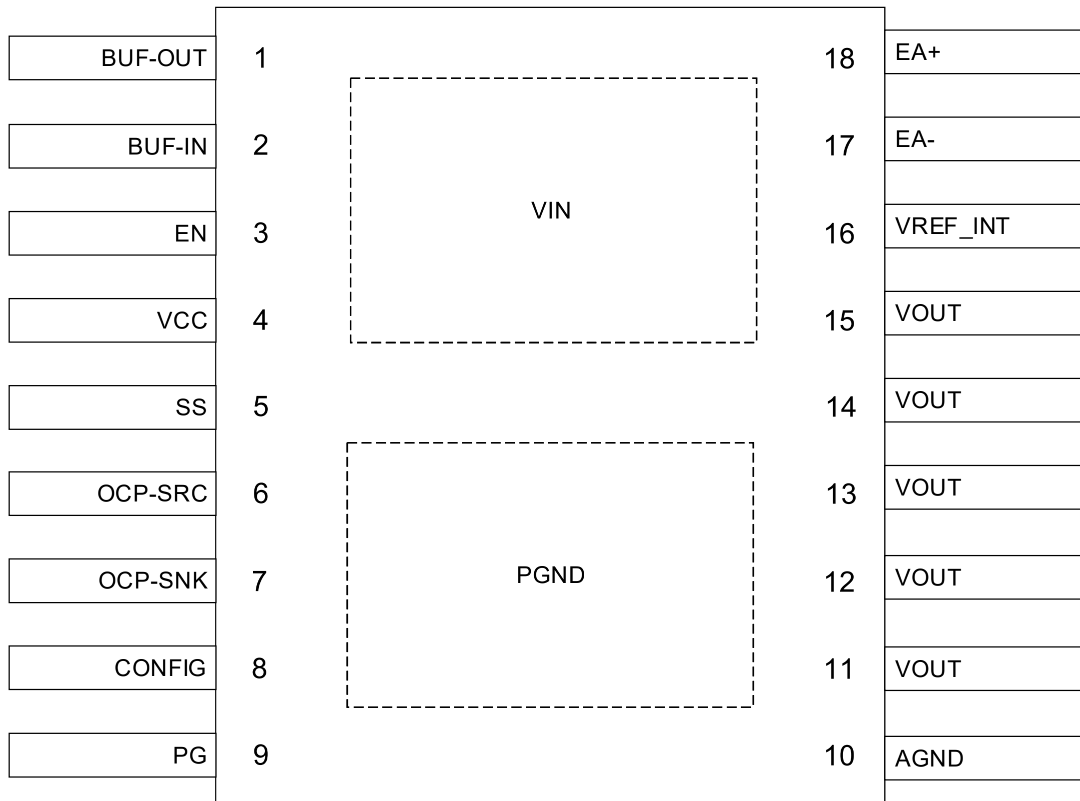


Figure 5. Functional Block Diagram

2. Pin Information

2.1 Pin Assignments



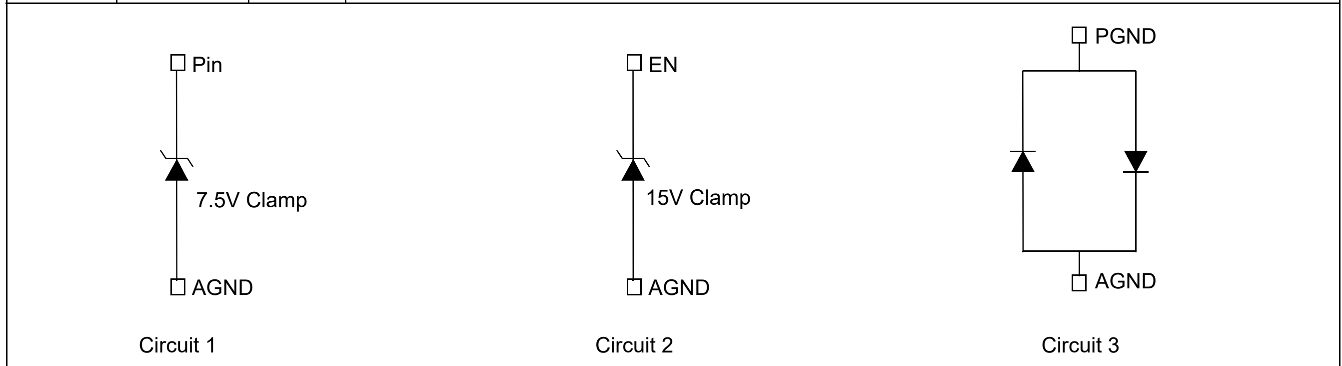
Note: Pin 1 has a protrusion in the package lead. See Package Outline Drawing.

Figure 6. Pin Assignments - Top View

2.2 Pin Descriptions

Pin Number	Pin Name	ESD Circuit	Description
1	BUF-OUT	1	Buffered reference outputs voltage 50% of BUF-IN for DDR applications. This pin can source or sink up to 10mA. Place a minimum 100nF, maximum 2.2µF capacitor on this pin to AGND for filtering. A minimum of 1µF is recommended for SEE mitigation. Buffered reference output is independent of EN input and active when BUF-IN is above 0.78V.
2	BUF-IN	1	Buffered reference input voltage VDDQ for DDR applications. An internal voltage divider outputs 50% of the input signal (VDDQ/2) on BUF-OUT pin. When VIN directly supplies BUF-IN, a 1kΩ/1µF filter is recommended at the input of BUF-IN for SEE mitigation.
3	EN	2	Enable pin for the LDO output.
4	VCC	1	Analog bias pin with 2.7V to 5.5V input range. Place a minimum 1µF capacitor on this pin to AGND for filtering.
5	SS	1	Soft-start pin. Place a capacitor on this pin for soft-start power up. A 20µA current source charges capacitor for ramping the reference of the error amplifier for a controlled start-up.
6	OCP-SRC	1	Sourcing overcurrent protection setting pin. A resistor on this pin to GND sets the Sourcing OCP level from 300mA to 3A. Short this pin to AGND for 4A typical sourcing OCP level.

Pin Number	Pin Name	ESD Circuit	Description
7	OCP-SNK	1	Sinking overcurrent protection setting pin. A resistor on this pin to GND sets the Sinking OCP level from 300mA to 3A. Short this pin to AGND for 4.1A typical sinking OCP level.
8	CONFIG	1	LDO VOUT and BUF-OUT discharge control pin. When low, discharge function disabled. When high, discharge function enabled. Internal switch discharges VOUT when EN = low. Internal switch discharges BUF-OUT when BUF-IN is below BUF-IN UVLO threshold.
9	PG	1	Open-drain, power-good indicator pin. Place a resistor from PG to VCC. When VOUT is in overvoltage or undervoltage, PG pin pulls low.
10	AGND	-	Analog ground pin.
11	VOUT	1	LDO output pin. Refer to section 6.5 for more information on output capacitor selection.
12			
13			
14			
15			
16	VREF_INT	1	Internal 500mV reference. Place a 0.1µF ceramic capacitor on this pin to AGND.
17	EA-	1	Inverting input to the error amplifier.
18	EA+	1	Non-inverting input to the error amplifier. Connect to VREF_INT for the 500mV internal reference or connect to BUF-OUT for DDR applications.
EPADU	VIN	1	LDO input voltage. A single 150µF tantalum capacitor and 2×10µF ceramic capacitor is recommended close to VIN and PGND connections. This is the upper EPAD on the backside of package. Connect EPADU to the PCB on multiple layers with thermal vias underneath the EPADU to maximize thermal performance.
EPADL	PGND	3	LDO power ground connection. Connect common to AGND pin. The lid of the part is internally connected to this pin. This is the lower EPAD on the backside of package. Connect EPADL to the PCB on multiple layers with thermal vias underneath the EPADL to maximize thermal performance.



3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
VCC to AGND	-0.3	+6.5	V
VCC to AGND[1]	-0.3	+6.2	V
VIN to PGND	-0.3	+6.5	V
VIN to PGND[1]	-0.3	+6.2	V
VOUT to PGND	- 0.3	VIN + 0.3	V
AGND to PGND	-0.3	+0.3	V
All Other Pins	AGND - 0.3	VCC + 0.3	V
Junction Temperature	-55	+150	°C
Storage Temperature	-65	+150	°C
Human Body Model (Tested per MIL-STD-883 TM3015.7)	-	2	kV
Charged Device Model (Tested per JS-002-2022)	-	1	kV
Latch-Up (Tested per JESD-78E; Class 2, Level A) at 125°C	-	±100	mA

1. Tested under a heavy ion environment at LET = 86MeV•cm^2/mg at 125°C.

3.2 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
VCC Voltage	+2.7	+5.5	V
VIN Voltage	+0.75	+5.5	V
BUF-IN	+1.0	+3.3	V
EN, CONFIG, PG	0	VCC	V
VOUT voltage	0	Limited by VIN-VOUT and VCC-VOUT Dropout Specifications	V
EA+ voltage	0	+1.65	V
Current on VOUT	-3	+3	A
Ambient Temperature	-55	+125	°C

3.3 Thermal Information

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	18Ld Ceramic Dual Flatpack	θ_{JA}[1]	Junction to ambient	21.3	°C/W
		θ_{JC}[2]	Junction to case	2.5	°C/W

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features, with vias under both the VIN land (to VIN plane) & PGND land (to PGND plane). See TB379.
2. For θ_{JC}, the case temperature location is the average temp at center of the two metal slugs on the package underside.

3.4 Electrical Specifications

3.4.1 DC Electrical Specifications

Unless otherwise specified: V_{CC} = 2.7V to 5.5V; V_{IN} = 0.75V to 5.5V; EN = V_{CC}; C_{OUT} = 150µF + 2x 10µF; OCP_SRC and OCP_SNK = AGND; T_A = 25°C. **Boldface specifications apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at 25°C with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Temperature	Min	Typ[1]	Max	Unit
Power Supply							
VCC Internal UVLO Rising Threshold	VCC_{UVLO_R}	V_{IN} = 3.3V; V_{OUT} = 0.5V; I_{OUT} = 0A	-55 to +125°C	**2.54**	2.62	**2.69**	V
VCC Internal UVLO Falling Threshold	VCC_{UVLO_F}	V_{IN} = 3.3V; V_{OUT} = 0.5V; I_{OUT} = 0A	-55 to +125°C	**2.44**	2.5	**2.6**	V
VCC UVLO Hysteresis	VCC_{UVLO_H}	-	-55 to +125°C	**90**	115	**140**	mV
VCC Enabled Supply Current	I_{VCC}	V_{CC} = 2.7V, V_{IN} = 0.75V, I_{OUT} = 0A; V_{CC} = 5.5V, V_{IN} = 5.5V, -3A < I_{OUT} < 3A; EA+ = VREF_INT; BUF-IN = 1V	-55 to +125°C	**2.7**	5	**7**	mA
VCC Disabled Supply Current	I_{VCC_SHDN1}	EN = 0V; V_{CC} = 5.5V; BUF-IN = 0V; EA+ = VREF_INT	-55 to +125°C	**120**	210	**300**	µA
	I_{VCC_SHDN2}	EN = 0V; V_{CC} = 5.5V; BUF-IN = 1V; EA+ = VREF_INT	-55 to +125°C	**310**	690	**1000**	µA
VIN Supply Current	I_{VIN}	EN = V_{CC}; V_{IN} = 3.3V; I_{OUT} = 0A; EA+ = VREF_INT	-55 to +125°C	**-**	5	**-**	µA
VIN UVLO Rising	VIN_{UVLO_R}	V_{CC} = 2.7V; BUF-IN = 1V; I_{OUT} = 0A	-55 to +125°C	**370**	472	**490**	mV
VIN UVLO Falling	VIN_{UVLO_F}	V_{CC} = 2.7V; BUF-IN = 1V; I_{OUT} = 0A	-55 to +125°C	**320**	425	**450**	mV
VIN UVLO Hysteresis	VIN_{UVLO_H}	-	-55 to +125°C	**10**	47	**70**	mV
Reference Voltage							
VREF_INT Voltage	V_{REF}	V_{IN} = 3.3V; EA+ = VREF_INT Established by Total Output Accuracy specifications	-55°C	495	500	505	mV
			+25°C	495	500	505	mV
			+125°C	492.5	500	507.5	mV
			+25°C (Post Rad)	492.5	500	507.5	mV
Error Amplifier							
Error Amplifier VOS	EA_VOS	(EA- to EA+); V_{CC} = 3.3V; V_{IN} = 0.8V; EA+ = VREF_INT; I_{OUT} = 0A	+25°C	-2.2	0	2.2	mV
		(EA- to EA+); 2.7V<V_{CC}<5.5V; 0.75V<V_{IN}<5.5V; EA+ = VREF_INT; -3A<I_{OUT}<3A; Includes Regulator Dead-Band	-55 to +125°C	**-2.2**	0	**2.2**	mV
Regulator Dead-Band	DBand	Change in Error Amp VOS from I_{OUT} = -1mA to I_{OUT} = 1mA	-55°C	250	600	850	µV
			+25°C	300	600	900	µV
			+125°C	300	600	1000	µV
			+25°C (Post Rad)	300	600	900	µV
EA+; EA- Input Bias Current	I_EA+; I_EA-	EA+ = EA- = 0.5V; V_{CC} = 3.3V; V_{IN} = 3.3V	-55 to +125°C	-	-	**0.35**	µA

Unless otherwise specified: V_{CC} = 2.7V to 5.5V; V_{IN} = 0.75V to 5.5V; EN = V_{CC}; C_{OUT} = 150µF + 2x 10µF; OCP_SRC and OCP_SNK = AGND; T_A = 25°C. **Boldface specifications apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at 25°C with exposure at a low dose rate of <10mrad(Si)/s.** (Cont.)

Parameter	Symbol	Test Conditions	Temperature	Min	Typ[1]	Max	Unit
LDO VOUT							
Output Accuracy	VOUT%	0.75V < V_{IN} < 5.5V; EA+ = VREF_INT; V_{OUT} = 0.5V, 1.2V, 1.8V, 3.3V; -3A < I_{OUT} < 3A; V_{OUT} < V_{CC}-1.5V; V_{OUT}< V_{IN}-0.25V for V_{OUT} = 0.5V; V_{OUT}< V_{IN}-0.3V for all other V_{OUT}	-55°C	-1	-	1	%
			+25°C	-1	-	1	%
			+125°C	-1.5	-	1.5	%
			+25°C (Post Rad)	-1.5	-	1.5	%
Line Regulation	$VOUT_{LINE}$	0.75V < V_{IN} < 5.5V; EA+ = VREF_INT; V_{OUT} = 0.5V, 1.2V, 1.8V, 3.3V; I_{OUT} = 0A; V_{OUT}< V_{CC}-1.5V; V_{OUT} < V_{IN}-0.25V for V_{OUT} = 0.5V; V_{OUT} < V_{IN}-0.3V for all other V_{OUT}	-55 to +125°C	**-0.16**	-	**0.16**	%/V
Sourcing Load Regulation	V_{OUT_LOAD1}	V_{IN} = 0.75V and 5.5V; EA+ = VREF_INT; V_{OUT} = 0.5V, 1.2V, 1.8V, 3.3V; 0A < I_{OUT} < 3A; V_{OUT} < V_{CC}-1.5V; V_{OUT} < V_{IN}-0.25V for V_{OUT} = 0.5V; V_{OUT} < V_{IN}-0.3V for all other V_{OUT}	-55 to +125°C	**-0.15**	-	-	%/A
Sinking Load Regulation	V_{OUT_LOAD2}	V_{IN} = 0.75V and 5.5V; EA+ = VREF_INT; V_{OUT} = 0.5V, 1.2V, 1.8V, 3.3V; -3A < I_{OUT} < 0A; V_{OUT} < V_{CC}-1.5V; V_{OUT} < V_{IN}-0.25V for V_{OUT} = 0.5V; V_{OUT} < V_{IN}-0.3V for all other V_{OUT}	-55 to +125°C	-	-	**0.20**	%/A

Unless otherwise specified: V_{CC} = 2.7V to 5.5V; V_{IN} = 0.75V to 5.5V; EN = V_{CC}; C_{OUT} = 150µF + 2x 10µF; OCP_SRC and OCP_SNK = AGND; T_A = 25°C. **Boldface specifications apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at 25°C with exposure at a low dose rate of <10mrad(Si)/s.** (Cont.)

Parameter	Symbol	Test Conditions	Temperature	Min	Typ[1]	Max	Unit
Output Accuracy DDR Configuration	V_DDR	V_{CC} = 2.75 - 5.5V; V_{IN} = BUF-IN = 2.5V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = 0A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**1.237**	1.25	**1.263**	V
		V_{CC} = 2.75 - 5.5V; V_{IN} = BUF-IN = 2.5V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = -1A to +1A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**1.237**	1.25	**1.263**	V
		V_{CC} = 2.75 - 5.5V; V_{IN} = BUF-IN = 2.5V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = -3A to +3A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**1.237**	1.25	**1.263**	V
	V_DDR2	V_{IN} = BUF-IN = 1.8V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = 0A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**0.891**	0.9	**0.909**	V
		V_{IN} = BUF-IN = 1.8V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = -1A to +1A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**0.891**	0.9	**0.909**	V
		V_{IN} = BUF-IN = 1.8V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = -3A to +3A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**0.891**	0.9	**0.909**	V
	V_DDR3	V_{IN} = BUF-IN = 1.5V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = 0A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**0.742**	0.75	**0.758**	V
		V_{IN} = BUF-IN = 1.5V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = -1A to +1A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**0.742**	0.75	**0.758**	V
		V_{IN} = BUF-IN = 1.5V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = -3A to +3A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**0.742**	0.75	**0.758**	V
	V_DDR3L	V_{IN} = BUF-IN = 1.35V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = 0A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**0.668**	0.675	**0.682**	V
		V_{IN} = BUF-IN = 1.35V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = -1A to +1A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**0.668**	0.675	**0.682**	V
		V_{IN} = BUF-IN = 1.35V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = -3A to +3A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**0.668**	0.675	**0.682**	V

Unless otherwise specified: V_{CC} = 2.7V to 5.5V; V_{IN} = 0.75V to 5.5V; EN = V_{CC}; C_{OUT} = 150µF + 2x 10µF; OCP_SRC and OCP_SNK = AGND; T_A = 25°C. **Boldface specifications apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at 25°C with exposure at a low dose rate of <10mrad(Si)/s.** (Cont.)

Parameter	Symbol	Test Conditions	Temperature	Min	Typ[1]	Max	Unit
Output Accuracy DDR Configuration (cont.)	V_DDR4	V_{IN} = BUF-IN = 1.2V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = 0A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**0.594**	0.6	**0.606**	V
		V_{IN} = BUF-IN = 1.2V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = -1A to +1A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**0.594**	0.6	**0.606**	V
		V_{IN} = BUF-IN = 1.2V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = -3A to +3A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**0.594**	0.6	**0.606**	V
	BUF3V3	V_{IN} = BUF-IN = 3.3V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = 0A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**1.633**	1.65	**1.667**	V
		V_{IN} = BUF-IN = 3.3V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = -1A to +1A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**1.633**	1.65	**1.667**	V
		V_{IN} = BUF-IN = 3.3V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = -3A to +3A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**1.633**	1.65	**1.667**	V
	BUF1V0	V_{IN} = BUF-IN = 1.0V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = 0A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**0.495**	0.5	**0.505**	V
		V_{IN} = BUF-IN = 1.0V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = -1A to +1A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**0.495**	0.5	**0.505**	V
		V_{IN} = BUF-IN = 1.0V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = -3A to +3A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**0.495**	0.5	**0.505**	V
VCC Dropout Voltage[2]	VCC_DO	I_{OUT} = 3A; V_{OUT} = 3.3V; V_{IN} = 3.6V; V_{CC} = 0.99 x V_{OUT} + VCC_DO; BUF-IN = 1V; EA+ = VREF_INT	-55 to +125°C	-	-	**1.38**	V
VIN-VOUT Dropout Voltage LDO Configuration	VIN_DO	I_{OUT} = 1A; V_{OUT} = V_{IN} - VIN_DO; 2.7V<V_{CC}<5.5V; V_{IN} = 0.5V	-55°C	-	35	50	mV
			+25°C	-	46	60	mV
			+125°C	-	59	70	mV
			+25°C (Post Rad)	-	46	60	mV
		I_{OUT} = 2A; V_{OUT} = V_{IN} - VIN_DO; 2.7V<V_{CC}<5.5V; V_{IN} = 0.5V	-55°C	-	70	00	mV
			+25°C	-	92	110	mV
			+125°C	-	119	140	mV
			+25°C (Post Rad)	-	92	110	mV
		I_{OUT} = 3A; V_{OUT} = V_{IN} - VIN_DO; 2.7V<V_{CC}<5.5V; V_{IN} = 0.5V	-55°C	-	105	130	mV
			+25°C	-	139	170	mV
			+125°C	-	179	210	mV
			+25°C (Post Rad)	-	139	170	mV

Unless otherwise specified: V_{CC} = 2.7V to 5.5V; V_{IN} = 0.75V to 5.5V; EN = V_{CC}; C_{OUT} = 150µF + 2x 10µF; OCP_SRC and OCP_SNK = AGND; T_A = 25°C. **Boldface specifications apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at 25°C with exposure at a low dose rate of <10mrad(Si)/s.** (Cont.)

Parameter	Symbol	Test Conditions	Temperature	Min	Typ[1]	Max	Unit
VIN-VOUT Dropout Voltage DDR Configuration	VIN_{DODDRA}	V_{CC} = 2.75V; BUF-IN = 2.5V; V_{IN} = 1.25V; V_{OUT} = V_{IN} - VIN_{DODDR}; I_{OUT} = 1A	-55°C	-	39	60	mV
			+25°C	-	51	70	mV
			+125°C	-	65	80	mV
			+25°C (Post Rad)	-	51	70	mV
	VIN_{DODDRB}	V_{CC} = 2.75V; BUF-IN = 2.5V; V_{IN} = 1.25V; V_{OUT} = V_{IN} - VIN_{DODDR}; I_{OUT} = 2A	-55°C	-	78	100	mV
			+25°C	-	101	120	mV
			+125°C	-	129	150	mV
			+25°C (Post Rad)	-	101	120	mV
	VIN_{DODDRC}	V_{CC} = 2.75V; BUF-IN = 2.5V; V_{IN} = 1.25V; V_{OUT} = V_{IN} - VIN_{DODDR}; I_{OUT} = 3A	-55°C	-	117	140	mV
			+25°C	-	152	180	mV
			+125°C	-	194	220	mV
			+25°C (Post Rad)	-	152	180	mV
	$VIN_{DODDR2A}$	V_{CC} = 2.7V; BUF-IN = 1.8V; V_{IN} = 0.9V; V_{OUT} = V_{IN} - VIN_{DODDR}; I_{OUT} = 1A	-55°C	-	37	60	mV
			+25°C	-	48	70	mV
			+125°C	-	62	80	mV
			+25°C (Post Rad)	-	48	70	mV

Unless otherwise specified: V_{CC} = 2.7V to 5.5V; V_{IN} = 0.75V to 5.5V; EN = V_{CC}; C_{OUT} = 150µF + 2x 10µF; OCP_SRC and OCP_SNK = AGND; T_A = 25°C. **Boldface specifications apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at 25°C with exposure at a low dose rate of <10mrad(Si)/s.** (Cont.)

Parameter	Symbol	Test Conditions	Temperature	Min	Typ[1]	Max	Unit
VIN-VOUT Dropout Voltage DDR Configuration	$VIN_{DODDR2B}$	V_{CC} = 2.7V; BUF-IN = 1.8V; V_{IN} = 0.9V; V_{OUT} = V_{IN} - VIN_{DODDR}; I_{OUT} = 2A	-55°C	-	75	100	mV
			+25°C	-	97	120	mV
			+125°C	-	124	150	mV
			+25°C (Post Rad)	-	97	120	mV
	$VIN_{DODDR2C}$	V_{CC} = 2.7V; BUF-IN = 1.8V; V_{IN} = 0.9V; V_{OUT} = V_{IN} - VIN_{DODDR}; I_{OUT} = 3A	-55°C	-	111	140	mV
			+25°C	-	145	180	mV
			+125°C	-	187	220	mV
			+25°C (Post Rad)	-	145	180	mV
	$VIN_{DODDR3A}$	V_{CC} = 2.7V; BUF-IN = 1.5V; V_{IN} = 0.75V; V_{OUT} = V_{IN} - VIN_{DODDR}; I_{OUT} = 1A	-55°C	-	36	60	mV
			+25°C	-	48	70	mV
			+125°C	-	62	80	mV
			+25°C (Post Rad)	-	48	70	mV
	$VIN_{DODDR3B}$	V_{CC} = 2.7V; BUF-IN = 1.5V; V_{IN} = 0.75V; V_{OUT} = V_{IN} - VIN_{DODDR}; I_{OUT} = 2A	-55°C	-	73	100	mV
			+25°C	-	96	120	mV
			+125°C	-	123	150	mV
			+25°C (Post Rad)	-	96	120	mV
	$VIN_{DODDR3C}$	V_{CC} = 2.7V; BUF-IN = 1.5V; V_{IN} = 0.75V; V_{OUT} = V_{IN} - VIN_{DODDR}; I_{OUT} = 3A	-55°C	-	110	140	mV
			+25°C	-	144	180	mV
			+125°C	-	185	220	mV
			+25°C (Post Rad)	-	144	180	mV
	$VIN_{DODDR3LA}$	V_{CC} = 2.7V; BUF-IN = 1.35V; V_{IN} = 0.675V; V_{OUT} = V_{IN} - VIN_{DODDR}; I_{OUT} = 1A	-55°C	-	36	60	mV
			+25°C	-	48	70	mV
			+125°C	-	61	80	mV
			+25°C (Post Rad)	-	48	70	mV
	$VIN_{DODDR3LB}$	V_{CC} = 2.7V; BUF-IN = 1.35V; V_{IN} = 0.675V; V_{OUT} = V_{IN} - VIN_{DODDR}; I_{OUT} = 2A	-55°C	-	73	100	mV
			+25°C	-	95	120	mV
			+125°C	-	123	150	mV
			+25°C (Post Rad)	-	95	120	mV

Unless otherwise specified: V_{CC} = 2.7V to 5.5V; V_{IN} = 0.75V to 5.5V; EN = V_{CC}; C_{OUT} = 150µF + 2x 10µF; OCP_SRC and OCP_SNK = AGND; T_A = 25°C. **Boldface specifications apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at 25°C with exposure at a low dose rate of <10mrad(Si)/s.** (Cont.)

Parameter	Symbol	Test Conditions	Temperature	Min	Typ[1]	Max	Unit
VIN-VOUT Dropout Voltage DDR Configuration	$VIN_{DODDR3LC}$	V_{CC} = 2.7V; BUF-IN = 1.35V; V_{IN} = 0.675V; V_{OUT} = V_{IN} - VIN_{DODDR}; I_{OUT} = 3A	-55°C	-	109	140	mV
			+25°C	-	143	180	mV
			+125°C	-	184	220	mV
			+25°C (Post Rad)	-	143	180	mV
	$VIN_{DODDR4A}$	V_{CC} = 2.7V; BUF-IN = 1.2V; V_{IN} = 0.6V; V_{OUT} = V_{IN} - VIN_{DODDR}; I_{OUT} = 1A	-55°C	-	36	60	mV
			+25°C	-	47	70	mV
			+125°C	-	61	80	mV
			+25°C (Post Rad)	-	47	70	mV
	$VIN_{DODDR4B}$	V_{CC} = 2.7V; BUF-IN = 1.2V; V_{IN} = 0.6V; V_{OUT} = V_{IN} - VIN_{DODDR}; I_{OUT} = 2A	-55°C	-	72	100	mV
			+25°C	-	95	120	mV
			+125°C	-	122	150	mV
			+25°C (Post Rad)	-	95	120	mV
	$VIN_{DODDR4C}$	V_{CC} = 2.7V; BUF-IN = 1.2V; V_{IN} = 0.6V; V_{OUT} = V_{IN} - VIN_{DODDR}; I_{OUT} = 3A	-55°C	-	108	140	mV
			+25°C	-	142	180	mV
			+125°C	-	183	220	mV
			+25°C (Post Rad)	-	142	180	mV
Adjustable OCP; Sourcing	$OCP+_{HIGH}$	V_{OUT} = 0V; V_{IN} = 2V; V_{CC} = 2.7V; $R_{OCP-SRC}$ = 3kΩ	-55 to +125°C	**2.7**	3.0	**3.5**	A
	$OCP+_{LOW}$	V_{OUT} = 0V; V_{IN} = 2V; V_{CC} = 2.7V; $R_{OCP-SRC}$ = 30kΩ	-55 to +125°C	**0.15**	0.3	**0.6**	A
Adjustable OCP; Sinking	$OCP-_{HIGH}$	V_{OUT} = 1V; V_{IN} = 2V; V_{CC} = 2.7V; $R_{OCP-SNK}$ = 3kΩ	-55 to +125°C	**-3.5**	-3.0	**-2.7**	A
	$OCP-_{LOW}$	V_{OUT} = 1V; V_{IN} = 2V; V_{CC} = 2.7V; $R_{OCP-SNK}$ = 30kΩ	-55 to +125°C	**-0.6**	-0.3	**-0.15**	A
Internal OCP; Sourcing	OCP+	V_{OUT} = 0V; V_{IN} = 2V; V_{CC} = 2.7V; $R_{OCP-SRC}$ = 0Ω	-55 to +125°C	**3.3**	4	**5.0**	A
Internal OCP; Sinking	OCP-	V_{OUT} = 1V; V_{IN} = 2V; V_{CC} = 2.7V; $R_{OCP-SNK}$ = 0Ω	-55 to +125°C	**-5.0**	-4.1	**-3.3**	A
Over-Temperature Protection; Rising	OTP_R	-	-	-	165	-	°C
Over-Temperature Recovery; Hysteresis	OTP_H	-	-	-	10	-	°C
Buffered Reference							
Buffer Input Voltage	BUF-IN	-	-55 to +125°C	**1.0**	-	**3.3**	V
Buffer Input Resistance	BUF_R	BUF-IN = 1V	-55 to +125°C	**1.5**	-	**2.5**	MΩ
Buffer Input UVLO; Rising	BUF_{UVLOR}	V_{CC} = 2.7V; V_{IN} = 3.3V; CONFIG = V_{CC}	-55 to +125°C	**0.75**	0.78	**0.82**	V
Buffer Input UVLO; Falling	BUF_{UVLOF}	V_{CC} = 2.7V; V_{IN} = 3.3V; CONFIG = V_{CC}	-55 to +125°C	**0.72**	0.76	**0.78**	V

Unless otherwise specified: V_{CC} = 2.7V to 5.5V; V_{IN} = 0.75V to 5.5V; EN = V_{CC}; C_{OUT} = 150µF + 2x 10µF; OCP_SRC and OCP_SNK = AGND; T_A = 25°C. **Boldface specifications apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at 25°C with exposure at a low dose rate of <10mrad(Si)/s.** (Cont.)

Parameter	Symbol	Test Conditions	Temperature	Min	Typ[1]	Max	Unit
Buffer Input UVLO; Hysteresis	BUF_{UVLOH}	-	-55 to +125°C	**10**	23	**50**	mV
Buffer Output Voltage	BUF-OUT	As a percentage of BUF-IN; 1.0V < BUF-IN < 3.3V; -10mA < $I_{BUF-OUT}$ < 10mA	-55 to +125°C	**49.5**	50	**50.5**	%
BUF-OUT Voltage Tolerance to BUF-IN	$BUFOUT_{TOL}$	1.0V < BUF-IN < 3.3V; -10mA < $I_{BUF-OUT}$ < 10mA	-55 to +125°C	**-5**	-	**5**	mV
Buffer Output Current Limit; Sourcing	BUF_{OUT+}	BUF-OUT = 0V; V_{IN} = V_{CC} = 2.7V; BUF-IN = 1.2V; V_{IN} = V_{CC} = 5.5V; BUF-IN = 3.3V	-55 to +125°C	**15**	20	**27**	mA
Buffer Output Current Limit; Sinking	BUF_{OUT-}	BUF-OUT = V_{CC}; V_{IN} = V_{CC} = 2.7V; BUF-IN = 1.2V; V_{IN} = V_{CC} = 5.5V; BUF-IN = 3.3V	-55 to +125°C	**-27**	-20	**-15**	mA
ENABLE Pin							
Enable Threshold; Rising	EN_R	VREF_INT rising (200mV); V_{IN} = V_{CC} = 3.3V	-55 to +125°C	**1.05**	1.1	**1.15**	V
Enable Threshold; Falling	EN_F	VREF_INT falling (200mV); V_{IN} = V_{CC} = 3.3V	-55 to +125°C	**0.9**	0.98	**1.1**	V
Enable Threshold; Hysteresis	EN_H	-	-55 to +125°C	**10**	128	**160**	mV
Enable Propagation Delay; Rising	EN_PDR	EN = 0V to 5V; EN rising edge to VREF_INT = 450mV; V_{IN} = V_{CC} = 3.3V; C_{VREF_INT} = 100nF	-55 to +125°C	**60**	105	**130**	µs
Enable Propagation Delay; Falling	EN_PDF	EN = 5V to 0V; EN falling edge to VREF_INT = 450mV; V_{IN} = V_{CC} = 3.3V; C_{VREF_INT} = 100nF	-55 to +125°C	**4**	6.2	**8**	µs
Enable Input Leakage	I_EN	EN = 5.5V	-55 to +125°C	-	0.5	**1**	µA
Soft-Start							
Soft-Start Current	I_SS	SS = 0V; V_{IN} = V_{CC} = 3.3V	-55 to +125°C	**17**	20	**25**	µA
Soft-Start Done Threshold	SS_Done	V_{IN} = V_{CC} = 3.3V; PG = 2V	-55 to +125°C	**1.65**	2.08	**2.6**	V
Soft-Start Clamp Voltage	SS_Clamp	V_{IN} = V_{CC} = 3.3V	-55 to +125°C	**2.5**	3	**3.5**	V
SS Pin Discharge Resistance	R_SS	SS = 1V; EN = 0; V_{IN} = V_{CC} = 3.3V	-55 to +125°C	**8**	15	**22**	Ω

Unless otherwise specified: V_{CC} = 2.7V to 5.5V; V_{IN} = 0.75V to 5.5V; EN = V_{CC}; C_{OUT} = 150µF + 2x 10µF; OCP_SRC and OCP_SNK = AGND; T_A = 25°C. **Boldface specifications apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at 25°C with exposure at a low dose rate of <10mrad(Si)/s.** (Cont.)

Parameter	Symbol	Test Conditions	Temperature	Min	Typ[1]	Max	Unit
Power Good							
PG Overvoltage Threshold; Rising	PG_OVR	V_{IN} = V_{CC} = 3.3V; EA- as a % of EA+; EA+ = 0.5V (Ramp EA-, PG = 2V falling, R_{PG} =10kΩ)	-55 to +125°C	**107**	111	**114**	%
PG Overvoltage Hysteresis	PG_OVH	V_{IN} = V_{CC} = 3.3V; EA- as a % of EA+; EA+ = 0.5V	-55 to +125°C	**1.5**	3.9	**5**	%
PG Undervoltage Threshold; Falling	PG_UVF	V_{IN} = V_{CC} = 3.3V; EA- as a % of EA+; EA+ = 0.5V (Ramp EA-, PG = 2V falling, R_{PG} =10kΩ)	-55 to +125°C	**87**	89	**91**	%
PG Undervoltage Hysteresis	PG_UVH	V_{IN} = V_{CC} = 3.3V; EA- as a % of EA+; EA+ = 0.5V	-55 to +125°C	**1.5**	4.2	**5**	%
PG Output Low Voltage	PG_LOW	I_PG = 1mA; V_{IN} = V_{CC} = 2.7V; EN = 0V	-55 to +125°C	-	0.03	**0.4**	V
PG Leakage Current	PG_LEAK	V_{IN} = V_{CC} =5.5V; PG = 5.5V; V_{OUT} in regulation	-55 to +125°C	-	-	**0.01**	µA
PG Delay; Rising	PG_PDR	V_{IN} = V_{CC} = 2.7V; EA- rising edge (0.5V) to PG Rising (89% of V_{CC})	-55 to +125°C	**5**	6.4	**8**	µs
PG Delay; Falling	PG_PDF	V_{IN} = V_{CC} = 2.7V; EA- falling edge (0.4V) to PG Falling (89% of V_{CC})	-55 to +125°C	**0.75**	1.04	**1.25**	µs
CONFIG Pin - VOUT and BUF-OUT Discharge							
CONFIG Pin Threshold	CFIG_R	V_{IN} = V_{CC} = 2.7V; EN=0V; Rising Threshold when V_{OUT} falls to 0.8V	-55 to +125°C	**1.05**	1.1	**1.15**	V
CONFIG Pin Hysteresis	CFIG_H	-	-55 to +125°C	**90**	106	**140**	mV
BUF-OUT Discharge Resistance	$BUF\text{-}OUT_{_R}$	BUF-IN = 0.5V; V_{IN} = V_{CC} = CONFIG = 2.7V; BUF-OUT sinking current = 10mA	-55 to +125°C	**9**	17	**29**	Ω
VOUT Discharge Resistance	VOUT_R	EN = 0V; V_{IN} = V_{CC} = CONFIG = 2.7V; VOUT sinking current = 20mA	-55 to +125°C	**3**	6.5	**12**	Ω

1. Typical values are at 25°C and are not guaranteed.
2. VCC dropout is defined by the difference V_{CC}-V_{OUT} where the regulated V_{OUT} voltage produces a 1% drop in V_{OUT} from its nominal value established when V_{CC}-V_{OUT}>V_{CC_DO}.

3.4.2 AC Electrical Specifications

Unless otherwise specified: EN = V_{CC}; C_{OUT} = 2x150µF + 0.1µF; T_A = 25°C.

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
VOUT PSRR						
VCC PSRR; Sourcing	$PSSR_{VCC+}$	V_{CC} = 3.3V; V_{IN} = 1.5V; V_{OUT} = 0.5V; I_{OUT} = 3A V_{RIPPLE}(VCC) = 150mV_{P-P}; Frequency = 100kHz	-	66	-	dB
VCC PSRR; Sinking	$PSSR_{VCC-}$	V_{CC} = 3.3V; V_{IN} = 1.5V; V_{OUT} = 0.5V; I_{OUT} = -3A V_{RIPPLE}(VCC) = 150mV_{P-P}; Frequency = 100kHz	-	71	-	dB
VIN PSRR; Sourcing	$PSSR_{VIN+}$	V_{CC} = 3.3V; V_{IN} = 1.5V; V_{OUT} = 0.5V; I_{OUT} = 3A V_{RIPPLE}(VIN) = 150mV_{P-P}; Frequency = 100kHz	-	60	-	dB

Unless otherwise specified: EN = V_{CC}; C_{OUT} = 2x150µF + 0.1µF; T_A = 25°C. **(Cont.)**

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
VIN PSRR; Sinking	$PSSR_{VIN-}$	V_{CC} = 3.3V; V_{IN} = 1.5V; V_{OUT} = 0.5V; I_{OUT} = -3A V_{RIPPLE}(VIN) = 150mV_{P-P}; Frequency = 100kHz	-	87	-	dB
VOUT Noise						
VOUT RMS Noise		V_{CC} = 3.3V; V_{IN} = 1.5V; V_{OUT} = 0.5V; I_{OUT} = 3A; BW = 10Hz < f < 100kHz; EA- = OUT	-	22.8	-	μV_{RMS}

1. Typical values are at 25°C and are not guaranteed.

3.5 Operation Burn-In Deltas

Table 1. Burn-In Deltas

Parameter	Test Conditions	Min	Max	Unit
VCC Enabled Supply Current	VCC = 5.5V, VIN = 5.5V, EA+ = VREF; BUF-IN = 1V; -3A < IOUT < 3A	-0.645	0.645	mA
VREF Voltage	2.7V < VCC < 5.5V; 2.7V < VIN < 5.5V, VOUT = 0.5V, IOUT = 1mA	-1	1	mV
Error Amplifier VOS	(EA- to EA+); 2.7V < VCC < 5.5V; 0.75V < VIN < 5.5V; EA+ = VREF; -3A < IOUT < 3A	-0.88	0.88	mV
VIN-VOUT Dropout Voltage LDO Configuration	2.7V < VCC < 5.5V; VIN = 0.5V; VOUT = VIN-VIN_DO; IOUT = 3A	-14.5	14.5	mV
VIN-VOUT Dropout Voltage DDR Configuration	VCC = 2.75V; BUF-IN = 2.5V; VIN = 1.25V; VOUT = VIN - VINDODDR; IOUT = 3A	-15.5	15.5	mV
Buffer Output Voltage	As a percentage of BUF-IN; 1.0V < BUF-IN < 3.3V; -10mA < IBUF-OUT < 10mA	-0.1	0.1	%

4. Typical Performance Graphs

V_{CC} = 3.3V, V_{IN} = 3.3V, C_{OUT} = 2x150µF Tantalum, 0.1µF ceramic, C_{SS} = 10nF, C_{BUF-IN} = 1µF, R_{BUF-IN} = 1kΩ, T_A = +25°C, unless otherwise stated.

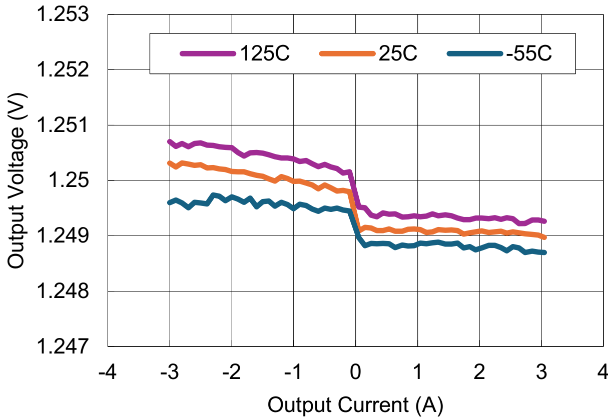


Figure 7. Output Voltage vs Output Current; DDR (BUF-IN = 2.5V)

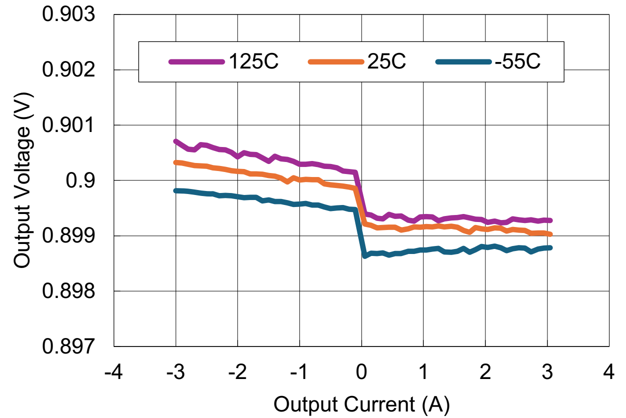


Figure 8. Output Voltage vs Output Current; DDR2 (BUF-IN = 1.8V)

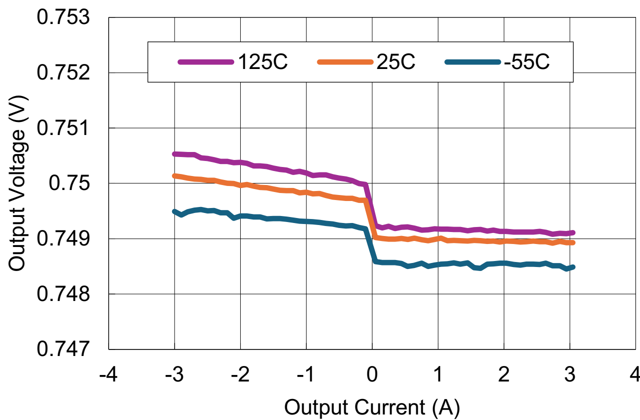


Figure 9. Output Voltage vs Output Current; DDR3 (BUF-IN = 1.5V)

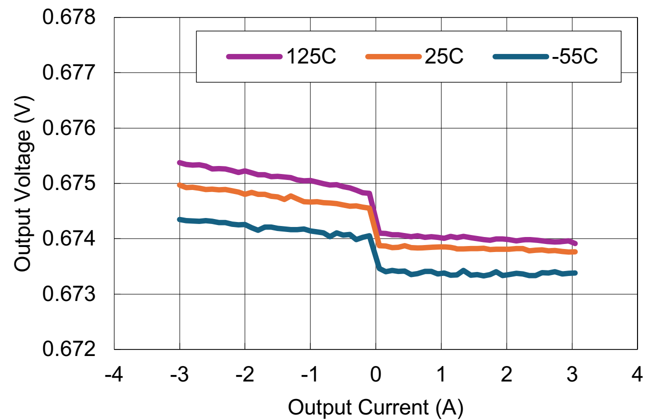


Figure 10. Output Voltage vs Output Current; DDR3L (BUF-IN = 1.35V)

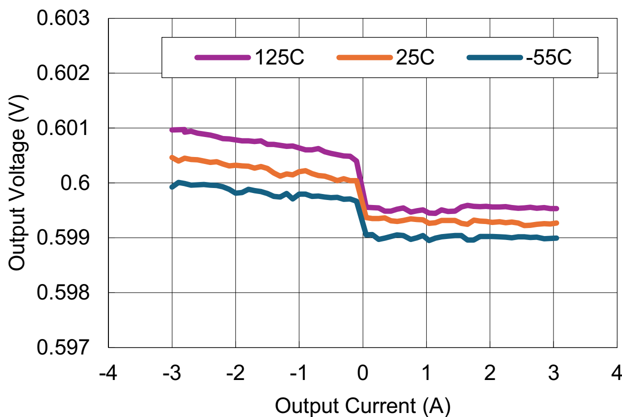


Figure 11. Output Voltage vs Output Current; DDR4 (BUF-IN = 1.2V)

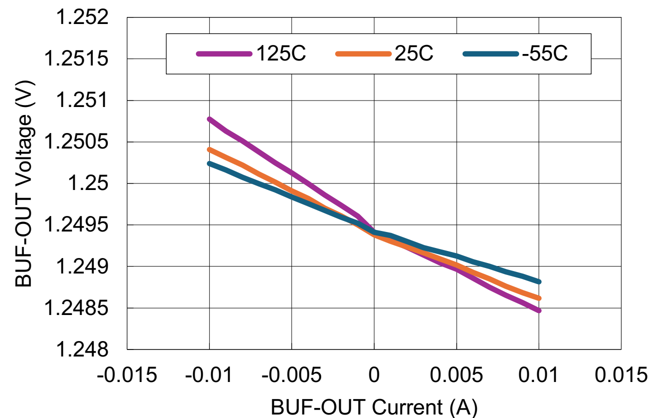


Figure 12. BUF-OUT Voltage vs BUF-OUT Current; DDR (BUF-IN = 2.5V)

V_{CC} = 3.3V, V_{IN} = 3.3V, C_{OUT} = 2x150µF Tantalum, 0.1µF ceramic, C_{SS} = 10nF, $C_{BUF\text{-}IN}$ = 1µF, $R_{BUF\text{-}IN}$ = 1kΩ, T_A = +25°C, unless otherwise stated. (Cont.)

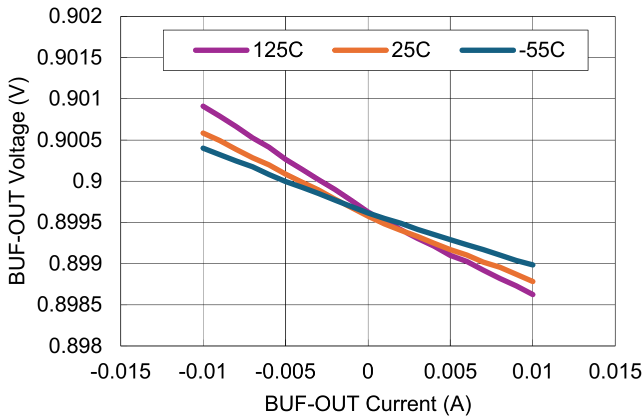


Figure 13. BUF-OUT Voltage vs BUF-OUT Current; DDR2 (BUF-IN = 1.8V)

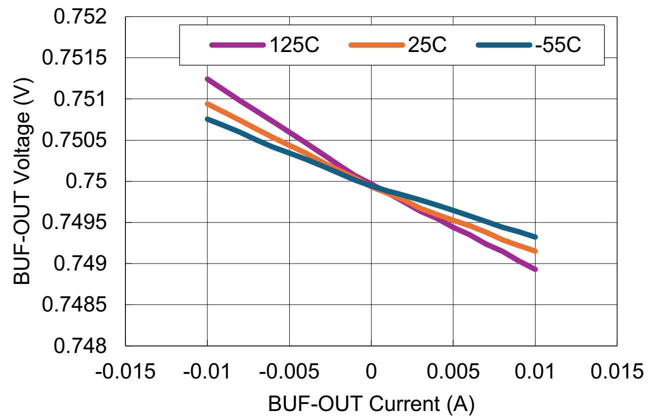


Figure 14. BUF-OUT Voltage vs BUF-OUT Current; DDR3 (BUF-IN = 1.5V)

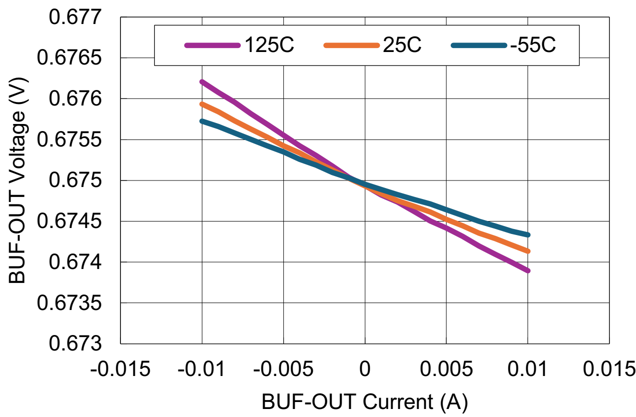


Figure 15. BUF-OUT Voltage vs BUF-OUT Current; DDR3L (BUF-IN = 1.35V)

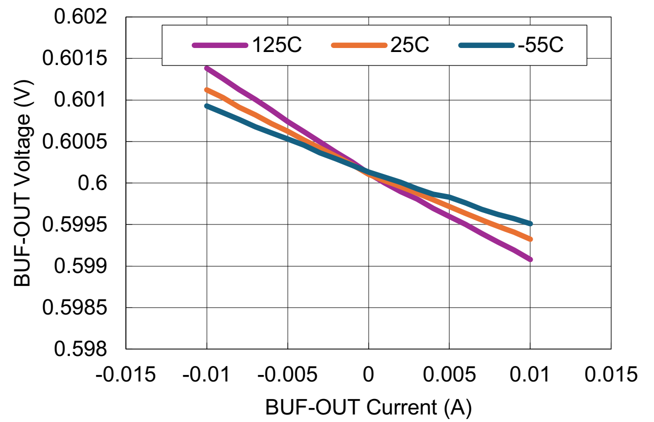


Figure 16. BUF-OUT Voltage vs BUF-OUT Current; DDR4 (BUF-IN = 1.2V)

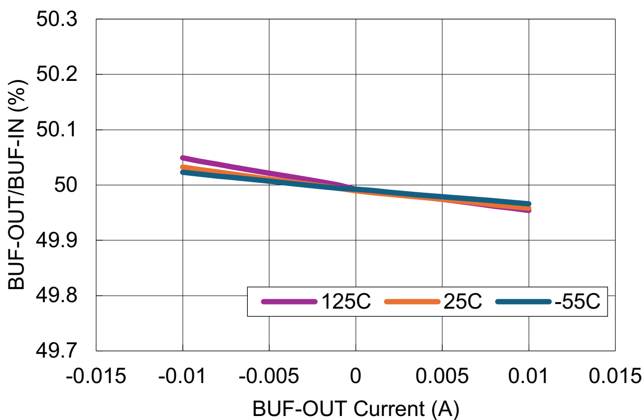


Figure 17. BUF-OUT/BUF-IN Percentage vs BUF-OUT Current; DDR (BUF-IN = 2.5V)

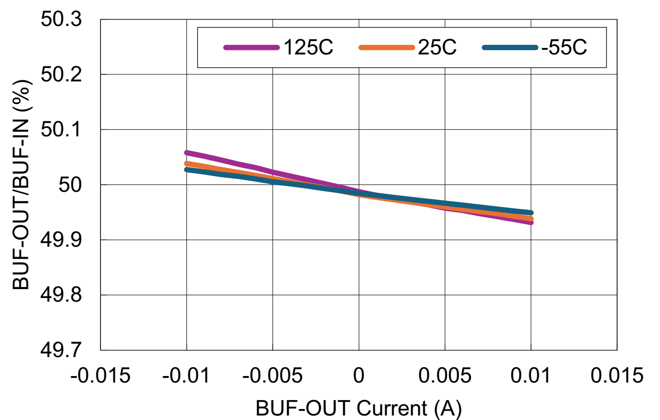


Figure 18. BUF-OUT/BUF-IN Percentage vs BUF-OUT Current; DDR2 (BUF-IN = 1.8V)

V_{CC} = 3.3V, V_{IN} = 3.3V, C_{OUT} = 2x150µF Tantalum, 0.1µF ceramic, C_{SS} = 10nF, $C_{BUF\text{-}IN}$ = 1µF, $R_{BUF\text{-}IN}$ = 1kΩ, T_A = +25°C, unless otherwise stated. (Cont.)

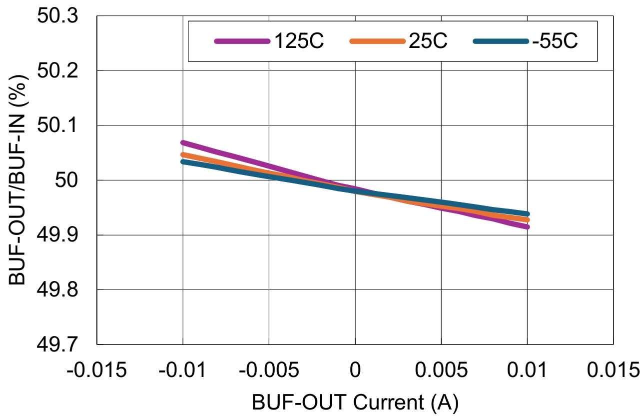


Figure 19. BUF-OUT/BUF-IN Percentage vs BUF-OUT Current; DDR3 (BUF-IN = 1.5V)

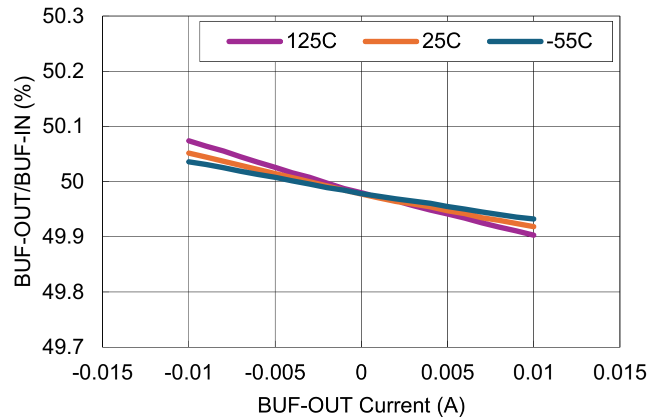


Figure 20. BUF-OUT/BUF-IN Percentage vs BUF-OUT Current; DDR3L (BUF-IN = 1.35V)

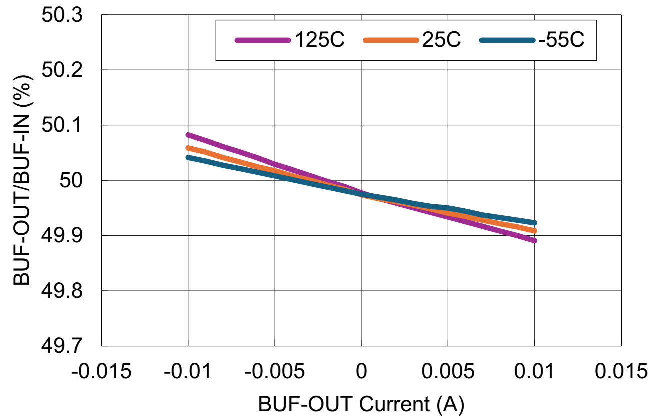


Figure 21. BUF-OUT/BUF-IN Percentage vs BUF-OUT Current; DDR4 (BUF-IN = 1.2V)

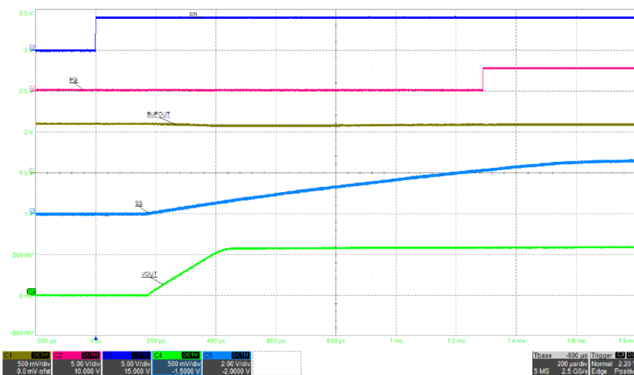


Figure 22. Startup with Soft-Start; DDR Mode (V_{IN} = BUF-IN = 1.2V, V_{CC} = 2.7V, EA+ = BUF-OUT, V_{OUT} = 0.6V, I_{OUT} = 0A)

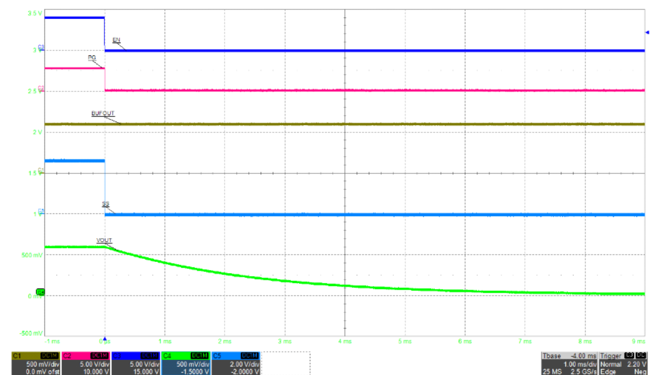


Figure 23. Shutdown; DDR Mode, Config High (V_{IN} = BUF-IN = 1.2V, V_{CC} = 2.7V, EA+ = BUF-OUT, V_{OUT} = 0.6V, I_{OUT} = 0A)

V_{CC} = 3.3V, V_{IN} = 3.3V, C_{OUT} = 2x150µF Tantalum, 0.1µF ceramic, C_{SS} = 10nF, C_{BUF-IN} = 1µF, R_{BUF-IN} = 1kΩ, T_A = +25°C, unless otherwise stated. (Cont.)

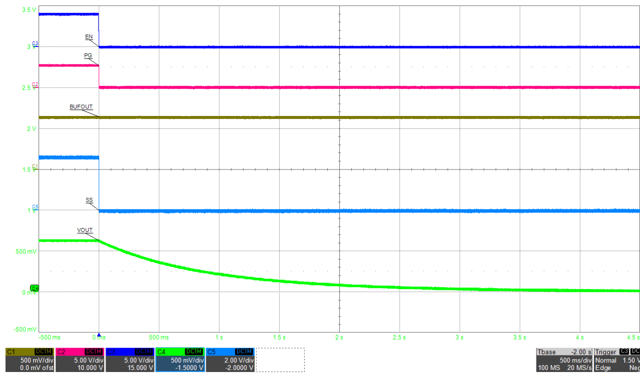


Figure 24. Shutdown; DDR Mode, Config Low (V_{IN} = BUF-IN = 1.2V, V_{CC} = 2.7V, EA+ = BUF-OUT, V_{OUT} = 0.6V, I_{OUT} = 0A)

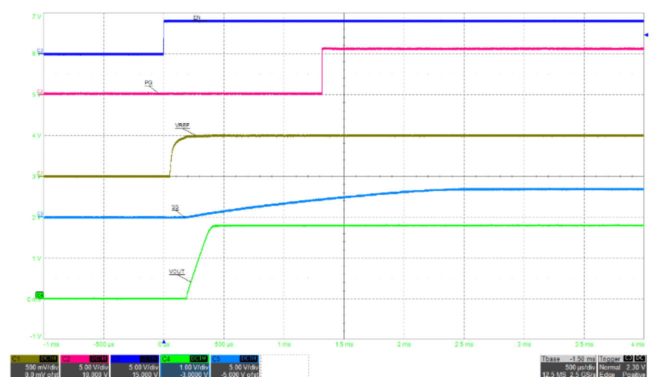


Figure 25. Startup with Soft-Start; LDO Mode (V_{IN} = 3.6V, V_{CC} = 5.5V, EA+ = VREF_INT, V_{OUT} = 1.8V, I_{OUT} = 0A)

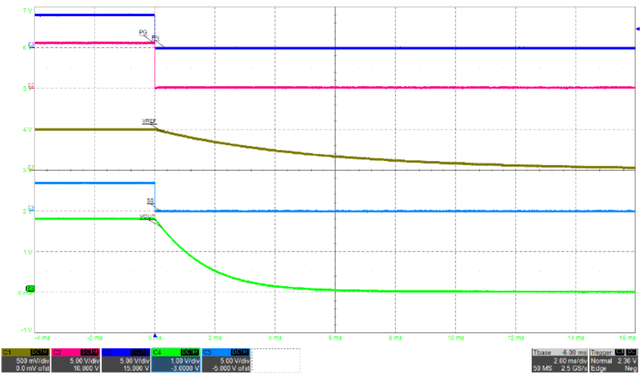


Figure 26. Shutdown; LDO Mode, Config High (V_{IN} = 3.6V, V_{CC} = 5.5V, EA+ = VREF_INT, V_{OUT} = 1.8V, I_{OUT} = 0A)

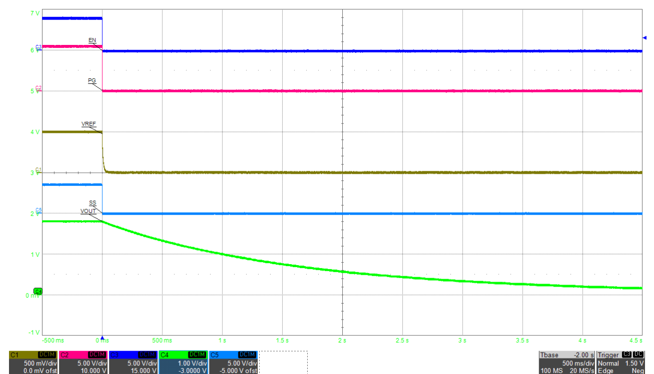


Figure 27. Shutdown; LDO Mode, Config Low (V_{IN} = 3.6V, V_{CC} = 5.5V, EA+ = VREF_INT, V_{OUT} = 1.8V, I_{OUT} = 0A)

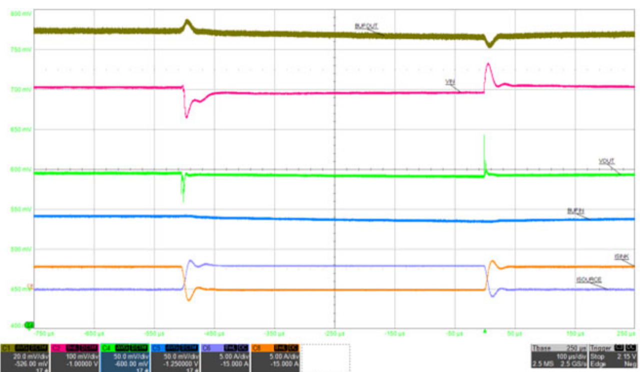


Figure 28. Load Transient Response; DDR4 (V_{IN} = BUF-IN = 1.2V, V_{CC} = 2.7V, Load step = -3A to +3A)

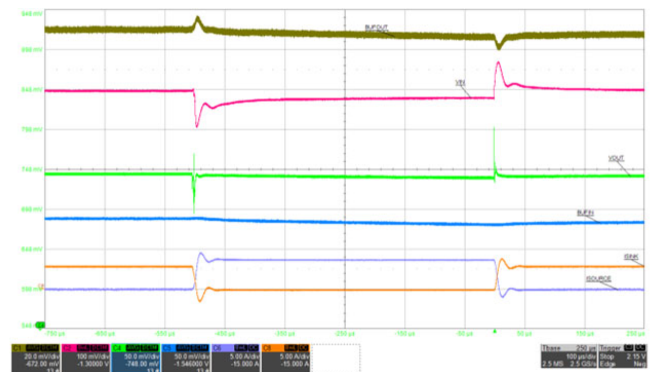


Figure 29. Load Transient Response; DDR3 (V_{IN} = BUF-IN = 1.5V, VCC = 2.7V, EA+ = BUF-OUT. Load Step = -3A to +3A)

V_{CC} = 3.3V, V_{IN} = 3.3V, C_{OUT} = 2x150µF Tantalum, 0.1µF ceramic, C_{SS} = 10nF, C_{BUF-IN} = 1µF, R_{BUF-IN} = 1kΩ, T_A = +25°C, unless otherwise stated. (Cont.)

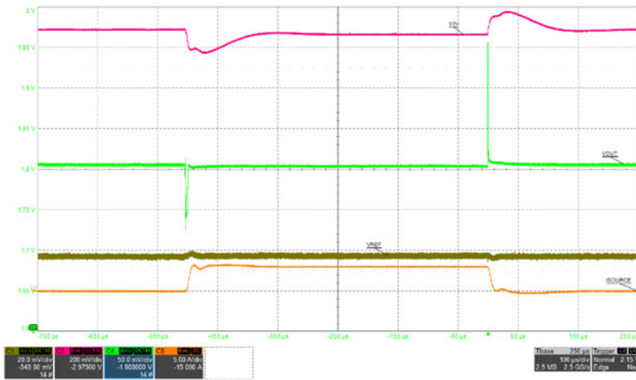


Figure 30. Load Transient Response; 1.8V LDO (V_{IN} = 3.6V, V_{CC} = 5.5V, EA+ = VREF_INT, Load Step = 0 to +3A)

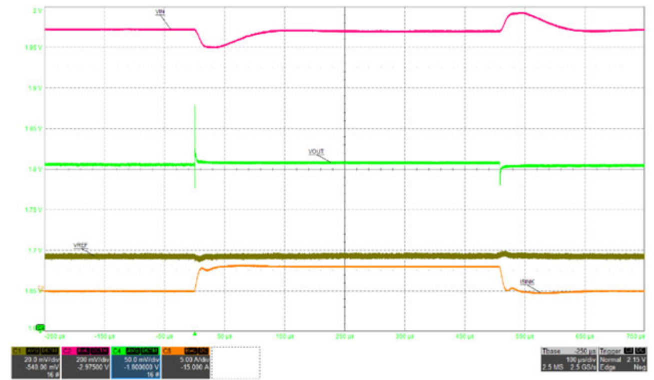


Figure 31. Load Transient Response; 1.8V LDO (V_{IN} = 3.6V, V_{CC} = 5.5V, EA+ = VREF_INT, Load Step = 0A to -3A)

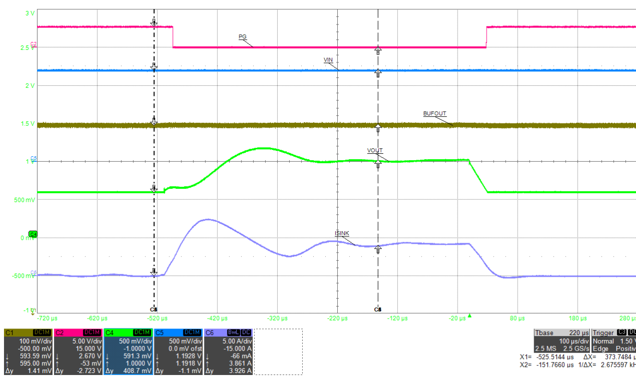


Figure 32. Overcurrent Limit Response; DDR4 - Sinking (V_{IN} = BUF-IN = 1.2V, V_{CC} = 2.7V)

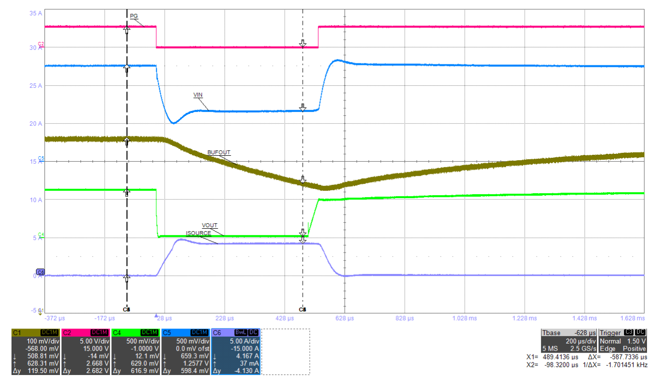


Figure 33. Overcurrent Limit Response; DDR4 - Sourcing (V_{IN} = BUF-IN = 1.2V, V_{CC} = 2.7V)

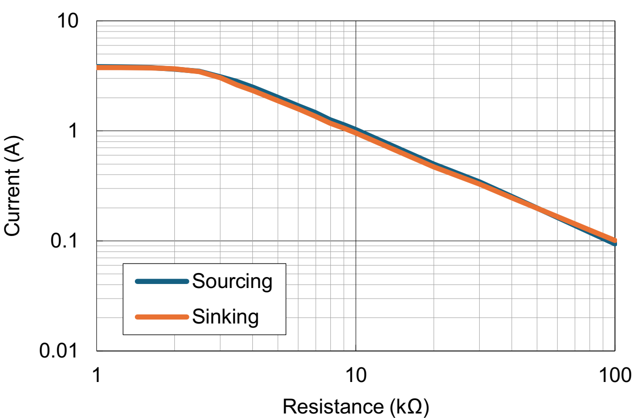


Figure 34. Overcurrent Protection Limit vs OCP Resistor

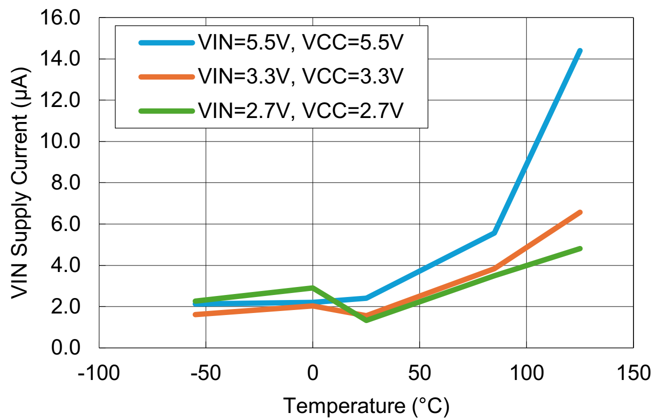


Figure 35. VIN Supply Current (EN = V_{CC}, EA+ = VREF_INT, V_{OUT} = 0.5V, I_{OUT} = 0A)

V_{CC} = 3.3V, V_{IN} = 3.3V, C_{OUT} = 2x150µF Tantalum, 0.1µF ceramic, C_{SS} = 10nF, C_{BUF-IN} = 1µF, R_{BUF-IN} = 1kΩ, T_A = +25°C, unless otherwise stated. (Cont.)

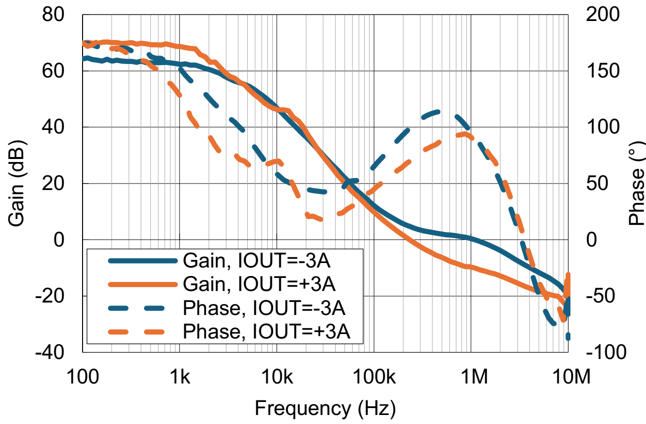


Figure 36. Bode Plot; DDR4 (V_{IN} = BUF = IN = 1.2V, V_{CC} = 3.3V, EA+ = BUF-OUT)

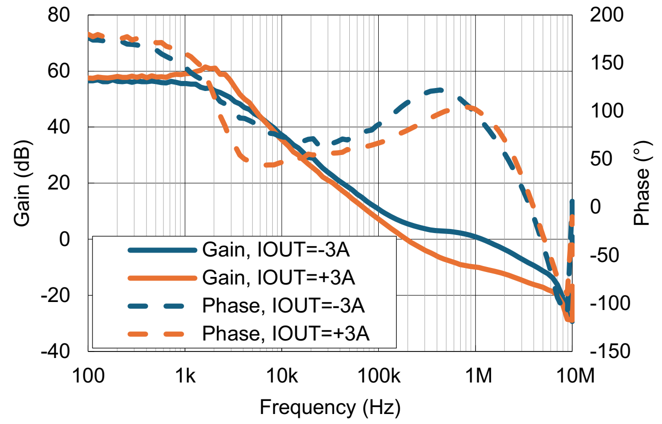


Figure 37. Bode Plot; 1.2V LDO (V_{IN} = 3.3V, V_{CC} = 3.3V, EA+ = VREF_INT, C_{OUT} = 1×330µF)

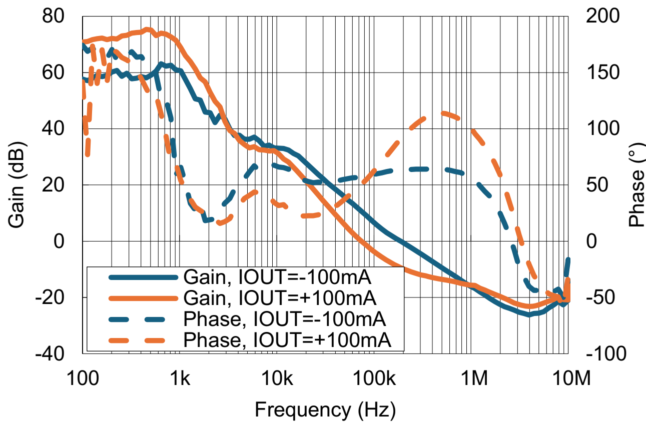


Figure 38. Bode Plot; DDR4 Light Load (V_{IN} = BUF = IN = 1.2V, V_{CC} = 3.3V, EA+ = BUF-OUT)

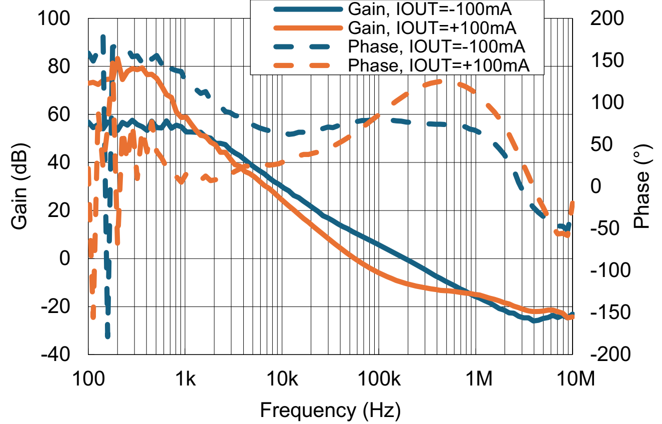


Figure 39. Bode Plot; 1.2V LDO Light Load (V_{IN} = 3.3V, V_{CC} = 3.3V, EA+ = VREF_INT, C_{OUT} = 1×330µF)

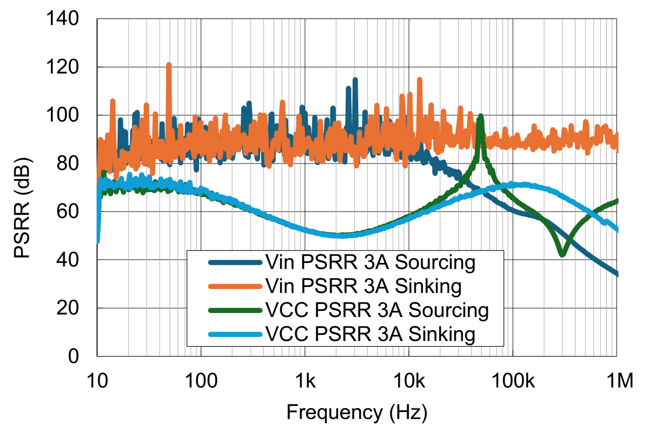


Figure 40. PSRR; 0.5V LDO (V_{IN} = 1.5V, V_{CC} = 3.3V, V_{OUT} = 0.5V)

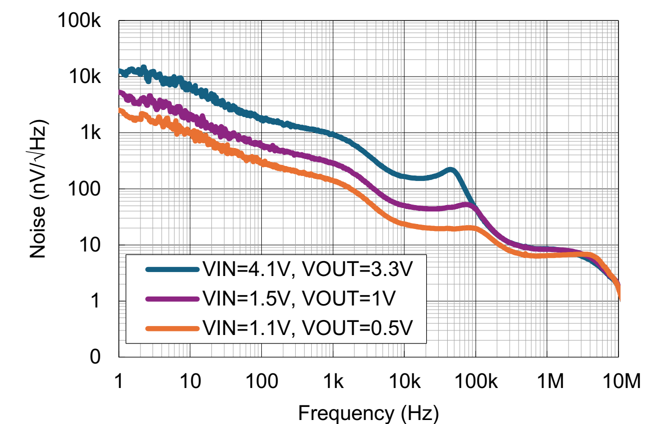


Figure 41. Noise; LDO Mode (V_{CC} = 2.7V, or 5V for V_{OUT} = 3.3V, I_{OUT} = 1A Sourcing)

5. Functional Description

The ISL75055SLH is a radiation hardened 0.75V to 5.5V input, 3A sourcing and sinking low dropout linear regulator designed for powering the VTT termination rail of DDR memory modules or as a high performance general purpose point-of-load regulator. A buffered reference amplifier provides an accurate VREF reference supply for the DDR. Individual adjustable overcurrent protection (OCP) for sourcing and sinking allows the current limit of the LDO to be configured down to 300mA.

The ISL75055SLH features external error amplifier inputs to set VDDQ/2 as the reference voltage in DDR applications. It also features an internal 0.5V reference for standard LDO applications. Separate VCC bias and LDO VIN pins, combined with a very low dropout allows minimal internal losses while maintaining highly accurate output regulation.

5.1 LDO Architecture

The ISL75055SLH LDO provides both sourcing and sinking capabilities through the implementation of an NMOS power stage. The device is capable of 3A sourcing and 3A sinking for VTT termination rails in DDR memory. Highly accurate output voltage regulation is made possible through a low offset voltage error amplifier with a dead band of only 600µV. This makes the ISL75055SLH ideal for VTT rails in DDR4 applications with stringent output voltage specs.

The error amplifier achieves very low dead band crossover and achieves very fast transition times when moving between sourcing and sinking regulation, which results in a faster transient response and reduces the output capacitance required. For configurations where the error amplifier is operating with unity gain, such as DDR mode, the dead band is 600µV typical. For standard LDO applications, the dead band is amplified with V_{OUT}/0.5V ratio due to feedback gain.

The LDO also features an internal buffer that is accessible using the BUF-IN and BUF-OUT pins. This buffer provides a fixed output of BUF-IN/2 to generate the VTT reference voltage of VDDQ/2 in DDR applications.

An internal 500mV voltage reference is also implemented to allow for the flexibility required in programming the output voltage for standard LDO applications.

Separate from the main LDO input VIN, a VCC bias rail powers the gate drive and internal circuitry enabling the LDO to achieve very low dropout. The VIN to VOUT and VCC to VOUT headroom determine the regulator dropout voltage.

5.2 Error Amplifier Inputs

The ISL75055SLH provides pins for both the inverting (EA-) and non-inverting (EA+) inputs to the error amplifier. The dedicated EA+ pin configures the part for either DDR or standard LDO configurations. In the DDR configuration, BUF-OUT is used as the input to EA+, providing BUF-IN/2 as the reference voltage. In the standard LDO configuration, VREF_INT is used as the input to EA+, providing a fixed 500mV reference voltage.

The EA- pin is used for the output voltage feedback that is compared to the reference voltage on EA+. For the DDR configuration, EA- should be connected directly to VOUT at the required output voltage regulation sense point. For standard LDO configurations where V_{OUT} = 0.5V, EA- is similarly connected directly to VOUT. For all other LDO mode output voltages greater than 0.5V, the output voltage is set by a feedback resistor divider between VOUT, EA-, and AGND. Feedback resistor selection is described in more detail in LDO Output Voltage.

5.3 LDO Fault Protection

The ISL75055SLH features protection for undervoltage, overvoltage, over-temperature, and overcurrent.

Both the VCC and VIN inputs are protected by undervoltage lockout (UVLO). If both inputs are not above their respective UVLO thresholds of 2.62V typical for VCC rising and 472mV typical for VIN rising, the LDO is disabled.

Output undervoltage and overvoltage protection is implemented by monitoring the EA- voltage as a percentage of EA+. When the EA- voltage rises above PG overvoltage threshold or falls below the PG undervoltage threshold, PG is pulled low.

Overcurrent protection is implemented through current sensing in both the sourcing and sinking paths. When the source or sink current reaches the current limit threshold, the output is forced into constant current regulation. Sourcing and sinking OCP are independently resistor adjustable from 300mA to 3A typical, or tie OCP pins to GND for 4A typical sourcing limit and 4.1A typical sinking limit.

The die junction temperature is monitored internally. When the internal temperature reaches 165°C (typical), the LDO output is disabled. After the internal temperature falls below 155°C (typical), the device resumes normal operation. To determine the expected temperature rise of the device from ambient to junction or case to junction, calculate power dissipation using Equation 1 and Equation 2. While sourcing the voltage drop across the pass device is the difference in V_{IN} and V_{OUT}. While sinking, the voltage drop across the pass device is the difference in V_{OUT} and PGND voltage, which is typically 0V.

Sourcing LDO power dissipation:

(EQ. 1) $$P_{SRC} = (V_{IN} - V_{OUT}) \times I_{OUT}$$

Sinking LDO power dissipation:

(EQ. 2) $$P_{SNK} = V_{OUT} \times I_{OUT}$$

Using the greater of the sinking/sourcing power dissipations (P_{max}), the maximum expected ambient temperature (T_{Amax}), and the maximum junction temperature (T_{Jmax}) use Equation 3 to calculate the required thermal impedance to meet the worst-case operating conditions.

(EQ. 3) $$\theta_{JAmax} = \frac{T_{Jmax} - T_{Amax}}{P_{max}}$$

To avoid thermal shutdown, ensure the specified θ_{JA} is less than the calculated θ_{JAmax}. The θ_{JA} value used must take into account copper area, airflow, and use of heatsinks in a given system.

5.4 CONFIG Pin

The CONFIG pin enables and disables the active discharge feature of VOUT and BUF-OUT. When CONFIG is above the rising threshold, typically 1.1V, active discharge is enabled. CONFIG can be tied to VCC to set it high. When CONFIG is below the typical value of 1V, the active discharge is disabled. CONFIG can be tied to GND to set it low.

Both the VOUT and BUF-OUT discharge circuits are comprised of an NMOS FET that is turned on when discharge conditions are met. For VOUT, discharge occurs when EN falls low and disables the LDO. For BUF-OUT, discharge occurs when BUF-IN falls below its UVLO threshold.

5.5 Enable

The EN pin enables and disables the LDO output. When EN is above the Enable Threshold; Rising (1.1V typical), the LDO is enabled. When EN falls below the Enable Threshold; Falling (0.98V typical), the LDO is disabled.

EN also controls the biasing of the internal voltage reference, VREF_INT. When the EN rising/falling thresholds are met, there is a delay to VREF_INT turning on/off. This is shown as Enable Propagation Delay; Rising and Enable Propagation Delay; Falling in DC Electrical Specifications.

Tie EN to VCC if an external enable control is not required.

The EN signal falling below the enable threshold also results in VOUT discharge when the discharge function is enabled using the CONFIG pin.

Note: The buffer output (BUF-OUT) is independent of EN and is active when BUF-IN and VCC are above their respective UVLO thresholds.

5.6 Soft Start

Soft start is implemented by placing a capacitor on the SS pin. This functionality reduces inrush current and provides a smooth V_{OUT} ramp during startup. V_{OUT} starts to ramp when the SS voltage is greater than a typical value of 20mV to overcome the offset of the error amplifier. SS charges to the soft-start done threshold, typically 2.08V, at which point PG is released. V_{OUT} tracks the SS voltage until SS is greater than the EA+ voltage. SS is clamped to a typical voltage of 3V.

During the fault conditions (undervoltage, overvoltage, or over-temperature), SS discharges so that soft start can re-initiate as part of fault recovery. SS also discharges when EN is low.

The error amplifier uses the lower of SS and EA+ voltage as the non-inverting reference for regulation.

6. Application Information

6.1 Power Supply Biasing

The VIN pins function as the power supply input. A minimum input voltage of 0.75V or $V_{OUT} + V_{IN_DO}$ is required on VIN for regulation. The maximum recommended operating voltage on VIN is 5.5V. The input capacitor should be selected to avoid VIN drooping below dropout voltage during load transients. VIN transient performance is also dependent on system factors such as the input supply bulk capacitance, distance from the LDO, and transient performance. Renesas recommends using a 150µF tantalum capacitor and two 10µF ceramic capacitors on VIN. Additional ceramic capacitors can be placed on VIN for high frequency noise filtering.

A bias supply is required on VCC to provide biasing to internal circuitry. The minimum VCC supply voltage is 2.7V or 1.5V greater than the target output voltage to provide headroom for the VCC dropout voltage of 1.4V. The maximum recommended operating voltage on VCC is 5.5V. A 1µF capacitor is required on VCC and should be placed near the device pin.

6.2 Soft-Start Capacitor

Based on the typical soft-start current of 20µA, a soft-start capacitance can be chosen for a given EA+ rise time using Equation 4. This equation is used because V_{OUT} tracks the SS ramp until it exceeds the EA+ voltage.

(EQ. 4) $$C_{SS} = \frac{I_{SS} \times t_{SS}}{EA+}$$

where:

- C_{SS} is the soft-start capacitor value.
- I_{SS} is the soft-start current.
- t_{SS} is the soft-start time.
- EA+ is the voltage on the non-inverting input of the error amplifier.

V_{OUT} is equal to EA+ in DDR configuration. In standard LDO configuration where a resistor divider is used to set the output voltage, V_{OUT} is scaled to EA+ based on the resistor divider.

C_{OUT} is charged up to V_{OUT} in t_{ss}, resulting in an inrush current that can be calculated using Equation 5:

Although the supply is in regulation, PG is not active until SS reaches the soft-start done threshold of 2.08V typical.

(EQ. 5) $$I_{INRUSH} = C_{OUT} \times \frac{V_{OUT}}{t_{SS}}$$

6.3 Buffer Input and Output for DDR Applications

In DDR applications, the VDDQ rail is typically used as the LDO input supply, VIN. Because DDR memory power supplies specify VTT as VDDQ/2, the internal buffer on the ISL75055SLH generates the VTT reference voltage. For applications where VDDQ is tied to both VIN and BUF-IN, Renesas recommends placing an RC low pass filter of 1kΩ and 1µF between the VIN and BUF-IN pins. This filter mitigates SETs and transients on the input supply so that the BUF-IN voltage is stable.

A minimum 1µF capacitor is recommended on BUF-OUT for SEE mitigation. The buffer output is independent of the EN pin. BUF-OUT is active if BUF-IN and VCC UVLO thresholds are met.

6.3.1 Buffer Input Range for EA+

To guarantee soft-start functionality, the recommended maximum input to BUF-IN is 3.3V when BUF-OUT is connected to EA+. The resulting BUF-OUT voltage of 1.65V, is equal to the minimum Soft-Start Done Threshold specified in DC Electrical Specifications. While BUF-IN is rated for voltages up to the VCC voltage, there are reasons to avoid voltages greater than 3.3V, when BUF-OUT is used as the reference voltage to EA+. When BUF-OUT is greater than Soft-Start Done Threshold, PG timing is affected since PG functionality becomes active before the supply reaches its regulation point, removing any delays. Additionally, the minimum soft-start clamp voltage is 2.5V. This means that for BUF-IN voltage greater than 5V (or EA+ greater than 2.5V), full regulation is not reached since the lowest of SS and EA+ is used for the error amplifier reference and the SS voltage is used as the regulation point.

6.3.2 VREF_INT for Standard LDO Applications

VREF_INT is the output of the internal 500mV voltage reference. VREF_INT becomes active when both VCC UVLO and EN rising thresholds are met. A minimum bypass capacitance of 0.1µF should be placed on this pin. For standard LDO applications, VREF_INT is used as the input to the error amplifier non-inverting input (EA+), where it acts as a voltage reference allowing for the LDO output to be programmed down to 0.5V.

6.4 LDO Output Voltage

In DDR applications, where BUF-OUT is used as the input to EA+, connect EA- directly to VOUT at the point of load (PoL) for VTT rail regulation. Under this configuration, output voltage is regulated to BUF-IN/2.

In a standard LDO application where VREF_INT is used as the input to EA+, a resistor divider placed from VOUT to EA- sets the output voltage. Use Equation 6 to determine the required resistors for a target output voltage. For supplies that require an output voltage of 0.5V, a resistor divider is not required and EA- can connect directly to VOUT at the point of load.

(EQ. 6)
$$V_{OUT} = VREF_INT \times \left(1 + \frac{R_{FBT}}{R_{FBB}}\right)$$

where:

- R_{FBT} is the top feedback divider resistor.
- R_{FBB} is the bottom feedback resistor divider.

For applications where V_{OUT} is set through a resistor divider between VOUT and EA-, the dead band proportionally scales to the gain from EA+ to VOUT. The increase in dead band voltage from feedback loop gain increases the delta of the regulation set point as the linear regulator transitions from sourcing to sinking current.

6.5 Output Capacitance

Recommended output capacitance depends on whether the device is operating in a DDR or standard LDO configuration. In DDR mode, where the control loop is operating with unity gain, Renesas recommends using two 150µF/15mΩ Tantalum Polymer capacitors in parallel to achieve loop stability. Additionally, place a 4.99kΩ resistor between the output and EA- pin. This resistor creates a pole at the target frequency of 1.5MHz with the internal capacitance on the EA- node.

In LDO mode, where additional loop gain is introduced by the feedback resistor divider, Renesas recommends using a single 330µF/25mΩ Tantalum Polymer capacitor to achieve loop stability.

Place Tantalum Polymer capacitors near the device VOUT and PGND pins to minimize effects of ESR and ESL. Additional ceramic capacitors are not necessary for stability. If used for high frequency decoupling, place a 0.1µF capacitor near the PoL.

Bench evaluations were performed with the T530X157M016ATE015, 150µF/15mΩ ESR capacitor for DDR mode and the T541X337M016AH6520, 330µF/25mΩ capacitor for LDO mode. Stability should be validated using a bode plot and load transient analysis in the end application.

6.6 Power Good (PG)

The PG pin is an open-drain output and requires a pull-up resistor to VCC. Renesas recommends placing a 10kΩ resistor between PG and VCC.

PG pulls low during output overvoltage, undervoltage, and over-temperature conditions. PG is also low when SS is below the soft-start done threshold.

6.7 Adjustable Source and Sink Current Limit

The current limit can be programmed individually for both sourcing and sinking paths. A resistor to AGND from the OCP-SRC pin (sourcing) and OCP-SNK pin (sinking) sets the current limit. When the OCP pins are connected directly to AGND, the maximum limit of sourcing (4A typical) and sinking (4.1A typical) are set internally.

Renesas recommends using a maximum OCP resistor value of 30kΩ, which equates to a minimum sourcing/sinking current limit of 300mA. Use Equation 7 to calculate the OCP resistance based on target current limit. Figure 34 shows a typical curve for current limit vs OCP resistance in both the sinking and scouring direction. OCP resistor values above 30kΩ further reduce the current limit, but accuracy of the threshold becomes degraded and is not recommended.

(EQ. 7) $$R_{OCP} = \frac{9000[mA \times k\Omega]}{I_{OCP}}$$

where:

- R_{OCP} is the sinking or sourcing OCP resistance in kΩ.
- I_{OCP} is the target sinking or sourcing current limit in mA.

6.8 Recommended PCB Layout

PCB layout is critical for optimizing LDO performance. See Figure 42 for a recommended layout.

- Place bulk output capacitors as close as possible to the VOUT pins. Ensure the VOUT plane is wide enough to handle 3A of current.
- Connect EA- to VOUT at the point of load to avoid inaccuracies in output voltage sensing. When a resistor divider is used for setting the output voltage, place the resistors near the EA- pin to prevent noise coupling to the high impedance EA- trace.
- Place bypass capacitors on VREF_INT, VCC, BUF-IN, and BUF-OUT near the respective pins.
- Tie both VIN EPADU and PGND EPADL to large planes to maximize thermal dissipation from the package to the PCB. Additionally, place thermal vias in the pad to transfer heat to other PCB layers.

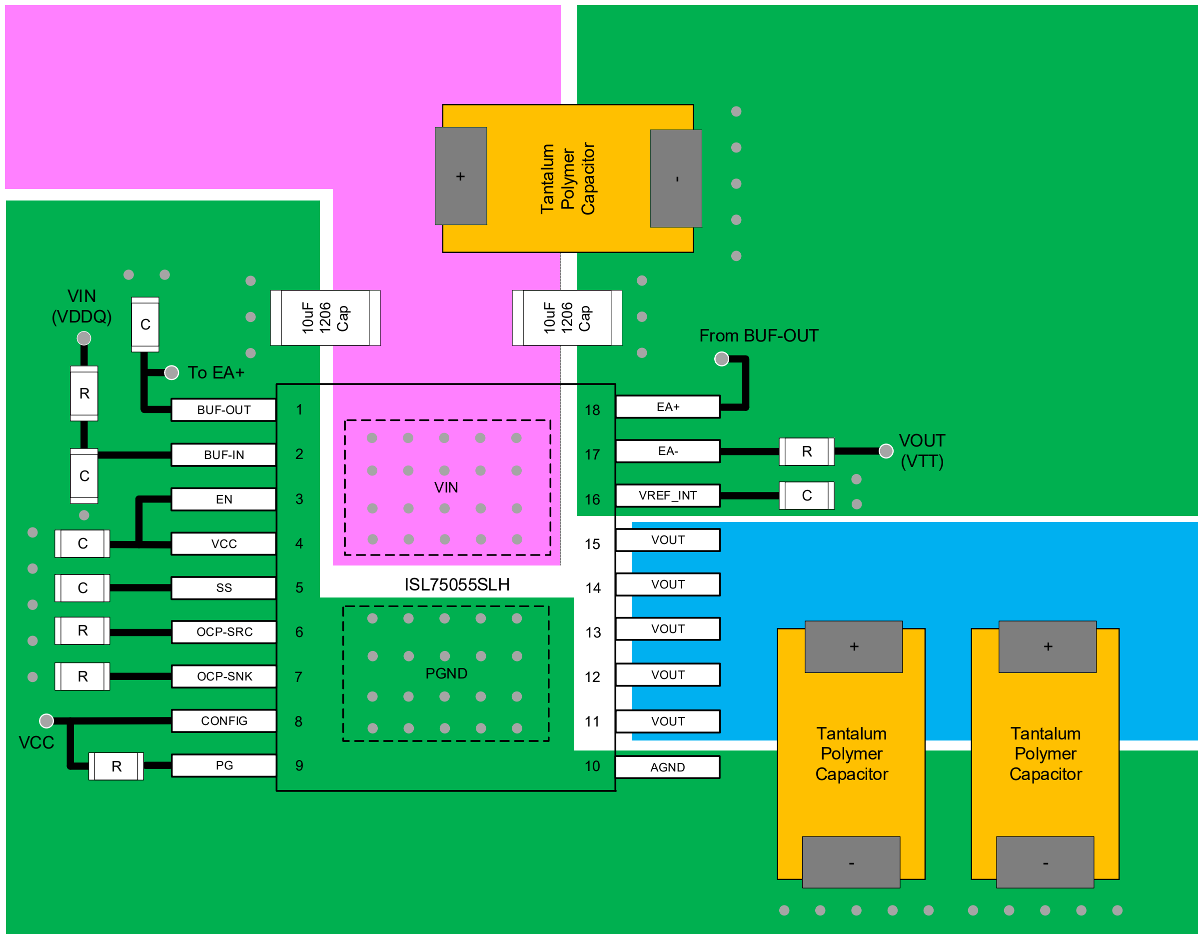


Figure 42. Layout Example

7. Die and Assembly Characteristics

Manufactured on a 250nm BiCMOS process.

Table 2. Die and Assembly Characteristics

Die Information	
Dimensions	4500µm×4500µm (177 mils×177 mils) Thickness: 483µm ±25µm (19 mils ±1 mil)
Interface Materials	
Glassivation	Type: 17kÅ planarized HDP and TEOS under 1.5kÅ Oxide under 6kÅ Nitride
Top Metallization	Type: Al, 0.5%Cu
Backside Finish	Silicon
Process	0.25µm BiCMOS
Assembly Information	
Substrate Potential	GND
Additional Information	
Worst Case Current Density	$1.6 \times 10^5 A/cm^2$
Transistor Count	49667
Weight of Packaged Device	1.42 grams
Lid Characteristics	Finish: Gold Potential: PGND
Bottom Metal Characteristics, Upper EPAD	Finish: Gold Potential: VIN
Bottom Metal Characteristics, Lower EPAD	Finish: Gold Potential: PGND

7.1 Metallization Mask Layout

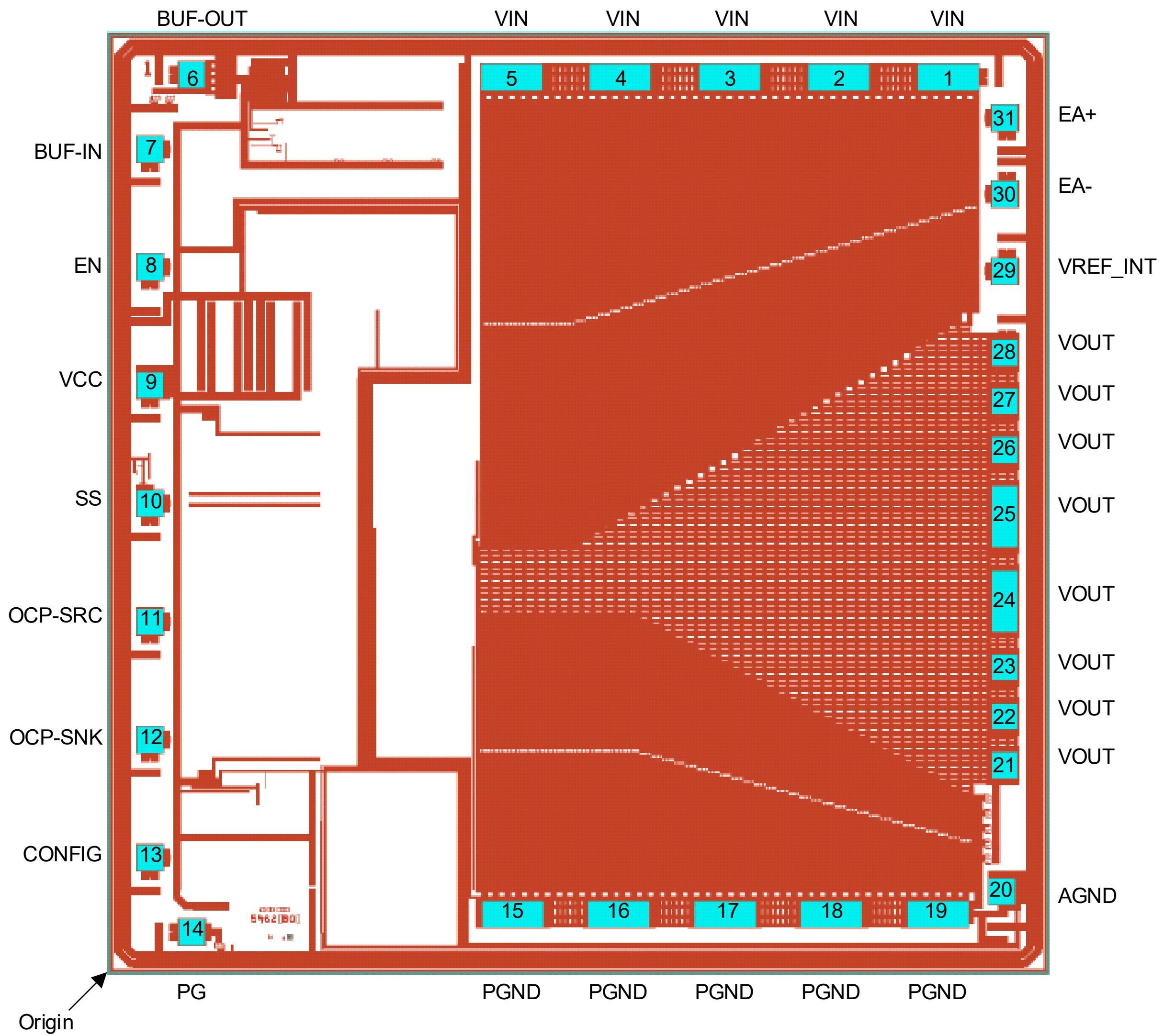


Figure 43. Mask Layout

Table 3. Die Layout X-Y Coordinates

Pad Name	Pad Number	Pad Size X	Pad Size Y	X-Coordinate (um)	Y-Coordinate (um)
VIN	1	280	117	3931.28	4194.81
VIN	2	280	117	3422.77	4194.81
VIN	3	280	117	2914.77	4194.81
VIN	4	280	117	2406.77	4194.81
VIN	5	280	117	1898.1	4194.81
BUF-OUT	6	117	117	408.5	4206.14
BUF-IN	7	117	117	213.86	3860
EN	8	117	117	213.86	3310
VCC	9	117	117	213.86	2760
SS	10	117	117	213.86	2210
OCP-SRC	11	117	117	213.86	1660
OCP-SNK	12	117	117	213.86	1110

Table 3. Die Layout X-Y Coordinates (Cont.)

Pad Name	Pad Number	Pad Size X	Pad Size Y	X-Coordinate (um)	Y-Coordinate (um)
CONFIG	13	117	117	213.86	560
PG	14	117	117	408.5	213.86
PGND	15	280	117	1903.8	297.87
PGND	16	280	117	2398.75	297.87
PGND	17	280	117	2893.7	297.87
PGND	18	280	117	3388.65	297.87
PGND	19	280	117	3883.6	297.87
AGND	20	117	117	4181.14	403.5
VOUT	21	117	117	4196.14	990.55
VOUT	22	117	117	4196.14	1218.55
VOUT	23	117	117	4196.14	1446.55
VOUT	24	117	280	4196.14	1756.05
VOUT	25	117	280	4196.14	2148.05
VOUT	26	117	117	4196.14	2457.55
VOUT	27	117	117	4196.14	2685.55
VOUT	28	117	117	4196.14	2913.55
VREF_INT	29	117	117	4196.14	3292.39
EA-	30	117	117	4196.14	3649.35
EA+	31	117	117	4196.14	4006.31

8. Package Outline Drawing

The package outline drawing is located at the end of this document and is accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

9. Ordering Information

<table>
<tr><th>Part Number</th><th>Radiation Hardness (Total Ionizing Dose)</th><th>Package Description (RoHS Compliant)</th><th>Pkg. Dwg #</th><th>Carrier Type</th><th>Temp. Range</th></tr>
<tr><td>ISL75055SLHMF[1]</td><td>LDR to 75krad(Si)</td><td rowspan="2">18 Ld Ceramic DFP</td><td rowspan="2">K18.F</td><td rowspan="2">Tray</td><td rowspan="2">-55 to +125°C</td></tr>
<tr><td>ISL75055SLHF/PROTO[1][2]</td><td>N/A</td></tr>
<tr><td>ISL75055SLHMX[3]</td><td>LDR to 75krad(Si)</td><td rowspan="2">Die</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-55 to +125°C</td></tr>
<tr><td>ISL75055SLHX/SAMPLE[2][3]</td><td>N/A</td></tr>
<tr><td>ISL75055SLHEV1Z[4]</td><td colspan="5">Evaluation Board for DDR VTT Termination and Standard LDO Applications with CDFP package</td></tr>
</table>

1. This product is in compliance with EU Directive 2015/863/EU amending Annex II to EU Directive 2011/65/EU (RoHS) and contains Pb according to RoHS exemption 7c-i, Pb in a glass or ceramic other than dielectric ceramic in capacitors. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in this datasheet. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in this datasheet. The /SAMPLE parts do not receive 100% screening across temperature to the electrical limits. These part types do not come with a Certificate of Conformance.
3. Die product tested at T_A = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in Electrical Specifications. The die is sourced from wafer lots that have been qualified for Group C and Group E per MIL-PRF-38535 (Refer to *R34TB0001: Renesas Radiation Hardened Hermetic Screening and QCI Flow* for more information).
4. Evaluation board uses the /PROTO parts and /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

10. Revision History

Revision	Date	Description
1.03	May 11, 2026	Updated the Burn In Delta table Error Amplifier VOS spec from ±0.44mV to ±0.88mV.
1.02	Mar 17, 2026	Updated VIN UVLO Rising and Falling Minimum specifications.
1.01	Feb 6, 2026	Updated the ordering information table.
1.00	Oct 27, 2025	Initial release

A. ECAD Design Information

This information supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

A.1 Part Number Indexing

Orderable Part Number	Number of Pins	Package Type	Package Code/POD Number
ISL75055SLHMF	18	CDFP	CF0018AA/K18.F

A.2 Symbol Pin Information

A.2.1 18-CDFP

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	BUF-OUT	Output	-
2	BUF-IN	Input	-
3	EN	Input	-
4	VCC	Power	-
5	SS	Output	-
6	OCP-SRC	Input	-
7	OCP-SNK	Input	-
8	CONFIG	Input	-
9	PG	Output	-
10	AGND	Power	-
11	VOUT	Power	-
12	VOUT	Power	-
13	VOUT	Power	-
14	VOUT	Power	-
15	VOUT	Power	-
16	VREF_INT	Power	-
17	EA-	Input	-
18	EA+	Input	-
EPAD19	VIN	Power	-
EPAD20	PGND	Power	-

A.3 Symbol Parameters

Orderable Part Number	Qualification	Radiation Qualification	LDR	Mounting Type	RoHS	Min Operating Temperature	Max Operating Temperature	Min Input Voltage	Max Input Voltage	Output Current
ISL75055SLHMF	Space	Radiation Hardened	75 krad(Si)	SMD	Compliant	-55 °C	125 °C	0.75 V	5.5 V	3 A

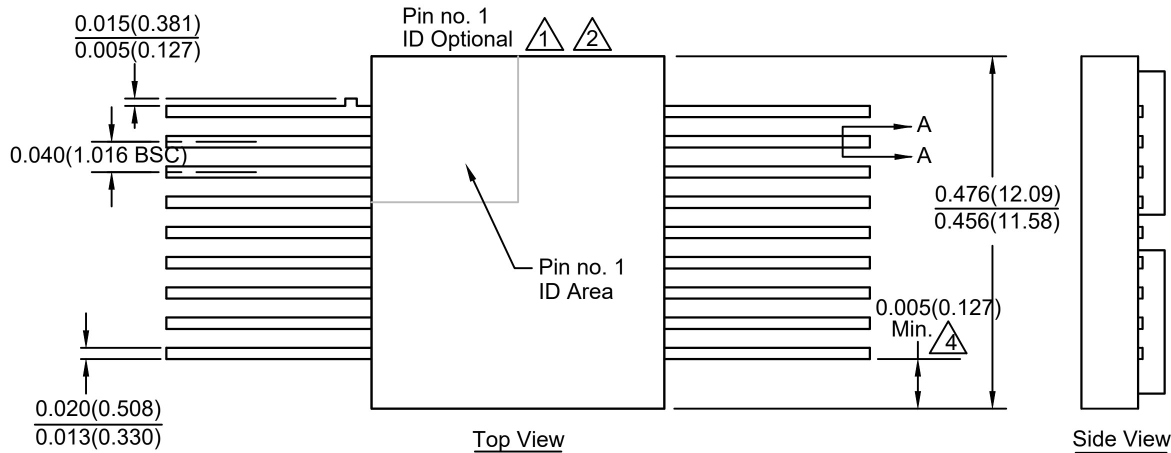
A.4 Footprint Design Information

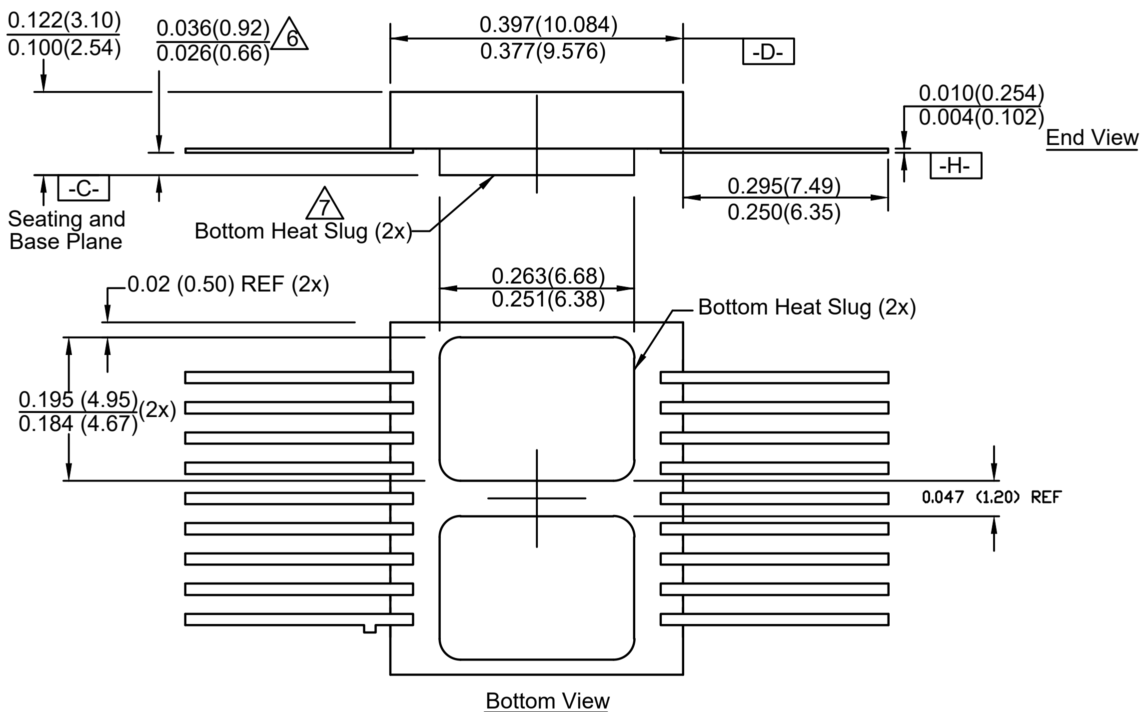
A.4.1 18-CDFP

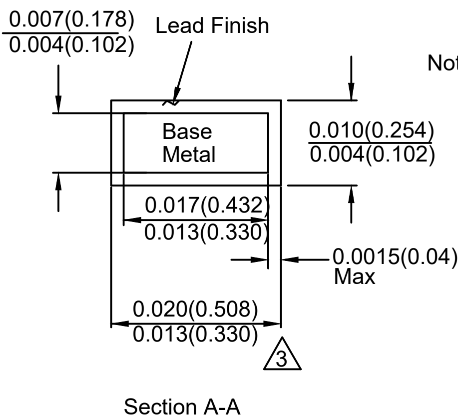
Follow the POD drawing for footprint generation of the 18 Lead Ceramic Metal Seal Flatpack Package.

Package Outline Drawing

K18.F
CF0018AA
18 Lead Ceramic Metal Seal Flatpack Package with Two Bottom Heat Slugs
Rev.01, Sep 8, 2025







Notes:

1. Index area: A notch or a pin one identification mark is located adjacent to pin one and is located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) are measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials are molded to the bottom of the of the package to cover the leads.
6. Dimension is measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum is reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. The bottom of the package consists of two solderable metal heat slugs.
8. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
9. Dimensions = Inch (mm). Controlling dimension: Inch.

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