# ISL72814SEH, ISL73814SEH

16-Channel Driver Circuit with an Integrated Decoder

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The ISL72814SEH and ISL73814SEH are radiation hardened high-voltage, high-current, driver circuit ICs fabricated using the Renesas proprietary PR40 Silicon-On-Insulator (SOI) process technology to mitigate single-event effects. The devices integrate 16 driver channels that feature a high-voltage (42V), high-current (700mA) open-emitter PNP output stage.

To further reduce solution size, the ISL72814SEH and ISL73814SEH integrate a 4-bit, 16-channel decoder with Enable. This conveniently allows you to select 1 of 16 available driver channels or disable all channels. The inputs to the decoder are TTL and CMOS compatible, allowing an easy interface to FPGAs and microprocessors.

The ISL7x814SEH devices operate across the military temperature range from -55°C to +125°C and are available in a 28 lead hermetically sealed Ceramic Dual Flatpack (CDFP) package or die.

## Applications

- RF waveguide and coaxial switches
- Relays
- Line drivers
- Logic buffers
- Lamp drivers

## Features

- Electrically screened to DLA SMD 5962-18221
- Integrated 4-bit to 16-channel decoder
- High current outputs: 700mA
- High voltage outputs: 42V
- Ultra low saturation voltage: 1.35V maximum at 500mA
- Internal clamping diodes for inductive loads
- Wide operating $V_{CC}$ supply range 3V to 13.2V
- Full military temperature range operation
  - $T_A$ = -55°C to +125°C
  - $T_J$ = -55°C to +150°C
- Radiation acceptance testing - ISL72814SEH
  - HDR (50-300rad(Si)/s): 100krad(Si)
  - LDR (0.01rad(Si)/s): 75krad(Si)
- Radiation acceptance testing - ISL73814SEH
  - LDR (0.01rad(Si)/s): 75krad(Si)
- SEE hardness (see SEE report for details)
  - No SEB/SEL $LET_{TH,}$ $V_{CH}$ = 34V: 86MeV•cm$^2$/mg

## Related Literature

For a full list of related documents, visit our website:

- ISL72814SEH and ISL73814SEH device pages

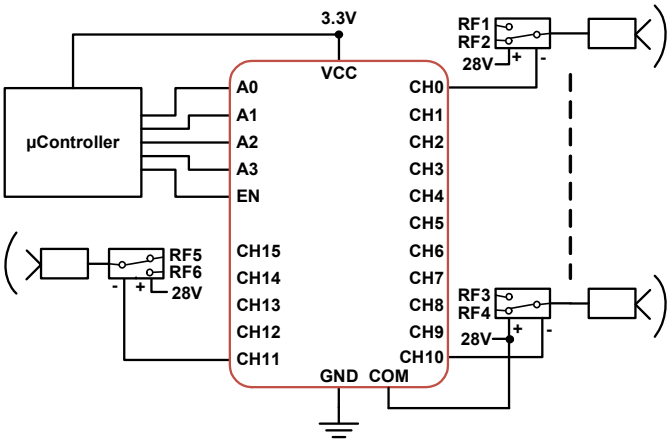



**Figure 1. RF Switching Module**

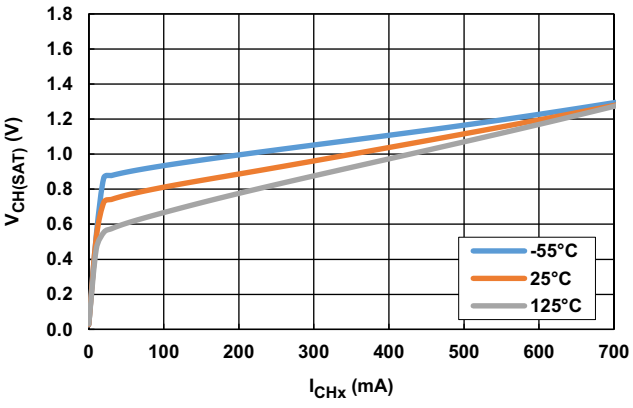



**Figure 2. $V_{CH(SAT)}$ vs $I_{CHx}$ vs Temperature**

# Contents

# 1. Overview

## 1.1 Typical Application Schematic

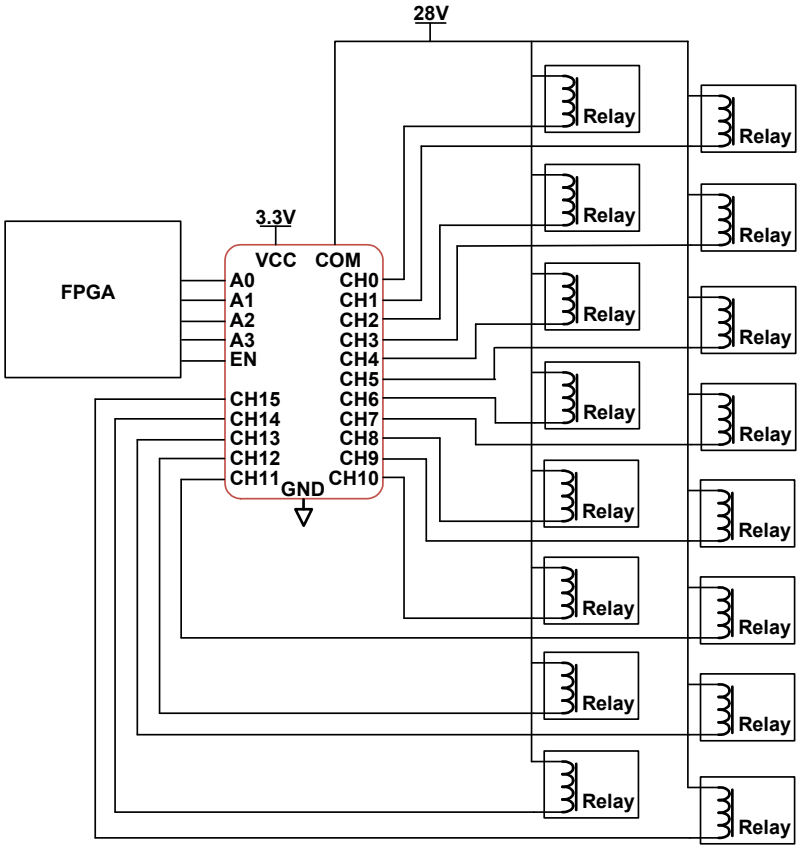



**Figure 3. Typical Relay Application Diagram**

## 1.2 Functional Block Diagram

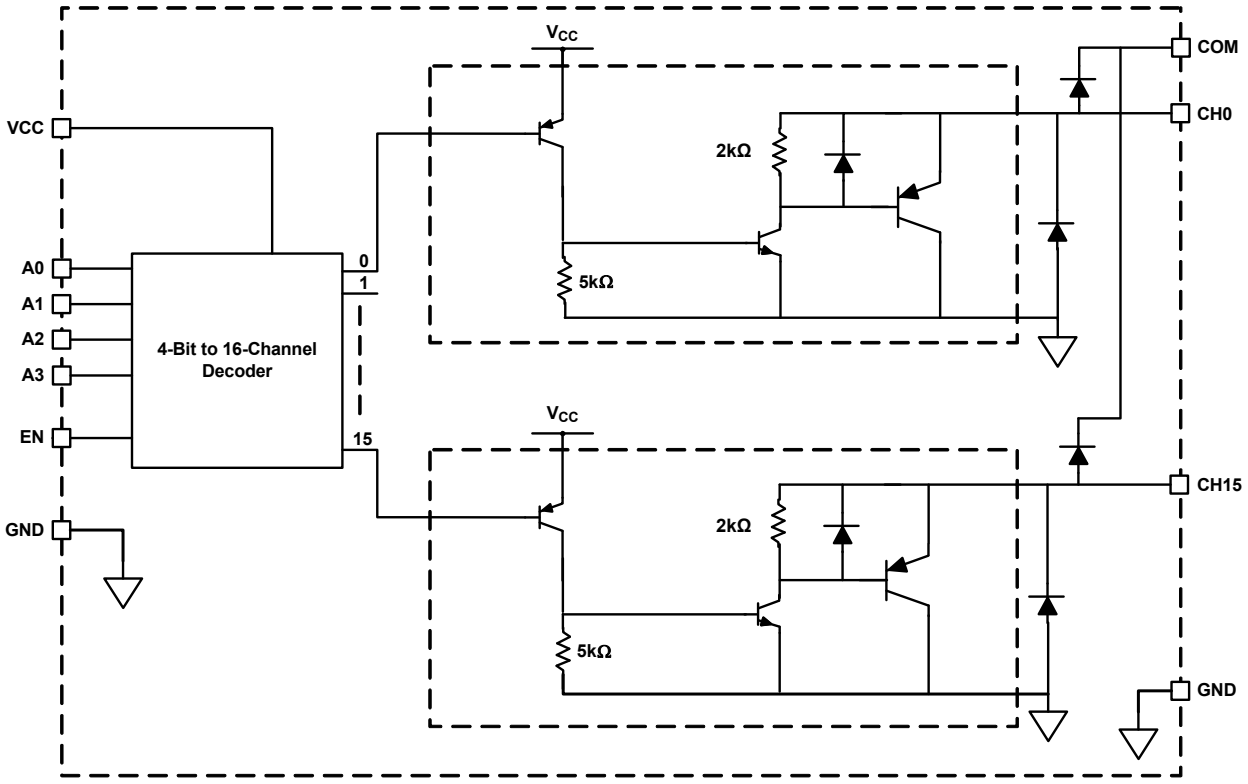



**Figure 4. Block Diagram**

## 1.3 Ordering Information

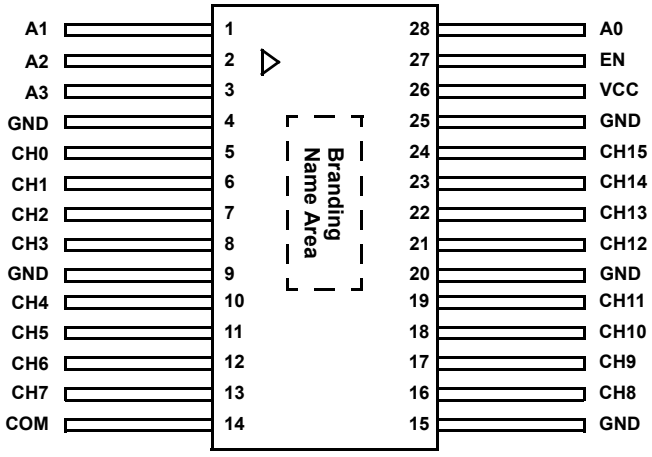
| Ordering SMD Number (Note 1) | Part Number (Note 2) | Radiation Hardness (Total Ionizing Dose) | Temperature Range (°C) | Package (RoHS Compliant) | Package Drawing |
|---|---|---|---|---|---|
| 5962R1822101VXC | ISL72814SEHVF | HDR to 100krad(Si), LDR to 75krad(Si) | -55 to +125 | 28 Ld CDFP | K28.A |
| 5962R1822101V9A | ISL72814SEHVX | | -55 to +125 | Die | N/A |
| 5962L1822102VXC | ISL73814SEHVF | LDR to 75krad(Si) | -55 to +125 | 28 Ld CDFP | K28.A |
| 5962L1822102V9A | ISL73814SEHVX | | -55 to +125 | Die | N/A |
| N/A | ISL72814SEHF/PROTO (Note 3) | N/A | -55 to +125 | 28 Ld CDFP | K28.A |
| N/A | ISL73814SEHF/PROTO (Note 3) | N/A | -55 to +125 | 28 Ld CDFP | K28.A |
| N/A | ISL72814SEHX/SAMPLE (Note 3) | N/A | -55 to +125 | Die | N/A |
| N/A | ISL73814SEHX/SAMPLE (Note 3) | N/A | -55 to +125 | Die | N/A |
| N/A | ISL72814SEHEV1Z (Note 4) | Evaluation Board | | | |

Notes:

1. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
2. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
3. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD at +25°C only. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.
4. Evaluation board uses the /PROTO parts and /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

## 1.4 Pin Configuration

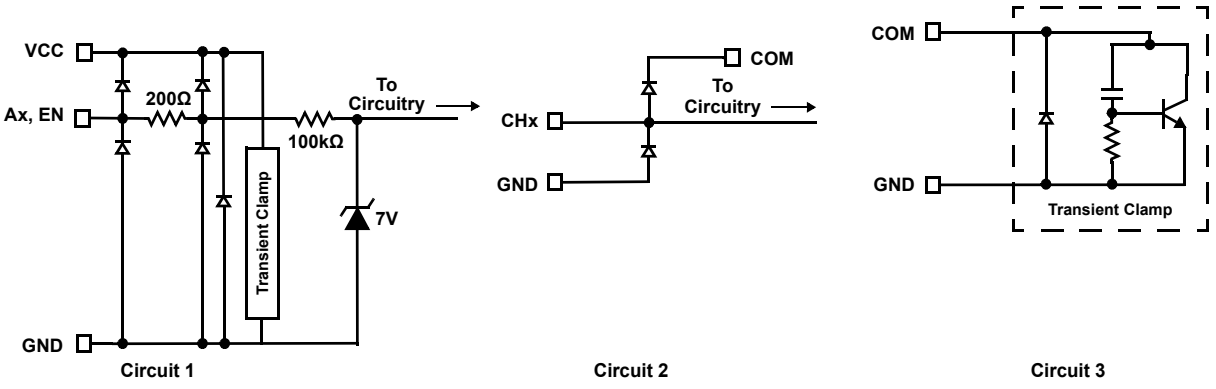
ISL72814SEH, ISL73814SEH
28 Ld CDFP
Top View




Note: The ESD triangular mark is indicative of Pin #1. It is a part of the device marking and is placed on the lid in the quadrant where Pin #1 is located.

## 1.5 Pin Descriptions

| Pin Number | Pin Name | ESD Circuit | Description |
|---|---|---|---|
| 1 - 3, 28 | Ax | 1 | Address lines for the decoder. |
| 4, 9, 15, 20, 25 | GND | 1,2,3 | Supply and output driver ground. Connect this pin to the PCB ground plane. |
| 5-8, 10-13, 16-19, 21-24 | CHx | 2 | Channels 0 through 15 open emitter PNP outputs. |
| 14 | COM | 3 | ESD Clamp rail. It can be used to terminate inductances connected to the CHx pins and should be tied to the highest relay coil supply rail in the system. When not switching inductive loads, tie it to the supply rail of the CHx channel with the highest voltage. |
| 26 | VCC | 1 | Bias supply for the decoder and the level shift circuit. Connect to a voltage between 3V to 13.2V. |
| 27 | EN | 1 | Active high enable input to the decoder. |
| LID | N/A | N/A | Package Lid is internally connected to GND (Pin 15). |



# 2. Specifications

## 2.1 Absolute Maximum Ratings

| Parameter | Minimum | Maximum | Unit |
|---|---|---|---|
| VCC | GND - 0.3V | GND + 14.7 | V |
| Logic Input Voltage (EN, Ax) | GND - 0.3V | $V_{CC}$ + 0.3 | V |
| Logic Input Current (EN, Ax) | -15 | 15 | mA |
| CHx | GND - 0.3V | GND + 42 | V |
| CHx (Under beam LET = 86MeV) | GND - 0.3V | GND + 34 | V |
| COM to GND | - | GND + 42 | V |
| COM to GND (Under beam LET = 86MeV) | - | GND + 34 | V |
| COM to CHx | Highest Positive CHx Voltage - 0.3V | GND + 42 | V |
| COM to CHx (Under beam LET = 86MeV) | Highest Positive CHx Voltage - 0.3V | GND + 34 | V |
| Peak $I_{CHx}$, (100ms) | - | 1.1 | A |
| Power Dissipation, PD (Case Temperature +125°C) | - | 1.3 | W |
| VCC and COM Maximum Supply Turn-On Ramp Rate | - | 1 | V/µs |
| **ESD Rating** | **Value** | | **Unit** |
| Human Body Model (Tested per MIL-STD-883 TM3015.7) | 5 | | kV |
| Charged Device Model (Tested per JS-002-2014) | 1 | | kV |

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

## 2.2 Thermal Information

| Thermal Resistance (Typical) | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| CDFP Package K28.A (Notes 5, 6) | 34.5 | 18.8 |

Notes:

5. $\theta_{JA}$ is measured in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. See TB379.
6. For $\theta_{JC}$, the “case temp” location is the center of the package underside.

| Parameter | Minimum | Maximum | Unit |
|---|---|---|---|
| Maximum Junction Temperature | - | +150 | °C |
| Storage Temperature Range | -65 | +150 | °C |

## 2.3 Recommended Operating Conditions

| Parameter | Minimum | Maximum | Unit |
|---|---|---|---|
| Temperature | -55 | +125 | °C |
| VCC | 3.0 | 13.2 | V |
| CHx | 5 | 34 | V |

| Parameter | Minimum | Maximum | Unit |
|---|---|---|---|
| **Channel Current Duty Cycle Limit, 1.6 x $10^5$ hours Metallic Electromigration limited lifetime at +125°C junction temperature to 0.1% failures.** | | | |
| $I_{CHX}$ = 400mA | - | 100 | % |
| $I_{CHX}$ = 500mA | - | 73 | % |
| $I_{CHX}$ = 600mA | - | 51 | % |
| $I_{CHX}$ = 700mA | - | 37 | % |
| **Channel Current Duty Cycle Limit, 1.6 x $10^5$ hours Metallic Electromigration limited lifetime at +150°C junction temperature to 0.1% failures.** | | | |
| $I_{CHX}$ = 250mA | - | 100 | % |
| $I_{CHX}$ = 300mA | - | 70 | % |
| $I_{CHX}$ = 400mA | - | 39 | % |
| $I_{CHX}$ = 500mA | - | 25 | % |
| $I_{CHX}$ = 600mA | - | 17 | % |
| $I_{CHX}$ = 700mA | - | 13 | % |

## 2.4 Electrical Specifications

Unless otherwise noted, $V_{CC}$ = 3V - 13.2V; $V_{CHX}$ = 34V (Disabled), Logic High = $V_{CC}$, Logic Low = GND; $T_A$ = $T_J$ = +25°C. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 100krad(Si) with exposure at a high dose rate of 50 to 300rad(Si)/s (ISL72814SEH only); or over a total ionizing dose of 75krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.**

| Parameter | Symbol | Test Conditions | Temperature (°C) | Min (Note 8) | Typ (Note 7) | Max (Note 8) | Unit |
|---|---|---|---|---|---|---|---|
| **$V_{CC}$ Power Supply** | | | | | | | |
| Supply Current | $I_{CC}$ | $V_{CC}$ = 3.6V, 13.2V, CHx = OPEN, EN = $V_{CC}$, COM = 0V, A0-A3 = 0V | -55 to +125 | **4.5** | 7.03 | **8.5** | mA |
| Quiescent Supply Current | $I_{CCQ}$ | $V_{CC}$ = 3.6V, 13.2V, CHx = OPEN, EN = 0V, COM = 0V, A0-A3 = 0V | -55 to +125 | **350** | 643 | **800** | µA |
| **Driver Circuit** | | | | | | | |
| Single Channel Leakage Current | $I_{CHLK}$ | $V_{CHX}$ (under test) = 34V, All other $V_{CHX}$ channels = 35V, $V_{CC}$ = 3V, 5.5V, COM = 35V, A0-A3 = 0V, EN = 0V | -55 and +25 | -25 | 3.45 | 25 | nA |
| | | | +125 | -10 | - | 90 | nA |
| | | | Post Radiation (+25) | -25 | - | 25 | nA |
| All Channels + COM Leakage Current | $I_{TOTCHLK}$ | $V_{CH0 - CH15}$ = COM = 34V, $V_{CC}$ = 3V, 5.5V, A0-A3 = 0V, EN = 0V | -55 and +25 | -30 | 8.37 | 30 | nA |
| | | | +125 | -30 | - | 1000 | nA |
| | | | Post Radiation (+25) | -30 | - | 100 | nA |
| Output Channel Saturation Voltage | $V_{CHX(SAT)}$ | $I_{CHx}$ = 700mA, $V_{CC}$ = 3V, 5.5V, COM = 35V, EN = $V_{CC}$ | -55 to +125 | **0.85** | 1.23 | **1.5** | V |
| | | $I_{CHx}$ = 600mA, $V_{CC}$ = 3V, 5.5V, COM = 35V, EN = $V_{CC}$ | -55 to +125 | **0.8** | 1.15 | **1.4** | V |
| | | $I_{CHx}$ = 500mA, $V_{CC}$ = 3V, 5.5V, COM = 35V, EN = $V_{CC}$ | -55 to +125 | **0.65** | 1.08 | **1.35** | V |
| | | $I_{CHx}$ = 350mA, $V_{CC}$ = 3V, 5.5V, COM = 35V, EN = $V_{CC}$ | -55 to +125 | **0.6** | 0.997 | **1.3** | V |
| | | $I_{CHx}$ = 200mA, $V_{CC}$ = 3V, 5.5V, COM = 35V, EN = $V_{CC}$ | -55 to +125 | **0.5** | 0.875 | **1.2** | V |

Unless otherwise noted, $V_{CC}$ = 3V - 13.2V; $V_{CHX}$ = 34V (Disabled), Logic High = $V_{CC}$, Logic Low = GND; $T_A = T_J$ = +25°C. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 100krad(Si) with exposure at a high dose rate of 50 to 300rad(Si)/s (ISL72814SEH only); or over a total ionizing dose of 75krad(Si) with exposure at a low dose rate of <10mrad(Si)/s. (Continued)**

| Parameter | Symbol | Test Conditions | Temperature (°C) | Min (Note 8) | Typ (Note 7) | Max (Note 8) | Unit |
|---|---|---|---|---|---|---|---|
| COM to CHx Inductive Kickback Clamp Diode Forward Voltage | $V_F$ | $I_{CHx}$ = 200mA, COM = 0V, $V_{CC}$ = 0V, A0-A3 = 0V, EN = 0V | -55 to +125 | **0.85** | 1.09 | **1.3** | V |
| | | $I_{CHx}$ = 700mA, COM = 0V, $V_{CC}$ = 0V, A0-A3 = 0V, EN = 0V | -55 to +125 | **1.0** | 1.59 | **2.25** | |
| COM to CHx Inductive Kickback Clamp Diode Leakage Current | $I_R$ | $V_{COM}$ = 34V, $V_{CC}$ = 0V, A0-A3 = 0V, EN = 0V, CHx channel under test = 0V, other CHx channels = open | -55 to +125 | **-15** | 0.0 | **15** | nA |
| **Decoder and Enable Inputs** | | | | | | | |
| Logic Input High | $V_{IH}$ | $V_{CC}$ = 3V, 13.2V, COM = $V_{CC}$ | -55 to +125 | **2** | 1.48 | - | V |
| Logic Input Low | $V_{IL}$ | $V_{CC}$ = 3V, 13.2V, COM = $V_{CC}$ | -55 to +125 | - | 1.42 | **0.8** | V |
| Input High Current | $I_{IH}$ | $V_{CC}$ = 3.0V, 5.5V, COM = $V_{CC}$, A0-A3 = EN = 2.0V | -55 to +125 | **-250** | -56 | **250** | nA |
| Input Low Current | $I_{IL}$ | $V_{CC}$ = 3.0V, 5.5V, COM = $V_{CC}$, A0-A3 = EN = 0.8V | -55 to +125 | **-250** | -83 | **250** | nA |
| **Switching Characteristics** | | | | | | | |
| Enable Turn-On Time (Notes 9, 10) | $t_{EN}$ | $V_{CC}$ = 3V, 13.2V, COM = 35V, A0-A3 = 0V. CH0 channel under test connected to 97Ω to 34V, other CHx channels connected to 10kΩ to 34V (see Figure 5) | -55 to +125 | - | 2.36 | **5** | µs |
| Disable Turn-Off Time (Notes 9, 10) | $t_{DIS}$ | $V_{CC}$ = 3V, 13.2V, COM = 35V, A0-A3 = 0V. CH0 channel under test connected to 97Ω to 34V, other CHx channels connected to 10kΩ to 34V (see Figure 5) | -55 to +125 | - | 5.96 | **15** | µs |

Notes:

7. Typical values shown are not guaranteed.
8. Parameters with MIN and/or MAX limits are 100% tested at -55°C, +25°C, and +125°C, unless otherwise specified.
9. Addressing should only be changed while EN = GND, otherwise multiple outputs can be momentarily activated. See "Ensuring Break-Before-Make (BBM) Operation" on page 13.
10. After disabling (EN = 0) and changing addresses, delay at least 10µs before enabling (EN = 1) to the new channel. This prevents multiple outputs from being momentarily on at the same time. See "Ensuring Break-Before-Make (BBM) Operation" on page 13.

## 2.5 Timing Diagram

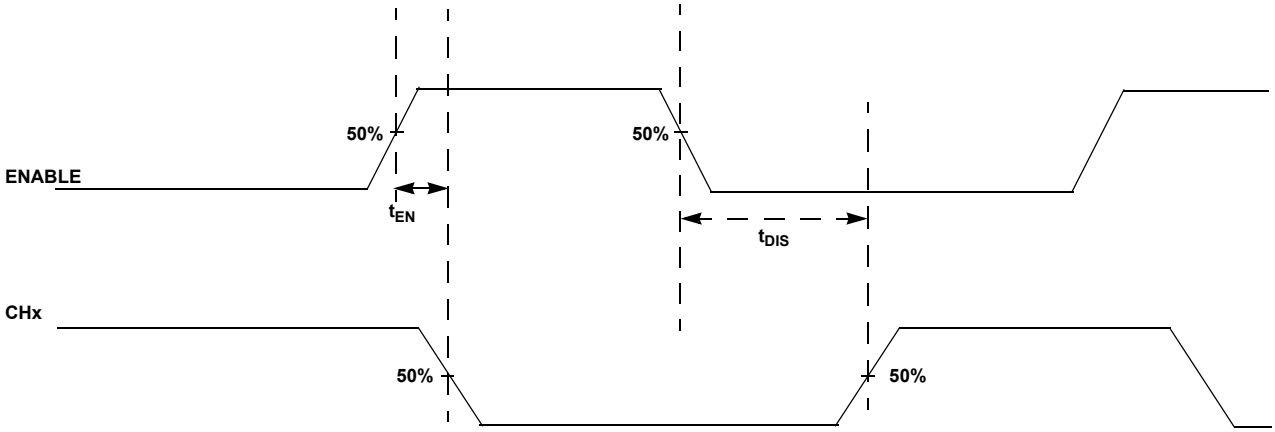



**Figure 5. Timing Diagram**

**Table 1. Truth Table**

| A3 | A2 | A1 | A0 | EN | Activated Channel Output |
|---|---|---|---|---|---|
| X | X | X | X | 0 | None |
| 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | 2 |
| 0 | 0 | 1 | 1 | 1 | 3 |
| 0 | 1 | 0 | 0 | 1 | 4 |
| 0 | 1 | 0 | 1 | 1 | 5 |
| 0 | 1 | 1 | 0 | 1 | 6 |
| 0 | 1 | 1 | 1 | 1 | 7 |
| 1 | 0 | 0 | 0 | 1 | 8 |
| 1 | 0 | 0 | 1 | 1 | 9 |
| 1 | 0 | 1 | 0 | 1 | 10 |
| 1 | 0 | 1 | 1 | 1 | 11 |
| 1 | 1 | 0 | 0 | 1 | 12 |
| 1 | 1 | 0 | 1 | 1 | 13 |
| 1 | 1 | 1 | 0 | 1 | 14 |
| 1 | 1 | 1 | 1 | 1 | 15 |

# 3. Typical Performance Curves

Unless otherwise noted, $V_{CC}$ = 5.5V; CHx = 34V; $T_A$ = +25°C

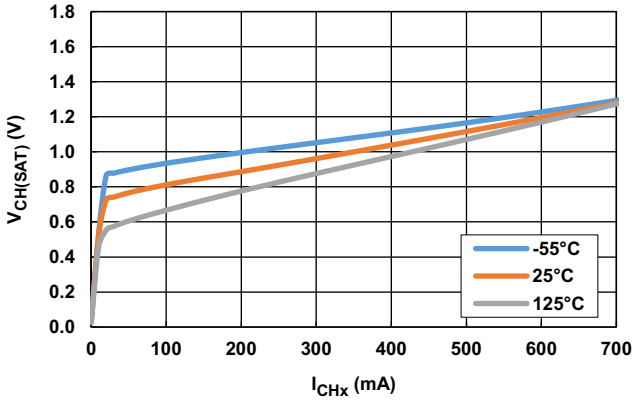



Figure 6. $V_{CH(SAT)}$ vs $I_{CHx}$ vs Temperature

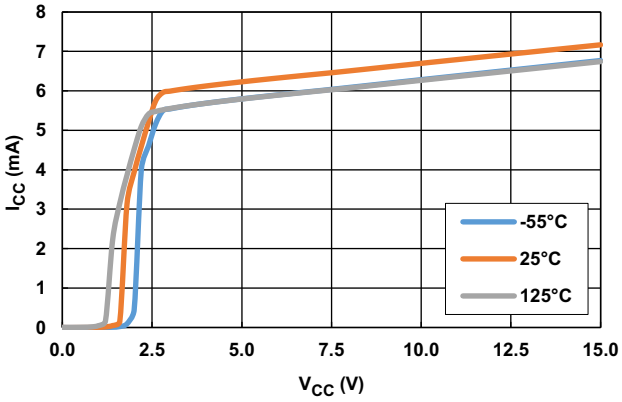



Figure 7. $I_{CC}$ vs $V_{CC}$ vs Temperature

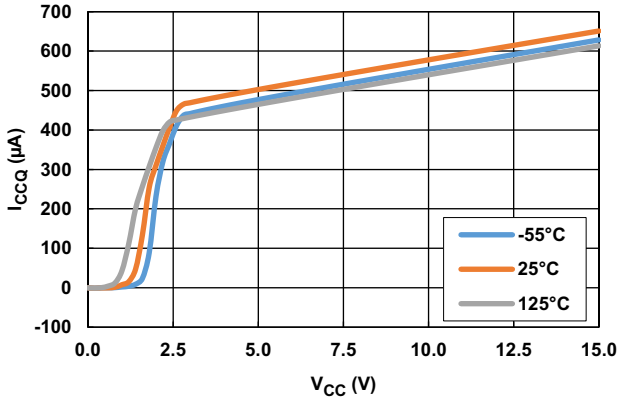



Figure 8. $I_{CCQ}$ vs $V_{CC}$ vs Temperature

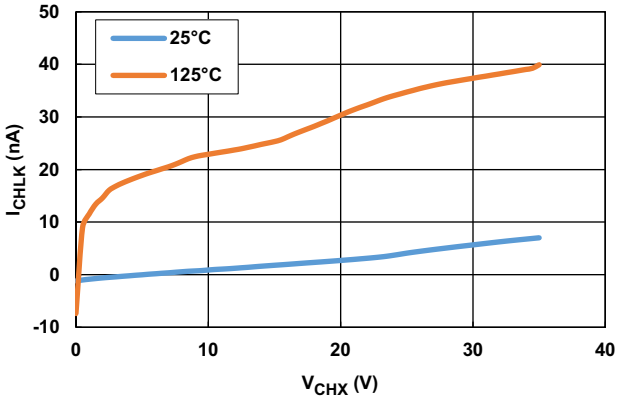



Figure 9. Single Channel Leakage vs Channel Voltage vs Temperature

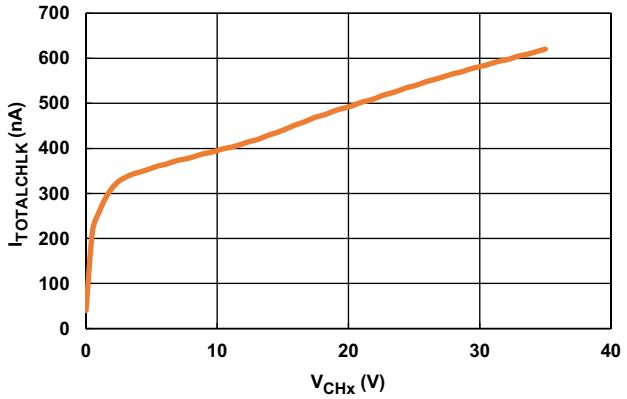



Figure 10. All Channels + COM Leakage Current vs Channel Voltage at +125°C

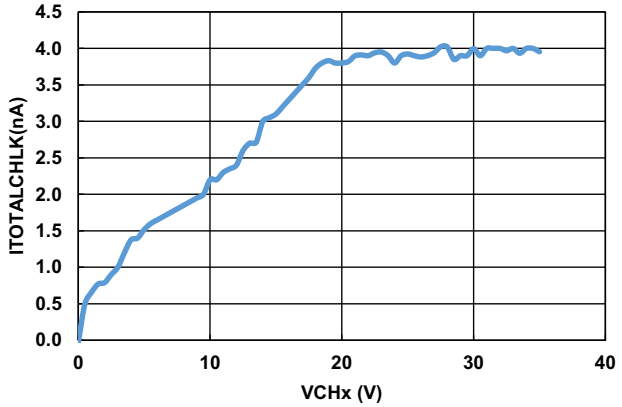



Figure 11. All Channels + COM Leakage Current vs Channel Voltage at +25°C

Unless otherwise noted, $V_{CC}$ = 5.5V; CHx = 34V; $T_A$ = +25°C **(Continued)**

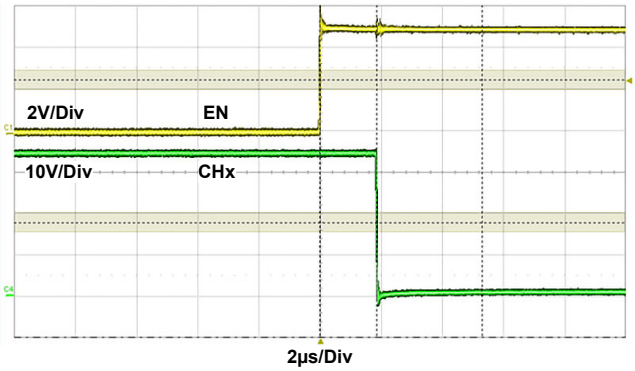



**Figure 12. $T_{ENABLE}$ ($t_{EN}$)**

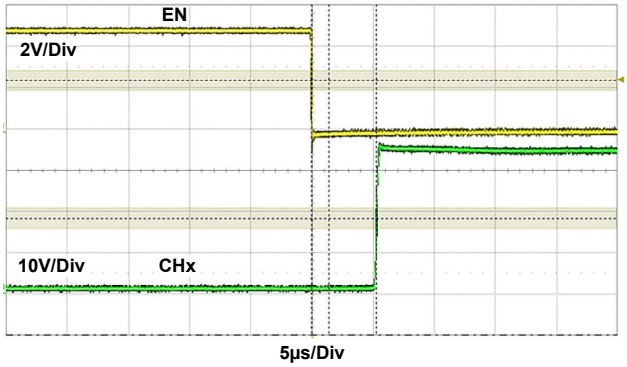



**Figure 13. $T_{DISABLE}$ ($t_{DIS}$)**

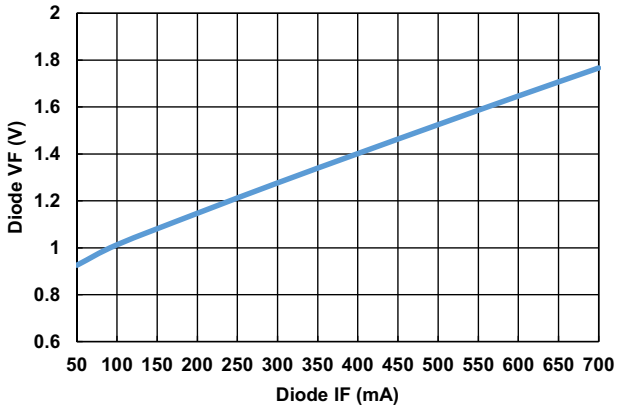



**Figure 14. Clamp Diode Forward Voltage vs Diode Current**

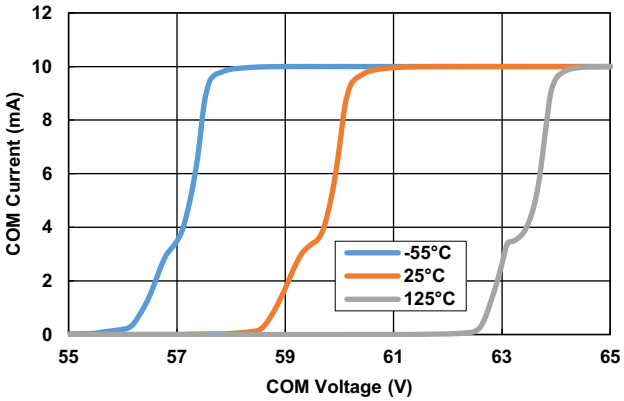



**Figure 15. COM Breakdown Voltage (Current Limited to 10mA)**

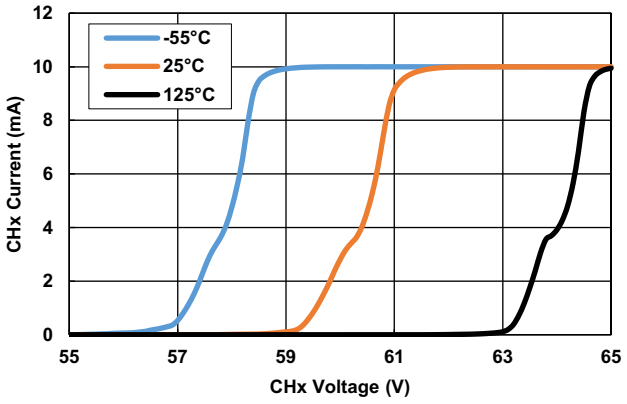



**Figure 16. CHx Channel Breakdown Voltage (Current Limited to 10mA)**

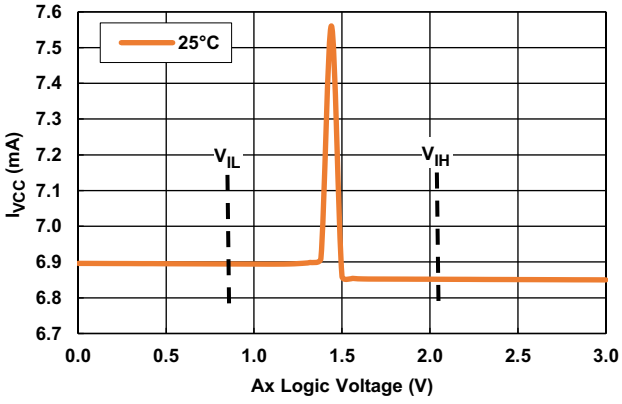



**Figure 17. $I_{VCC}$ vs Ax Logic Voltage vs Temperature**

# 4. Applications Information

## 4.1 Functional Description

The ISL7x814SEH are radiation hardened, high-voltage, high-current, driver circuit ICs fabricated using the Renesas proprietary PR40 silicon-on-insulator process technology to mitigate single-event effects. The devices integrate 16 driver channels that feature a high-voltage (42V), high-current (700mA) open-emitter PNP output stage. The ISL72814SEH and ISL73814SEH integrate a 4-bit, 16-channel decoder with Enable that further reduces the solution size. This allows you to select 1 of 16 available driver channels or to disable all channels.

## 4.2 Ensuring Break-Before-Make (BBM) Operation

The ISL7x814SEH devices do not have internal circuitry to ensure Break-Before-Make (BBM) operation when switching from one channel to another. The design is prone to Make-Before-Break (MBB) operation if the following protocol is not observed and the possibility exists that multiple channels can be momentarily ON when switching from one channel to another.

If the logic settings at the A0-A3 address pins are changed while the output channels remain enabled (EN = High), there is a brief period of time that two or more channels can be on at the same time. Eventually, only the channel that is being addressed continues to be on and the other channels turn off.

During the period when multiple channels are simultaneously on, these channels conduct current through their respective switch cells into GND. This current draw, depending on the loading at the channels, could interfere with proper operation of the application. Care must be taken to prevent MBB operation by properly using the enable pin to implement BBM operation.

Ensuring BBM operation (only one channel on at any time) requires using the enable pin to disable all output channels before switching between channels. Complete the following steps to implement BBM operation:

(1) Before switching from one channel to another, drive the enable pin (EN) to the LOW state (logic 0). This will turn all the channels off.

(2) Wait at least 10µs after taking EN low before proceeding to Step 3. This allows the enable low state change to propagate through the internal logic.

(3) Change the address to select the desired channel by applying the appropriate logic levels to the A0-A3 address pins.

(4) Wait at least 10µs after changing the address state to allow the address change to propagate through the internal logic; then proceed to Step 5.

(5) Drive the enable pin (EN) to the HIGH state (logic 1). This will enable the part. Only the channel that is addressed will be on.

## 4.3 Power Supply Sequencing

Starting with the VCC, COM, EN, CH0-CH15, and A0-A3 pins all at 0V, connect COM to the power supply of the CHx channel with the highest voltage, the recommended power-on sequence is:

(1) VCC: Ramp the $V_{CC}$ supply up no faster than 1V/µs.

(2) COM: Ramp the COM supply up no faster than 1V/µs. Note: You must connect COM to the power supply of the CHx channel with the highest voltage.

(3) A0-A3 Logic Inputs: Apply the correct logic voltages to these pins to select a driver channel.

(4) CH0-CH15: Apply the voltage to the CHx channels.

(5) EN Logic Input: Set to a logic 1 (High) to turn on the channel that is addressed by the logic levels at the A0-A3 logic pins.

Note:

• If VCC is left floating, it is possible for the current driven into the logic inputs to cause the part to begin operating.

• VCC should ramp no faster than 1V/µs to avoid turning ON unintended channels.

## 4.4 COM Pin

Each of the 16 driver channels has an internal kickback diode connected to the COM pin. The kickback diode allows the COM pin to suppress the inductive transient voltage generated when a channel is driven by a relay load. Connecting the COM pin to the same supply as the relay in the system with the highest DC coil voltage clamps any inductive transient voltage generated at a channel by preventing the channel voltage from exceeding the COM voltage by more than clamp diode forward voltage, which for a current of 700mA has a maximum $V_F$ of 2.25V.

Note: If the COM pin is floating, the inductive kickback voltage can easily exceed the 42V breakdown of the driver circuit, which damages the part and other components in the system.

Figure 18 shows a scope plot with the COM pin connected to a $28V_{DC}$ supply and the driver channel CH0 connected to a $28V_{DC}$ relay coil that draws 590mA when the channel is on. When the CH0 channel turns off, the voltage transient at the CH0 channel gets clamped to just a couple of volts above the 28V supply rail by the internal CH0 to COM kickback diode. Testing shows that if COM is left floating, the transient voltage at the CH0 channel while switching off can reach 60V and cause permanent damage to the driver circuit.

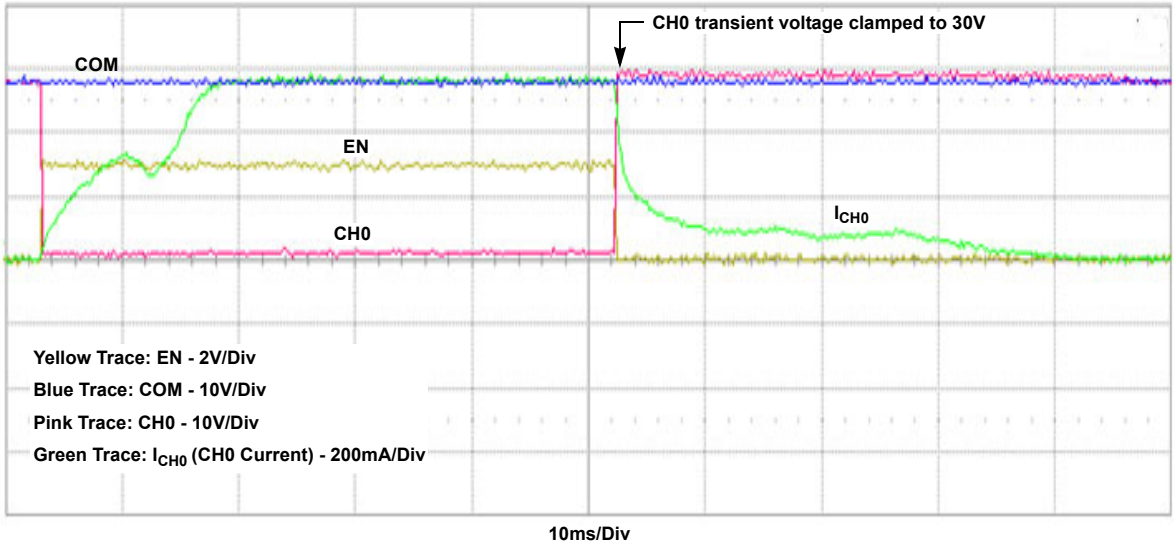



**Figure 18. Plot when Switching $28V_{DC}$, 590mA Relay Coil with COM at $28V_{DC}$**

When switching non inductive loads, tie the COM pin to the supply rail of the channel with the highest DC voltage.

# 5. Die and Assembly Characteristics

**Table 2. Die and Assembly Related Information**

| | |
|---|---|
| **Die Information** | |
| Dimensions | 5461µm x 6350µm (215 mils x 250 mils)<br>Thickness: 482.6µm ±25.4µm (19 mils ± 1 mil) |
| **Interface Materials** | |
| Glassivation | Type: Nitrox<br>Thickness: 15kÅ |
| Top Metallization | Type: AlCu (99.5%/0.5%)<br>Thickness: 30kÅ |
| Backside Finish | Silicon |
| Process | Dielectrically Isolated Advanced Bipolar Technology - PR40 |
| **Assembly Information** | |
| Substrate Potential | Floating |
| **Additional Information** | |
| Worst Case Current Density | $<2 \times 10^5 A/cm^2$ |
| Transistor Count | 2075 |
| Weight of Packaged Device | 2.15 grams (typical) - K28.A package |
| Lid Characteristics | Finish: Gold<br>Lid Potential: GND |

## 5.1 Metallization Mask Layout

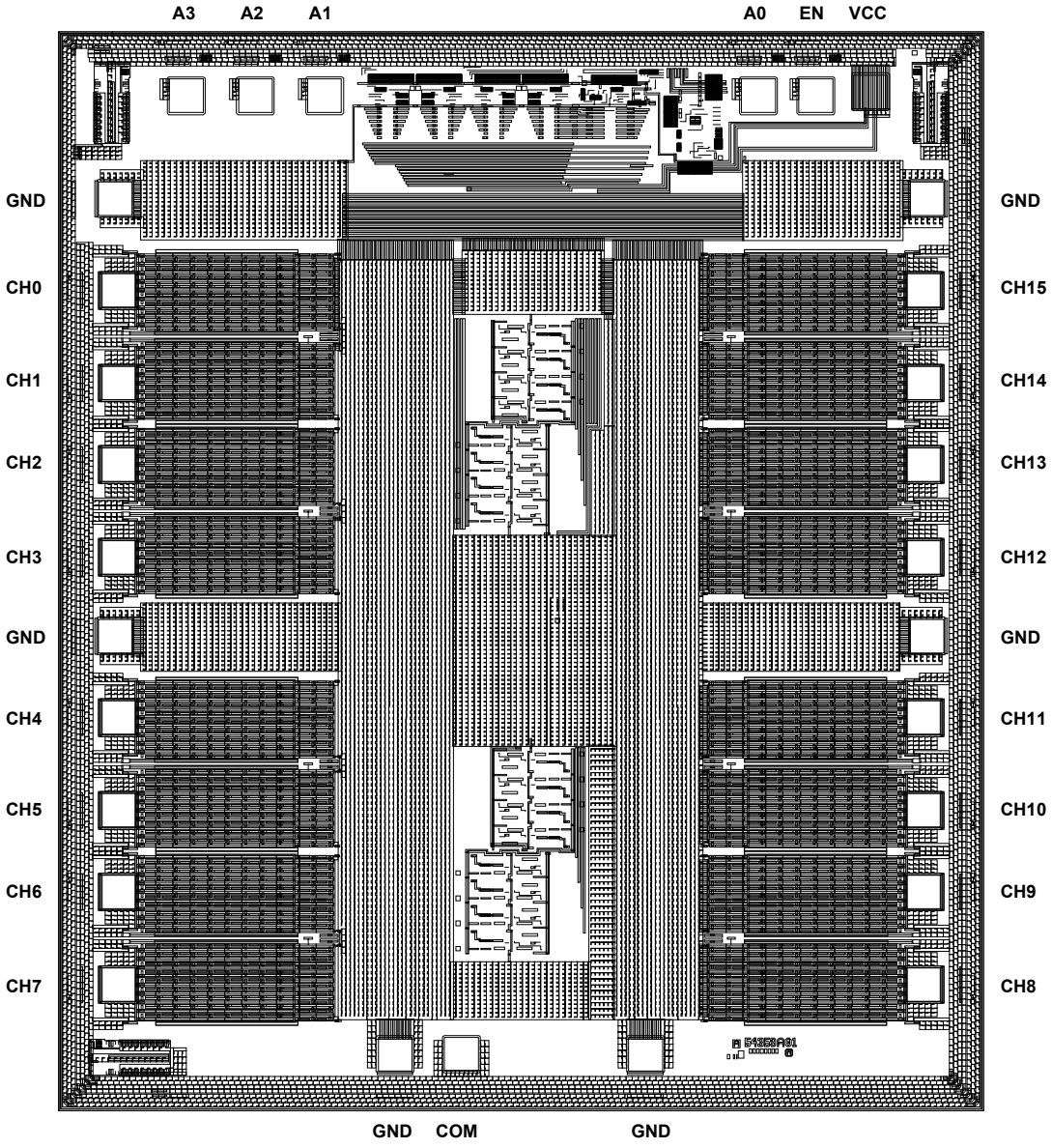


**Table 3. Layout X-Y Coordinates (Centroid of bond pad)**

| Pad Name | Pad Number | X (µm) | Y (µm) |
|---|---|---|---|
| VCC | 1 | 2020.5 | 2771.5 |
| EN | 2 | 1704.0 | 2749.0 |
| A0 | 3 | 1372.0 | 2749.0 |
| A1 | 4 | -1137.0 | 2749.0 |
| A2 | 5 | -1537.0 | 2749.0 |
| A3 | 6 | -1937.0 | 2749.0 |
| GND | 7 | -2347.5 | 2154.5 |
| CH0 | 8 | -2327.0 | 1624.0 |
| CH1 | 9 | -2327.0 | 1088.0 |
| CH2 | 10 | -2327.0 | 616.0 |
| CH3 | 11 | -2327.0 | 80.0 |
| GND | 12 | -2347.5 | -374.5 |
| CH4 | 13 | -2327.0 | -846.0 |
| CH5 | 14 | -2327.0 | -1382.0 |
| CH6 | 15 | -2327.0 | -1854.0 |
| CH7 | 16 | -2327.0 | -2390.0 |
| GND | 17 | -729.0 | -2792.0 |
| COM | 18 | -345.5 | -2792.0 |
| GND | 19 | 719.5 | -2792.0 |
| CH8 | 20 | 2327.0 | -2390.0 |
| CH9 | 21 | 2327.0 | -1854.0 |
| CH10 | 22 | 2327.0 | -1382.0 |
| CH11 | 23 | 2327.0 | -846.0 |
| GND | 24 | 2347.5 | -374.5 |
| CH12 | 25 | 2327.0 | 80.0 |
| CH13 | 26 | 2327.0 | 616.0 |
| CH14 | 27 | 2327.0 | 1088.0 |
| CH15 | 28 | 2327.0 | 1624.0 |
| GND | 29 | 2347.5 | 2154.5 |

Notes:

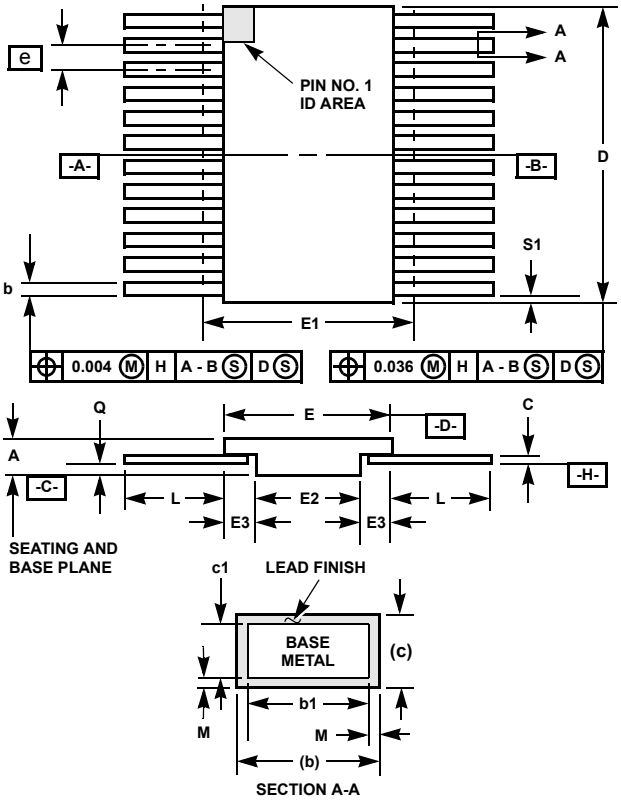
11. Origin of coordinates is the center of the die.
12. Pad size for all pads: 195µm x 195µm.
13. Bond wire size: 0.002”.
14. Pad Number 17 does not get bonded out in the package version.

# 6. Revision History

| Rev. | Date | Description |
|---|---|---|
| 1.00 | Feb 7, 2019 | Initial release |

# 7. Package Outline Drawing

For the most recent package outline drawing, see K28.A.




## K28.A MIL-STD-1835 CDFP3-F28 (F-11A, CONFIGURATION B)

**28 lead ceramic metal seal flatpack package**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | 0.045 | 0.115 | 1.14 | 2.92 | - |
| b | 0.015 | 0.022 | 0.38 | 0.56 | - |
| b1 | 0.015 | 0.019 | 0.38 | 0.48 | - |
| c | 0.004 | 0.009 | 0.10 | 0.23 | - |
| c1 | 0.004 | 0.006 | 0.10 | 0.15 | - |
| D | - | 0.740 | - | 18.80 | 3 |
| E | 0.460 | 0.520 | 11.68 | 13.21 | - |
| E1 | - | 0.550 | - | 13.97 | 3 |
| E2 | 0.180 | - | 4.57 | - | - |
| E3 | 0.030 | - | 0.76 | - | 7 |
| e | 0.050 BSC | | 1.27 BSC | | - |
| k | 0.008 | 0.015 | 0.20 | 0.38 | 2 |
| L | 0.250 | 0.370 | 6.35 | 9.40 | - |
| Q | 0.026 | 0.045 | 0.66 | 1.14 | 8 |
| S1 | 0.00 | - | 0.00 | - | 6 |
| M | - | 0.0015 | - | 0.04 | - |
| N | 28 | | 28 | | - |

Rev. 0 5/18/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

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