ISL71710SLHM

Radiation Hardened Active-Input High Speed Digital Isolator

The ISL71710SLHM is an active input digital signal isolator with CMOS output, using Giant Magnetoresistive (GMR) technology for small size, high speed, and low power. The ISL71710SLHM is the fastest isolator of its type, with a 150Mbps typical data rate. The symmetric magnetic coupling barrier provides a typical propagation delay of only 10ns and a pulse-width distortion as low as 0.3ns, achieving the best specifications of any isolator.

The ISL71710SLHM has unsurpassed common-mode transient immunity of 50kV/µs. It is ideal for isolating applications such as PROFIBUS, RS-485, and RS-422.

The ISL71710SLHM is offered in an 8 Ld 5mmx4mm SOIC package and is fully specified across the military ambient temperature range of -55°C to +125°C.

Applications

- RS-485 and RS-422
- CAN bus/device net
- Multiplexed data transmission
- Data interfaces
- Ground loop elimination
- Peripheral interfaces
- Serial communication
- Logic level shifting
- Isolated power

Features

- Electrically screened to VID V62/23615
- Barrier Voltage Endurance
  - 2.5kV$_{RMS}$ for 1 minute, 600V$_{RMS}$ continuous (VDE V 0884-10 certified: file 5022321-4880-0001)
  - 1.5kV$_{DC}$ continuous
  - 500V$_{DC}$ at 60MeV•cm^2/mg SEDR
- Production testing and qualification follow the AS6294/1 standard (see Radiation Hardened Plastic Production and QCI Flow)
- UL 1577 recognized: file reference E483309
- 5V/3.3V CMOS/TTL compatible
- High speed: 150Mbps typical
- 10ns typical propagation delay
- 300ps typical pulse-width distortion
- 4ns typical propagation delay skew
- 50kV/µs typical common-mode transient immunity
- Low EMI/RFI emissions
- Excellent magnetic immunity
- Passes NASA low outgassing specifications
- NiPdAu-Ag leadframes (Pb-free, Sn-free)
- Full military temperature range operation
  - T_A = -55°C to +125°C
- TID Rad Hard Assurance (RHA) testing
  - Low Dose Rate (LDR) (0.01rad(Si)/s): 75krad(Si)
- SEE characterization
  - No DSEE with V_{DD} = 6.5V at LET 86MeV•cm^2/mg

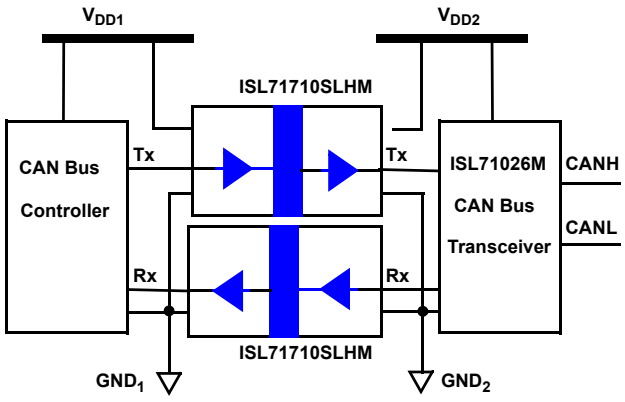


Figure 1. Typical CAN Bus Application

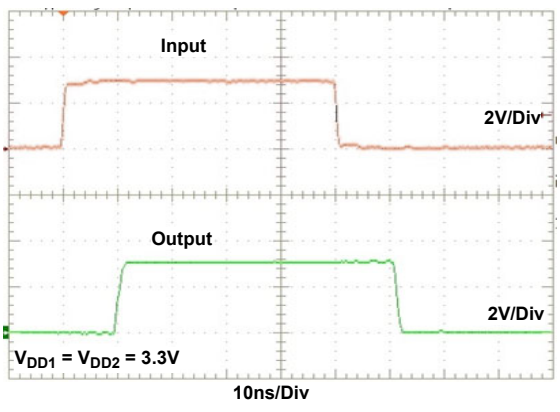
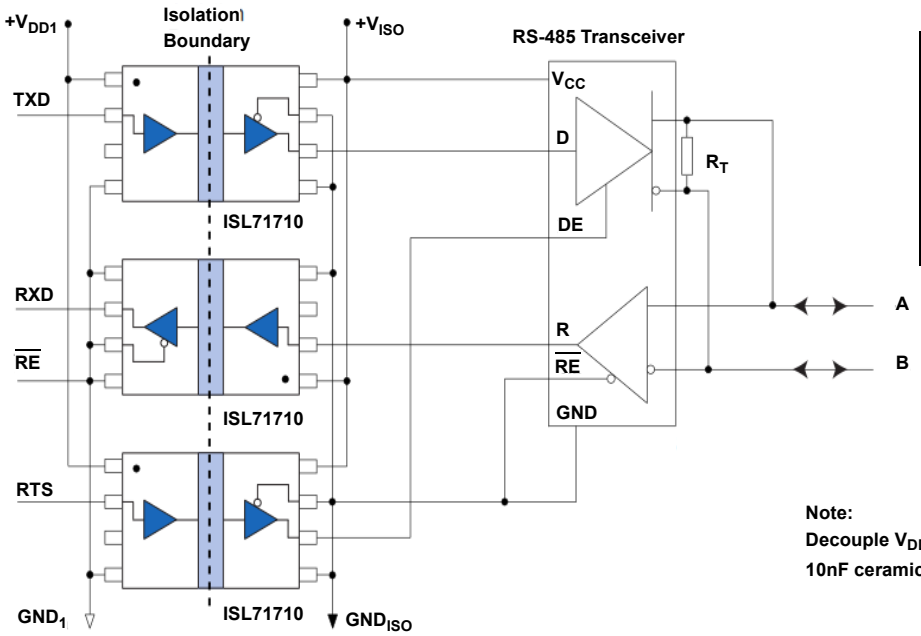


Figure 2. 10MHz Input and Output Waveforms



RS-485 Truth Table

TXD	RTS	A	B	RXD
1	0	Z	Z	X
0	0	Z	Z	X
1	1	1	0	1
0	1	0	1	0

Figure 3. RS-485 Multi-Chip Isolated Transceiver Application Schematic

Contents

1. Overview

1.1 Functional Block Diagram

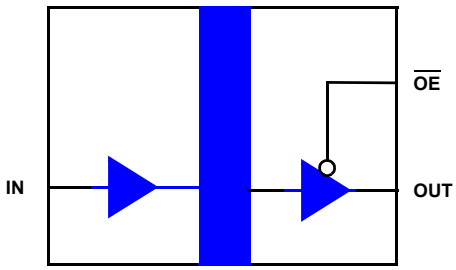
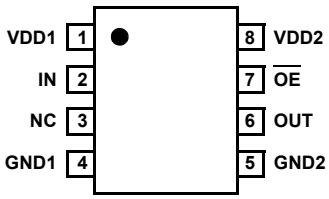


Figure 4. ISL71710SLHM Block Diagram

2. Pin Information

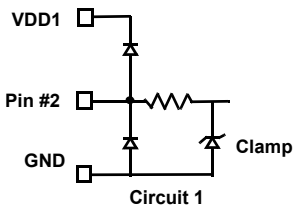
2.1 Pin Assignments

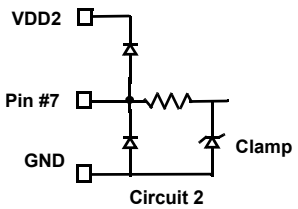


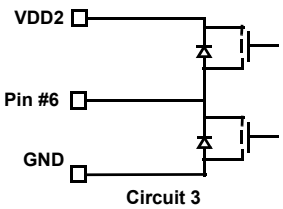
Top View

2.2 Pin Descriptions

Pin Number	Pin Name	ESD Circuit	Description
1	VDD1	N/A	Supply voltage
2	IN	1	Data in
3	NC	N/A	No internal connection. Leave this pin floating or connect it to VDD1 or GND1.
4	GND1	N/A	Ground return for VDD1
5	GND2	N/A	Ground return for VDD2
6	OUT	3	Data output
7	$\overline{OE}$	2	Output enable, active low. Internally pulled low with 100kΩ to enable the output when this pin is not connected.
8	VDD2	N/A	Supply voltage







3. Specifications

3.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
Maximum Supply Voltage, VDD1 to GND1	-0.5	+7	V
Maximum Supply Voltage, VDD2 to GND2	-0.5	+7	V
In-Beam Maximum Supply Voltage VDD1 to GND1	-0.5	+7	V
In-Beam Maximum Supply Voltage VDD2 to GND2	-0.5	+7	V
IN Voltage	-0.5	V_{DD1} + 0.5	V
$\overline{OE}$ Voltage	-0.5	V_{DD2} + 0.5	V
OUT Voltage	-0.5	V_{DD2} + 0.5	V
Output Current Drive	-	10	mA
Human Body Model (Tested per AEC-Q100-002)	-	1.2	kV
Charge Device Model (Tested per AEC-Q100-011)	-	1.5	kV
Latch-up (Tested per JESD-78E; Class 2, Level A) at +125°C	-	100	mA

3.2 Outgas Testing

Specification (Tested per ASTM E 595, 1.5)	Value	Unit
Total Mass Lost[1]	0.06	%
Collected Volatile Condensible Material[1]	<0.01	%
Water Vapor Recovered	0.03	%

1. Outgassing results meet NASA low requirements of total mass loss of <1% and collected volatile condensible material of <0.1%.

3.3 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)[1]	θ_{JC} (°C/W) (Top)	θ_{JC} (°C/W) (Bottom)	Ψ_{JT} (°C/W)[2]
8 Ld NSOIC Package	60	61	37	10

1. θ_{JA} is measured with the component soldered to double-sided board; free air.
2. For Ψ_{JT} characterization parameter, the package top temperature is measured at the top center of the mounted package. See TB379.

Parameter	Minimum	Maximum	Unit
Power Dissipation, P_D	-	675	mW
Maximum Junction Temperature	-	+150	°C
Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	See TB493		

3.4 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Ambient Operating Temperature	-55	+125	°C
Supply Voltage V_{DD1}, V_{DD2}	3.0	5.5	V
IN Logic High Voltage	2.4	V_{DD1}	V
IN Logic Low Voltage	0	0.8	V
$\overline{OE}$ Logic High Voltage	2.4	V_{DD2}	V
$\overline{OE}$ Logic Low Voltage	0	0.8	V
Input Signal Rise and Fall Time	-	1	µs

3.5 Insulation Specifications

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Creepage Distance (external)	-	-	4.03	-	-	mm
Total Barrier Thickness (internal)	-	-	12	13	-	µm
Leakage Current[1]	-	$240V_{RMS}$, 60Hz	-	200	-	nA
Barrier Resistance[1]	R_{IO}	$500V_{DC}$	-	$>10^{14}$	-	Ω
Barrier Capacitance[1]	C_{IO}	1MHz	-	1.1	-	pF
Comparative Tracking Index	CTI	Per IEC:60112	≥175	-	-	V
Working Voltage	V_{IORM}	Per VDE V 0884-10, V084-11 pending	600	-	-	V_{RMS}
Barrier Life	-	100°C, $1000V_{RMS}$, 60% Confidence Level activation energy	-	44000	-	Years

1. Device is considered a two terminal device: Pins 1-4 shorted and Pins 5-8 shorted.

3.6 Safety and Approvals

- VDE V 0884-10 (VDE V 0884-11 pending) (Basic Isolation; VDE File Number 5022321-4880-0001)
  - Working voltage (V_{IORM}): $600V_{RMS}$ ($848V_{PK}$); basic insulation; pollution degree 2
  - Isolation voltage (V_{ISO}): $2500V_{RMS}$
  - Transient overvoltage (V_{IOTM}): $4000V_{PK}$
  - Surge rating: 4000V
  - Each part tested at $1590V_{PK}$ for 1s, 5pC partial discharge limit
  - Samples tested at $4000V_{PK}$ for 60s; then $1358V_{PK}$ for 10s with 5pC partial discharge limit

Safety-Limiting Values	Symbol	Value	Unit
Safety Rating Ambient Temperature	T_S	+180	°C
Safety Rating Power	P_S	270	mW
Supply Current Safety Rating (Total of Supplies)	I_S	54	mA

- UL 1577 (Component Recognition Program File Number E483309)
  - Each part tested at $3000V_{RMS}$ ($4240V_{PK}$) for 1s; each lot sample tested at $2500V_{RMS}$ ($3530V_{PK}$) for 1min

3.7 Electrical Specifications

Unless otherwise noted, V_{DD1} V_{DD2} = 3V - 5.5V; OUT and $\overline{OE}$ are open, V_{DD1} and V_{DD2} are bypassed to GND with a 47nF X7R capacitor; $T_A = T_J$ = +25°C. Limits apply across the operating temperature range, -55°C to +125°C unless otherwise stated.

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
3.3V Electrical Specifications						
Input Quiescent Supply Current Figure 12	I_{DD1}	-	-	4	40	µA
		Post Radiation 75krad(Si)	-	2.6	2.8	mA
Output Quiescent Supply Current Figure 13	I_{DD2}	-	-	1.2	1.75	mA
Logic Input Current	I_I	-	-10	-	10	µA
Logic High Output Voltage Figure 20	V_{OH}	I_O = -20µA, $V_I = V_{IH}$	V_{DD} - 0.1	V_{DD}	-	V
		I_O = -4mA, $V_I = V_{IH}$	0.8 x V_{DD}	0.9 x V_{DD}	-	V
Logic Low Output Voltage Figure 21	V_{OL}	I_O = 20µA, $V_I = V_{IL}$	-	0	0.1	V
		I_O = 4mA, $V_I = V_{IL}$	-	0.5	0.8	V
Switching Specifications (V_{DD} = 3.3V)						
Maximum Data Rate		C_L = 15pF	130	140	-	Mbps
Pulse Width[2]	PW	50% Points, V_O	10	7.5	-	ns
Propagation Delay Input to Output (High-to-Low) Figure 14	t_{PHL}	C_L = 15pF	-	12	18	ns
Propagation Delay Input to Output (Low-to-High) Figure 15	t_{PLH}	C_L = 15pF	-	12	18	ns
Propagation Delay Enable to Output (High-to-High Impedance) Figure 22	t_{PHZ}	C_L = 15pF	-	3	7	ns
Propagation Delay Enable to Output (Low-to-High Impedance) Figure 23	t_{PLZ}	C_L = 15pF	-	3	7	ns
Propagation Delay Enable to Output (High Impedance-to-High) Figure 24	t_{PZH}	C_L = 15pF	-	3	7	ns
Propagation Delay Enable to Output (High Impedance-to-Low) Figure 25	t_{PZL}	C_L = 15pF	-	3	7	ns
Pulse-Width Distortion[3] Figure 18	PWD	C_L = 15pF	-	1	4	ns
Pulse Jitter[4]	t_J	C_L = 15pF	-	100		ps
Propagation Delay Skew[5]	t_{PSK}	C_L = 15pF	-	4	6	ns
Output Rise Time (10% to 90%) Figure 16	t_R	C_L = 15pF	-	2	5	ns
Output Fall Time (10% to 90%) Figure 17	t_F	C_L = 15pF	-	2	5	ns
Common-Mode Transient Immunity (Output Logic High or Logic Low)[6]	$\|CM_H\|,\|CM_L\|$	V_{CM} = 1500V_{DC}, $t_{TRANSIENT}$ = 25ns	30	50	-	kV/µs
Dynamic Power Consumption[7], Figure 19	-	-	-	140	240	µA/Mbps
		Post Radiation 75krad(Si)	-	400	450	µA/Mbps
Magnetic Field Immunity[8] (V_{DD2} = 3V, 3V < V_{DD1} < 5.5V)						
Power Frequency Magnetic Immunity	H_{PF}	50Hz/60Hz	1000	1500	-	A/m
Pulse Magnetic Field Immunity	H_{PM}	t_P = 8µs	1800	2000	-	A/m

Unless otherwise noted, V_{DD1} V_{DD2} = 3V - 5.5V; OUT and $\overline{OE}$ are open, V_{DD1} and V_{DD2} are bypassed to GND with a 47nF X7R capacitor; $T_A = T_J$ = +25°C. Limits apply across the operating temperature range, -55°C to +125°C unless otherwise stated. **(Cont.)**

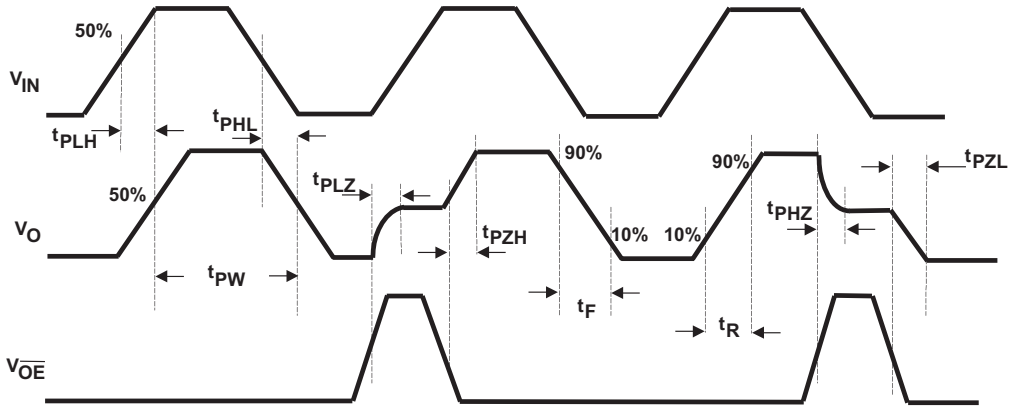
Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Damped Oscillatory Magnetic Field	H_{OSC}	0.1Hz - 1MHz	1800	2000	-	A/m
Cross-Axis Immunity Multiplier[9]	K_X	-	-	2.5	-	-
5V Electrical Specifications						
Input Quiescent Supply Current Figure 12	I_{DD1}	-	-	6	75	µA
		Post Radiation 75krad(Si)	-	3	3.4	mA
Output Quiescent Supply Current Figure 13	I_{DD2}	-	-	1.8	2.5	mA
Logic Input Current	I_I	-	-10	-	10	µA
Logic High Output Voltage Figure 20	V_{OH}	I_O = -20µA, $V_I = V_{IH}$	V_{DD} - 0.1	V_{DD}	-	V
		I_O = -4mA, $V_I = V_{IH}$	0.8 x V_{DD}	0.9 x V_{DD}	-	V
Logic Low Output Voltage Figure 21	V_{OL}	I_O = 20µA, $V_I = V_{IL}$	-	0	0.1	V
		I_O = 4mA, $V_I = V_{IL}$	-	0.5	0.8	V
Switching Specifications (V_{DD} = 5V)						
Maximum Data Rate	-	C_L = 15pF	130	150	-	Mbps
Pulse Width[2]	PW	50% Points, V_O	10	7.5	-	ns
Propagation Delay Input to Output (High-to-Low) Figure 14	t_{PHL}	C_L = 15pF	-	10	16	ns
Propagation Delay Input to Output (Low-to-High) Figure 15	t_{PLH}	C_L = 15pF	-	10	16	ns
Propagation Delay Enable to Output (High-to-High Impedance) Figure 22	t_{PHZ}	C_L = 15pF	-	3	7	ns
Propagation Delay Enable to Output (Low-to-High Impedance) Figure 23	t_{PLZ}	C_L = 15pF	-	3	7	ns
Propagation Delay Enable to Output (High Impedance-to-High) Figure 24	t_{PZH}	C_L = 15pF	-	3	7	ns
Propagation Delay Enable to Output (High Impedance-to-Low) Figure 25	t_{PZL}	C_L = 15pF	-	3	7	ns
Pulse-Width Distortion[3], Figure 18	PWD	C_L = 15pF	-	0.3	4	ns
Propagation Delay Skew[5]	t_{PSK}	C_L = 15pF	-	4	6	ns
Output Rise Time (10% to 90%) Figure 16	t_R	C_L = 15pF	-	1	4	ns
Output Fall Time (10% to 90%) Figure 17	t_F	C_L = 15pF	-	1	4	ns
Common Mode Transient Immunity (Output Logic High or Logic Low)[6]	$\|CM_H\|$,$\|CM_L\|$	V_{CM} = 1500V_{DC}, $t_{TRANSIENT}$ = 25ns	30	50	-	kV/µs
Dynamic Power Consumption [7], Figure 19	-	-	-	200	340	µA/Mbps
		Post Radiation 75krad(Si)	-	480	530	µA/Mbps

Unless otherwise noted, V_{DD1} V_{DD2} = 3V - 5.5V; OUT and $\overline{OE}$ are open, V_{DD1} and V_{DD2} are bypassed to GND with a 47nF X7R capacitor; $T_A = T_J$ = +25°C. Limits apply across the operating temperature range, -55°C to +125°C unless otherwise stated. **(Cont.)**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Magnetic Field Immunity[8] (V_{DD2} = 5V, 3V < V_{DD1} < 5.5V)						
Power Frequency Magnetic Immunity	H_{PF}	50Hz/60Hz	2800	3500	-	A/m
Pulse Magnetic Field Immunity	H_{PM}	t_P = 8µs	4000	4500	-	A/m
Damped Oscillatory Magnetic Field	H_{OSC}	0.1Hz - 1MHz	4000	4500	-	A/m
Cross-axis Immunity Multiplier[9]	K_X	-	-	2.5	-	-

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
2. Minimum pulse width is the minimum value at which specified PWD is ensured.
3. PWD is defined as $|t_{PHL} - t_{PLH}|$. %PWD is equal to PWD divided by pulse width.
4. 66535-bit pseudo-random binary signal (PRBS) NRZ bit pattern with no more than five consecutive 1s or 0s; 800ps transition time.
5. t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} between devices at +25°C.
6. CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CML is the maximum common-mode input voltage that can be sustained while maintaining $V_O < 0.8V$. The common-mode voltage slew rate apply to both rising and falling common-mode voltage edges.
7. Dynamic power consumption is calculated per channel and is supplied by the input side power supply of the channel.
8. The relevant test and measurement methods are given in Electromagnetic Compatibility.
9. External magnetic field immunity is improved by this factor if the field direction is end-to-end rather than pin-to-pin (see Figure 26).

3.8 Timing Diagram



Legend

t_{PLH}	Propagation Delay, Low-to-High
t_{PHL}	Propagation Delay, High-to-Low
t_{PW}	Minimum Pulse Width
t_{PLZ}	Propagation Delay, Low-to-High Impedance
t_{PZH}	Propagation Delay, High Impedance-to-High
t_{PHZ}	Propagation Delay, High-to-High Impedance
t_{PZL}	Propagation Delay, High Impedance-to-Low
t_R	Rise Time
t_F	Fall Time

Figure 5. Timing Diagram

4. Typical Performance Curves

T_A = +25°C, unless otherwise specified.

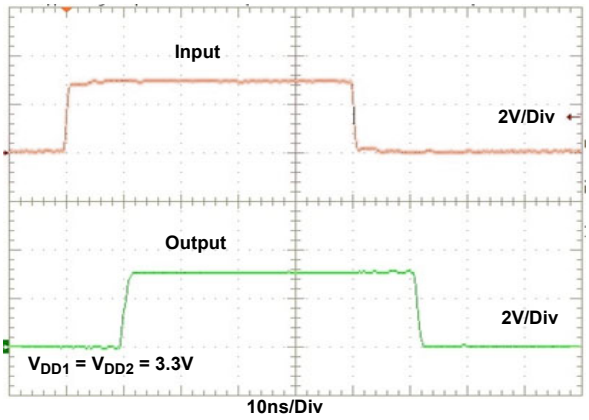


Figure 6. 10MHz Input and Output Waveforms

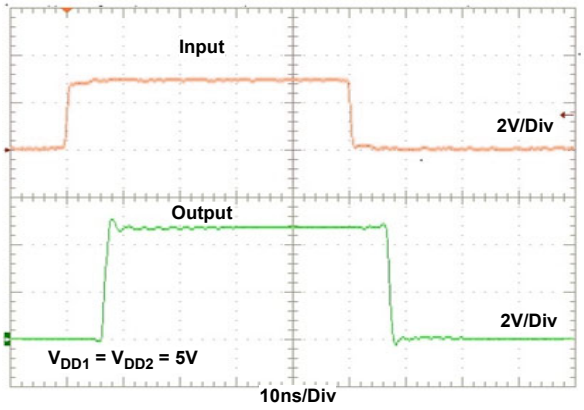


Figure 7. 10MHz Input and Output Waveforms

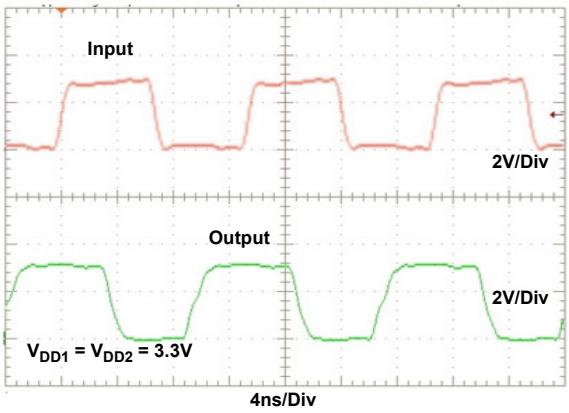


Figure 8. 75MHz Input and Output Waveforms

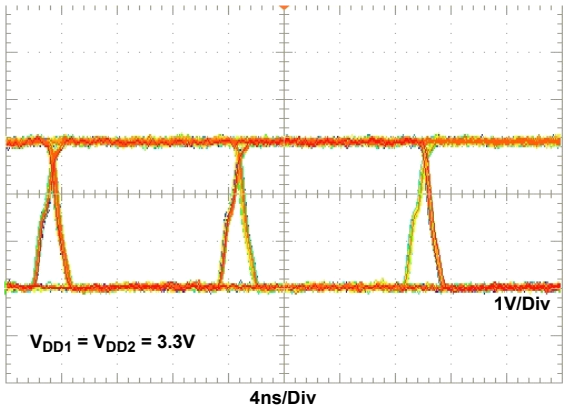


Figure 9. 75Mbps Eye Diagram

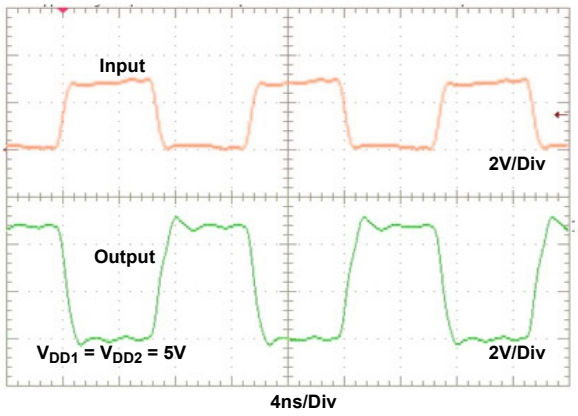


Figure 10. 75MHz Input and Output Waveforms

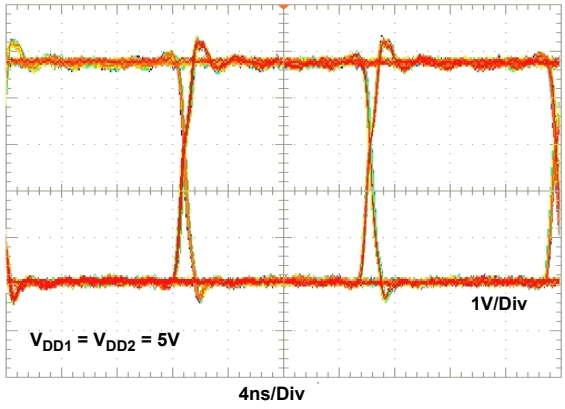


Figure 11. 75Mbps Eye Diagram

T_A = +25°C, unless otherwise specified. (Cont.)

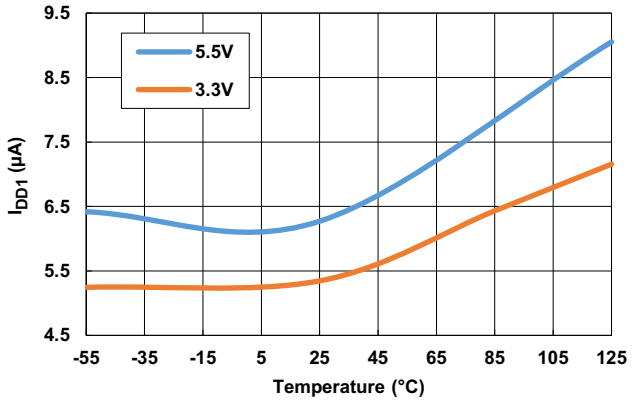


Figure 12. Input Quiescent Supply Current vs Temperature vs V_{DD1} Voltage

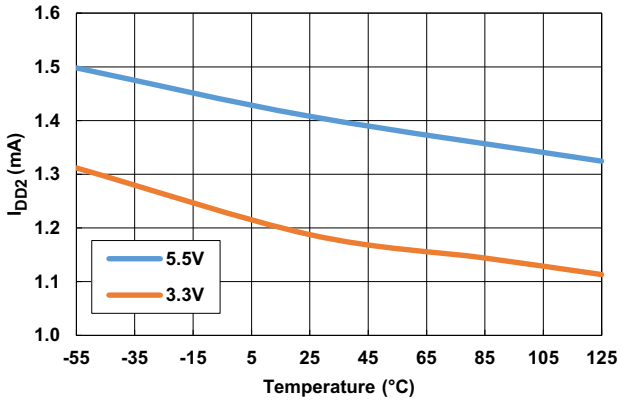


Figure 13. Output Quiescent Supply Current vs Temperature vs V_{DD2} Voltage

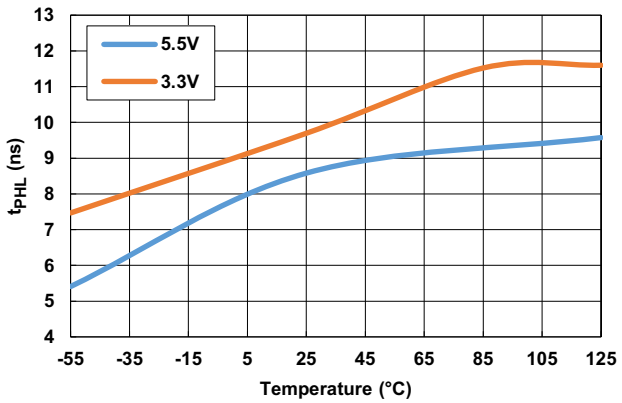


Figure 14. Propagation Delay (High-to-Low) vs Temperature vs V_{DD} Voltage

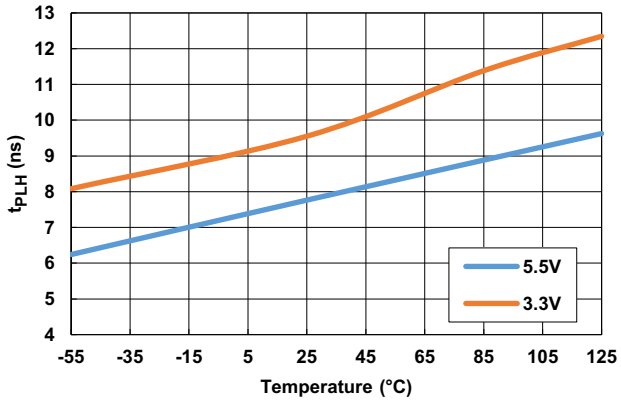


Figure 15. Propagation Delay (Low-to-High) vs Temperature vs V_{DD} Voltage

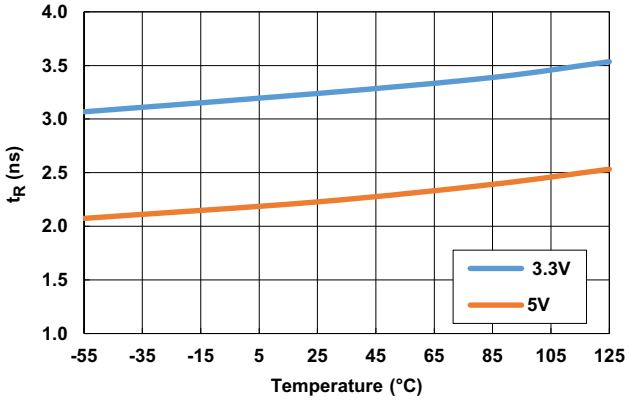


Figure 16. Output Rise Time vs Temperature vs V_{DD} Voltage

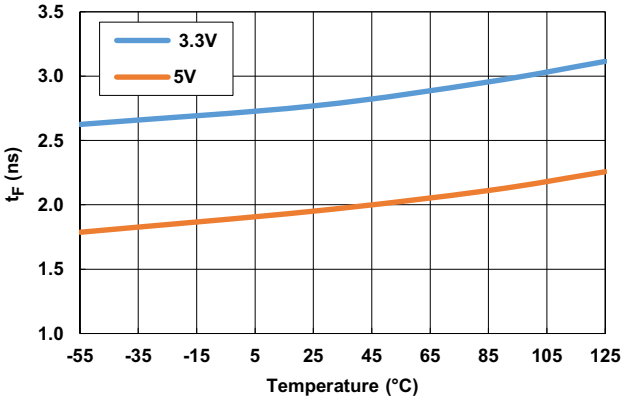


Figure 17. Output Fall Time vs Temperature vs V_{DD} Voltage

T_A = +25°C, unless otherwise specified. (Cont.)

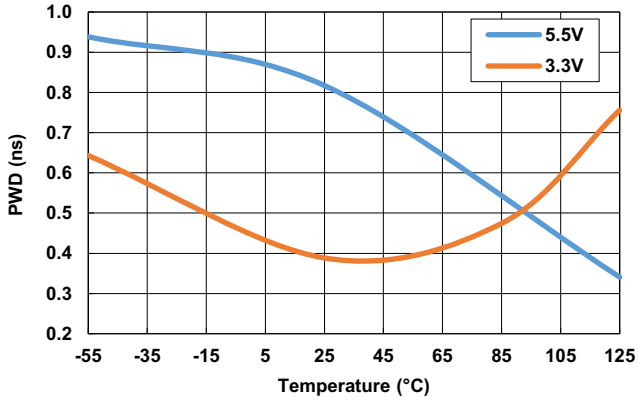


Figure 18. 5.5V Pulse-Width Distortion vs Temperature vs V_{DD} Voltage

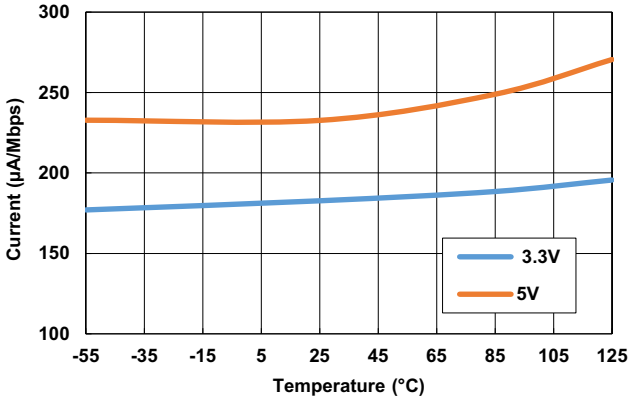


Figure 19. Dynamic Power Consumption vs Temperature

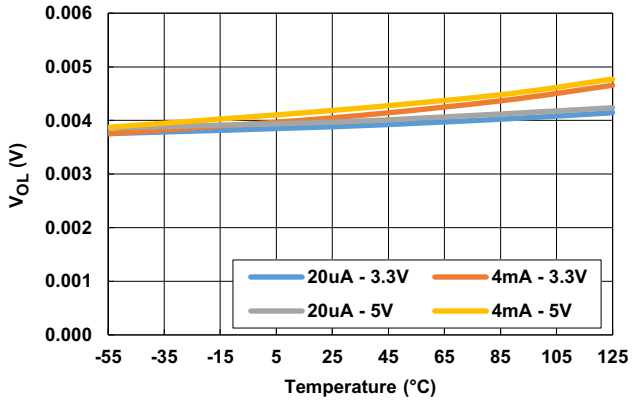


Figure 20. Logic Low Output Voltage vs Temperature

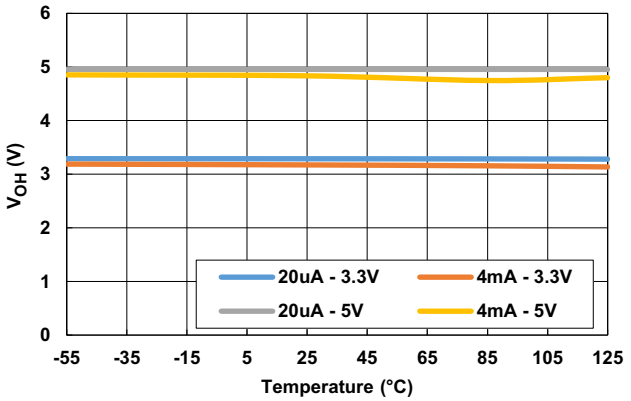


Figure 21. Logic High Output Voltage vs Temperature

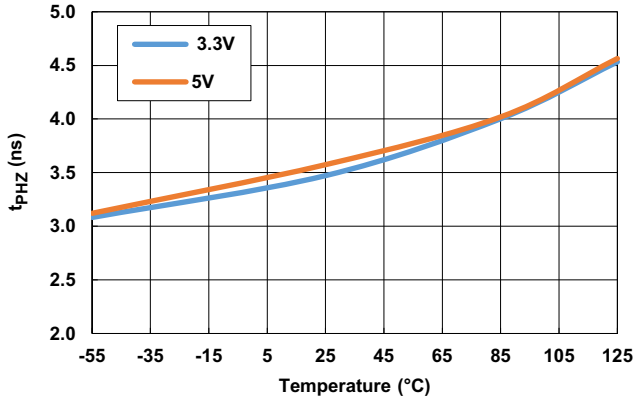


Figure 22. Propagation Delay Enable to Output (High-to-High Impedance) vs Temperature

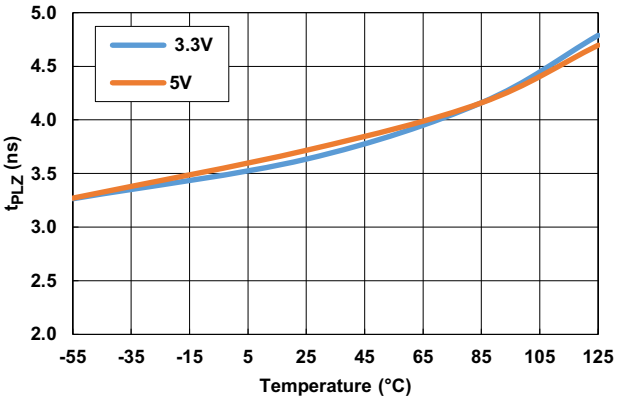


Figure 23. Propagation Delay Enable to Output (Low-to-High Impedance) vs Temperature

T_A = +25°C, unless otherwise specified. (Cont.)

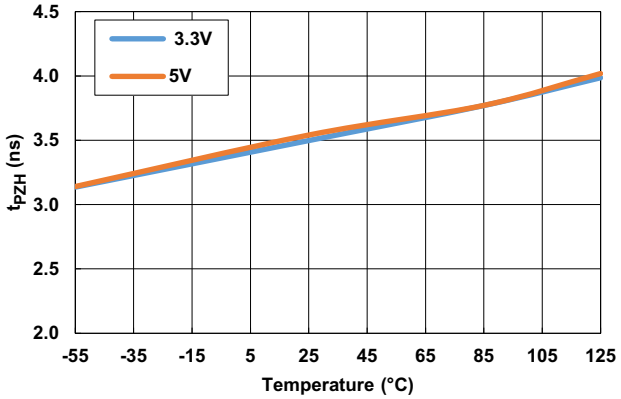


Figure 24. Propagation Delay Enable to Output (High Impedance-to-High) vs Temperature

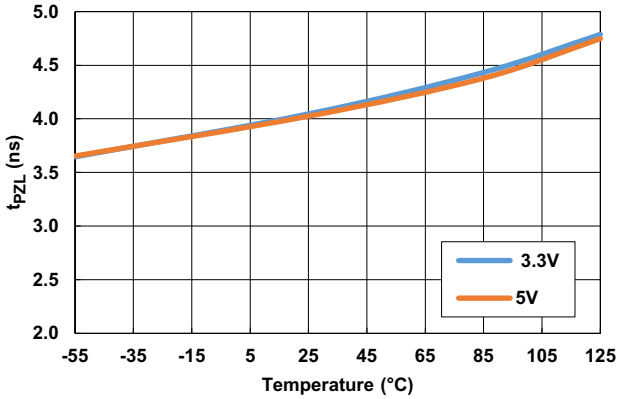


Figure 25. Propagation Delay Enable to Output (High Impedance-to-Low) vs Temperature

5. Device Information

5.1 Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in Absolute Maximum Ratings. However, Renesas recommends that all integrated circuits are handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

5.2 Electromagnetic Compatibility

The ISL71710SLHM has the lowest EMC footprint of any isolation technology. Its Wheatstone bridge configuration and differential magnetic field signaling ensure excellent EMC performance against all relevant standards.

Immunity to external magnetic fields is even higher if the field direction is end-to-end rather than pin-to-pin as shown in Figure 26:

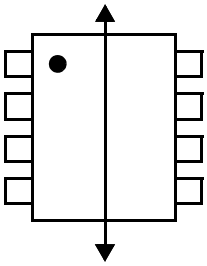


Figure 26. Cross-Axis Field Direction

5.3 Dynamic Power Consumption

The ISL71710SLHM achieves its low power consumption from the way it transmits data across the isolation barrier. By detecting the edge transitions of the input logic signal and converting these to narrow current pulses, a magnetic field is created around the GMR Wheatstone bridge. Depending on the direction of the magnetic field, the bridge causes the output comparator to switch following the input logic signal. The power consumption is independent of mark-to-space ratio and solely dependent on frequency, because the current pulses are narrow, about 2.5ns. This has obvious advantages over optocouplers, which have power consumption heavily dependent on mark-to-space ratio.

5.4 Power Supply Decoupling

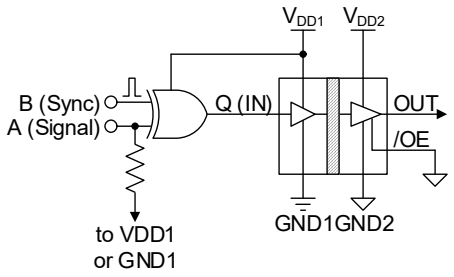
Decouple both power supplies to this device with low ESR 47nF ceramic capacitors. Ground planes for both GND1 and GND2 are highly recommended for data rates above 10Mbps. Capacitors must be located as close as possible to the VDD pins.

5.5 Signal Status on Start-Up

To minimize power dissipation, input signals are differentiated and then per GMR technology magnetically latched on the output side of the isolation barrier. Here, the latched state of the GMR resistor bridge on the isolator's secondary side is independent of the secondary supply, V_{DD2}. Applying V_{DD2} only enables the comparator to detect the GMR bridge voltage and to reconstruct the output signal electrically.

Magnetic latching has the advantage that the magnetic state of the GMR bridge remains, even during a loss of V_{DD2}. However, it can also lead to an indeterminate output state after power-up, shutdown, and power loss sequencing events.

To ensure that the isolator is in a known output state, the input signal must be EXOR-ed with a sync-pulse (see Figure 27). Here, the required output state after power-up is defined by the logic state of EXOR input A. When V_{DD1} is fully established, applying a sync-pulse (low – high – low) to EXOR input B causes a pulse at the isolator input (IN). This latches the logic state at input A into the GMR bridge across the barrier. *Note*: The pulse width at IN must be ≥10ns. After the application of the sync pulse, powering up V_{DD2}, the isolator output assumes the required output state.



Sig A	Sync B	IN Q
0	0	0
	1	1
	0	0
1	0	1
	1	0
	0	1

Figure 27. Sync Circuit with EXOR Truth Table

Complete the following supply sequencing steps to ensure the output starts in a known output state:

1. Start with V_{DD1}, V_{DD2}, and /OE being at 0V.
2. Apply V_{DD1}.
3. After V_{DD1} is fully established, apply the sync-pulse at input B. Ensure that the pulse width at IN is ≥10ns.
4. Apply V_{DD2}. Observe that V_{OUT} starts in the state set by input A.

5.6 Data Transmission Rates

The reliability of a transmission system is directly related to the accuracy and quality of the transmitted digital information. For a digital system, parameters that determine the limits of the data transmission are pulse-width distortion and propagation delay skew.

Propagation delay is the time taken for the signal to travel through the device. This is usually different when sending a low-to-high signal than when sending a high-to-low signal. This difference, or error, is called Pulse-Width Distortion (PWD) and is usually in nanoseconds. It may also be expressed as a percentage:

- PWD% = [Maximum Pulse-Width Distortion (ns)/Signal Pulse Width (ns)] x 100%

For example, with data rates of 12.5Mbps:

- PWD% = [3ns/80ns] x 100% = 3.75%

This figure is almost three times better than any available optocoupler with the same temperature range, and two times better than any optocoupler regardless of published temperature range. The ISL71710SLHM exceeds the 10% maximum PWD recommended by PROFIBUS, and runs to nearly 35Mbps within the 10% limit.

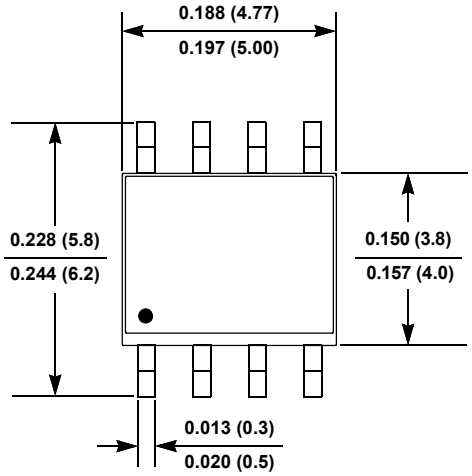
Propagation delay skew is the signal propagation difference between two or more channels. This becomes significant in clocked systems because it is undesirable for the clock pulse to arrive before the data has settled. Short propagation delay skew is therefore especially critical in high data rate parallel systems for establishing and maintaining accuracy and repeatability. Worst-case channel-to-channel skew in an ISL71710SLHM isolator is only 4ns, which is ten times better than any optocoupler. ISL71710SLHM isolators have a maximum propagation delay skew of 6ns, which is five times better than any optocoupler.

6. Package Outline Drawing

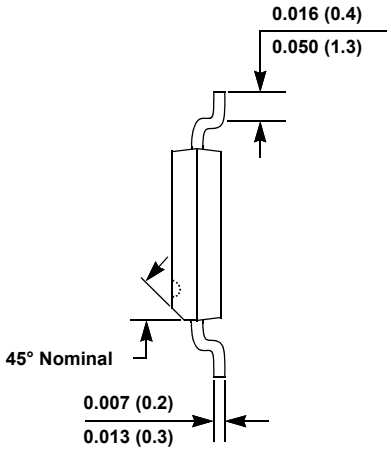
For the most recent package outline drawing, see M8.15G.

M8.15G

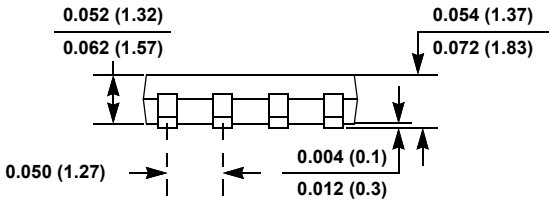
8 Lead Narrow Body Small Outline Plastic Package
Rev 2, 10/18



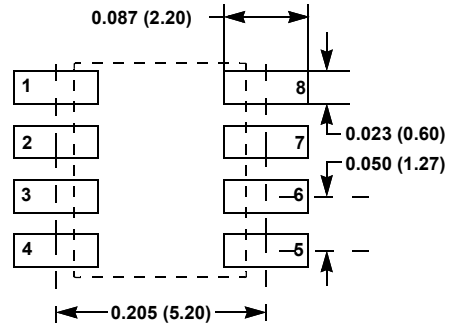
Top View



Side View



End View



Typical Recommended Land Pattern

Notes:
1. Dimensions in inches (mm); scale = approximately 5X.
2. Pin spacing is a BASIC dimension; tolerances do not accumulate.

7. Ordering Information

Part Number[1][2]	Part Marking	Radiation Tolerance (Total Ionizing Dose)	Package Description (RoHS Compliant)	Pkg. Dwg #	Carrier Type	Temp. Range
ISL71710SLHMBZ	71710MBZ	LDR to 75krad(Si)	8 Ld NSOIC	M8.15G	Tray	-55 to +125°C
ISL71610-710EV1Z	Evaluation Board					

1. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate-e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the Product Options on the ISL71710SLHM product page (click the packaging icon). For more information about MSL, see TB363.

8. Revision History

Revision	Date	Description
1.02	Feb 4, 2026	Updated Signal Status on Start-Up section.
1.01	Dec 1, 2023	Updated Features section.
1.00	Jul 26, 2021	Initial release

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