Datasheet

ISL71218M

Dual 36V Precision Single-Supply, Rail-to-Rail Output, Low-Power Operational Amplifier

Description

The ISL71218M is a radiation tolerant dual, low-power precision amplifier optimized for single-supply applications. This op amp features a common-mode input voltage range extending to 0.5V below the V^- rail, a rail-to-rail differential input voltage range, and rail-to-rail output voltage swing, which makes it ideal for single-supply applications where input operation at ground is important.

This op amp features low-power, low-offset voltage, and low-temperature drift, making it ideal for applications requiring both high DC accuracy and AC performance. It is designed to operate over a single supply range of 3V to 36V, or a split supply voltage range of +1.8V/-1.2V to ±18V. The combination of precision and small footprint provides the user with outstanding value and flexibility relative to similar competitive parts.

Applications for these amplifiers include precision instrumentation, data acquisition, and precision power supply controls.

The ISL71218M is available in an 8 Ld SOIC and operates across the extended temperature range of -55°C to +125°C.

Applications

- Low Earth orbit
- High altitude avionics
- Precision instruments
- Data acquisition
- Power supply control

Features

- Qualified to Renesas Rad Tolerant Screening and QCI Flow (R34TB0004EU)
- Passes NASA low outgassing specifications
- Wide single and dual supply range: 3V to 30V (±10%)
- Low current consumption: 850µA, typical
- Low input offset voltage: 40µV, typical
- Rail-to-rail output: <10mV
- NiPdAu-Ag lead finish
- Dielectrically isolated PR40 process
- Rail-to-rail input differential voltage range for comparator applications
- Operating temperature range: -55°C to +125°C
- Below-ground (V^-) input capability to -0.5V
- Low noise voltage: 5.6nV/√Hz, typical
- Low noise current: 355fA/√Hz, typical
- Offset voltage temperature drift: 0.3µV/°C, typical
- No phase reversal
- TID Radiation Lot Acceptance Testing (RLAT) (LDR ≤10mrad(Si)/s)
  - ISL71218M30BZ: 30krad(Si)
  - ISL71218M50BZ: 50krad(Si)
- SEE Characterization
  - No DSEE with V_S = ±20V at 43MeV•cm^2/mg
  - $|V_{OUT}$ SET$|$ < 10% at 28MeV•cm^2/mg

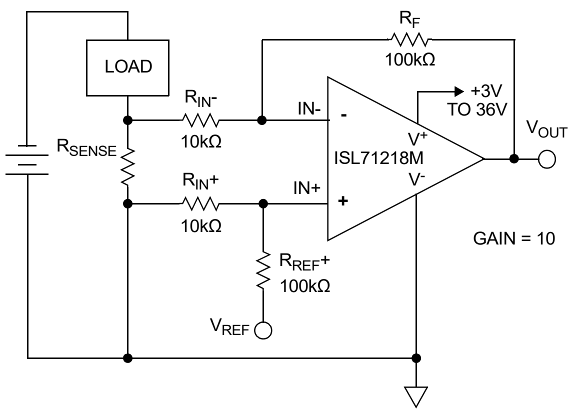


Figure 1. Typical Application: Single-Supply, Low-Side Current Sense Amplifier

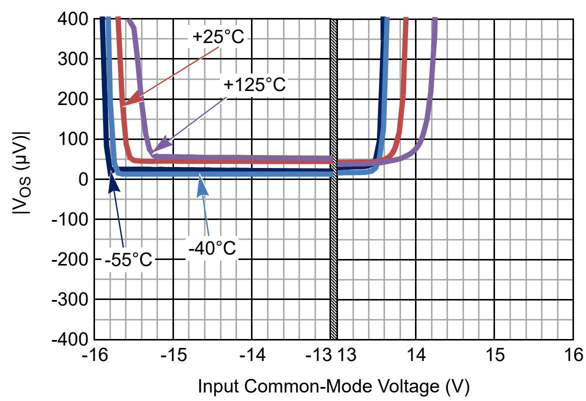


Figure 2. Input Offset Voltage vs Input Common-Mode Voltage, V_S = ±15V

Contents

1. Pin Information

1.1 Pin Assignments

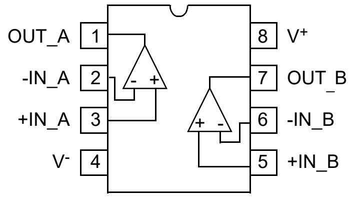
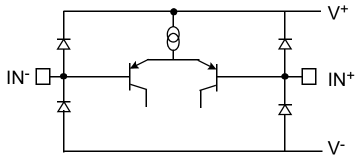


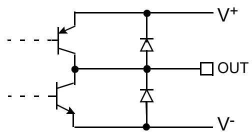
Figure 3. Pin Assignments - Top View

1.2 Pin Descriptions

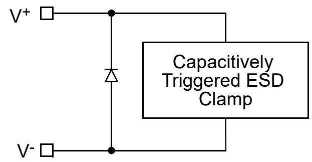
Pin Number	Pin Name	Equivalent Circuit	Description
1	OUT_A	Circuit 2	Amplifier A output
2	-IN_A	Circuit 1	Amplifier A inverting input
3	+IN_A	Circuit 1	Amplifier A non-inverting input
4	V-	Circuit 1, 2, 3	Negative power supply
5	+IN_B	Circuit 1	Amplifier B non-inverting input
6	-IN_B	Circuit 1	Amplifier B inverting input
7	OUT_B	Circuit 2	Amplifier B output
8	V+	Circuit 1, 2, 3	Positive power supply



Circuit 1



Circuit 2



Circuit 3

2. Specifications

2.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
Maximum Supply Voltage	-	42	V
Maximum Supply Voltage[1]	-	40	V
Maximum Differential Input Current	-	20	mA
Maximum Differential Input Voltage	V^- - 0.5	V^+ + 0.5	V
Minimum/Maximum Input Voltage	V^- - 0.5	V^+ + 0.5	V
Minimum/Maximum Input Current	-	±20	mA
Output Short-Circuit Duration (1 output at a time)	-	Indefinite	
Storage Temperature Range	-65	+150	°C
Human Body Model (Tested per JS-001-2014)	-	5.5	kV
Machine Model (Tested per JESD22-A115-C)	-	300	V
Charged Device Model (Tested per JS-002-2014)	-	2	kV
Latch-Up (Tested per JESD78E; Class 2, Level A)	-	100 at +125°C	mA

1. Tested in a heavy ion environment at LET = 43MeV•cm^2/mg at +125°C (TC) for SEB.

2.2 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Ambient Operating Temperature Range	-55	+125	°C
Maximum Operating Junction Temperature	-	+150	°C
Single Supply Voltage	3	30	V
Dual Supply Voltage	+1.8/-1.2	±15	V

2.3 Outgas Testing

Specification (Tested per ASTM E595, 1.5)	Value	Unit
Total Mass Lost[1]	0.06	%
Collected Volatile Condensible Material [1]	<0.01	%
Water Vapor Recovered	0.03	%

1. Outgassing results meet NASA requirements of total mass loss <1% and collected volatile condensible material of <0.1%.

2.4 Thermal Information

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	8 Ld SOIC Package	θ_{JA}[1]	Junction to ambient	105	°C/W
		θ_{JC}[2]	Junction to case	50	°C/W

1. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379.
2. For θ_{JC}, the case temperature location is the package top center.

2.5 Electrical Specifications

2.5.1 V_S = ±15V

V_S ±15V, V_{CM} = 0, V_O = 0V, R_L = Open, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL71218M30BZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL71218M50BZ).**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Offset Voltage	V_{OS}	-	-230	40	230	µV
			-320	-	**320**	µV
Offset Voltage Drift	TCV_{OS}	-	-	0.3	**1.4**	µV/°C
Input Offset Voltage Match Channel-to-Channel	ΔV_{OS}	-	-	44	280	µV
			-	-	**365**	µV
Input Offset Current	I_{OS}	-	-50	4	50	nA
			-75	-	**75**	nA
Input Bias Current	I_B	-	-575	-135	-	nA
			-800	-	-	nA
Common-Mode Input Voltage Range	V_{CMIR}	Ensured by CMRR Test	(V^-) - 0.5	-	(V^+) - 1.8	V
			V^-	-	**(V^+) - 1.8**	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = V^- to V^+ -1.8V	100	120	-	dB
		V_{CM} = V^- to V^+ -1.8V	**97**	-	-	dB
Power Supply Rejection Ratio	PSRR	V_S = 3V to 40V, V_{CMIR} = Valid input voltage	105	124	-	dB
			100	-	-	dB
Open-Loop Gain	A_{VOL}	R_L = 10kΩ to ground, V_O = -13V to +13V	120	130	-	dB
			115	-	-	dB
Output Voltage High, V^+ to V_{OUT}	V_{OH}	R_L = 10kΩ	-	-	110	mV
			-	-	**120**	mV
Output Voltage Low, V_{OUT} to V^-	V_{OL}	R_L = 10kΩ	-	-	80	mV
			-	-	**90**	mV
Supply Current/Amplifier	I_S		-	0.85	1.10	mA
			-	-	**1.40**	mA
Source Current Capability	I_{S+}		**10**	20	-	mA
Sink Current Capability	I_{S-}		**10**	32	-	mA
Supply Voltage Range	V_{SUPPLY}	Ensured by PSRR Test	3	-	30	V
AC Specifications						
Gain Bandwidth Product	GBW	A_{CL} = 101, V_{OUT} = 100mV$_{P-P}$; R_L = 2k	-	4	-	MHz
Voltage Noise	e_{np-p}	0.1Hz to 10Hz, V_S = ±18V	-	300	-	nV$_{P-P}$
Voltage Noise Density	e_n	f = 10Hz, V_S = ±18V	-	8.5	-	nV/√Hz
		f = 100Hz, V_S = ±18V	-	5.8	-	nV/√Hz
		f = 1kHz, V_S = ±18V	-	5.6	-	nV/√Hz
		f = 10kHz, V_S = ±18V	-	5.6	-	nV/√Hz
Current Noise Density	in	f = 1kHz, V_S = ±18V	-	355	-	fA/√Hz
Total Harmonic Distortion + Noise	THD + N	1kHz, G = 1, V_O = 3.5V$_{RMS}$, R_L = 10kΩ	-	0.0003	-	%

V_S ±15V, V_{CM} = 0, V_O = 0V, R_L = Open, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL71218M30BZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL71218M50BZ). (Cont.)**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Transient Response						
Slew Rate	SR	A_V = 1, R_L = 2kΩ, V_O = $10V_{P-P}$	±1.0	±1.2	-	V/µs
			±0.4	-	-	V/µs
Rise Time 10% to 90% of V_{OUT}	t_r, t_f, Small Signal	A_V = 1, V_{OUT} = $100mV_{P-P}$, R_f = 0Ω, R_L = 2kΩ to V_{CM}	-	100	200	ns
			-	-	**400**	ns
Fall Time 90% to 10% of V_{OUT}		A_V = 1, V_{OUT} = $100mV_{P-P}$, R_f = 0Ω, R_L = 2kΩ to V_{CM}	-	100	230	ns
			-	-	**400**	ns
Settling Time to 0.01% 10V Step; 10% to V_{OUT}	t_s	A_V = 1, V_{OUT} = $10V_{P-P}$, R_f = 0Ω R_L = 2kΩ to V_{CM}	-	8.5	-	µs
Positive Overshoot	OS+	A_V = 1, V_{OUT} = $10V_{P-P}$, R_f = 0Ω R_L = 2kΩ to V_{CM}	-	5	-	%
			-	-	**20**	%
Negative Overshoot	OS-	A_V = 1, V_{OUT} = $10V_{P-P}$, R_f = 0Ω R_L = 2kΩ to V_{CM}	-	5	-	%
			-	-	**20**	%

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

2.5.2 V_S = ±5V

V_S ±5V, V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL71218M30BZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL71218M50BZ).**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Offset Voltage	V_{OS}	-	230	40	230	µV
			-320	-	**320**	µV
Input Offset Voltage Match Channel-to-Channel	ΔV_{OS}	-	-	44	280	µV
			-	-	**365**	µV
Input Offset Current	I_{OS}	-	-50	4	50	nA
			-75	-	**75**	nA
Input Bias Current	I_B	-	-575	-135	-	nA
			-800	-	-	nA
Common-Mode Input Voltage Range	V_{CMIR}	Ensured by CMRR Test	$(V^-) - 0.5$	-	$(V^+) - 1.8$	V
			V^-	-	**$(V^+) - 1.8$**	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = V^- - 0.5V to V^+ - 1.8 V_{CM} = V^- to V^+ - 1.8V	92	117	-	dB
			79	-	-	dB
Power Supply Rejection Ratio	PSRR	V_S = 3V to 40V, V_{CMIR} = Valid input voltage	102	120	-	dB
			98	-	-	dB
Open-Loop Gain	A_{VOL}	R_L = 10kΩ to ground V_O = -3V to +3V	115	130	-	dB
			112	-	-	dB
Output Voltage High, V^+ to V_{OUT}	V_{OH}	R_L = 10kΩ	-	36	65	mV
			-	-	**70**	mV
Output Voltage Low, V_{OUT} to V^-	V_{OL}	R_L = 10kΩ	-	28	45	mV
			-	-	**50**	mV

V_S ±5V, V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL71218M30BZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL71218M50BZ). (Cont.)**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Supply Current/Amplifier	I_S	-	-	0.74	1.10	mA
			-	-	**1.40**	mA
Source Current Capability	I_{S+}	T_A = +25°C, +125°C	10	13	-	mA
		T_A = -55°C	6	-	-	mA
Sink Current Capability	I_{S-}	-	**10**	23	-	mA
AC Specifications						
Gain Bandwidth Product	GBW	-	-	3.2	-	MHz
Voltage Noise	e_{np-p}	0.1Hz to 10Hz	-	320	-	nV_{P-P}
Voltage Noise Density	e_n	f = 10Hz	-	9	-	nV/√Hz
Voltage Noise Density	e_n	f = 100Hz	-	5.7	-	nV/√Hz
Voltage Noise Density	e_n	f = 1kHz	-	5.5	-	nV/√Hz
Voltage Noise Density	e_n	f = 10kHz	-	5.5	-	nV/√Hz
Current Noise Density	in	f = 1kHz	-	380	-	fA/√Hz
Total Harmonic Distortion + Noise	THD + N	1kHz, G = 1, V_O = 1.25V_{RMS}, R_L = 10kΩ	-	0.0003	-	%
Transient Response						
Slew Rate	SR	A_V = 1, R_L = 2kΩ, V_O = 4V_{P-P}	-	±1	-	V/µs
Rise Time 10% to 90% of V_{OUT}	t_r, t_f, Small Signal	A_V = 1, V_{OUT} = 100mV_{P-P} , R_f = 0Ω, R_L = 2kΩ to V_{CM}	-	100	-	ns
Fall Time 90% to 10% of V_{OUT}		A_V = 1, V_{OUT} = 100mV_{P-P} , R_f = 0Ω, R_L = 2kΩ to V_{CM}	-	100	-	ns
Settling Time to 0.01% 4V Step; 10% to V_{OUT}	t_s	A_V = 1, V_{OUT} = 4V_{P-P}, R_f = 0Ω R_L = 2kΩ to V_{CM}	-	4	-	µs
Positive Overshoot	OS+	A_V = 1, V_{OUT} = 10V_{P-P}, R_f = 0Ω R_L = 2kΩ to V_{CM}	-	5	-	%
Negative Overshoot	OS-	A_V = 1, V_{OUT} = 10V_{P-P}, R_f = 0Ω R_L = 2kΩ to V_{CM}	-	5	-	%

Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

3. Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified.

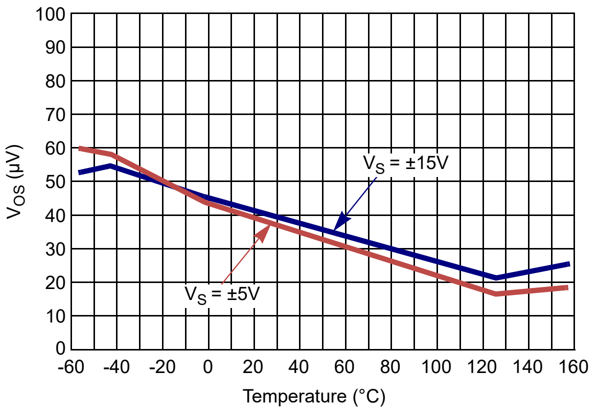


Figure 4. V_{OS} vs Temperature

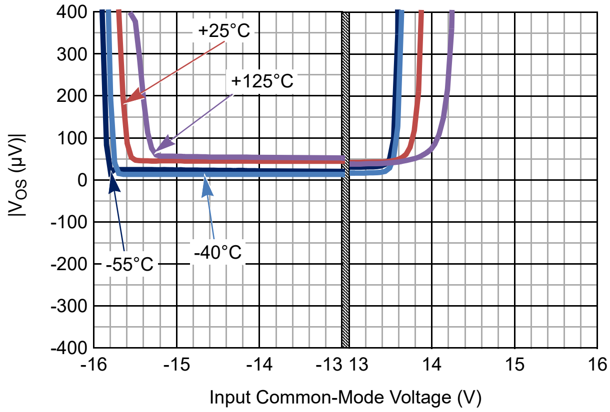


Figure 5. Input Offset Voltage vs Input Common-Mode Voltage, V_S = ±15V

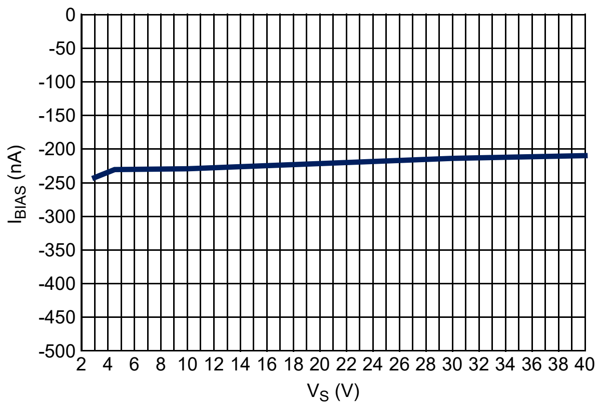


Figure 6. I_{BIAS} vs V_S

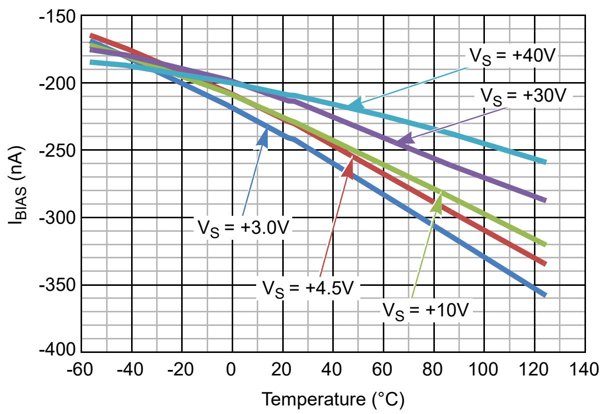


Figure 7. I_{BIAS} vs Temperature vs Supply

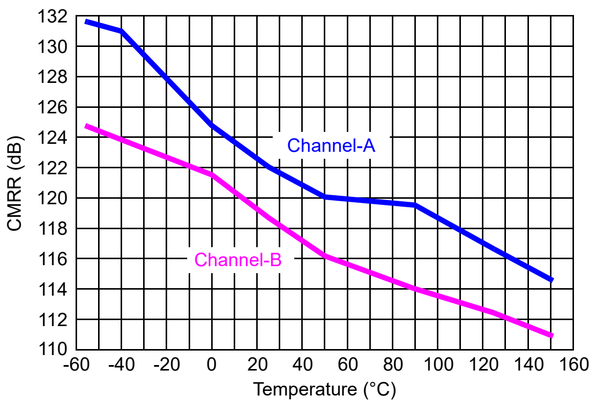


Figure 8. CMRR vs Temperature, V_S = ±15V

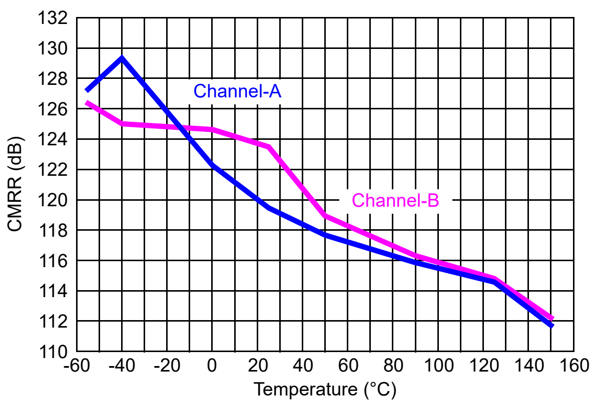


Figure 9. CMRR vs Temperature, V_S = ±5V

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. (Cont.)

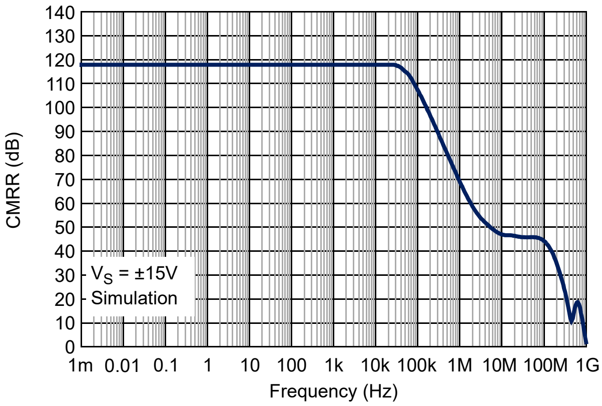


Figure 10. CMRR vs Frequency, V_S = ±15V

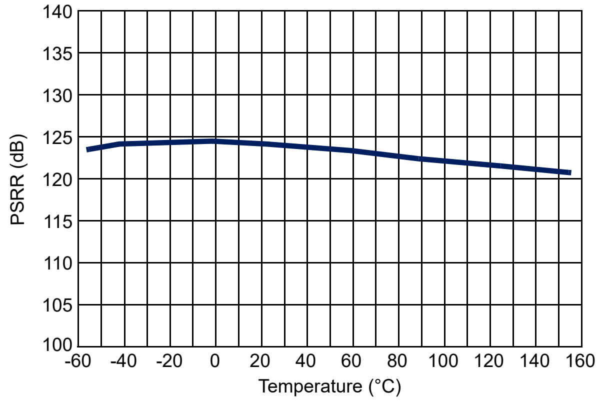


Figure 11. PSRR vs Temperature, V_S = ±15V

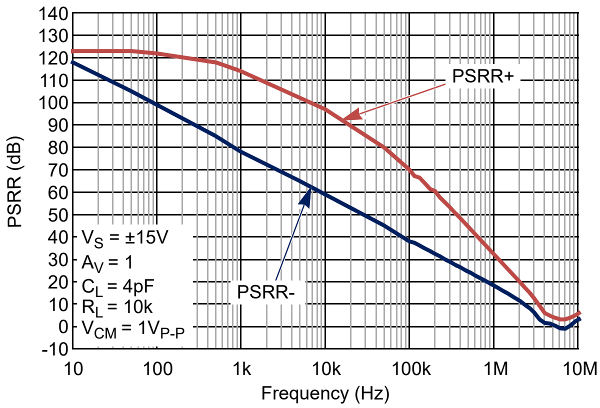


Figure 12. PSRR vs Frequency, V_S = ±15V

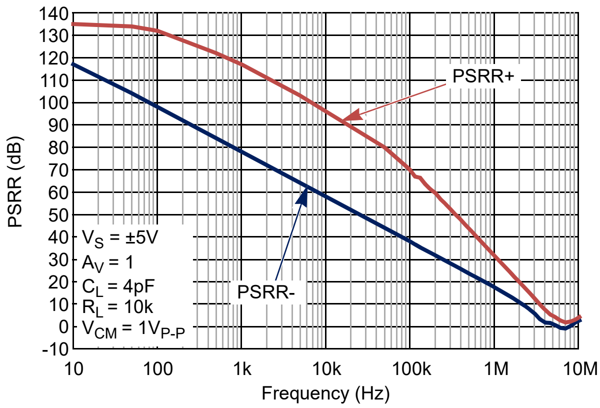


Figure 13. PSRR vs Frequency, V_S = ±5V

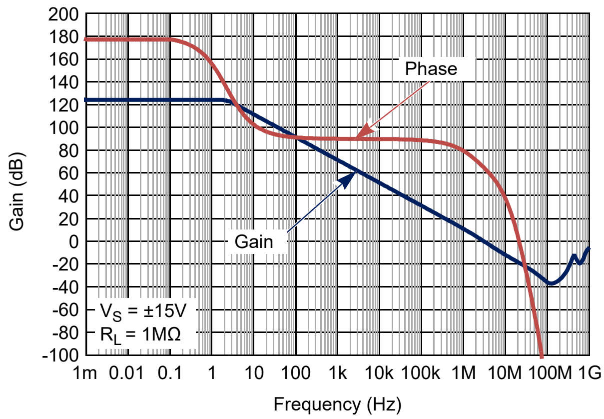


Figure 14. Open-Loop Gain, Phase vs Frequency, V_S = ±15V

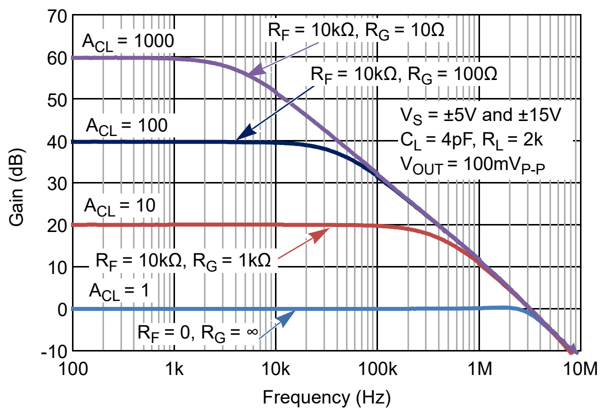


Figure 15. Frequency Response vs Closed-Loop Gain

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. (Cont.)

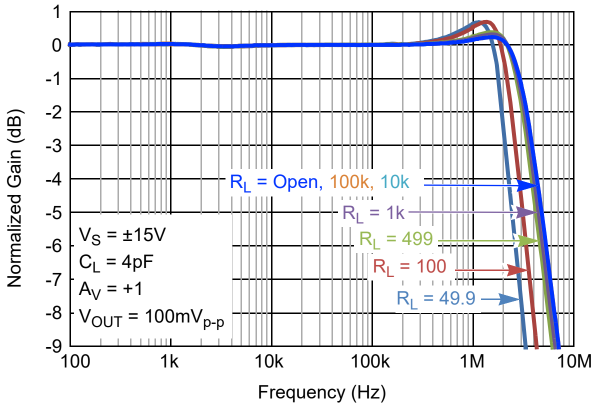


Figure 16. Gain vs Frequency vs R_L, V_S = ±15V

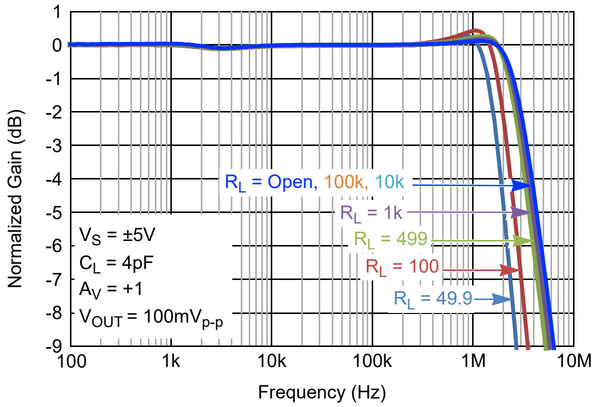


Figure 17. Gain vs Frequency vs R_L, V_S = ±5V

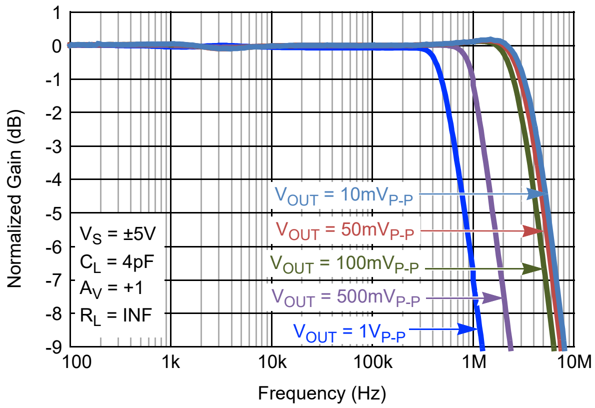


Figure 18. Gain vs Frequency vs Output Voltage

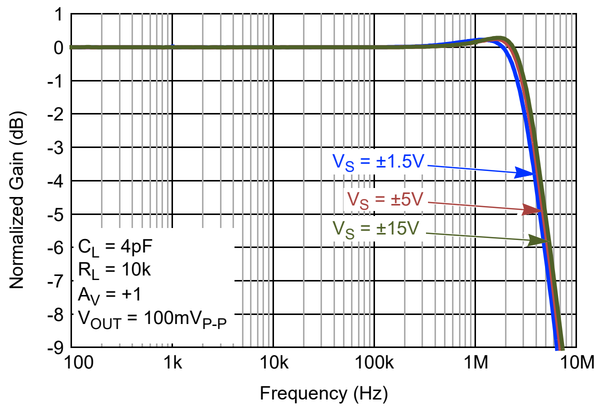


Figure 19. Gain vs Frequency vs Supply Voltage

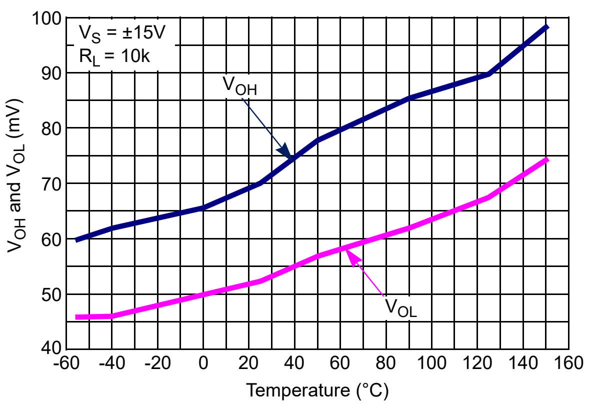


Figure 20. Output Overhead Voltage vs Temperature, V_S = ±15V, R_L = 10k

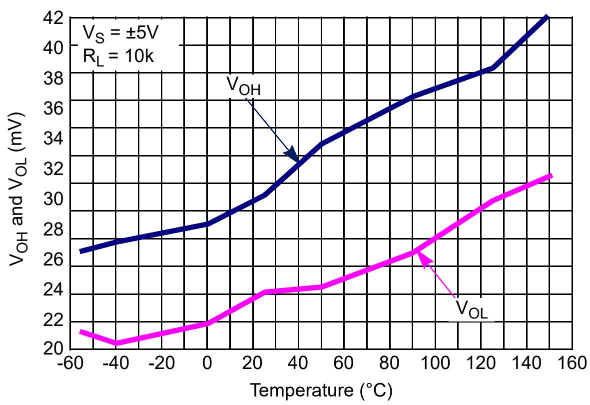


Figure 21. Output Overhead Voltage vs Temperature, V_S = ±5V, R_L = 10k

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. (Cont.)

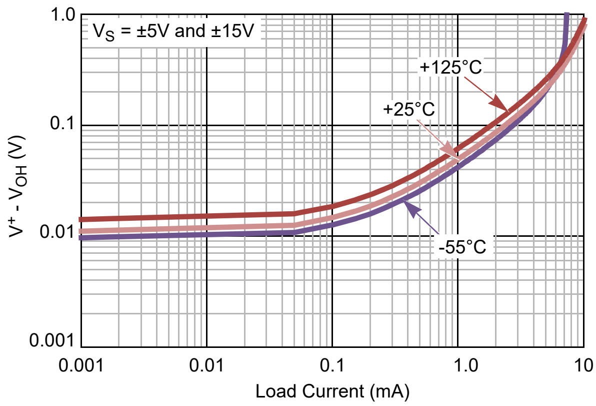


Figure 22. Output Overhead Voltage High vs Load Current, V_S = ±5V and ±15V

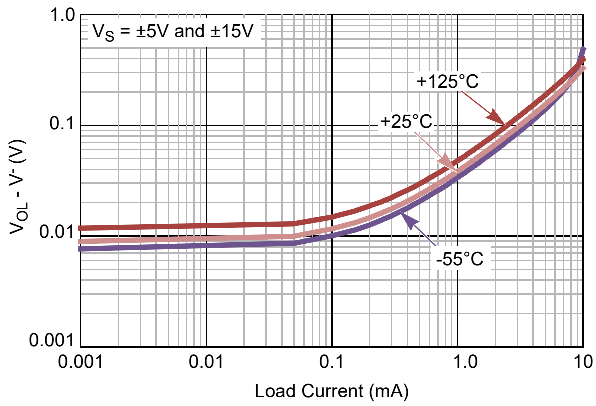


Figure 23. Output Overhead Voltage Low vs Load Current, V_S = ±5V and ±15V

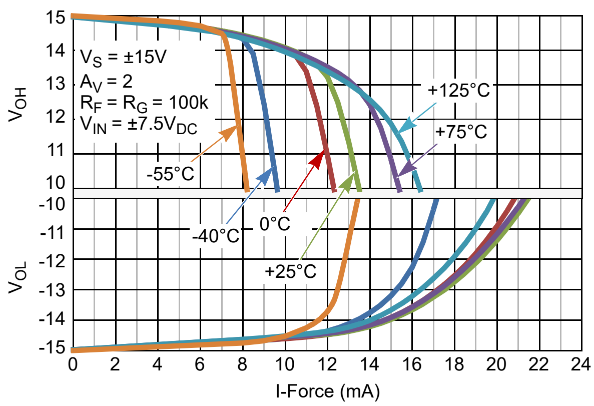


Figure 24. Output Voltage Swing vs Load Current, V_S = ±15V

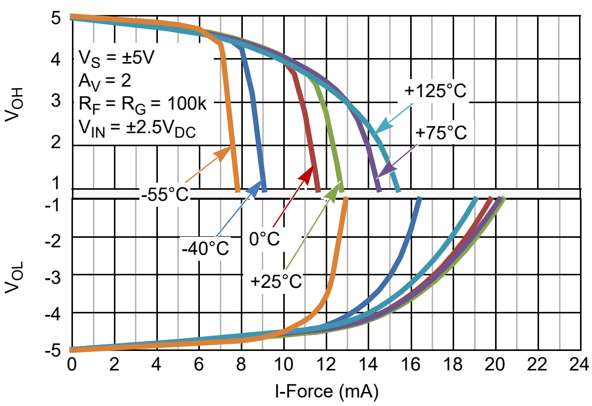


Figure 25. Output Voltage Swing vs Load Current, V_S = ±5V

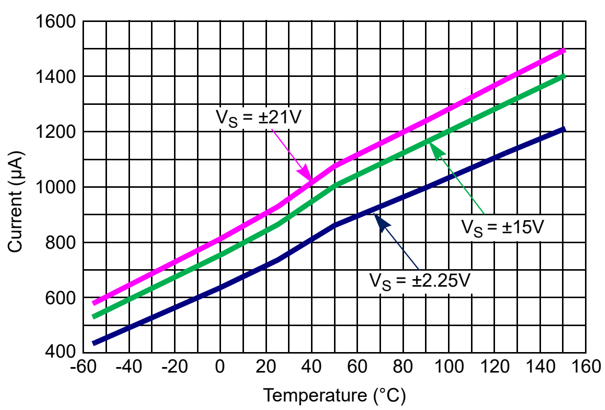


Figure 26. Supply Current vs Temperature vs Supply Voltage

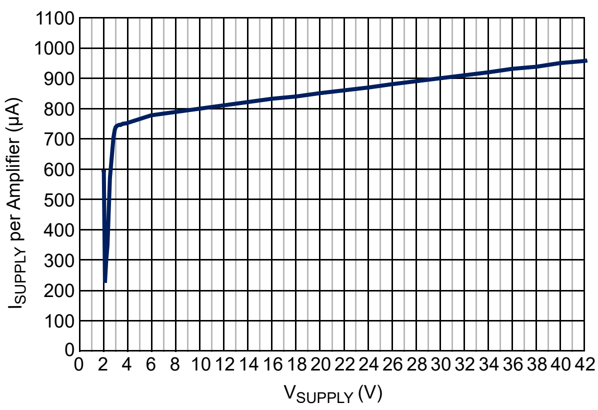


Figure 27. Supply Current vs Supply Voltage

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. (Cont.)

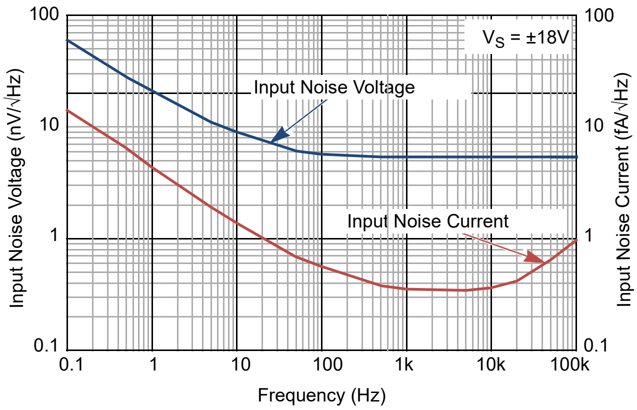


Figure 28. Input Noise Voltage (en) and Current (in) vs Frequency, V_S = ±18V

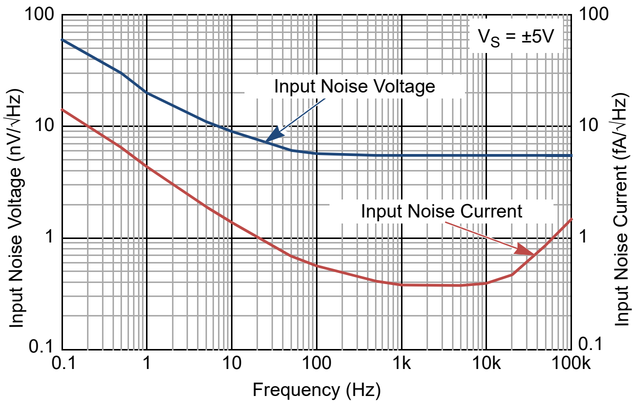


Figure 29. Input Noise Voltage (en) and Current (in) vs Frequency, V_S = ±5V

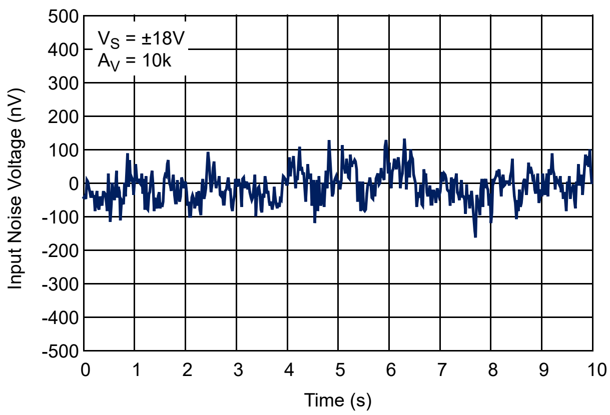


Figure 30. Input Noise Voltage 0.1Hz to 10Hz, V_S = ±18V

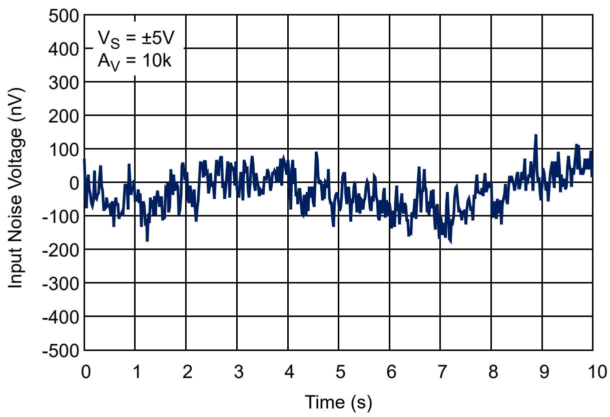


Figure 31. Input Noise Voltage 0.1Hz to 10Hz, V_S = ±5V

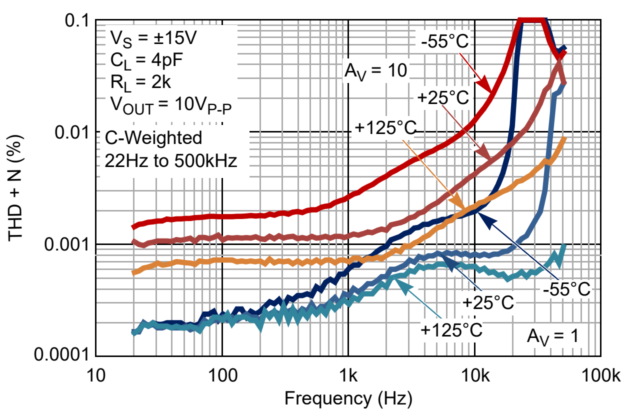


Figure 32. THD+N vs Frequency vs Temperature, A_V = 1, 10, R_L = 2k

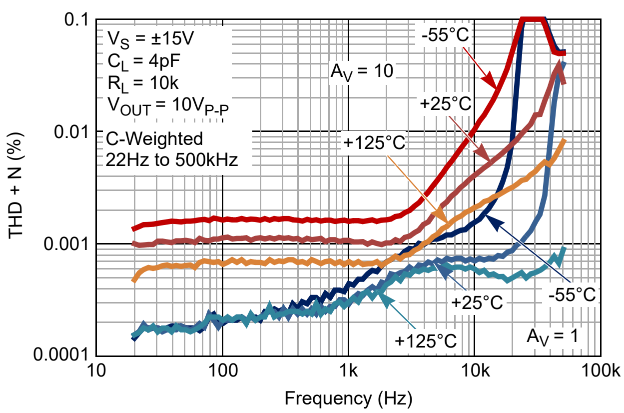


Figure 33. THD+N vs Frequency vs Temperature, A_V = 1, 10, R_L = 10k

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. (Cont.)

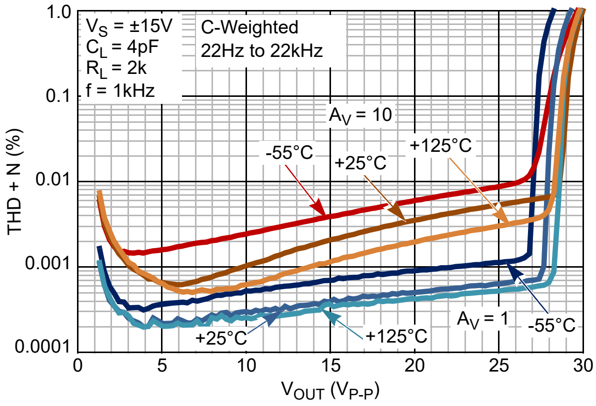


Figure 34. THD+N vs Output Voltage (V_{OUT}) vs Temperature, A_V = 1, 10, R_L = 2k

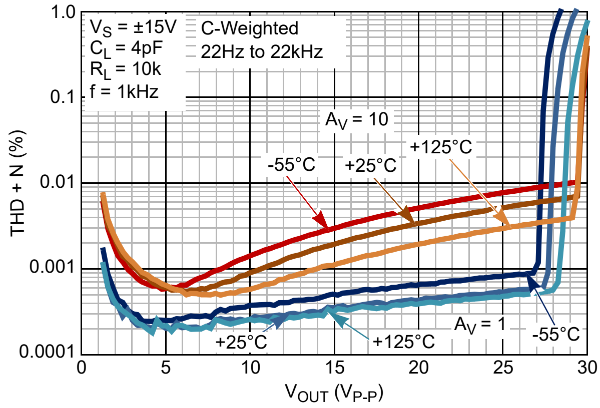


Figure 35. THD+N vs Output Voltage (V_{OUT}) vs Temperature, A_V = 1, 10, R_L = 10k

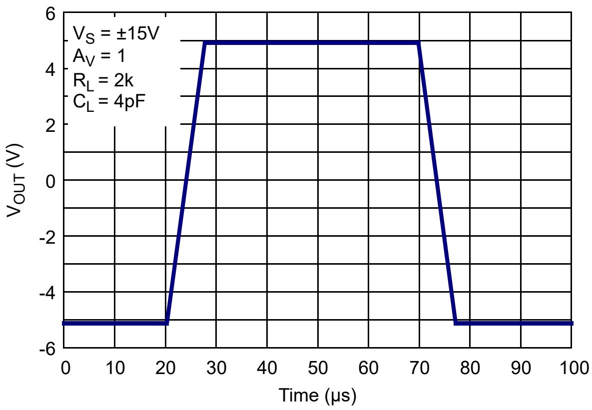


Figure 36. Large Signal 10V Step Response, V_S = ±15V

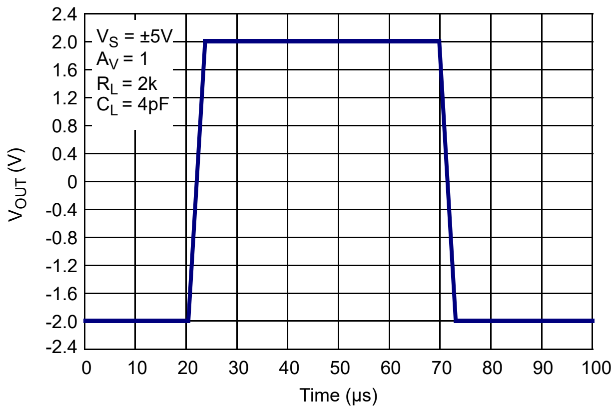


Figure 37. Large Signal 4V Step Response, V_S = ±5V

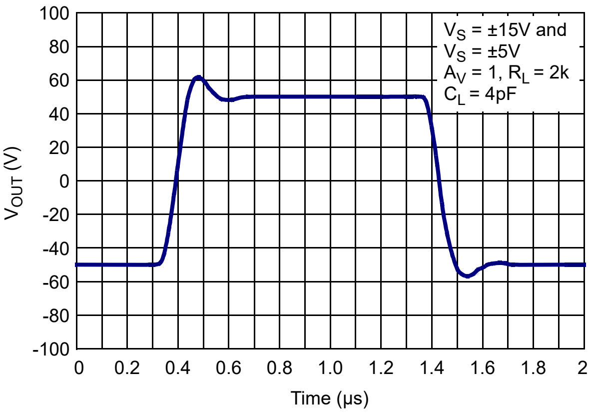


Figure 38. Small Signal Transient Response, V_S = ±5V, ±15V

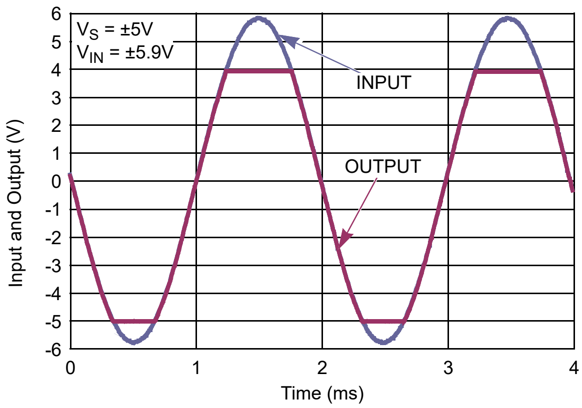


Figure 39. No Phase Reversal

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. (Cont.)

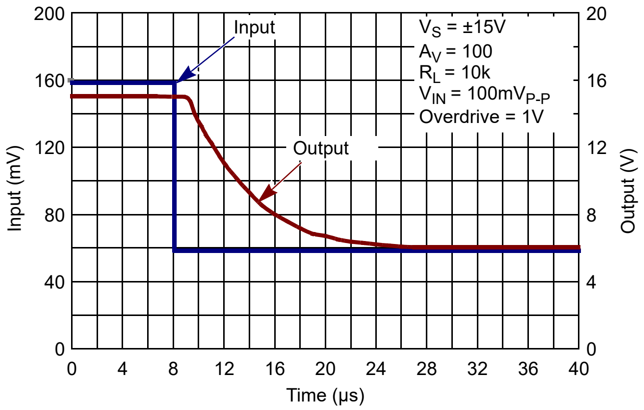


Figure 40. Positive Output Overload Response Time, V_S = ±15V

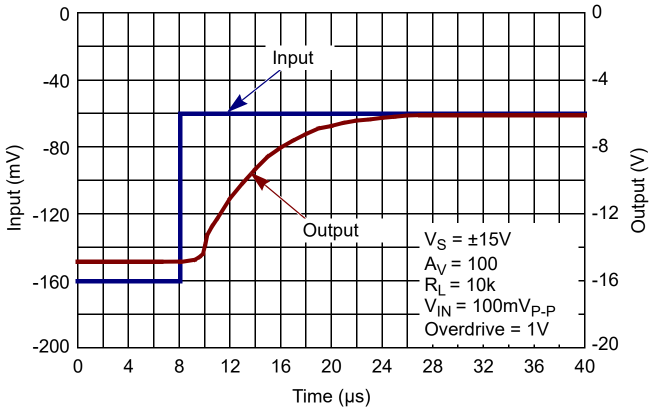


Figure 41. Negative Output Overload Response Time, V_S = ±15V

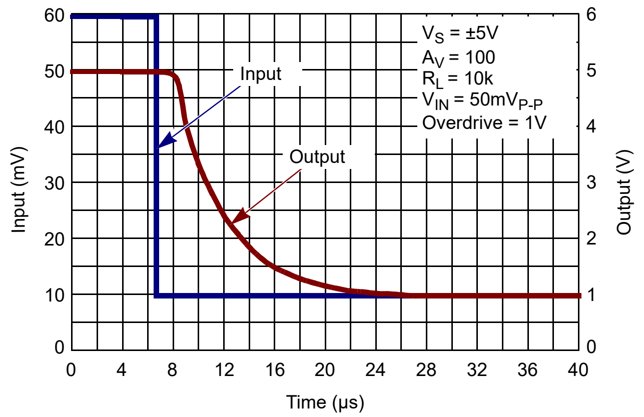


Figure 42. Positive Output Overload Response Time, V_S = ±5V

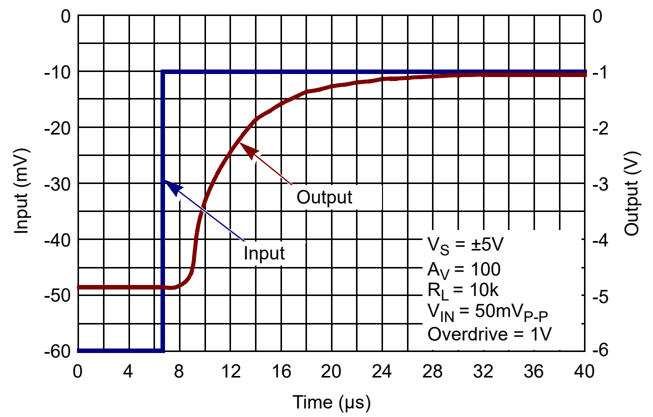


Figure 43. Negative Output Overload Response Time, V_S = ±5V

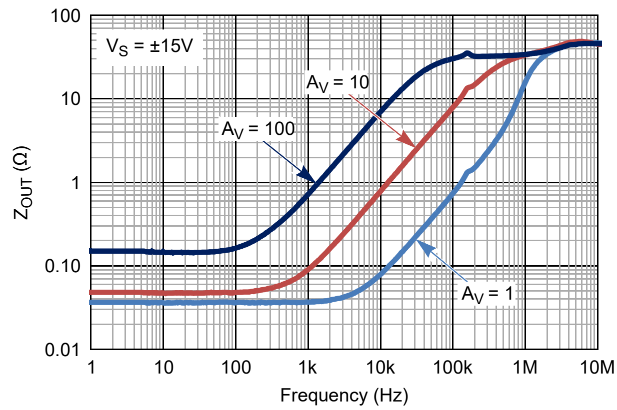


Figure 44. Output Impedance vs Frequency, V_S = ±15V

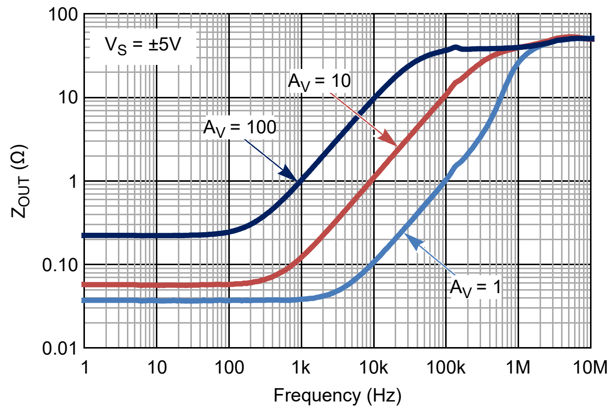


Figure 45. Output Impedance vs Frequency, V_S = ±5V

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. (Cont.)

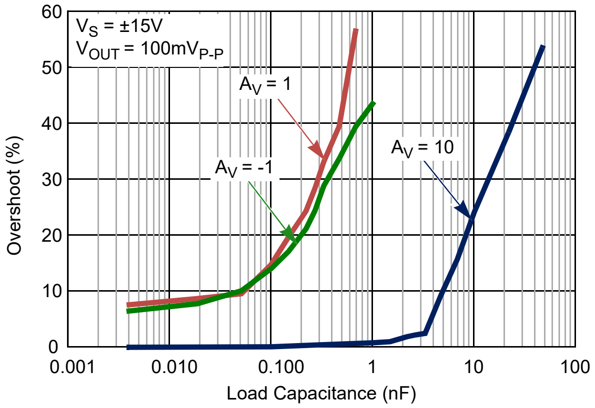


Figure 46. Overshoot vs Capacitive Load, V_S = ±15V

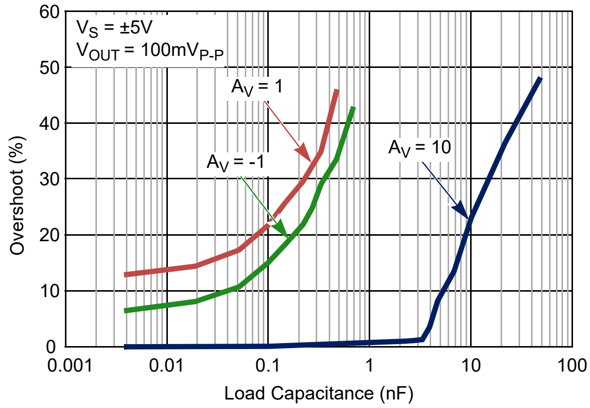


Figure 47. Overshoot vs Capacitive Load, V_S = ±5V

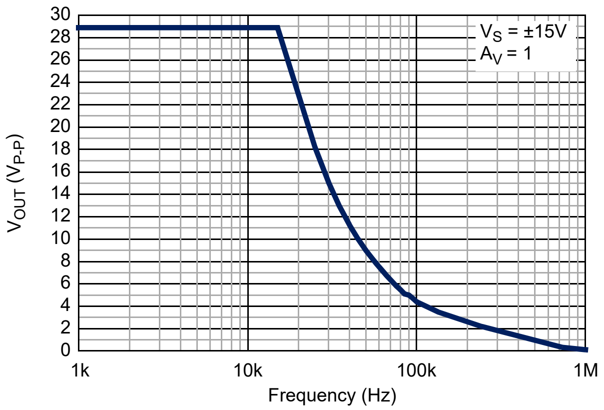


Figure 48. I_{MAX} Output Voltage vs Frequency

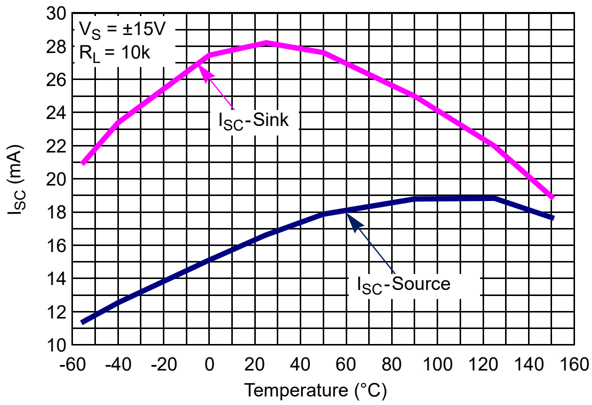


Figure 49. Short-Circuit Current vs Temperature, V_S = ±15V

4. Applications Information

4.1 Functional Description

The ISL71218M is a dual, 3.2MHz, single or dual supply, rail-to-rail output amplifier with a common-mode input voltage range extending to a range of 0.5V below the V^- rail. The input stage is optimized for precision sensing of ground-referenced signals in single-supply applications. The input stage is able to handle large input differential voltages without phase inversion, making this amplifier suitable for high-voltage comparator applications. The bipolar design features high open-loop gain and excellent DC input and output temperature stability. This op amp features very low quiescent current of 850µA, and low temperature drift. The device is fabricated in a new precision 40V complementary bipolar DI process and is immune from latch-up for up to a 36V supply range.

4.2 Operating Voltage Range

The op amp is designed to operate over a single supply range of 3V to 36V, or a split supply voltage range of +1.8V/-1.2V to ±18V. The device is fully characterized at 30V (±15V). Both DC and AC performance remain virtually unchanged over the complete operating voltage range. Parameter variation with operating voltage is shown in the Typical Performance Curves.

The input common-mode voltage to the V^+ rail (V^+ - 1.8V across the full temperature range) may limit amplifier operation when operating from split V^+ and V^- supplies. Figure 5 shows the common-mode input voltage range variation over temperature.

4.3 Input Stage Performance

The ISL71218M PNP input stage has a common-mode input range extending up to 0.5V below ground at +25°C. Full amplifier performance is ensured for input voltage down to ground (V^-) across the -55°C to +125°C temperature range. For common-mode voltages down to -0.5V below ground (V^-), the amplifiers are fully functional, but performance degrades slightly over the full temperature range. This feature provides excellent CMRR, AC performance, and DC accuracy when amplifying low-level, ground-referenced signals. The input stage has a maximum input differential voltage equal to a diode drop greater than the supply voltage and does not contain the back-to-back input protection diodes found on many similar amplifiers. This feature enables the device to function as a precision comparator by maintaining very high input impedance for high-voltage differential input comparator voltages. The high differential input impedance also enables the device to operate reliably in large signal pulse applications, without the need for anti-parallel clamp diodes required on MOSFET and most bipolar input stage op amps. Therefore, input signal distortion caused by nonlinear clamps under high slew rate conditions is avoided.

In applications in which one or both amplifier input terminals are at risk of exposure to voltages beyond the supply rails, current-limiting resistors might be required at each input terminal (see Figure 50, R_{IN+}, R_{IN-}) to limit current through the power-supply ESD diodes to 20mA.

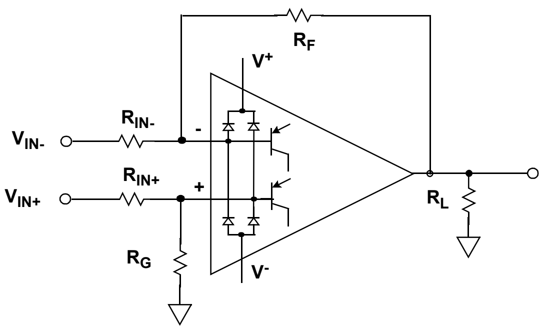


Figure 50. Input ESD Diode Current Limiting

4.4 Output Drive Capability

The bipolar rail-to-rail output stage features low saturation levels that enable an output voltage swing to less than 15mV when the total output load (including feedback resistance) is held below 50µA (Figure 22 and Figure 23). With ±15V supplies, this can be achieved by using feedback resistor values >300kΩ.

The output stage is internally current limited. Output current limit over temperature is shown in Figure 24 and Figure 25. The amplifiers can withstand a short-circuit to either rail as long as the power dissipation limits are not exceeded. This applies to only one amplifier at a time for the dual op amp. Continuous operation under these conditions may degrade long-term reliability.

The amplifiers perform well when driving capacitive loads (Figure 46 and Figure 47). The unity gain, voltage follower (buffer) configuration provides the highest bandwidth, but is also the most sensitive to ringing produced by load capacitance found in BNC cables. Unity gain overshoot is limited to 35% at capacitance values to 0.33nF. At gains of 10 and higher, the device is capable of driving more than 10nF without significant overshoot.

4.5 Output Phase Reversal

Output phase reversal is a change of polarity in the amplifier transfer function when the input voltage exceeds the supply voltage. The ISL71218M is immune to output phase reversal out to 0.5V beyond the rail ($V_{ABS\ MAX}$) limit (see Figure 39).

4.6 Single Channel Usage

The ISL71218M is a dual op amp. If the application requires only one channel, the user must configure the unused channel to prevent it from oscillating. The unused channel oscillates if the input and output pins are floating. This results in higher-than-expected supply currents and possible noise injection into the channel being used. The proper way to prevent oscillation is to short the output to the inverting input, and ground the positive input (Figure 51).

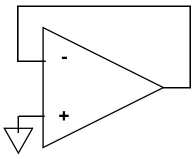


Figure 51. Preventing Oscillations in Unused Channels

4.7 Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package types must be modified to remain in the safe operating area. These parameters are related using Equation 1:

(EQ. 1) $$T_{JMAX} = T_{MAX} + \theta_{JA} x PD_{MAXTOTAL}$$

where:

- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package

PD_{MAX} for each amplifier can be calculated using Equation 2:

(EQ. 2) $$PD_{MAX} = V_S \times I_{qMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L}$$

where:

- PD_{MAX} = Maximum power dissipation of one amplifier
- V_S = Total supply voltage
- I_{qMAX} = Maximum quiescent supply current of one amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application
- R_L = Load resistance

5. Radiation Tolerance

The ISL71218M is a radiation tolerant device for commercial space applications, Low Earth Orbits (LEO) applications, high altitude avionics, launch vehicles, and other harsh environments. This device's response to Total Ionizing Dose (TID) radiation effects, and Single Event Effects (SEE) has been measured, characterized, and reported in the proceeding sections. The TID performance of the ISL71218M is not guaranteed through radiation lot acceptance testing (RLAT). The ISL71218M30BZ is RLAT to 30krad(Si) and the ISL71218M50BZ is RLAT to 50krad(Si).

5.1 Total Ionizing Dose (TID) Testing

5.1.1 Introduction

Total dose testing of the ISL71218MBZ proceeded in accordance with the guidelines of MIL-STD-883 Test Method 1019. Testing was performed on two separate sample sets. For the first sample set, test downpoints were 0krad(Si), 10krad(Si), and 30krad(Si). The second sample set was irradiated to 50krad(Si).

The characterization matrix of the first sample set consisted of 11 samples irradiated under bias and 12 samples irradiated with all pins grounded. The characterization matrix of the second sample set consisted of 7 samples irradiated under bias and 7 samples irradiated with all pins grounded. Two control units were used. The bias configuration is shown in Figure 52.

Samples of the ISL71218MBZ-T were drawn from fabrication lot X8E5X and packaged in the production 8 Ld plastic SOIC (package outline drawing M8.15). The samples were screened to datasheet limits at room temperature only, before irradiation.

Total dose irradiations were performed using a Hopewell Designs N40 panoramic vault-type low dose rate 60Co irradiator located in the Resesas Palm Bay, Florida facility. The dose rate was 0.01rad(Si)/s (10mrad(Si)/s). PbAl spectrum hardening filters were used to shield the test board and devices under test against low energy secondary gamma radiation.

All electrical testing was performed outside the irradiator using production Automated Test Equipment (ATE) with data logging of all parameters at each down-point. All down-point electrical testing was performed at room temperature.

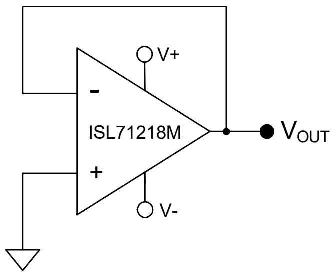


Figure 52. Irradiation Bias Configuration for the ISL71218M

5.1.2 Results

Table 1 summarizes the attributes data.

Table 1. ISL71218M Total Dose Test Attributes Data

Dose Rate mrad(Si)/s	Bias	Sample Size	Down Points	Pass[1]
8.9	Figure 52	11	Pre-Rad	11
			10krad(Si)	11
			20krad(Si)	11
			30krad(Si)	11
			50krad(Si)	7
8.9	Grounded	12	Pre-Rad	12
			10krad(Si)	12
			20krad(Si)	12
			30krad(Si)	12
			50krad(Si)	7

1. A Pass indicates a device that passes all the datasheet specification limits.

The plots in Figure 53 through Figure 59 show data for key parameters at all down points. The plots show the average as a function of total dose for each of the irradiation conditions. The error bars, if visible, show the maximum and minimum measured values. All parts showed excellent stability over irradiation.

Table 2 shows the average of other key parameters with respect to total dose in tabular form.

5.1.3 Typical Radiation Performance

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. The exposure rate for total ionizing dose was <10mrad(Si)/sec at +25°C.

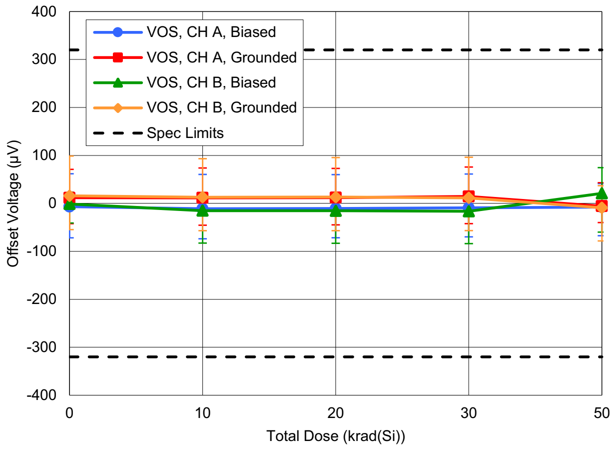


Figure 53. V_{OS} vs TID

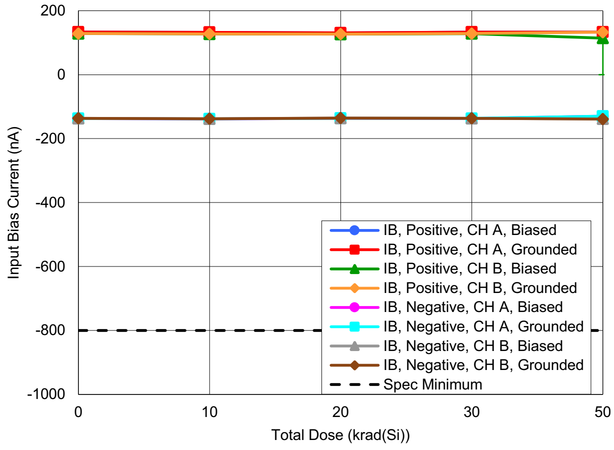


Figure 54. I_{BIAS} vs TID

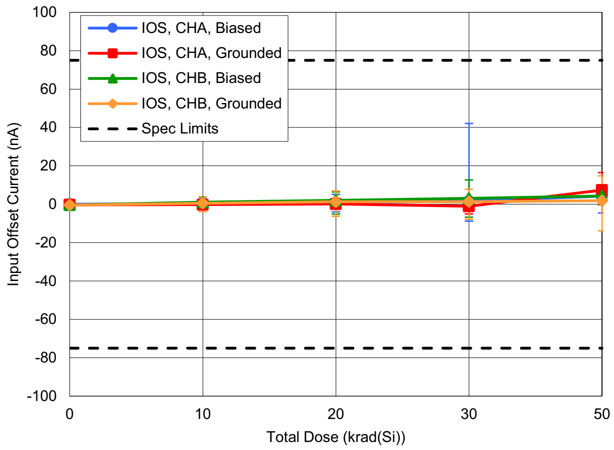


Figure 55. I_{OS} vs TID

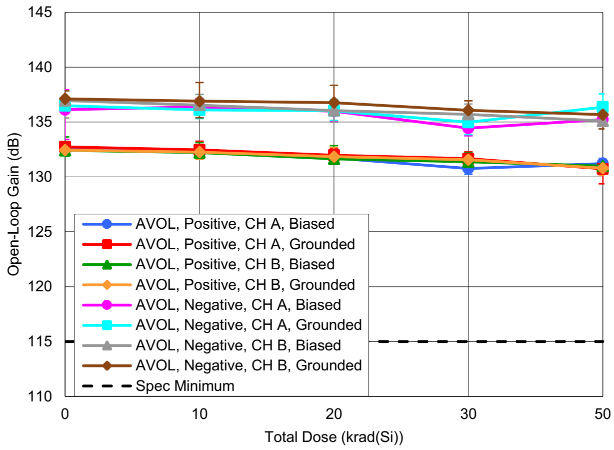


Figure 56. A_{VOL} vs TID

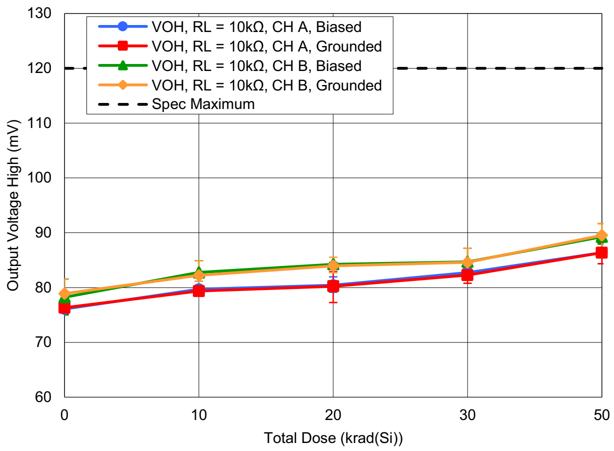


Figure 57. V_{OH} vs TID

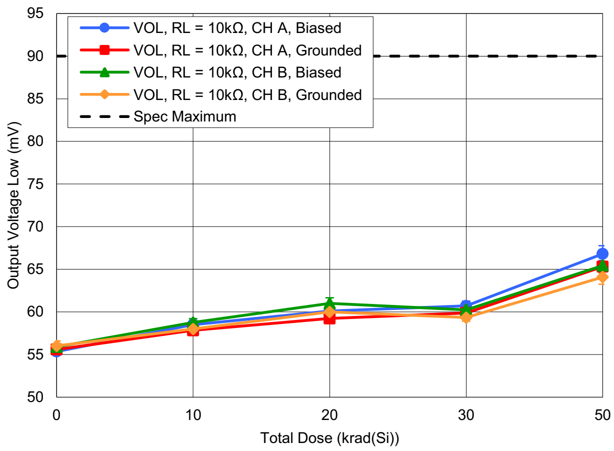


Figure 58. V_{OL} vs TID

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. The exposure rate for total ionizing dose was <10mrad(Si)/sec at +25°C. (Cont.)

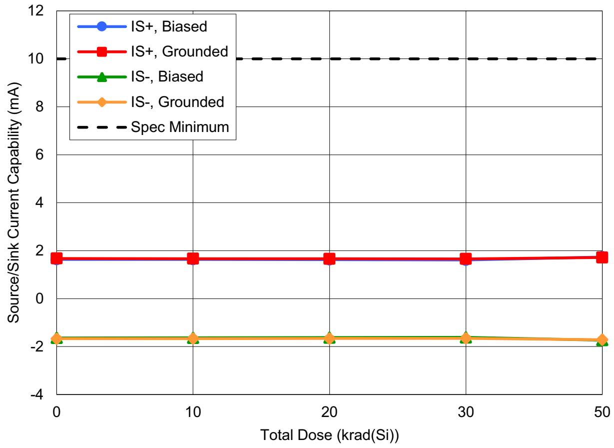


Figure 59. Supply Current vs TID

Table 2. ISL71218M Response of Key Parameters vs TID (V_S = ±15V)

Test Parameter Name and Conditions	Symbol	Irradiation Conditions	0krad(Si)	10krad(Si)	20krad(Si)	30krad(Si)	50krad(Si)	Unit
Input Offset Voltage V_{CM} = 0V V_{CM} = V^+ to V^-	V_{OS}, CH A	Biased	-6.83706	-11.0919	-10.7104	-9.4158	-7.70372	µV
		Grounded	11.74369	11.55418	12.0237	14.47662	-5.80379	µV
		Min	-320	-320	-320	-320	-320	µV
		Max	320	320	320	320	320	µV
	V_{OS}, CH B	Biased	-1.12149	-15.2122	-15.3934	-16.4672	20.9102	µV
		Grounded	15.8378	12.82096	13.11413	11.47807	-9.18218	µV
		Min	-320	-320	-320	-320	-320	µV
		Max	320	320	320	320	320	µV
Input Offset Voltage Channel-to-Channel Match	ΔV_{OS}	Biased	-	-4.12031	-4.68302	-7.05141	28.61392	µV
		Grounded	-	1.266783	1.090436	-2.99856	-3.37839	µV
		Min	-	-	-	-	-	-
		Max	365	365	365	365	365	µV
Positive Input Bias Current V_{CM} = V^+ to V^-	I_{B+}, CH A	Biased	133.2656	132.2211	130.6132	133.0105	133.1473	nA
		Grounded	133.4601	132.4582	130.8754	133.2779	133.1588	nA
		Min	-800	-800	-800	-800	-800	nA
		Max	-	-	-	-	-	-
	I_{B+}, CH B	Biased	128.6172	127.4201	126.6101	128.3206	114.2575	nA
		Grounded	128.8039	127.6924	126.9003	128.6565	133.0544	nA
		Min	-800	-800	-800	-800	-800	nA
		Max	-	-	-	-	-	-

Table 2. ISL71218M Response of Key Parameters vs TID (V_S = ±15V) (Cont.)

Test Parameter Name and Conditions	Symbol	Irradiation Conditions	0krad(Si)	10krad(Si)	20krad(Si)	30krad(Si)	50krad(Si)	Unit
Negative Input Bias Current V_{CM} = V^+ to V^-	I_{B-}, CH A	Biased	-137.052	-138.445	-136.392	-136.976	-129.677	nA
		Grounded	-136.871	-138.223	-136.181	-136.748	-129.624	nA
		Min	-800	-800	-800	-800	-800	nA
		Max	-	-	-	-	-	-
	I_{B-}, CH B	Biased	-136.533	-138.05	-135.977	-136.582	-138.517	nA
		Grounded	-136.377	-137.764	-135.698	-136.342	-138.816	nA
		Min	-800	-800	-800	-800	-800	nA
		Max	-	-	-	-	-	-
Input Offset Current V_{CM} = V^+ to V^-	I_{OS}, CH A	Biased	0.013151	0.338423	0.687684	1.652572	4.218061	nA
		Grounded	-0.28544	-0.24414	0.13153	-1.03057	7.373366	nA
		Min	-75	-75	-75	-75	-75	nA
		Max	75	75	75	75	75	nA
	I_{OS}, CH B	Biased	-0.41063	1.093001	2.084476	3.037149	4.288074	nA
		Grounded	-0.42072	0.546974	1.302884	1.353728	1.85575	nA
		Min	-75	-75	-75	-75	-75	nA
		Max	75	75	75	75	75	nA
Positive Common-Mode Rejection Ratio V_{CM} = V^+ to V^-	CMRR+, CH A	Biased	119.1266	119.4099	119.0451	116.0873	116.6393	dB
		Grounded	120.8384	120.8631	120.9218	120.7108	122.4985	dB
		Min	97	97	97	97	97	dB
		Max	-	-	-	-	-	-
	CMRR+, CH B	Biased	122.5306	122.8636	122.778	122.364	117.8165	dB
		Grounded	122.9616	123.1112	123.238	123.097	116.4059	dB
		Min	97	97	97	97	97	dB
		Max	-	-	-	-	-	-
Negative Common-Mode Rejection Ratio V_{CM} = V+ to V-	CMRR-, CH A	Biased	117.9637	117.9082	117.7423	116.5957	116.4001	dB
		Grounded	119.7646	120.7821	121.2886	121.4314	119.2986	dB
		Min	97	97	97	97	97	dB
		Max	-	-	-	-	-	-
	CMRR-, CH B	Biased	122.3437	120.6121	120.3417	120.1333	118.3032	dB
		Grounded	122.5289	124.5	124.2211	124.8165	118.0274	dB
		Min	97	97	97	97	97	dB
		Max	-	-	-	-	-	-
Positive Power Supply Rejection Ratio V_{CM} = V+ to V-	PSRR+, CH A	Biased	123.2048	122.5896	122.8451	123.1816	118.3908	dB
		Grounded	120.5911	120.5841	120.5443	120.5729	122.7228	dB
		Min	100	100	100	100	100	dB
		Max	-	-	-	-	-	-
	PSRR+, CH B	Biased	120.8548	121.4353	121.41	121.5755	127.773	dB
		Grounded	119.3454	119.3573	119.33	119.3929	119.4568	dB
		Min	100	100	100	100	100	dB
		Max	-	-	-	-	-	-

Table 2. ISL71218M Response of Key Parameters vs TID (V_S = ±15V) (Cont.)

Test Parameter Name and Conditions	Symbol	Irradiation Conditions	0krad(Si)	10krad(Si)	20krad(Si)	30krad(Si)	50krad(Si)	Unit
Negative Power Supply Rejection Ratio V_{CM} = V+ to V-	PSRR-, CH A	Biased	124.3732	125.2169	125.1242	124.394	120.5548	dB
		Grounded	126.8897	125.5052	124.9438	124.7544	135.8085	dB
		Min	100	100	100	100	100	dB
		Max	-	-	-	-	-	-
	PSRR-, CH B	Biased	126.7814	126.3381	127.0045	126.161	125.2371	dB
		Grounded	126.7324	127.0553	127.204	127.282	126.1179	dB
		Min	100	100	100	100	100	dB
		Max	-	-	-	-	-	-
Positive Open-Loop Gain R_L = 10kΩ	A_{VOL+}, CH A	Biased	132.5782	132.3323	131.7193	130.7643	131.2149	dB
		Grounded	132.7357	132.4534	131.9733	131.6553	130.7387	dB
		Min	115	115	115	115	115	dB
		Max	-	-	-	-	-	-
	A_{VOL+}, CH B	Biased	132.4192	132.2133	131.6424	131.3685	130.9871	dB
		Grounded	132.4435	132.2666	131.8457	131.5637	130.7972	dB
		Min	115	115	115	115	115	dB
		Max	-	-	-	-	-	-
Negative Open-Loop Gain R_L = 10kΩ	A_{VOL-}, CH A	Biased	136.1258	136.3818	135.9794	134.4411	135.2292	dB
		Grounded	136.4889	136.1036	136.0223	134.9801	136.3588	dB
		Min	115	115	115	115	115	dB
		Max	-	-	-	-	-	-
	A_{VOL-}, CH B	Biased	136.9545	136.5449	136.0484	135.7037	135.0973	dB
		Grounded	137.1122	136.8985	136.7662	136.0752	135.6761	dB
		Min	115	115	115	115	115	dB
		Max	-	-	-	-	-	-
Output Voltage High R_L = 10kΩ	V_{OH}, CH A	Biased	76.09601	79.69345	80.42301	82.73845	86.3642	mV
		Grounded	76.3301	79.35254	80.23842	82.26308	86.36393	mV
		Min	-	-	-	-	-	-
		Max	120	120	120	120	120	mV
	V_{OH}, CH B	Biased	78.23649	82.76038	84.26146	84.7037	89.26405	mV
		Grounded	78.90312	82.2355	83.9773	84.59727	89.53163	mV
		Min	-	-	-	-	-	-
		Max	120	120	120	120	120	mV
Output Voltage Low R_L = 10kΩ	V_{OL}, CH A	Biased	55.35756	58.50903	60.10708	60.70936	66.81105	mV
		Grounded	55.58909	57.836	59.23524	59.8741	65.31109	mV
		Min	-	-	-	-	-	-
		Max	90	90	90	90	90	mV
	V_{OL}, CH B	Biased	55.89917	58.76074	61.00356	60.24566	65.43353	mV
		Grounded	56.01887	58.00328	59.99564	59.33543	64.08654	mV
		Min	-	-	-	-	-	-
		Max	90	90	90	90	90	mV

Table 2. ISL71218M Response of Key Parameters vs TID (V_S = ±15V) (Cont.)

Test Parameter Name and Conditions	Symbol	Irradiation Conditions	0krad(Si)	10krad(Si)	20krad(Si)	30krad(Si)	50krad(Si)	Unit
Positive Supply Current (Average per Channel)	I_{S+}	Biased	1.63862	1.63514	1.626156	1.612367	1.734259	mA
		Grounded	1.672756	1.667731	1.661754	1.655658	1.715841	mA
		Min	10	10	10	10	10	mA
		Max	-	-	-	-	-	-
Negative Supply Current (Average per channel)	I_{S-}	Biased	-1.63665	-1.63427	-1.62409	-1.6141	-1.73248	mA
		Grounded	-1.67064	-1.66679	-1.65983	-1.65712	-1.714	mA
		Min	10	10	10	10	10	mA
		Max	-	-	-	-	-	-
Large Signal Slew Rate (Rising) V_{OUT} = +18V	SR+, CH A	Biased	1.160269	1.167523	1.159259	1.157015	1.201031	V/µs
		Grounded	1.167869	1.172748	1.163885	1.162889	1.196923	V/µs
		Min	0.4	0.4	0.4	0.4	0.4	V/µs
		Max	-	-	-	-	-	-
	SR+, CH B	Biased	1.185981	1.180482	1.180573	1.17484	1.208039	V/µs
		Grounded	1.191943	1.179494	1.186758	1.163528	1.196561	V/µs
		Min	0.4	0.4	0.4	0.4	0.4	V/µs
		Max	-	-	-	-	-	-
Large Signal Slew Rate (Falling) V_{OUT} = +18V	SR-, CH A	Biased	1.22873	1.223584	1.207563	1.199737	1.328026	V/µs
		Grounded	1.242541	1.231481	1.21996	1.222628	1.313013	V/µs
		Min	0.4	0.4	0.4	0.4	0.4	V/µs
		Max	-	-	-	-	-	-
	SR-, CH B	Biased	1.264197	1.258265	1.244501	1.232336	1.341506	V/µs
		Grounded	1.273822	1.26352	1.255088	1.2534	1.332089	V/µs
		Min	0.4	0.4	0.4	0.4	0.4	V/µs
		Max	-	-	-	-	-	-
Output Rise Time R_L = 2kΩ	t_R, CH A	Biased	70.43377	78.44809	72.14947	80.46589	84.44485	ns
		Grounded	65.81869	76.01125	71.52429	66.73426	82.70154	ns
		Min	-	-	-	-	-	-
		Max	400	400	400	400	400	ns
	t_R, CH B	Biased	60.93007	61.01243	62.74845	65.06353	81.88772	ns
		Grounded	61.15665	60.85732	62.49393	62.67389	80.65565	ns
		Min	-	-	-	-	-	-
		Max	400	400	400	400	400	ns
Output Fall Time R_L = 2kΩ	t_F, CH A	Biased	79.53738	76.55518	80.93842	79.83761	83.44017	ns
		Grounded	79.51684	75.17785	80.86646	79.76992	87.7097	ns
		Min	-	-	-	-	-	-
		Max	400	400	400	400	400	ns
	t_F, CH B	Biased	60.96468	61.3481	63.63524	64.95984	78.47244	ns
		Grounded	60.84919	61.33439	63.35473	63.65973	79.37446	ns
		Min	-	-	-	-	-	-
		Max	400	400	400	400	400	ns

Table 2. ISL71218M Response of Key Parameters vs TID (V_S = ±15V) (Cont.)

Test Parameter Name and Conditions	Symbol	Irradiation Conditions	0krad(Si)	10krad(Si)	20krad(Si)	30krad(Si)	50krad(Si)	Unit
Positive Overshoot R_L = 2kΩ	OS+, CH A	Biased	0.048464	0.036527	0.056097	0.05961	0.000312	%
		Grounded	0.050122	0.042714	0.04113	0.04667	0.000292	%
		Min	-	-	-	-	-	-
		Max	20	20	20	20	20	%
	OS+, CH B	Biased	0.055783	0.050293	0.033697	0.038413	0.000488	%
		Grounded	0.044317	0.032269	0.040035	0.034072	0.000195	%
		Min	-	-	-	-	-	-
		Max	20	20	20	20	20	%
Negative Overshoot R_L = 2kΩ	OS-, CH A	Biased	0.116974	0.206726	0.129806	0.142029	0.001113	%
		Grounded	0.114854	0.170088	0.149688	0.095755	0.000916	%
		Min	-	-	-	-	-	-
		Max	20	20	20	20	20	%
	OS-, CH B	Biased	0.158099	0.176592	0.196722	0.141352	0.001048	%
		Grounded	0.121989	0.119473	0.214829	0.167776	0.000981	%
		Min	-	-	-	-	-	-
		Max	20	20	20	20	20	%

5.1.4 Conclusion

As shown in Table 2, and the selected graphs (Figure 53 through Figure 59), all parameters showed excellent stability over irradiation, with no observed bias sensitivity. Although, for brevity, only the ±15V results are shown; the ±5V results were just as stable.

5.2 Single Event Effects Testing

The intense heavy ion environment encountered in space applications can cause a variety of Single Event Effects (SEE). SEE can lead to system-level performance issues including disruption, degradation, and destruction. For predictable and reliable space system operation, individual electronic components should be characterized to determine their SEE response. The following is a summary of the SEE testing of the ISL71218M.

5.2.1 SEE Test Facility

Testing was performed at the Texas A&M University (TAMU) Cyclotron Institute heavy ion facility. This facility is coupled to a K500 superconducting cyclotron, which is capable of generating a wide range of test particles with the various energy, flux, and fluence level required for advanced radiation testing.

5.2.2 SEE Test Setup

The part was tested for Single Event Burnout and Latch-up (SEB/L), using Ag ions (LET = 43MeV•cm^2/mg) and Single Event Transient (SET) using Kr ions (LET = 28MeV•cm^2/mg). The Device Under Test (DUT) was mounted in the beam line and irradiated with heavy ions of the appropriate species. The parts were assembled in 10 Ld dual in-line packages with the metal lid removed for beam exposure. The beam was directed onto the exposed die and the beam flux, beam fluence and errors in the device outputs were measured.

The tests were controlled remotely from the control room. All input power was supplied from portable power supplies connected using cable to the DUT. The supply currents were monitored along with the device outputs. All currents were measured with digital ammeters, while all the output waveforms were monitored on a digital oscilloscope for ease of identifying the different types of SEE, which the part displayed. Events were captured by triggering on changes in the output.

A schematic of the evaluation board is shown in Figure 60. Each op amp was set up in a gain of 11V/V. The IN- inputs were grounded and the input signal was applied to the IN+ pin.

Table 3. ISL71218M Oscilloscope Setup for SEE Testing

Scope	CH1	CH2	CH3	CH4	Trigger/Measurements
1	OUTA	OUTB	OUTA	OUTB	Trigger: OUTA, ±80mV window
2	OUTA	OUTB	OUTA	OUTB	Trigger: OUTB, ±80mV window

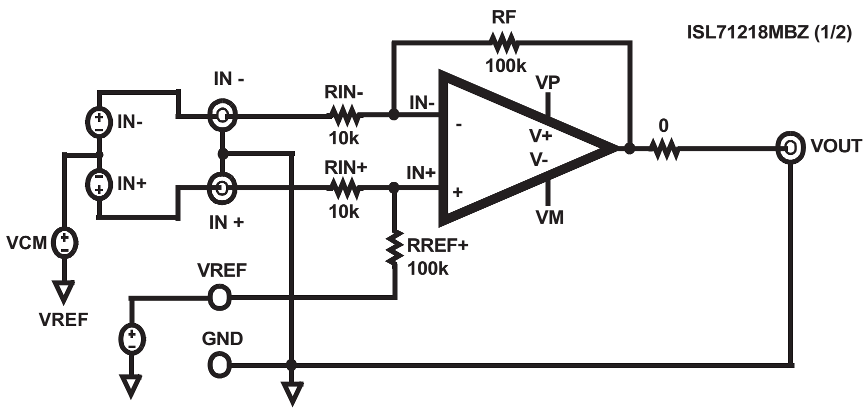


Figure 60. Simplified SEE Schematic

5.2.3 SEB/SEL Results

A failure due to burnout was indicated by a permanent change to the part's supply current after the beam was turned off. If the part's supply current reverted back to its pre-exposure value after a power cycle, the event was deemed as latch-up. A failure for burnout was indicated by a ±5% delta (which would allow for measurement repeatability) in supply current. The ISL71218M units did not exceed the aforementioned limit with V_S = ±20V at an LET of 43MeV•cm^2/mg and therefore are deemed as passing.

Table 4. ISL71218M SEB/L Results (V_S = ±20V, LET = 43MeV•cm^2/mg)

Unit	Temp (°C)	Supply Current Pre-Exposure		Supply Current Post-Exposure		SEB/L
		I+ (mA)	I- (mA)	I+ (mA)	I- (mA)	
1	+125°C	2.833	2.796	2.840	2.799	Pass
2	+125°C	3.036	2.998	3.042	3.001	Pass
3	+125°C	3.057	2.580	3.062	2.579	Pass
4	+125°C	2.888	2.410	2.892	2.413	Pass

5.2.4 SET Results

Figure 61 and Figure 62 show the typical SET performance of the ISL71218M at an LET of 28MeV•cm^2/mg with a fluence at 2x10^6/cm^2. In all cases the voltage deviations were within ±200mV of V_{OUT}. Transients were within 100µs and 600µs for V_S = ±18V and V_S = ±4.5V, respectively.

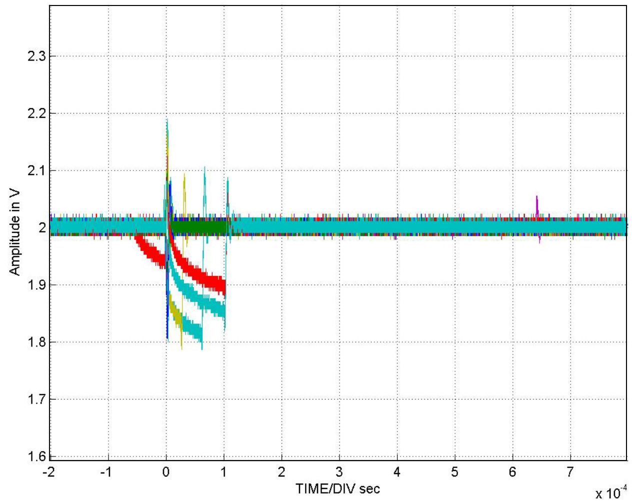


Figure 61. Typical Capture at LET of 28MeV•cm^2/mg (V_S = ±18V)

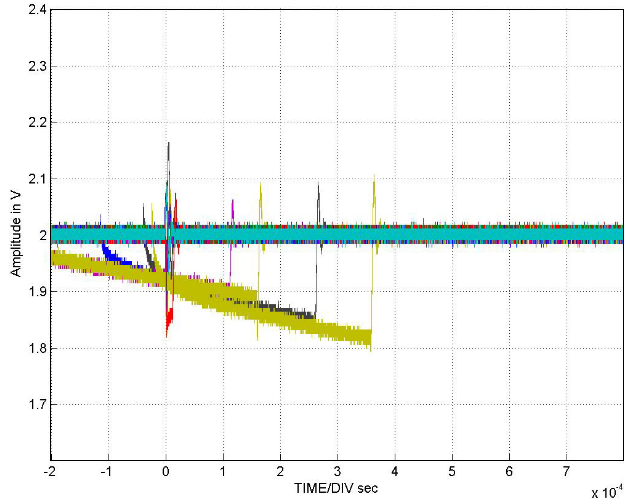


Figure 62. Typical Capture at LET of 28MeV•cm^2/mg (V_S = ±4.5V)

6. Package Outline Drawing

The package outline drawing is located at the end of this document and is accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

7. Ordering Information

Part Number[1][2]	Part Marking	Radiation Lot Acceptance Testing	Package Description[3] (RoHS Compliant)	Pkg. Dwg. #	Carrier Type [4]	Temp Range
ISL71218MBZ	71218 MBZ	N/A	8 Ld SOIC	M8.15	Tube	-55 to +125°C
ISL71218MBZ-T					Reel, 1k	
ISL71218MBZ-T7A					Reel, 250	
ISL71218M30BZ	71218 MBZ	30krad(Si)	8 Ld SOIC	M8.15	Tube	-55 to +125°C
ISL71218M30BZ-T					Reel, 1k	
ISL71218M30BZ-T7A					Reel, 250	
ISL71218M50BZ	71218 MBZ	50krad(Si)	8 Ld SOIC	M8.15	Tube	-55 to +125°C
ISL71218M50BZ-T					Reel, 1k	
ISL71218M50BZ-T7A					Reel, 250	
ISL71218MEVAL1Z	Evaluation Board					

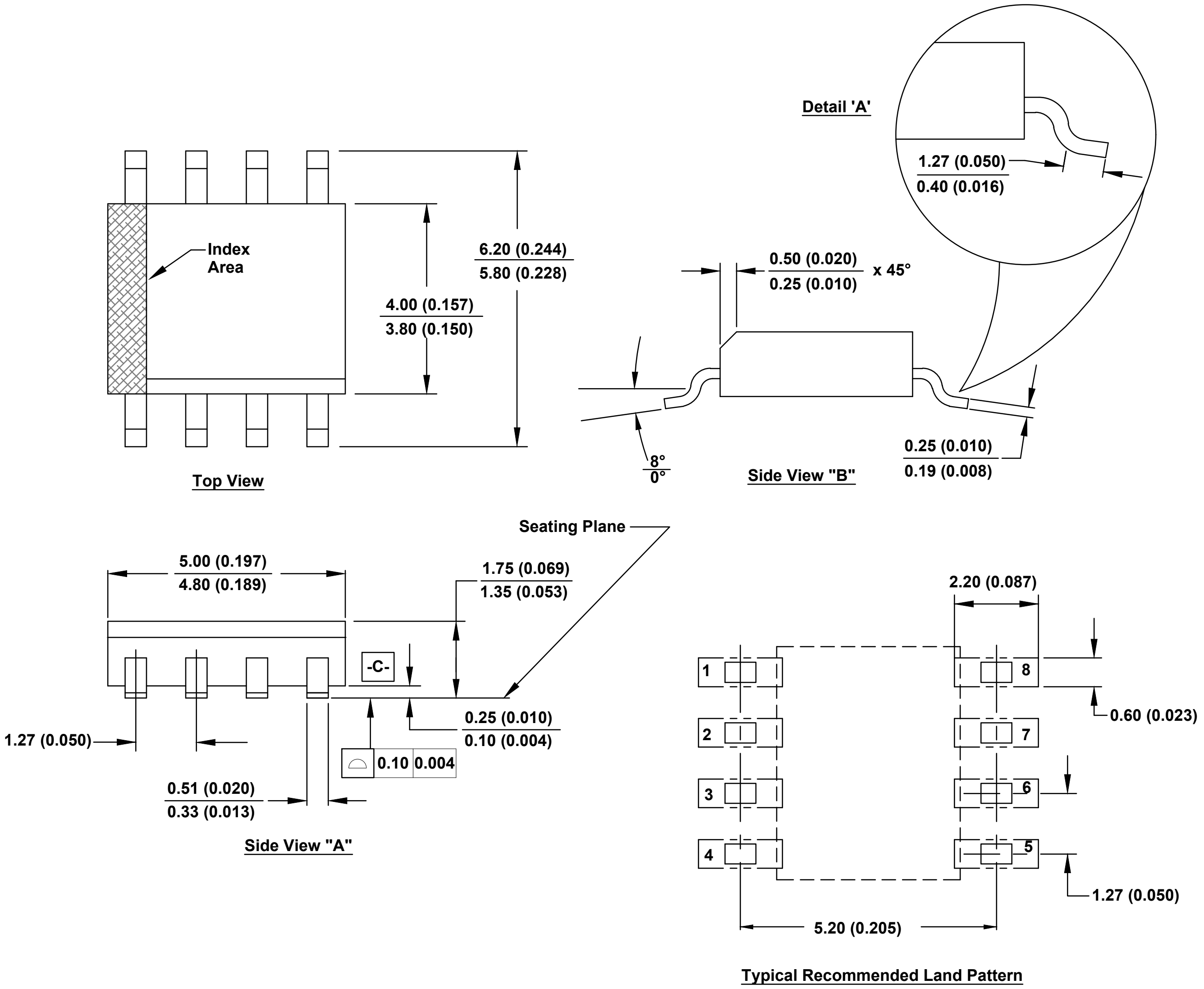
1. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. For Moisture Sensitivity Level (MSL), see the ISL71218M device page. For more information about MSL, see TB363.
3. For the Pb-Free Reflow Profile, see TB493.
4. See TB347 for details about reel specifications.

8. Revision History

Revision	Date	Description
2.01	Oct 6, 2025	Applied latest template. Updated Features bullets. Added M30/M50 part information throughout document. Updated Common-Mode Rejection Ratio minimum spec from 80dB to 79dB on page 6. Updated POD to the latest revision.
2.00	Jan 19, 2021	Updated links throughout Abs Max Ratings, Maximum Supply Voltage under beam - changed Max from 36V to 40V (page 4). Table 4 title, changed V_S = 20V to V_S = ±20V (on page 26). Updated Disclaimer
1.00	Mar 9, 2018	Features, page 1, added “Passes NASA Low Outgassing Specifications”. Ordering Information table, page 3, added Tape and Reel quantity column. Added tape and reel parts, and updated Note 1. Removed About Intersil section. Updated Disclaimer.
0.00	Sept 6, 2017	Initial release

Package Outline Drawing

M8.15
GS0008AC
8-Lead Narrow Body Small Outline Plastic Package 4.90 x 3.90 x 1.43 mm Body, 1.27 mm Pitch
Rev08, Jul 7, 2025



Notes:

1. Dimensioniong and tolerancing conform to ASME Y14.5M-1994.
2. Package length does not include mold flash, protrusion or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
7. Controlling dimension: MILLIMETER. Converted inch dimension are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

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