ISL70100SLH

Radiation Hardened 40V Current-Sense Amplifier

Description

The ISL70100SLH is a radiation hardened 40V current sense amplifier built on the Renesas proprietary PR40 SOI process. The device has a wide power supply range of 2.7V to 40V. The input common-mode voltage is independent of the supply voltage and extends from -0.3V to 40.0V, making it ideal to use in both high-side and low-side applications.

The ISL70100SLH is a transconductance amplifier that monitors current using an external sense resistor and outputs a current proportional to the sensed voltage. The overall voltage gain is adjustable with a single resistor from the output to ground.

The amplifier has an extremely low offset voltage and input bias currents, making it ideal for precision sensing applications. It has a minimum bandwidth of 500kHz with a slew rate of 500µA/µs that makes it useful for current feedback in telemetry applications. When the part is powered down (V+ = V- = 0V), the sense pins (RS+, RS-) are high impedance to avoid loading the monitored circuit.

The part is available in a plastic 14Ld TSSOP package with NiPdAu-Ag lead finish. It operates across the temperature range of -55°C to +125°C.

Features

- Qualified to Renesas Rad Hard QML-P Equivalent Screening and QCI Flow (R34TB0005EU)
  - All screening and QCI are in accordance with MIL-PRF-38535 Class P
- Power supply range: 2.7V to 40V
- Input common-mode range: -0.3V to 40V
- Transconductance: 2µA/mV (typical)
  - ±1% accuracy (T_A = 25°C)
  - ±1.5% accuracy (T_A = -55°C, 125°C)
- Voltage offset: 10µV (typical), V+ = 12V
- Adjustable gain with a single resistor
- Operating temperature range: -55°C to +125°C
- Passes NASA low outgassing specifications
- TID Rad Hard Assurance (RHA) testing
  - LDR (≤ 10mrad(Si)/s): 75krad(Si)
- SEE Characterization
  - No DSEE with RS+ = 35V and V+ = 35V at 86.4MeV•cm^2/mg
  - SET ≤ 2.74E-3cm^2 at 86.4MeV•cm^2/mg
  - SEFI < 10µm^2 at 86.4MeV•cm^2/mg

Applications

- High-side or low-side current sensing
- Battery monitoring
- Power management
- Motor control
- Command, telemetry, and control systems

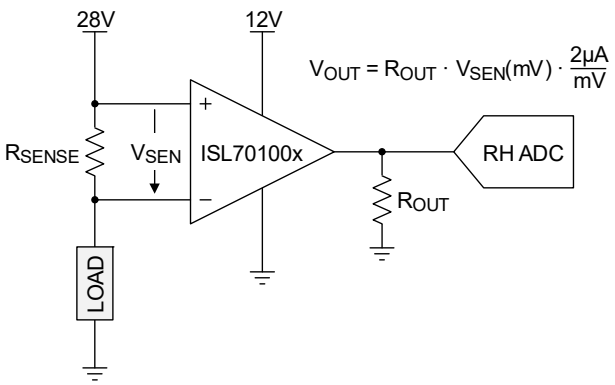

Figure 1. Typical Application: High-Side Current Sense for 28V Supply Rail

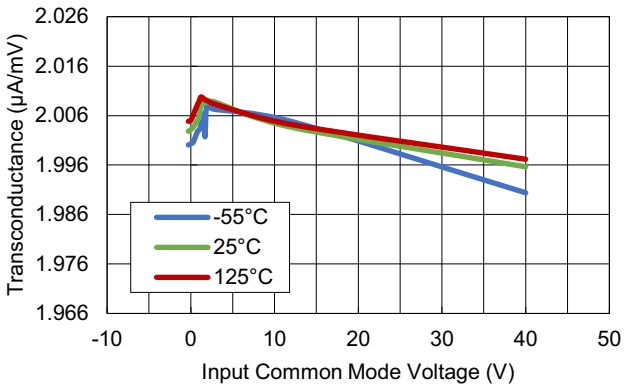

Figure 2. Transconductance, V+ = 12V

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1. Overview

1.1 Block Diagram

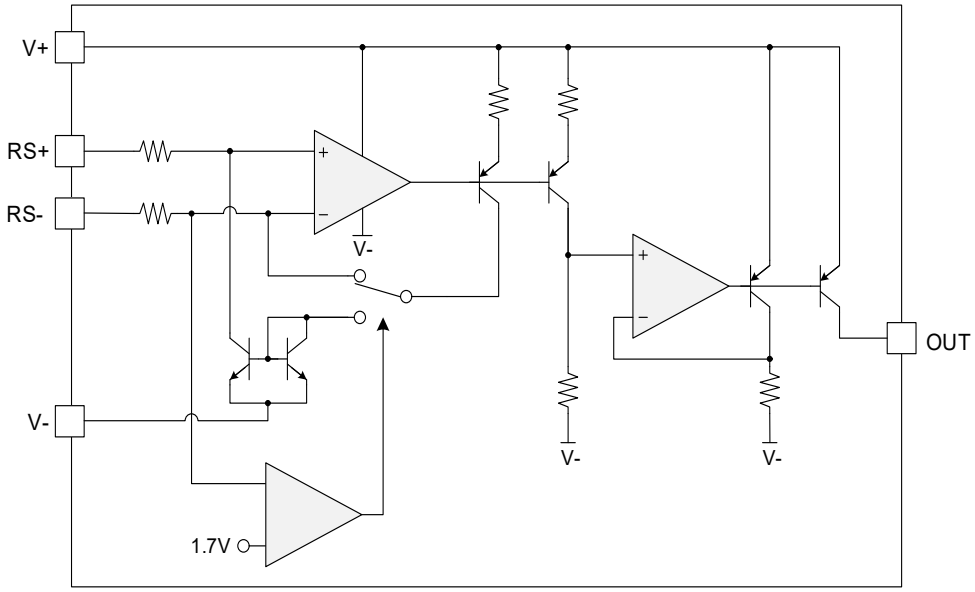


Figure 3. Block Diagram

2. Pin Information

2.1 Pin Assignments

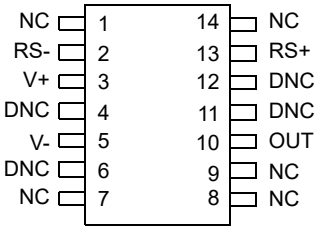
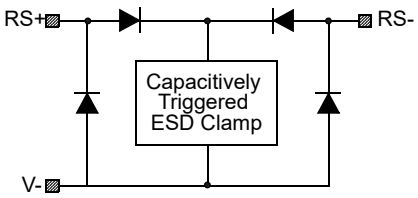


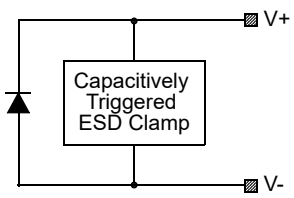
Figure 4. Pin Assignments - Top View

2.2 Pin Descriptions

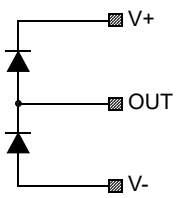
Pin Number	Pin Name	ESD Circuit	Description
1	NC	-	No Connect (Not bonded out)
2	RS-	1	Negative sense input of current sense amplifier
3	V+	2	Positive power supply
4	DNC	-	Do not connect, leave floating. This pin leaks to V-.
5	V-	-	Negative power supply
6	DNC	-	Do not connect, leave floating. This pin leaks to V-.
7	NC	-	No Connect (Not bonded out)
8	NC	-	No Connect (Not bonded out)
9	NC	-	No Connect (Not bonded out)
10	OUT	3	Output of the transconductance amplifier
11	DNC	-	Do not connect, leave floating. This pin leaks to V-.
12	DNC	-	Do not connect, leave floating. This pin leaks to V-.
13	RS+	1	Positive sense input of current sense amplifier
14	NC	-	No Connect (Not bonded out)



Circuit 1



Circuit 2



Circuit 3

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
V+ to V-	-	42	V
Input Common Mode Voltage Range (VRS+, VRS-)	-0.3	42	V
Maximum Input Voltage Differential (RS+ to RS-)	-42	42	V
Maximum Differential Input Current	-	4	mA
Maximum Power Supply Ramp Rate	-	10	V/µs
Maximum Junction Temperature	-	+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Human Body Model (Tested per MIL-STD-883 TM3015)	-	4	kV
Charged Device Model (Tested per JS-002-2022)	-	2	kV
Latch-Up (Tested per JESD78E; Class 2, Level A), at +125°C	-	100	mA

3.2 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
V+ to V-	2.7	40	V
Input Common-Mode Voltage Range (from V-)	-0.3	40	V
Input Voltage Differential (RS+ to RS-)	0	150	mV
Temperature	-55	+125	°C

3.3 Outgas Testing

Specification (Tested per ASTM E 595, 1.5)	Value	Unit
Total Mass Lost[1]	0.06	%
Collected Volatile Condensible Material[1]	<0.01	%
Water Vapor Recovered	0.03	%

1. Outgassing results meet NASA requirements of Total Mass Lost <1% and Collected Volatile Condensible Material of <0.1%.

3.4 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	14 Ld TSSOP Package	θ_{JA}[1]	Junction to ambient	92	°C/W
		θ_{JC}[2]	Junction to case	22	°C/W

1. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board. See TB379 for details.
2. For θ_{JC}, the case temperature location is taken at the package top center.

3.5 Electrical Specifications

3.5.1 V+ = 12V

Recommended operating conditions, V+ = V_{RS+} = 12V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 25kΩ and T_A = +25°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
Input Specifications						
Input Common-Mode Voltage Range	V_{CM}	Assured by CMRR Test	**-0.3**	-	**40**	V
Transconductance	g_m	V_{SEN} = 25mV to 150mV, V_{RS+} = V+ T_A = +25°C	1.976	1.997	2.016	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = V+, T_A = -55°C, +125°C	1.966	-	2.026	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = V+, T_A = +25°C, Post Radiation	1.976	1.997	2.016	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = 0V T_A = +25°C	1.940	2.009	2.060	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = 0V, T_A = -55°C, +125°C	1.930	-	2.070	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = 0V, T_A = +25°C, Post Radiation	1.940	2.009	2.060	µA/mV
Input Offset Voltage	V_{OS}	V_{SEN} = 5mV T_A = +25°C	-400	10	400	µV
		V_{SEN} = 5mV T_A = -55°C, +125°C	-700	-	700	µV
		V_{SEN} = 5mV T_A = +25°C, Post Radiation	-400	-20	400	µV
		V_{SEN} = 5mV, V_{RS+} = 0V T_A = +25°C	-400	10	400	µV
		V_{SEN} = 5mV, V_{RS+} = 0V T_A = -55°C, +125°C	-800	-	700	µV
		V_{SEN} = 5mV, V_{RS+} = 0V T_A = +25°C, Post Radiation	-400	-50	400	µV
Input Bias Current	I_{BIAS}	V_{SEN} = 0mV	-	12	**25**	µA
		V_{SEN} = 0mV, V_{RS+} = 0V	**-25**	-8	**-**	µA
Input Offset Current	I_{OS}	V_{SEN} = 0mV	**-1**	-	**1**	µA
		V_{SEN} = 0mV, V_{RS+} = 0V	**-1**	-	**1**	µA
Input Bias Current (Powered Off)	I_{OFF}	V+ = V_{SEN} = 0mV, V_{RS+} = 12V	**-0.8**	-	**0.8**	µA

Recommended operating conditions, V+ = V_{RS+} = 12V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 25kΩ and T_A = +25°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
Common-Mode Rejection Ratio	CMRR	V_{SEN} = 5mV, V_{RS+} = 2.7V, 40V	90	103	-	dB
		V_{SEN} = 5mV, V_{RS+} = 2.7V, 40V, T_A = -55°C, +125°C	85	-	-	dB
		V_{SEN} = 5mV, V_{RS+} = 2.7V, 40V, Post Radiation	90	103	-	dB
		V_{SEN} = 5mV, V_{RS+} = -0.3V, 40V	90	106	-	dB
		V_{SEN} = 5mV, V_{RS+} = -0.3V, 40V, T_A = -55°C, +125°C	85	-	-	dB
		V_{SEN} = 5mV, V_{RS+} = -0.3V, 40V, Post Radiation	90	106	-	dB
Output Specifications						
Minimum Output Voltage	V_{OL}	V_{SEN} = 0mV	**-**	-	**20**	mV
Maximum Output Voltage	V_{OH}	A_V = 100, V_{SEN} = 120mV	**10.0**	10.7	**11.4**	V
Minimum Guaranteed Linear Output Voltage	OVR	V_{SEN} = 150mV, R_L = OPEN	**10**	-	**-**	V
Maximum Linear Output Current Range	I_{OUT}	R_{OUT} = 0Ω, T_A = -55°C, +25°C, +125°C	1200	1550	1800	µA
		R_{OUT} = 0Ω, Post Radiation	1000	1250	1800	µA
Short-Circuit Current	-	V_{RS+} = 40V, V_{RS-} = 0V, R_{OUT} = 0Ω, T_A = -55°C, +25°C, +125°C	1200	1550	1800	µA
		V_{RS+} = 40V, V_{RS-} = 0V, R_{OUT} = 0Ω, Post Radiation	1000	1250	1800	µA
Power Supply Specifications						
Power Supply Range	V+	Assured by PSRR Test	**2.7**	-	**40**	V
Supply Current	I+	V_{SEN} = 0mV, V_{RS+} = 0V, V+	-	250	**400**	µA
Power Supply Rejection Ratio	PSRR	V_{SEN} = 5mV, V_{RS+} = 0V, 40V, V+ = 2.7V, 40V	90	96	-	dB
		V_{SEN} = 5mV, V_{RS+} = 0V, 40V, V+ = 2.7V, 40V, T_A = -55°C, +125°C	85	-	-	dB
		V_{SEN} = 5mV, V_{RS+} = 0V, 40V, V+ = 2.7V, 40V, Post Radiation	90	95	-	dB
AC Specifications						
500kHz Attenuation	Att_{500kHz}	V_{SEN} = 50mV, C_L = 10pF, A_V = 10, f_{TEST}=1kHz, 500kHz	-3	-0.17	**-**	dB
Settling Time	t_S	V_{SEN} = 5mV to 150mV (to 1% of final value)	-	0.8	-	µs
Input Step Response Time	t_{RES}	V_{SEN} = 5mV to 150mV 50% of input to 50% of output	-	0.32	**1**	µs
Slew Rate	SR	V_{SEN} = 5mV to 150mV (T_A = +25°C)	0.50	1.25	2.50	mA/µs
		V_{SEN} = 5mV to 150mV (T_A = +125°C)	0.50	1.90	2.50	mA/µs
		V_{SEN} = 5mV to 150mV (T_A = -55°C)	0.45	0.80	2.50	mA/µs
		V_{SEN} = 5mV to 150mV (T_A = +25°C, Post Rad)	0.50	1.25	2.50	mA/µs

1. Typical values are at 25°C and are not guaranteed.

3.5.2 V+ = 2.7V

Recommended operating conditions, V+ = V_{RS+} = 2.7V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 3.33kΩ and T_A = +25°C unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
Input Specifications						
Input Common-Mode Voltage Range	V_{CM}	Assured by CMRR Test	**-0.3**	-	**40**	V
Transconductance	g_m	V_{SEN} = 25mV to 150mV, V_{RS+} = V+ T_A = +25°C	1.986	2.007	2.026	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = V+, T_A = -55°C, +125°C	1.976	-	2.036	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = V+, T_A = +25°C, Post Radiation	1.986	2.007	2.026	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = 0V T_A = +25°C	1.940	2.013	2.060	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = 0V, T_A = -55°C, +125°C	1.930	-	2.070	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = 0V, T_A = +25°C, Post Radiation	1.940	2.013	2.060	µA/mV
Input Offset Voltage	V_{OS}	V_{SEN} = 5mV T_A = +25°C	-300	400	1000	µV
		V_{SEN} = 5mV T_A = -55°C, +125°C	-600	-	1300	µV
		V_{SEN} = 5mV T_A = +25°C, Post Radiation	-300	320	1000	µV
		V_{SEN} = 5mV, V_{RS+} = 0V T_A = +25°C	-300	250	900	µV
		V_{SEN} = 5mV, V_{RS+} = 0V T_A = -55°C, +125°C	-700	-	1300	µV
		V_{SEN} = 5mV, V_{RS+} = 0V T_A = +25°C, Post Radiation	-300	100	900	µV
Input Bias Current	I_{BIAS}	V_{SEN} = 0mV	-	11	**25**	µA
		V_{SEN} = 0mV, V_{RS+} = 0V	**-25**	-8	**-**	µA
Input Offset Current	I_{OS}	V_{SEN} = 0mV, V_{RS+} = 0V, V+	**-1**	-	**1**	µA
Input Bias Current (Powered Off)	I_{OFF}	V+ = V_{SEN} = 0mV, V_{RS+} = 2.7V	**-1**	-	**1**	µA
Common-Mode Rejection Ratio	CMRR	V_{SEN} = 5mV, V_{RS+} = 2.7V, 40V	90	103	-	dB
		V_{SEN} = 5mV, V_{RS+} = 2.7V, 40V, T_A = -55°C, +125°C	85	-	-	dB
		V_{SEN} = 5mV, V_{RS+} = 2.7V, 40V, Post Radiation	90	103	-	dB
		V_{SEN} = 5mV, V_{RS+} = -0.3V, 40V	90	106	-	dB
		V_{SEN} = 5mV, V_{RS+} = -0.3V, 40V, T_A = -55°C, +125°C	85	-	-	dB
		V_{SEN} = 5mV, V_{RS+} = -0.3V, 40V, Post Radiation	90	106	-	dB

Recommended operating conditions, V+ = V_{RS+} = 2.7V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 3.33kΩ and T_A = +25°C unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
Output Specifications						
Minimum Output Voltage	V_{OL}	V_{SEN} = 0mV	-	-	**14**	mV
Maximum Output Voltage	V_{OH}	Referred to V+, A_V = 100, V_{SEN} = 27mV	**0.7**	1.4	**2.1**	V
Minimum Guaranteed Linear Output Voltage	OVR	V_{SEN} = 150mV, R_L = Open	**0.7**	-	**-**	V
Maximum Linear Output Current Range	I_{OUT}	R_{OUT} = 0Ω	**300**	600	**1100**	µA
Short-Circuit Current		V_{RS+} = 40V, V_{RS-} = 0V, R_{OUT} = 0Ω	**300**	600	**1100**	µA
Power Supply Specifications						
Supply Current	I+	V_{SEN} = 0mV, V_{RS+} = 0V, V+	-	240	**400**	µA
AC Specifications						
500kHz Attenuation	Att_{500kHz}	V_{SEN} = 50mV, C_L = 10pF, A_V = 10, f_{TEST}=1kHz, 500kHz	-3	-0.20	**-**	dB
Settling Time	t_S	V_{SEN} = 5mV to 150mV (to 1% of final value)	-	0.8	**-**	µs
Input Step Response Time	t_{RES}	V_{SEN} = 5mV to 150mV 50% of input to 50% of output	-	0.4	**1**	µs
Slew Rate	SR	V_{SEN} = 5mV to 150mV (T_A = +25°C)	0.50	1.2	2.50	mA/µs
		V_{SEN} = 5mV to 150mV (T_A = +125°C)	0.50	1.8	2.50	mA/µs
		V_{SEN} = 5mV to 150mV (T_A = -55°C)	0.45	0.75	2.50	mA/µs
		V_{SEN} = 5mV to 150mV (T_A = +25°C, Post Rad)	0.50	1.1	2.50	mA/µs

1. Typical values are at 25°C and are not guaranteed.

3.5.3 V+ = 40V

Recommended operating conditions, V+ = V_{RS+} = 40V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 25kΩ and T_A = +25°C unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
Input Specifications						
Input Common-Mode Voltage Range	V_{CM}	Assured by CMRR Test	**-0.3**	-	**40**	V
Transconductance	g_m	V_{SEN} = 25mV to 150mV, V_{RS+} = V+ T_A = +25°C	1.970	1.988	2.010	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = V+, T_A = -55°C, +125°C	1.960	-	2.020	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = V+, T_A = +25°C, Post Radiation	1.970	1.988	2.010	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = 0V T_A = +25°C	1.940	2.011	2.060	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = 0V, T_A = -55°C, +125°C	1.930	-	2.070	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = 0V, T_A = +25°C, Post Radiation	1.940	2.011	2.060	µA/mV

Recommended operating conditions, V+ = V_{RS+} = 40V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 25kΩ and T_A = +25°C unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
Input Offset Voltage	V_{OS}	V_{SEN} = 5mV T_A = +25°C	-1200	-515	300	µV
		V_{SEN} = 5mV T_A = -55°C, +125°C	-1500	-	600	µV
		V_{SEN} = 5mV T_A = +25°C, Post Radiation	-1200	-650	300	µV
		V_{SEN} = 5mV, V_{RS+} = 0V T_A = +25°C	-1100	-365	300	µV
		V_{SEN} = 5mV, V_{RS+} = 0V T_A = -55°C, +125°C	-1600	-	600	µV
		V_{SEN} = 5mV, V_{RS+} = 0V T_A = +25°C, Post Radiation	-1100	-635	300	µV
Input Bias Current	I_{BIAS}	V_{SEN} = 0mV	-	15	**25**	µA
		V_{SEN} = 0mV, V_{RS+} = 0V	**-25**	-9	**-**	µA
Input Offset Current	I_{OS}	V_{SEN} = 0mV, V_{RS+} = 0V, V+	**-1**	-	**1**	µA
Input Bias Current (Powered Off)	I_{OFF}	V+ = V_{SEN} = 0mV, V_{RS+} = 40V	**-0.8**	-	**0.8**	µA
Common-Mode Rejection Ratio	CMRR	V_{SEN} = 5mV, V_{RS+} = 2.7V, 40V	90	103	-	dB
		V_{SEN} = 5mV, V_{RS+} = 2.7V, 40V, T_A = -55°C, +125°C	85	-	-	dB
		V_{SEN} = 5mV, V_{RS+} = 2.7V, 40V, Post Radiation	90	103	-	dB
		V_{SEN} = 5mV, V_{RS+} = -0.3V, 40V	90	106	-	dB
		V_{SEN} = 5mV, V_{RS+} = -0.3V, 40V, T_A = -55°C, +125°C	85	-	-	dB
		V_{SEN} = 5mV, V_{RS+} = -0.3V, 40V, Post Radiation	90	106	-	dB
Output Specifications						
Minimum Output Voltage	V_{OL}	V_{SEN} = 0mV	-	-	**4**	mV
Maximum Output Voltage	V_{OH}	Referred to V+, A_V = 400, V_{SEN} = 100mV	**38**	38.7	**39.4**	V
Minimum Guaranteed Linear Output Voltage	OVR	V_{SEN} = 150mV, R_L = OPEN	**38**	-	-	V
Maximum Linear Output Current Range	I_{OUT}	R_{OUT} = 0Ω, T_A = -55°C, +25°C, +125°C	1200	1600	1800	µA
		R_{OUT} = 0Ω, Post Radiation	1100	1300	1800	µA
Short-Circuit Current	I_{SC}	V_{RS+} = 40V, V_{RS-} = 0V, R_{OUT} = 0Ω, T_A = -55°C, +25°C, +125°C	1200	1600	1800	µA
		V_{RS+} = 40V, V_{RS-} = 0V, R_{OUT} = 0Ω, Post Radiation	1100	1300	1800	µA
Power Supply Specifications						
Supply Current	I+	V_{SEN} = 0mV, V_{RS+} = 0V, V+	**-**	280	**420**	µA
AC Specifications						
500kHz Attenuation	Att_{500kHz}	V_{SEN} = 50mV, C_L = 10pF, A_V = 10, f_{TEST}=1kHz, 500kHz	**-3**	-0.21	**-**	dB

Recommended operating conditions, V+ = V_{RS+} = 40V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 25kΩ and T_A = +25°C unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
Settling Time	t_S	V_{SEN} = 5mV to 150mV (to 1% of final value)	**-**	0.8	**-**	µs
Input Step Response Time	t_{RES}	V_{SEN} = 5mV to 150mV 50% of input to 50% of output	**-**	-	**1**	µs
Slew Rate	SR	V_{SEN} = 5mV to 150mV (T_A = +25°C)	0.50	1.3	2.50	mA/µs
		V_{SEN} = 5mV to 150mV (T_A = +125°C)	0.50	1.9	2.50	mA/µs
		V_{SEN} = 5mV to 150mV (T_A = -55°C)	0.45	0.8	2.50	mA/µs
		V_{SEN} = 5mV to 150mV (T_A = +25°C, Post Rad)	0.50	1.3	2.50	mA/µs

1. Typical values are at 25°C and are not guaranteed.

4. Typical Performance Curves

Recommended operating conditions, V+ = V_{RS+} = 12V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 25kΩ and T_A = +25°C, unless otherwise specified.

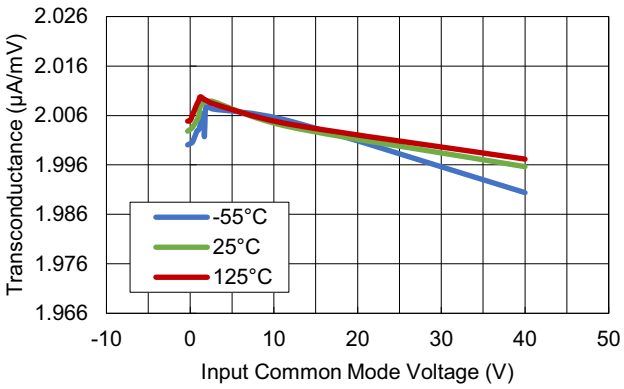


Figure 5. Transconductance, V+ = 12V

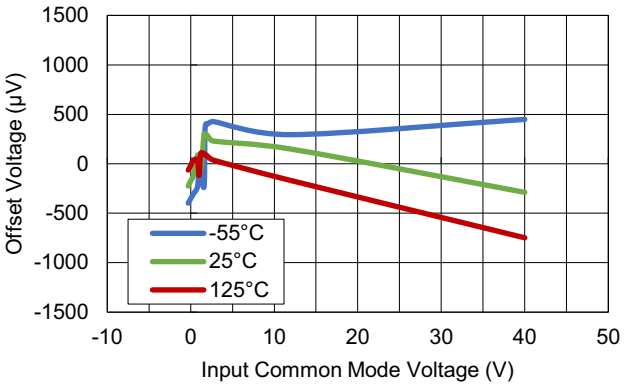


Figure 6. Common-Mode Voltage vs V_{OS}, V+ = 12V

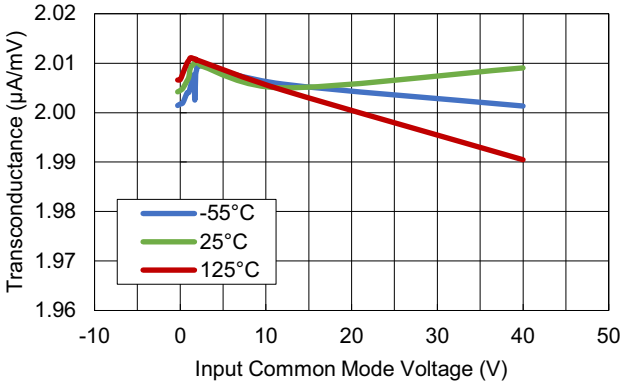


Figure 7. Transconductance, V+ = 40V

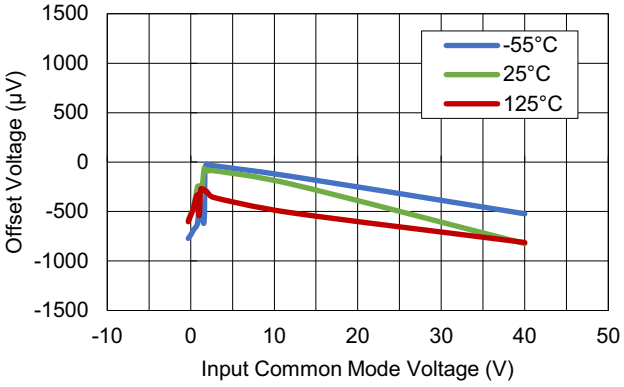


Figure 8. Common-Mode Voltage vs V_{OS}, V+ = 40V

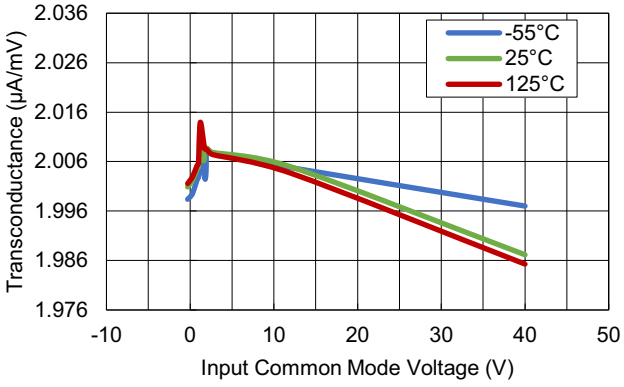


Figure 9. Transconductance, V+ = 2.7V

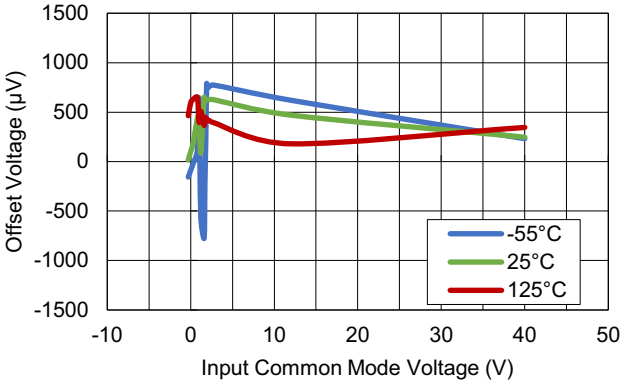


Figure 10. Common-Mode Voltage vs V_{OS}, V+ = 2.7V

Recommended operating conditions, V+ = V_{RS+} = 12V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 25kΩ and T_A = +25°C, unless otherwise specified. (Cont.)

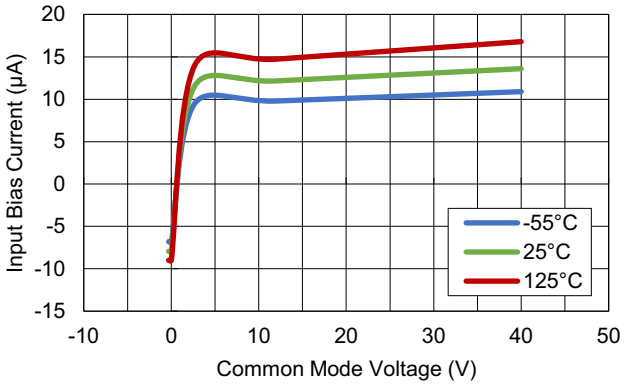


Figure 11. Input Bias Current vs VCM, V+ = 12V

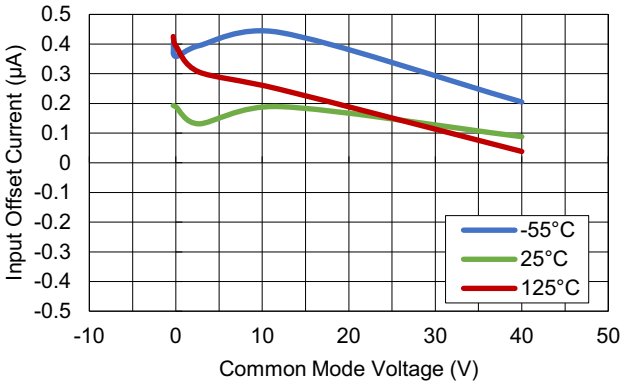


Figure 12. Input Offset Current vs VCM, V+ = 12V

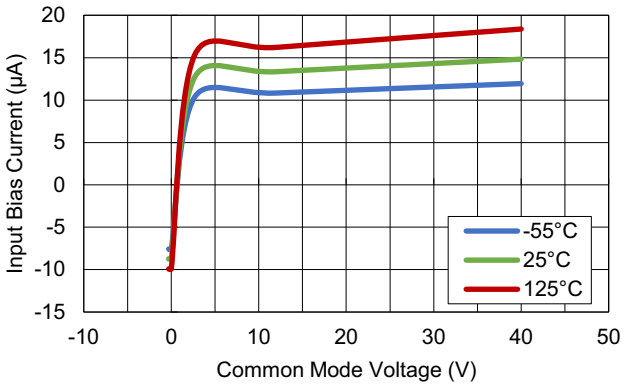


Figure 13. Input Bias Current vs VCM, V+ = 40V

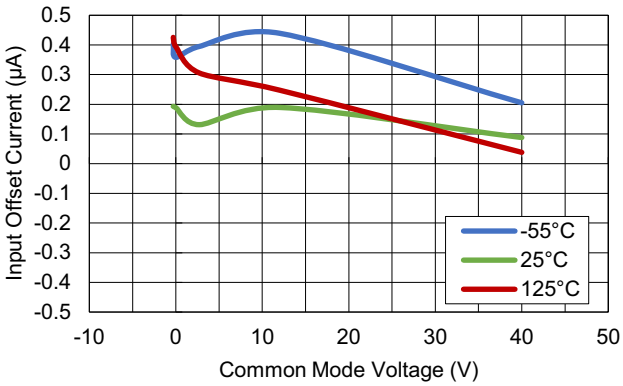


Figure 14. Input Offset Current vs VCM, V+ = 40V

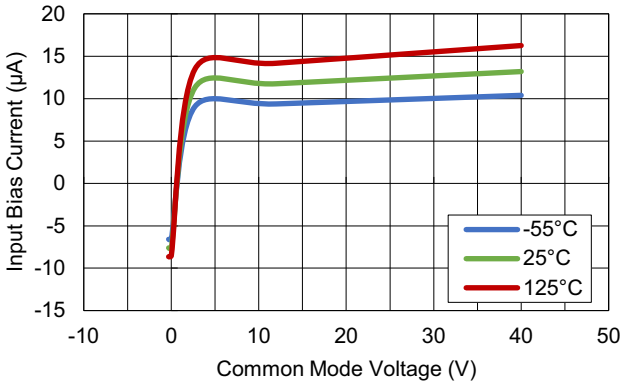


Figure 15. Input Bias Current vs VCM, V+ = 2.7V

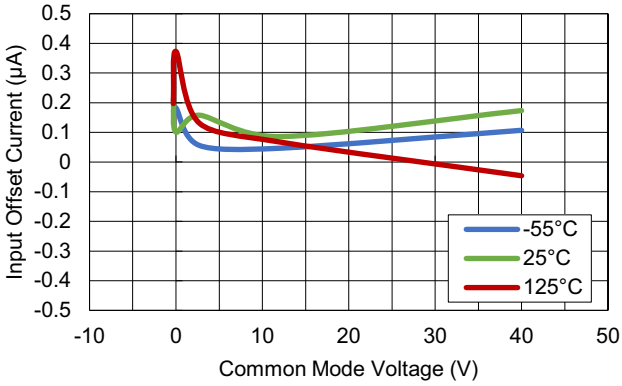


Figure 16. Input Offset Current vs VCM, V+ = 2.7V

Recommended operating conditions, V+ = V_{RS+} = 12V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 25kΩ and T_A = +25°C, unless otherwise specified. (Cont.)

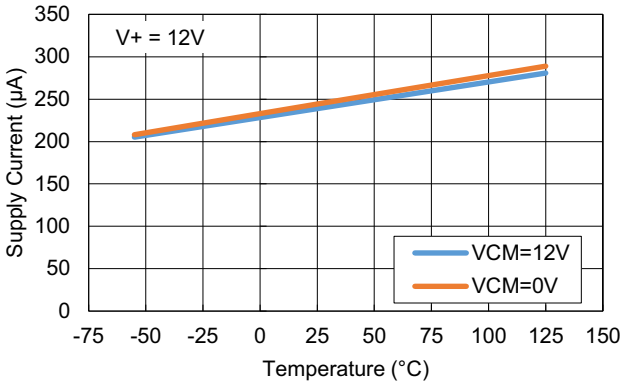


Figure 17. Supply Current, V+ = 12V

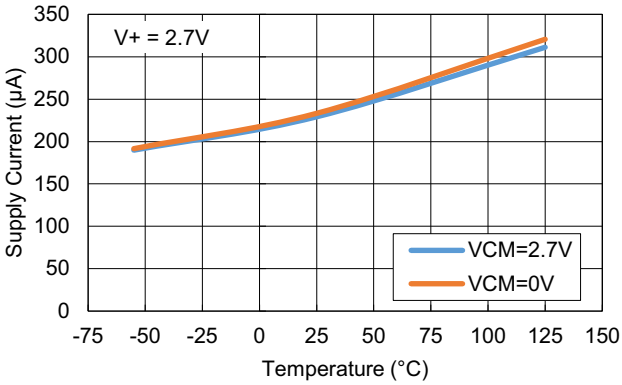


Figure 18. Supply Current, V+ = 2.7V

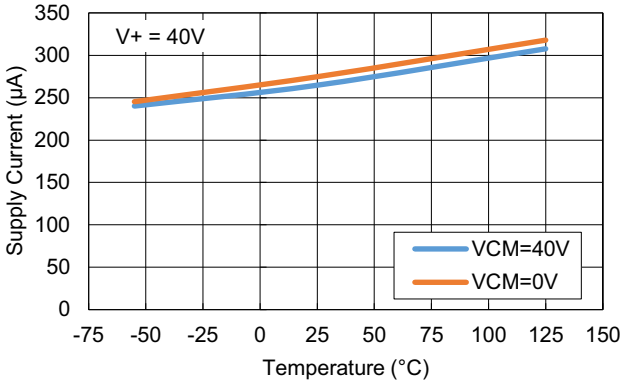


Figure 19. Supply Current, V+ = 40V

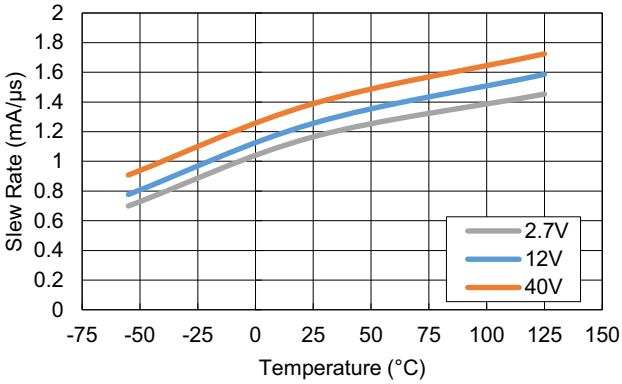


Figure 20. Slew Rate

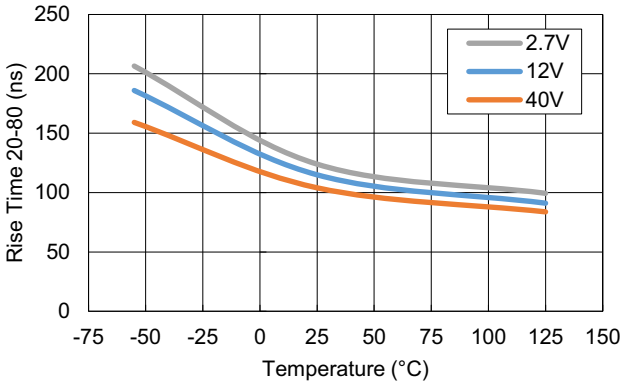


Figure 21. Rise Time

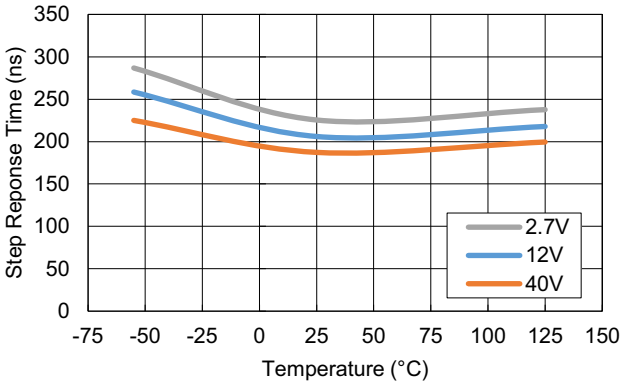


Figure 22. Step Response Time

Recommended operating conditions, V+ = V_{RS+} = 12V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 25kΩ and T_A = +25°C, unless otherwise specified. (Cont.)

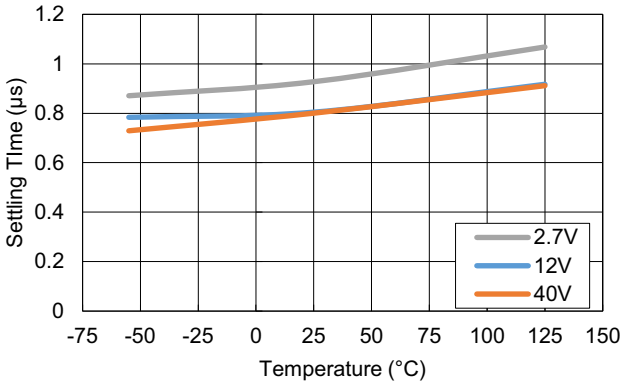


Figure 23. Settling Time

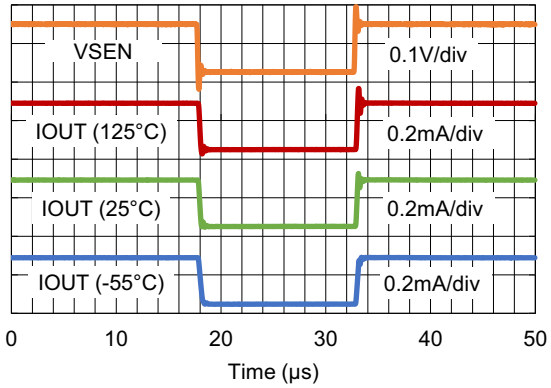


Figure 24. Input Step Response

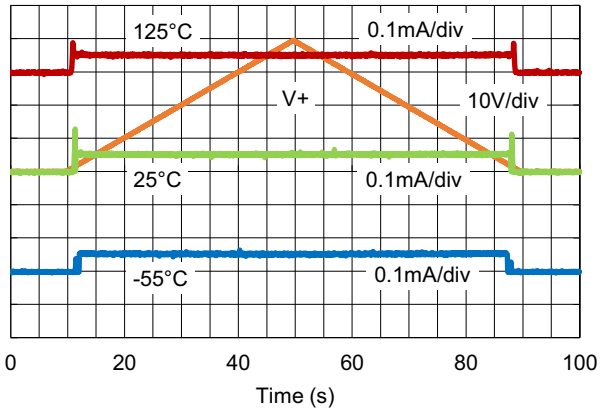


Figure 25. Power Supply Ramp at 1V/s

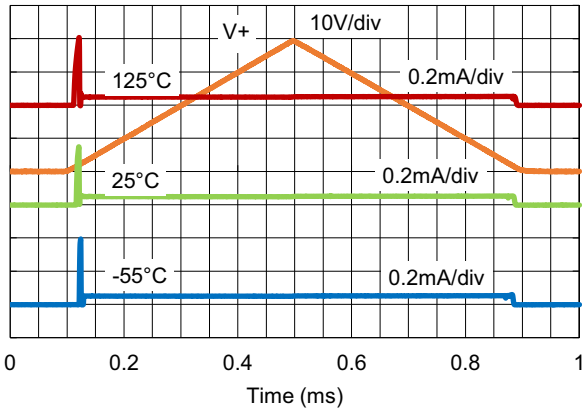


Figure 26. Power Supply Ramp at 1V/10µs

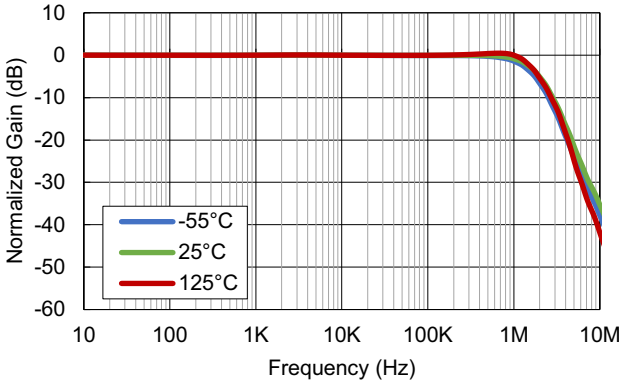


Figure 27. Normalized Gain, V+ = 12V

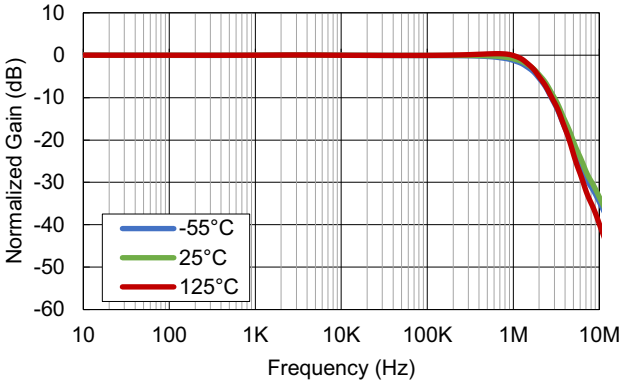


Figure 28. Normalized Gain, V+ = 40V

Recommended operating conditions, V+ = V_{RS+} = 12V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 25kΩ and T_A = +25°C, unless otherwise specified. (Cont.)

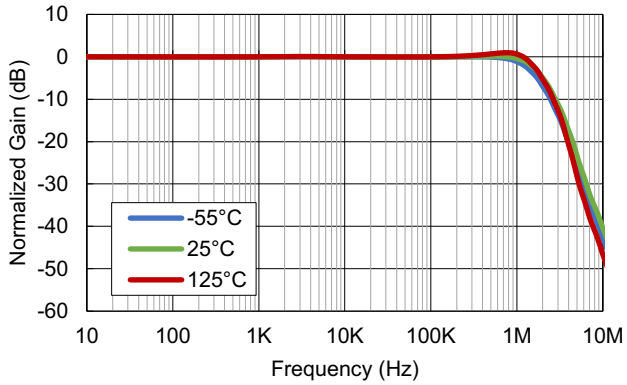


Figure 29. Normalized Gain, V+ = 2.7V

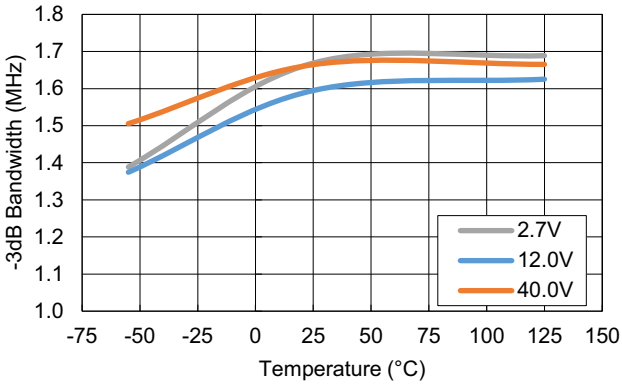


Figure 30. Bandwidth vs Temperature

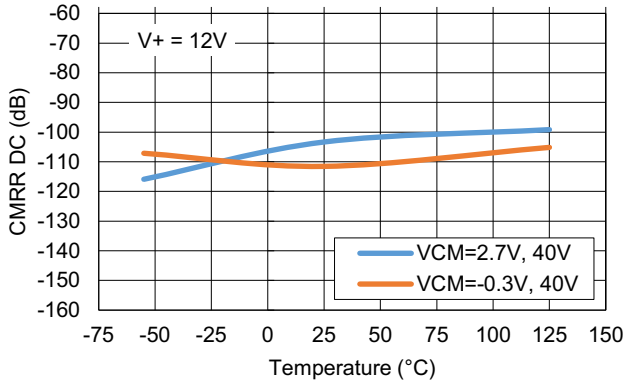


Figure 31. CMRR DC, V+ = 12V

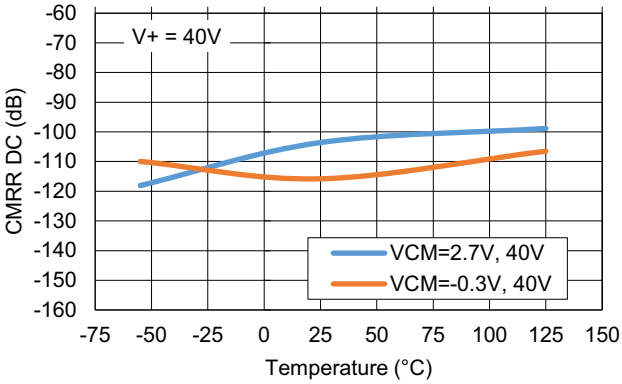


Figure 32. CMRR DC, V+ = 40V

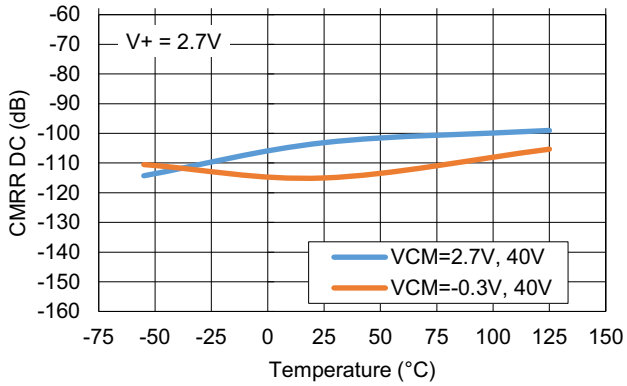


Figure 33. CMRR DC, V+ = 2.7V

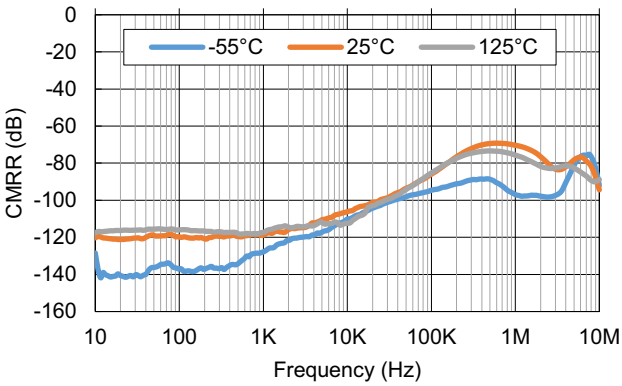


Figure 34. CMRR vs Frequency, V+ = 12V, V_{CM} = 2.7V

Recommended operating conditions, V+ = V_{RS+} = 12V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 25kΩ and T_A = +25°C, unless otherwise specified. (Cont.)

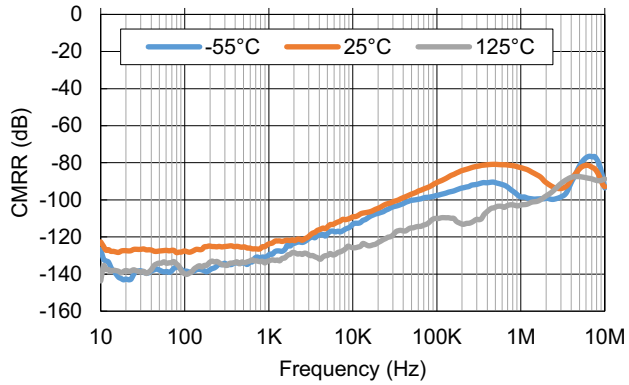


Figure 35. CMRR vs Frequency, V+ = 12V, V_{CM} = 12V

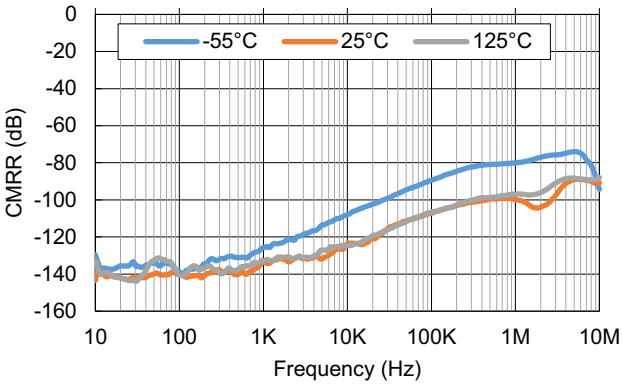


Figure 36. CMRR vs Frequency, V+ = 12V, V_{CM} = 40V

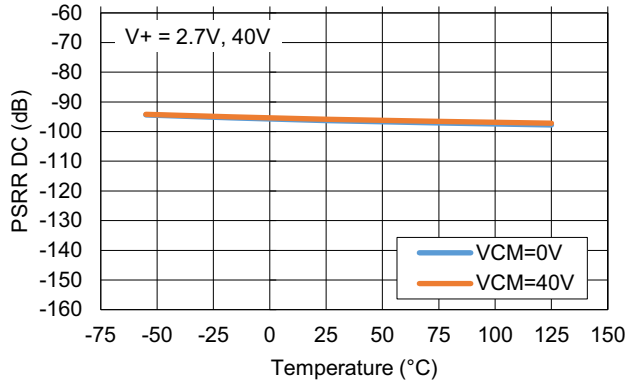


Figure 37. PSRR DC

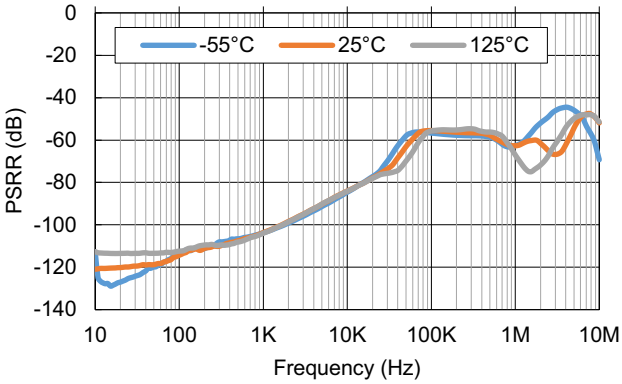


Figure 38. PSRR vs Frequency, V+ = 2.7V, V_{CM} = 12V

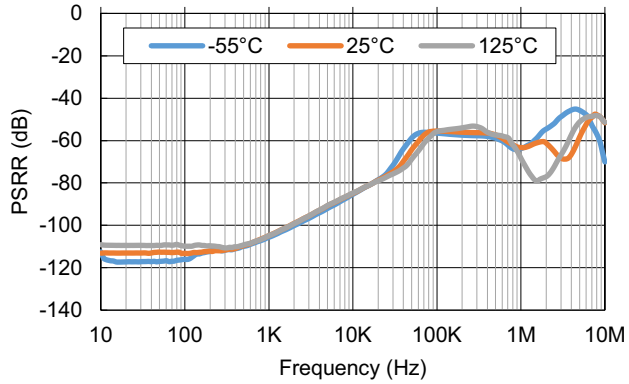


Figure 39. PSRR vs Frequency, V+ = 12V, V_{CM} = 12V

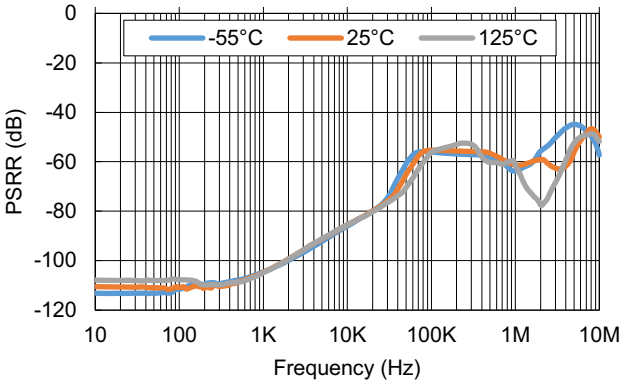


Figure 40. PSRR vs Frequency, V+ = 40V, V_{CM} = 12V

Recommended operating conditions, V+ = V_{RS+} = 12V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 25kΩ and T_A = +25°C, unless otherwise specified. (Cont.)

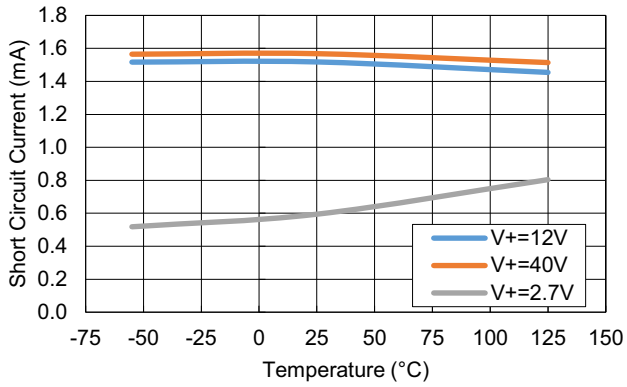


Figure 41. Short-Circuit Current

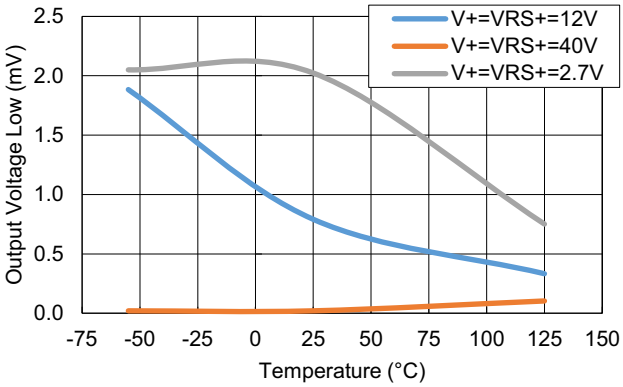


Figure 42. Output Voltage Low

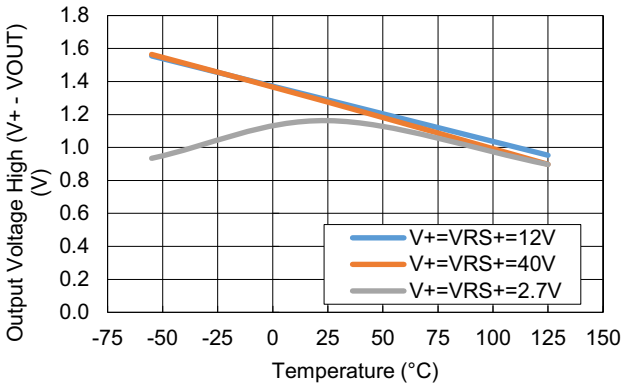


Figure 43. Output Voltage High (Referred to V+)

5. Functional Description

The ISL70100SLH is a transconductance current sense amplifier with a power supply range of 2.7V to 40V. Its input common-mode range extends from -0.3V to 40V, which makes it ideal for use in both low-side and high-side applications. The input common-mode voltage is independent of the power supply such that the ISL70100SLH can be powered by a 5V rail but sense a 40V common mode. The ISL70100SLH level shifts in the sensed voltage from the sensed power supply to a ground-referenced output. The output gain of the ISL70100SLH can be easily configured with a single resistor on the output. It outputs a current proportional to the input voltage differential and the output resistor sets the voltage gain seen by downstream devices.

The ISL70100SLH can be driven with bi-polar supplies with the positive voltage on V+ and the negative voltage on V-. The same voltage differentials should still be between 2.7V and 40V from V+ to V-. The output of the amplifier is referenced to V- so any downstream device must be able to handle a bipolar input.

5.1 Output Signal Range

The output range of the amplifier is limited on the low end by the input offset voltage and the saturation voltage of the output transistors on the top end. The maximum voltage is always about 2V below the voltage on V+. If the application calls for a large gain, the supply voltage may need to be increased to accommodate the full output voltage range. For example, if the supply voltage is 2.7V, the output can only get up to 0.7V before the output is saturated; this sets the maximum gain with 2.7V supply to 4.67 with a maximum sensing voltage of 150mV. If the sensing voltage range is reduced, higher gains can be used.

(EQ. 1) $$A_{CSA(MAX)} = \frac{V_{OH}}{V_{SEN(MAX)}}$$

where:

- $A_{CSA(MAX)}$ is the maximum output gain given the maximum input differential
- V_{OH} is the maximum output high voltage from the electrical specifications table in volts
- $V_{SEN(MAX)}$ is the maximum input differential that the application calls for in volts

Typically, the output of the ISL70100SLH is connected to the input of an Analog-to-Digital Converter (ADC), which has limited input voltage ranges. Ensure that the output voltage ($I_{OUT(MAX)} \times R_{OUT}$) does not exceed the input voltage range of the downstream ADC.

5.2 Input Common-Mode Range

The input common-mode range of the ISL70100SLH ranges from -0.3V to 40V regardless of the voltage on V+. The electrical specifications table shows that the offset voltage of these amplifiers changes very slightly over the full common-mode range. The inputs are also capable of either RS+ or RS- dropping to 0V without damaging the amplifier, this is particularly useful in monitoring protection fuse circuits where the output goes to the positive rail if the fuse is blown. If the input differential is reversed (RS- goes above RS+), the output does not phase invert, it remains at the output low voltage specified in the electrical specifications table.

5.3 Crossover Region

The ISL70100SLH accomplishes the wide input common-mode range using multiple input paths that are selected based on the common-mode voltage. The transition point between the high-side and low-side is typically 1.7V but can range from 1.5V to 2.0V across temperature. When the common-mode voltage has reached the transition point, there is a soft switchover from the low-side to the high-side.

5.4 Sources of Error

5.4.1 Input Impedance of Downstream Devices

The value of the output resistance is not critical if the circuit that is being driven has a high input impedance. If the driven circuit has a low input impedance, the accuracy of V_{OUT} is reduced. Using an example where the input impedance is 100 times larger than the output resistance. It can be seen that the accuracy drops by 1%.

(EQ. 2) $$V_{OUT} = I_{OUT} \times \frac{R_{OUT} \times R_{IN}}{R_{OUT} + R_{IN}} = I_{OUT} \times \frac{100}{101} = I_{OUT} \times R_{OUT} \times 0.99$$

where:

- V_{OUT} is the output voltage in volts
- I_{OUT} is the output current in amps
- R_{OUT} is output resistance loading the output of the ISL70100SLH in ohms
- R_{IN} is the input impedance of the downstream device in ohms

5.4.2 Input Offset Voltage

The dynamic range of the ISL70100SLH is inversely proportional to the input offset voltage. The dynamic range can be thought of as the maximum sense voltage divided by V_{OS}. These amplifiers have an offset voltage of 10µV typically. The electrical specification table shows how the offset voltage can vary across various operating points.

5.4.3 Input Bias and Offset Current

A typical current sense amplifier has the ability to change its transconductance by changing the input resistors. In this case, the input bias currents and offset currents can induce more error on top of the offset voltage. The ISL70100SLH gets around this by internalizing these input resistors and trimming out the error associated with them during production.

5.4.4 Sensed Current Error

Determine the effective current error using Equation 3. It shows the amount of current that the current-sense amplifier is blind to.

(EQ. 3) $$I_{ERROR} = \frac{V_{OS}}{R_{SENSE}}$$

where:

- V_{OS} is the offset voltage in µV.
- R_{SENSE} is the sense resistor in mΩ.
- I_{ERROR} is the current error in mA.

The R_{SENSE} can be increased to lower the current error, but this reduces the maximum current that can be sensed and increases power dissipation. Careful consideration must be made to balance power dissipation and accuracy.

6. Applications Information

6.1 Selection of the External Current-Sense Resistor

To pick the current-sense resistor value, a decision has to be made between power dissipation and measurement accuracy. As a general rule for all applications, the sense resistor should be as small as possible while still providing adequate input dynamic range across the operating range. The minimum accurately sensed input voltage is primarily limited by the offset voltage of the ISL70100SLH.

The sense resistor value can be calculated once the maximum sensed load current is determined. The maximum recommended sense voltage for the ISL70100SLH is 150mV, so dividing that by the maximum load current provides the sense resistor value.

(EQ. 4) $$R_{SENSE} = \frac{150mV}{I_{L(MAX)}}$$

where:

- R_{SENSE} is the sense resistor in mΩ.
- $I_{L(MAX)}$ is the maximum expected load current to be sensed in amps.

6.2 Gain Setting

The gain on the ISL70100SLH can be adjusted using a single resistor on the output. The ISL70100SLH outputs 2µA for every 1mV of differential across the inputs. Use Equation 5 to calculate the output load resistance to obtain a specific gain:

(EQ. 5) $$R_{OUT} = \frac{A_{CSA}}{g_m}$$

where:

- R_{OUT} is the output load resistance in kΩ.
- A_{CSA} is the required voltage gain.
- g_m is the transconductance of the ISL70100SLH which is 2µA/mV (typical).

6.3 Selection of Output Resistor

The output signal is a current conducted through the output resistor to generate a voltage. With a maximum input range of 150mV, the output current is 300µA. The voltage gain should be determined based on the input voltage range of the downstream device. For example, if there is a 5V ADC on the output of the ISL70100SLH, the output resistance should be 16.6kΩ to ensure that V_{OUT} stays under 5V. This also means that the minimum power supply voltage has to be 7V to achieve 5V on the output. Renesas recommends using resistors that have a low temperature coefficient on the output as it adds error to the measurement.

6.4 Output Filtering

Because the output of these amplifiers is a current source, filtering is straight forward. A capacitor can be placed in parallel to the output resistance to create a pole based on Equation 6:

(EQ. 6) $$f_{-3dB} = \frac{1}{2 \times \pi \times R_{OUT} \times C_{OUT}}$$

where:

- f_{-3dB} is frequency location of the pole in hertz
- R_{OUT} is the output resistance in ohms
- C_{OUT} is the output capacitance in parallel with R_{OUT} in farads

6.5 Response Time

The ISL70100SLH provides fast response time for circuit protection or signal transmission. The delay and speed of the response depend on the starting point of the step. If the sensed current is very low (near zero) before the transient, there may be an increased delay time to see the output react. If fast reaction times are required, increase the sense resistance such that there are a few millivolts (1-5mV) of differential across the inputs under the lowest current condition. The higher the differential is for the lowest current condition, the faster the response time is, but that results in increased DC power losses.

Figure 44 and Figure 45 show the step response difference from starting with a 0mV differential versus starting with a 25mV differential. For most applications the 40-50ns faster reaction time may not warrant the resulting power loss.

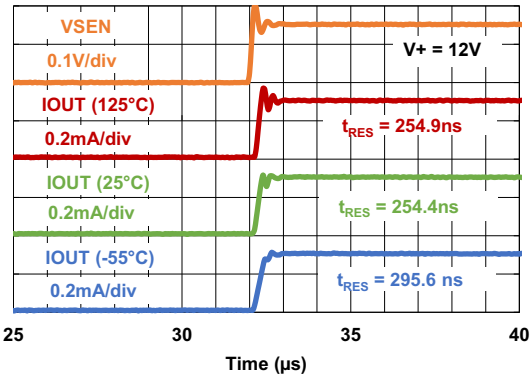


Figure 44. 0mV to 150mV Step Response

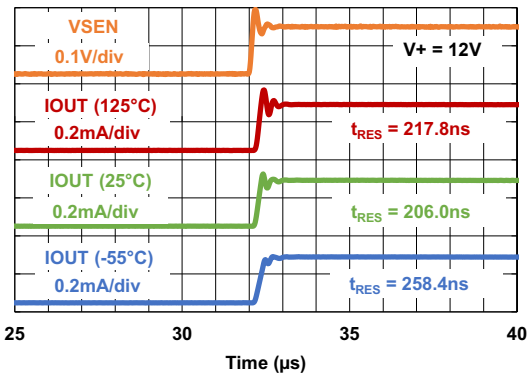


Figure 45. 25mV to 150mV Step Response

7. Die Characteristics

Table 1. Die and Assembly Related Information

Die Information	
Dimensions	2413µm x 3302µm (95 mils x 130 mils) Thickness: 279µm ± 25µm (11 mils ±1 mil)
Interface Materials	
Glassivation	Type: 15kÅ Nitrox
Top Metallization	Type: 30kÅ AlCu (99.5%/0.5%)
Backside Finish	Silicon
Process	PR40
Assembly Information	
Substrate Potential	Floating
Additional Information	
Worst Case Current Density	<2 x 10^5A/cm^2
Transistor Count	560
Weight of Packaged Device	0.054 grams

7.1 Metallization Mask Layout

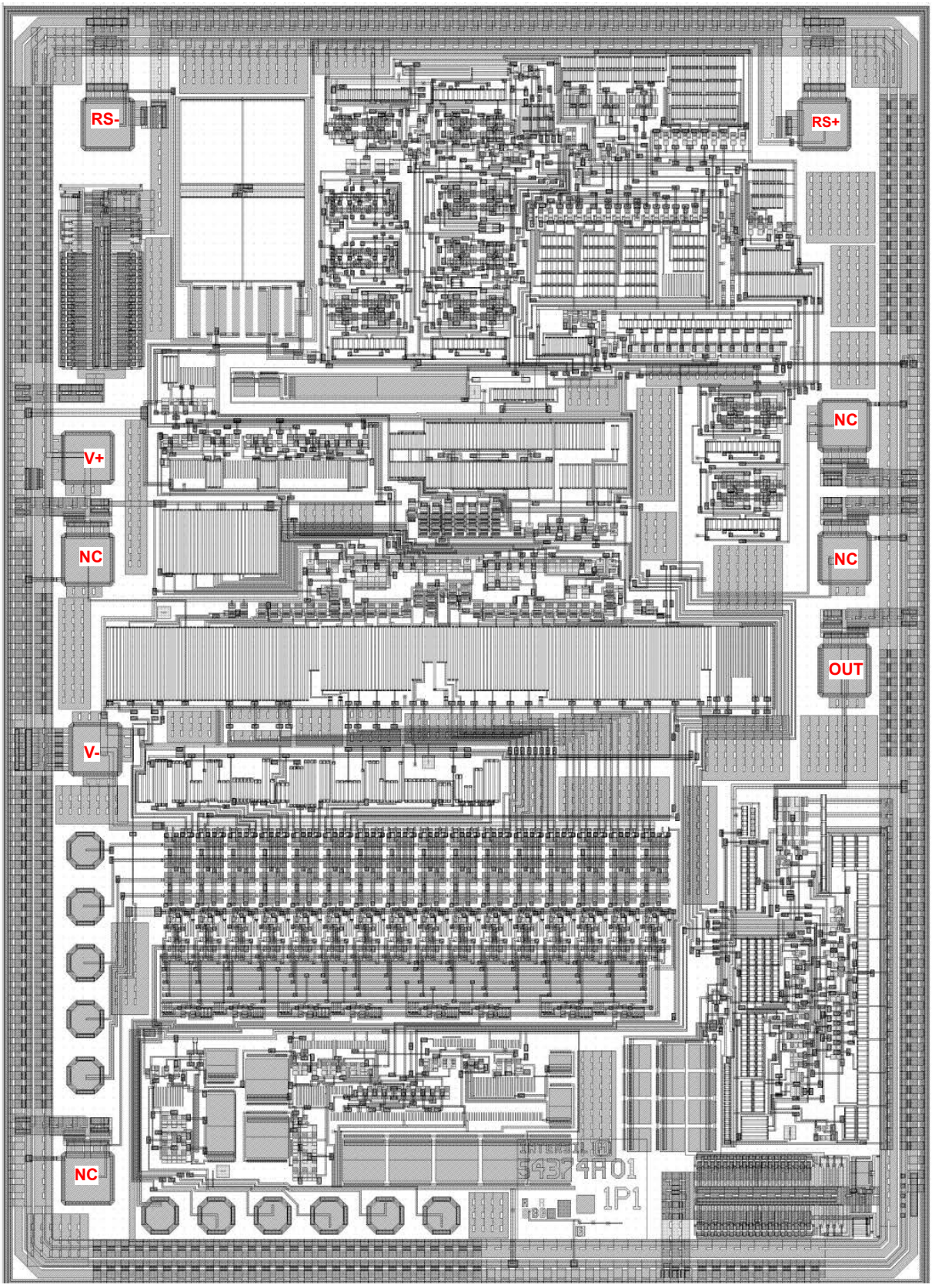


Table 2. Die Layout X-Y Coordinates[1]

Pad Name	ΔX (µm)	ΔY (µm)	X (µm)	Y (µm)
RS-	110	110	-891.0	1302.5
V+	110	110	-941.0	472.5
NC	110	110	-941.0	219.5
V-	110	110	-921.5	-252.5
NC	110	110	-941.0	-1320.5
OUT	110	110	941.0	-57.0
NC	110	110	941.0	223.0
NC	110	110	941.0	553.0
RS+	110	110	891.0	1302.5

1. Origin of coordinates is the center of the die.

8. Package Outline Drawing

The package outline drawing is located at the end of this document and is accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

9. Ordering Information

Part Number[1]	Part Marking	Radiation Lot Acceptance Testing	Package Description[2] (RoHS Compliant)	Package Drawing #	MSL Rating[3]	Carrier Type	Temp Range
ISL70100SLHMVZ	ISL70100 SLHMVZ	LDR to 75krad(Si)	14 Ld TSSOP	M14.173	3	Tray	-55 to +125°C

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and NiPdAu-Ag plate -e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. For the Pb-Free Reflow Profile, see TB493.
3. Moisture Sensitivity Level (MSL) tested per JEDEC J-STD-020. For more information about MSL, see TB363.

10. Revision History

Rev.	Date	Description
1.02	Aug 31, 2026	Updated Equation 4.
1.01	Aug 18, 2026	▪ Updated Equation 1 and the information below it. ▪ Updated POD to the latest revision. ▪ Updated Footprint Design Information.
1.00	Jun 25, 2025	Initial release

A. ECAD Design Information

This information supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

A.1 Part Number Indexing

Orderable Part Number	Number of Pins	Package Type	Package Code/POD Number
ISL70100SLHMVZ	14	TSSOP	M14.173/HV0014AA

A.2 Symbol Pin Information

A.2.1 14-TSSOP

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	NC	Passive	-
2	RS-	Input	-
3	V+	Power	-
4	DNC	Passive	-
5	V-	Power	-
6	DNC	Passive	-
7	NC	Passive	-
8	NC	Passive	-
9	NC	Passive	-
10	OUT	Output	-
11	DNC	Passive	-
12	DNC	Passive	-
13	RS+	Input	-
14	NC	Passive	-

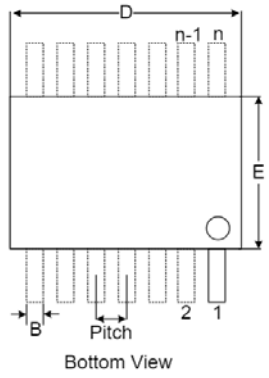
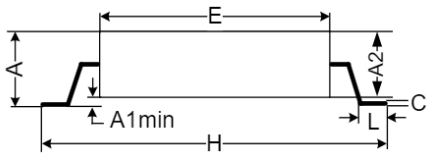
A.3 Symbol Parameters

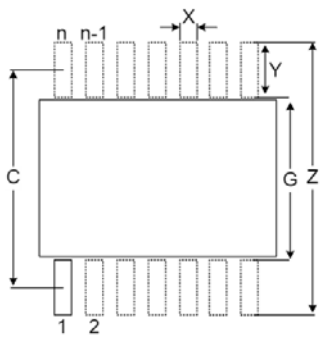
Orderable Part Number	Qualification	Radiation Qualification	LDR	Mounting Type	RoHS	Min Operating Temperature	Max Operating Temperature	Min Input Voltage	Max Input Voltage	Min Common Mode Input Voltage	Max Common Mode Input Voltage	Min Input Differential Voltage	Max Input Differential Voltage	Transconductance Accuracy 25°C	Transconductance Accuracy -55°C, 125°C
ISL70100SLHMVZ	Space	QML Class P	75 krad(Si)	SMD	Compliant	-55 °C	125 °C	2.7 V	40 V	-0.3 V	40 V	0 mV	150 mV	1 %	1.5 %

A.4 Footprint Design Information

A.4.1 14-TSSOP

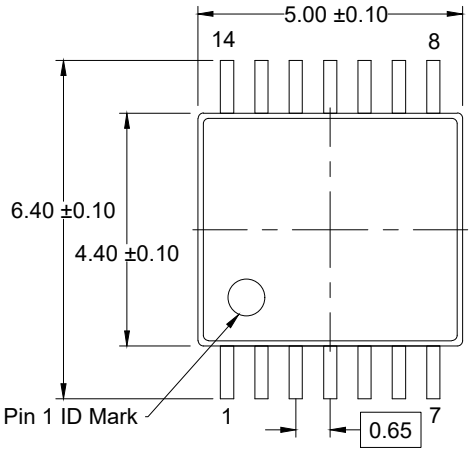
IPC Footprint Type	Package Code/ POD Number	Number of Pins
SOP	M14.173/HV0014AA	14

Description	Dimension	Value (mm)	Diagram
Minimum lead span (horizontal side)	Hmin	6.30	 Bottom View
Maximum lead span (horizontal side)	Hmax	6.50	
Minimum body span (horizontal side)	Dmin	4.90	
Maximum body span (horizontal side)	Dmax	5.10	
Minimum body span (vertical side)	Emin	4.30	
Maximum body span (vertical side)	Emax	4.50	
Minimum Lead Width	Bmin	0.20	
Maximum Lead Width	Bmax	0.30	
Minimum Lead Length	Lmin	0.45	 Side View
Maximum Lead Length	Lmax	0.75	
Maximum Height	Amax	1.20	
Minimum Standoff Height	A1min	0.05	
Minimum Lead Thickness	cmin	0.09	
Maximum Lead Thickness	cmax	0.20	
Total number of pin positions (including absent pins)	PinCount	14	
Distance between the center of any two adjacent pins	Pitch	0.65	

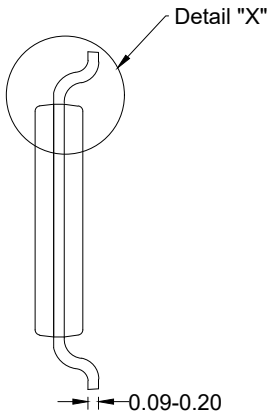
Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram**
Distance between left pad toe to right pad toe.	Z	7.0	 PCB Top View
Distance between left pad heel to right pad heel.	G	4.60	
Row spacing. Distance between pad centers	C	5.80	
Pad Width	X	0.25	
Pad Length	Y	1.20	

Package Outline Drawing

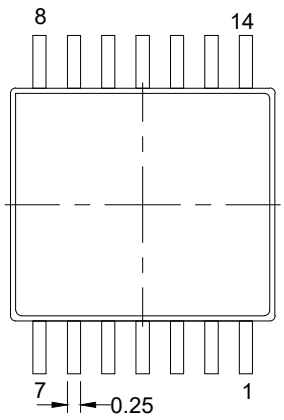
M14.173
HV0014AA
14-Lead Thin Shrink Small Outline package (TSSOP) 5.00 x 4.40 x 1.20 mm Body, 0.65 mm Pitch
Rev05, Aug 14, 2026



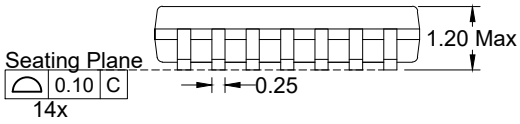
Top View



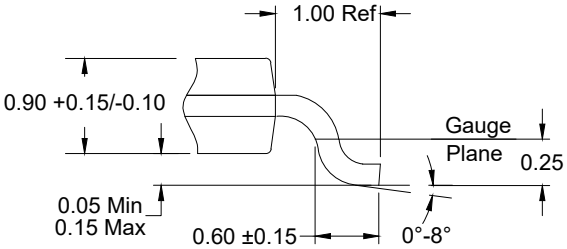
Side View



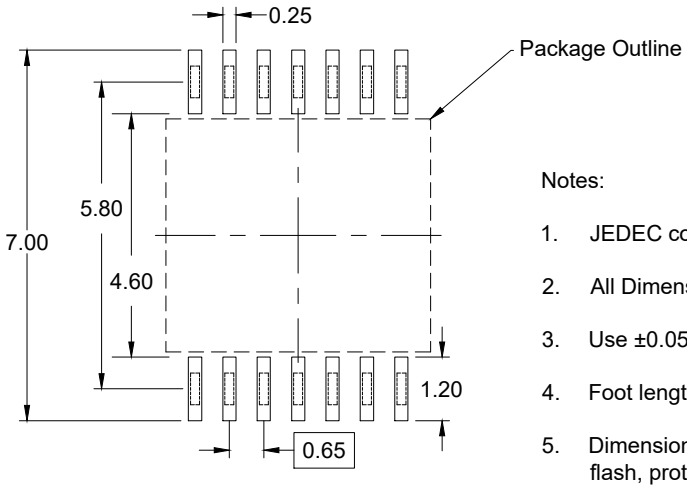
Bottom View



Side View



Detail "X"



Typical Recommended Land Pattern

Notes:

1. JEDEC compatible (MO-153, variation AB-1)
2. All Dimensions are in mm and angles are in degrees
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Foot length is measured at gauge plane 0.25 mm above seating plane.
5. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.
6. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 mm per side.
7. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.80mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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