ISL70020SEH, ISL73020SEH

40V, 65A Enhancement Mode GaN Power Transistors

The ISL70020SEH and ISL73020SEH are 40V N-channel enhancement mode GaN power transistors. These GaN FETs have been characterized for destructive Single Event Effects (SEE) and tested for Total Ionizing Dose (TID) radiation. Applications for these devices include commercial aerospace, medical, and nuclear power generation.

The exceptionally high electron mobility and low temperature coefficient of the GaN allows for very low $r_{DS(ON)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can operate at a higher switching frequency with more efficiency while reducing the overall solution size.

By combining the exceptional performance of the GaN FET in a hermetically sealed Surface Mount Device (SMD) package with manufacturing in a MIL-PRF-38535 like flow results in best-in-class power transistors that are ideally suited for high reliability applications.

Applications

- Switching regulation
- Motor drives
- Relay drives
- Inrush protection
- Down hole drilling

High reliability industrial

Features

- Very low $r_{DS(ON)}$ 3.5mΩ (typical)
- Ultra low total gate charge 19nC (typical)
- ISL70020SEH radiation acceptance testing
  - High dose rate (50-300rad(Si)/s): 100krad(Si)
  - Low dose rate (0.01rad(Si)/s): 75krad(Si)
- ISL73020SEH radiation acceptance testing
  - Low dose rate (0.01rad(Si)/s): 75krad(Si)
- SEE hardness (see the SEE report for details)
  - SEL/SEB LET_{TH} (V_{DS} = 40V, V_{GS} = 0V): 86.4MeV•cm^2/mg(Si)
- Ultra small hermetically sealed 4 Ld Surface Mount Device (SMD) package
  - Package area: 42mm^2
- Full military-temperature range operation
  - T_A = -55°C to +125°C
  - T_J = -55°C to +150°C
- Qualified to Renesas Rad Hard GaN FET Screening and QCI Flow (R34TB0003EU)
  - All screening and QCI are in accordance with MIL-PRF-38535L Class-V

Figure 1. ISL70020SEH 4 Ld SMD Package

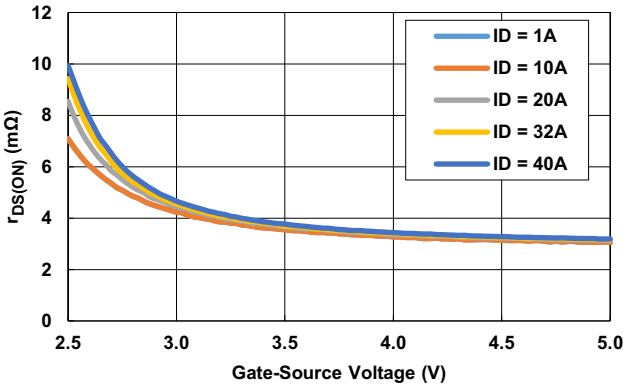


Figure 2. On-State Resistance (+25°C)

1. Overview

1.1 Ordering Information

Ordering Part Number (Note 1)	Radiation Hardness (Total Ionizing Dose)	Temperature Range (°C)	Package (RoHS Compliant)	Package Drawing
ISL70020SEHML	HDR to 100krad(Si) LDR to 75krad(Si)	-55 to +125	4 Ld SMD	J4.A
ISL70020SEHMX (Notes 3, 4)	HDR to 100krad(Si) LDR to 75krad(Si)	-55 to +125	Die	N/A
ISL70020SEHX/SAMPLE (Notes 3, 2, 4)	N/A	-55 to +125	Die	N/A
ISL70020SEHL/PROTO (Note 2)	N/A	-55 to +125	4 Ld SMD	J4.A
ISL73020SEHML	LDR to 75krad(Si)	-55 to +125	4 Ld SMD	J4.A
ISL73020SEHMX (Note 3, 4)	LDR to 75krad(Si)	-55 to +125	Die	N/A
ISL73020SEHX/SAMPLE (Notes 3, 2, 4)	N/A	-55 to +125	Die	N/A
ISL73020SEHL/PROTO (Note 2)	N/A	-55 to +125	4 Ld SMD	J4.A
ISL70040SEHEV5Z (Note 5)	ISL70040SEH and ISL70020SEH Evaluation Board			

Notes:

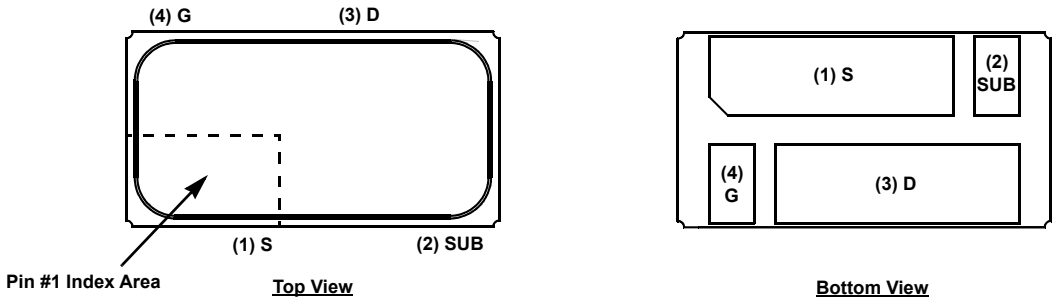
1. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. The /PROTO and /SAMPLE parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO and /SAMPLE parts meet the electrical limits and conditions across the temperature range specified in this datasheet and are of the same form and fit as the ISL70020SEHML/ISL73020SEHML devices. The /PROTO and /SAMPLE parts do not come with a Certificate of Conformance (C of C) and have no accompanying data or documentation.
3. Die product tested at T_A = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in "Electrical Specifications" on page 5.
4. The die solder bump composition is PbSn (95%/5%) with a melt point of 312°C. Recommended reflow profile includes a ramp-up to a peak of 350-360°C with a dwell time of 3 minutes at/near the peak before ramp-down in a hydrogen forming gas with 3% hydrogen.
5. Evaluation board uses the /PROTO parts and /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

Table 1. Key Differences Between Family of Parts

Part Number	Breakdown Voltage (V)	Drain Current (A)	$r_{DS(ON)}$ (mΩ)	Q_G (nC)
ISL7x020SEH	40	65	3.5	19
ISL7x023SEH	100V	60	5	14
ISL7x024SEH	200V	7.5	45	2.5

1.2 Pin Configuration

4 Ld SMD



Note: The ESD triangular mark indicates Pin #1. It is a part of the device marking and is placed on the lid in the quadrant where Pin #1 is located.

1.3 Pin Descriptions

Pin Number	Pin Name	Description
1	S	Source connection for the GaN FET.
2	SUB	Substrate connection for the GaN FET which is internally shorted in to source. Tie this pin to source on the PCB.
3	D	Drain connection for the GaN FET
4	G	Gate connection for the GaN FET. Minimize trace inductance from driver to reduce over-stressing the gate.
NA	Lid	Internally tied to the source pin.

2. Specifications

2.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Maximum	Unit
V_{DS} (Note 6)	40	V
V_{GS}	-4 to 6	V

Note:
6. Tested in a heavy ion environment at LET = 86.4MeV•cm^2/mg(Si) at +125°C (T_C).

2.2 ESD Ratings

ESD Model/Test	Rating	Unit
Drain-to-Source		
Human Body Model (Tested per MIL-STD-883 TM3015)	2	kV
Machine Model (Tested per JESD22-A115C)	200	V
Charged Device Model (Tested per JS-002-2014)	750	V
Gate-to-Source		
Human Body Model (Tested per MIL-STD-883 TM3015)	500	V
Machine Model (Tested per JESD22-A115C)	200	V
Charged Device Model (Tested per JS-002-2014)	750	V

2.3 Thermal Information

SMD Package J4.A			
Thermal Resistance	**Typical**	**Maximum**	**Unit**
θ_{JA} (Note 7)	23.0		°C/W
θ_{JC} (Note 8)	3.1	3.9	°C/W

Notes:
7. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
8. For θ_{JC}, the case temperature location is on the solder terminations adjacent to the center of the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature	-	+150	°C
Storage Temperature Range	-65	+150	°C

2.4 Recommended Operating Conditions

Parameter	Maximum	Unit
Ambient Temperature	-55 to +125	°C
V_{DS}	32	V
I_D (V_{GS} = 5.0V, T_C = +25°C) Note 9	65	A
I_D (V_{GS} = 5.0V, T_C = +105°C) Note 9	40	A

Note:
9. T_J = +150°C. Current limited by package constraints.

2.5 Electrical Specifications

Unless otherwise noted, V_{DS} = 32V. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 100krad(Si) with exposure at a high dose rate of 50-300rad(Si)/s (ISL70020SEH only); or over a total ionizing dose of 75krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Min (Note 11)	Typ (Note 10)	Max (Note 11)	Unit
Static Characteristics						
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 1.6mA	**40**	-	-	V
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 32V, V_{GS} = 0V	-	0.1	**1.5**	mA
Drain-to-Gate Leakage Current	I_{GSX}	V_{DS} = 32V, V_{GS} = 0V	-	0.1	**0.7**	mA
Gate-to-Source Forward Leakage	I_{GSS}	V_{GS} = 5V	-	1	**9**	mA
Gate-to-Source Reverse Leakage		V_{GS} = -4V	**-0.7**	-0.1	-	mA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 12mA	**0.7**	1.2	**2.5**	V
Drain-to-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 5V, I_D = 35A, T_A = +25°C	-	3.5	6	mΩ
		V_{GS} = 5V, I_D = 35A, T_A = 125°C	-	5.2	8	mΩ
		V_{GS} = 5V, I_D = 37A, T_A = +25°C (die only) (Note 12)	-	1.2	1.5	mΩ
Source-to-Drain Forward Voltage	V_{SD}	I_S = 0.5A, V_{GS} = 0V,	**0.7**	1.8	**3**	V
Dynamic Characteristics						
Input Capacitance	C_{ISS}	V_{DS} = 20V, V_{GS} = 0V (Note 12)	-	1920	-	pF
Output Capacitance	C_{OSS}	V_{DS} = 20V, V_{GS} = 0V, T_A = +25°C	-	1620	2430	pF
Gate Resistance	r_G	T_A = +25°C, (Note 12)	-	300	-	mΩ
Reverse Transfer Capacitance	C_{RSS}	V_{DS} = 20V, V_{GS} = 0V (Note 12)	-	29	-	pF
Total Gate Charge	Q_G	V_{DS} = 20V, I_D = 35A, V_{GS} = 5V, T_A = +25°C	-	19	25	nC
Gate Charge at Threshold	$Q_{G(th)}$	V_{DS} = 20V, I_D = 35A (Note 12)	-	3.8	-	nC
Gate-to-Drain Charge	Q_{GD}	V_{DS} = 20V, I_D = 35A, T_A = +25°C	-	7	13	nC
Gate-to-Source Charge	Q_{GS}	V_{DS} = 20V, I_D = 35A, T_A = +25°C	-	-	10	nC
Output Charge	Q_{OSS}	V_{DS} = 20V, V_{GS} = 0V (Note 12)	-	45	68	nC

Notes:

10. Typical values shown are not guaranteed.
11. Parameters with MIN and/or MAX limits are 100% tested at -55°C, +25°C, and +125°C, unless otherwise specified.
12. Limits are established by characterization and/or design, not tested.

3. Typical Performance Curves

Unless otherwise noted, V_{DS} = 32V; T_A = +25°C.

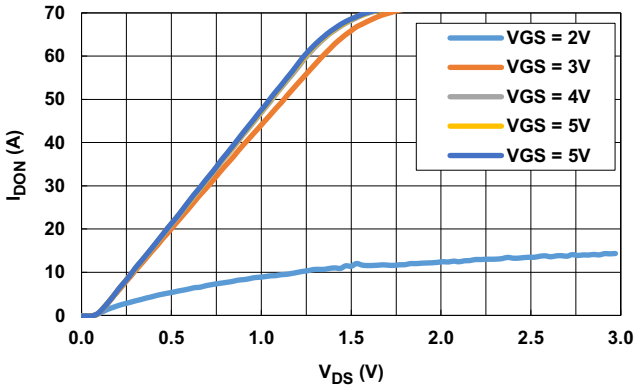


Figure 3. Output Characteristics (+25°C)

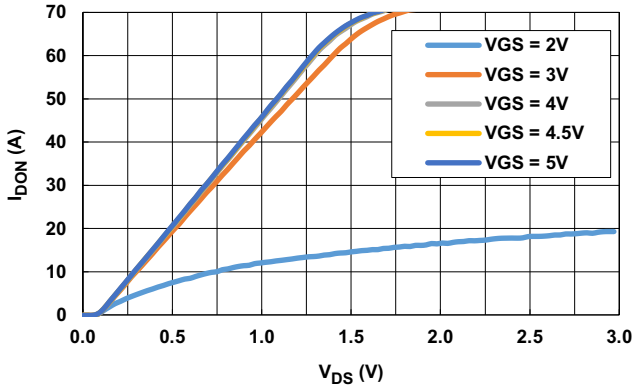


Figure 4. Output Characteristics (+125°C)

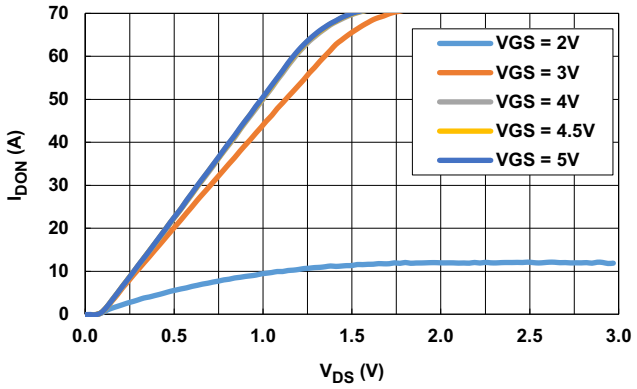


Figure 5. Output Characteristics (-55°C)

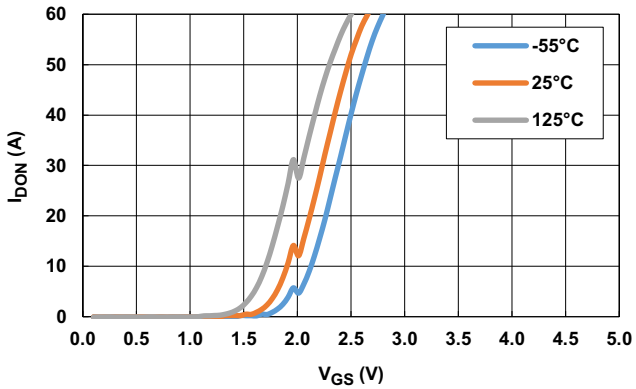


Figure 6. Transfer Characteristics

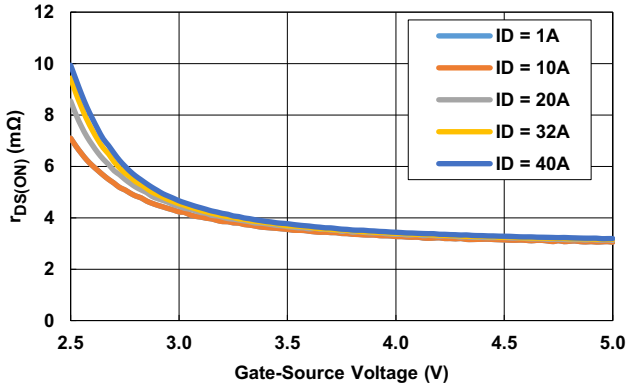


Figure 7. On-State Resistance (+25°C)

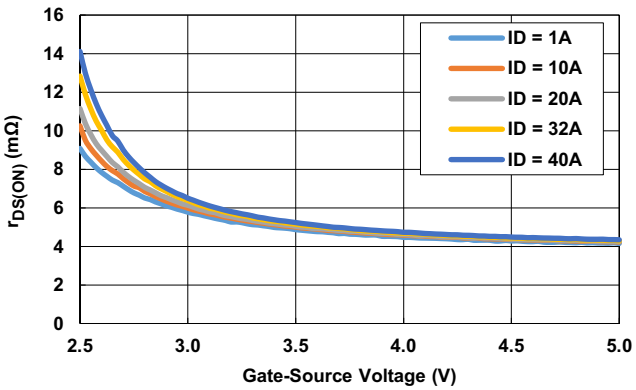


Figure 8. On-State Resistance (+125°C)

Unless otherwise noted, V_{DS} = 32V; T_A = +25°C. **(Continued)**

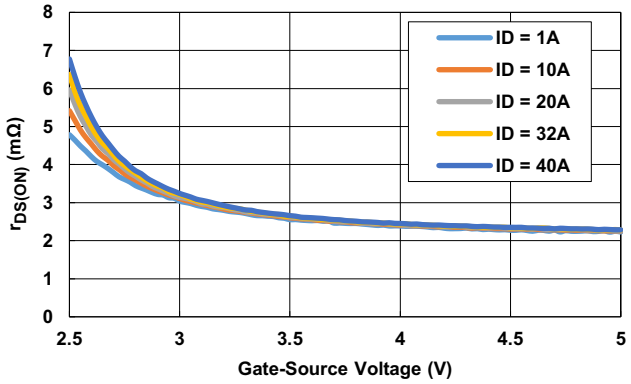


Figure 9. On-State Resistance (-55°C)

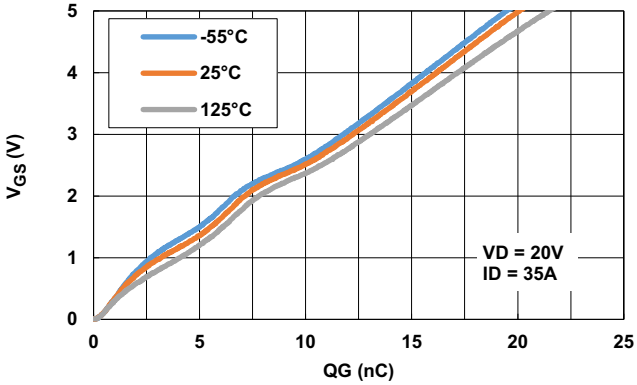


Figure 10. Gate Charge

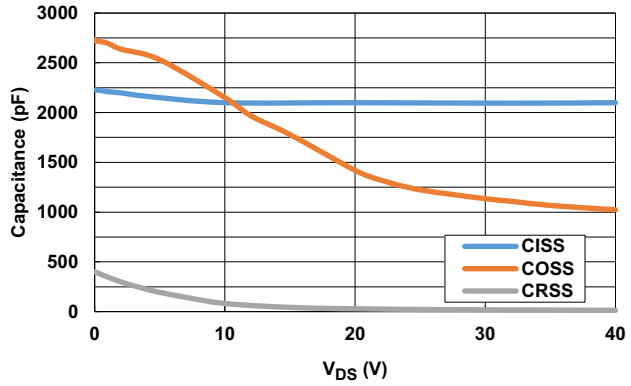


Figure 11. Capacitance (Linear Scale)

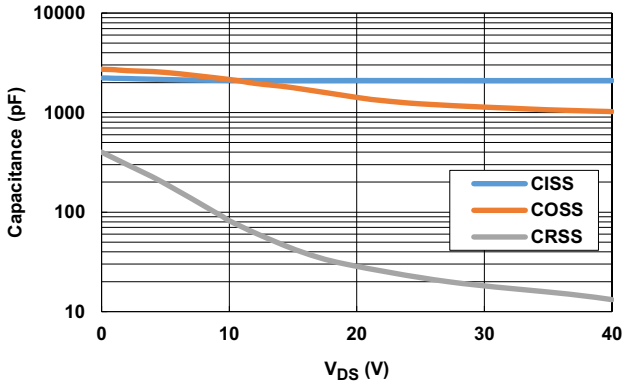


Figure 12. Capacitance (Log Scale)

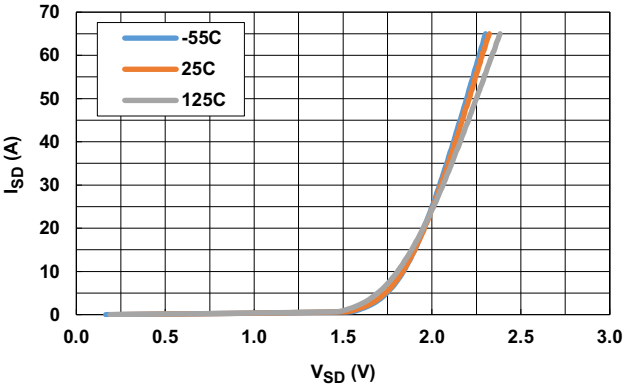


Figure 13. Reverse Drain-Source Characteristics

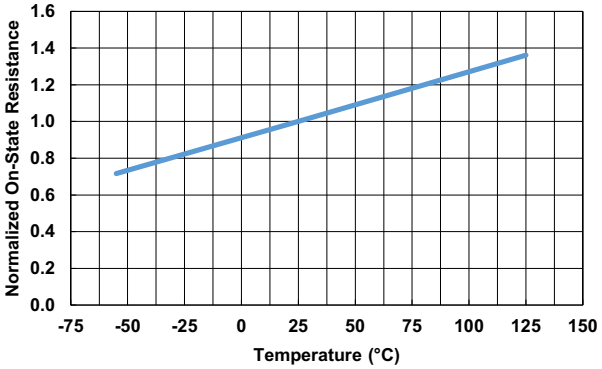


Figure 14. Normalized On-State Resistance

Unless otherwise noted, V_{DS} = 32V; T_A = +25°C. **(Continued)**

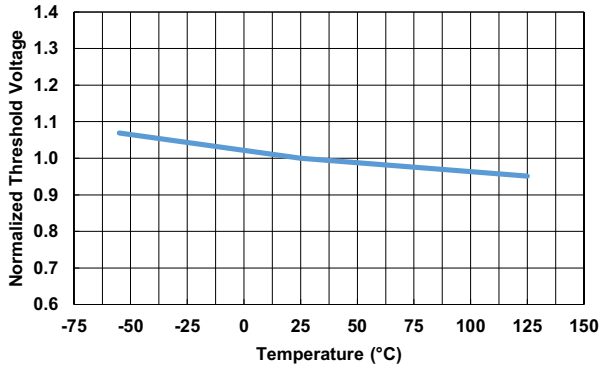


Figure 15. Normalized Threshold Voltage

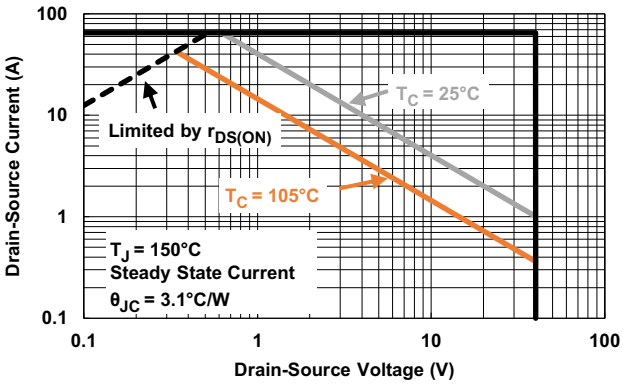


Figure 16. Safe Operating Area

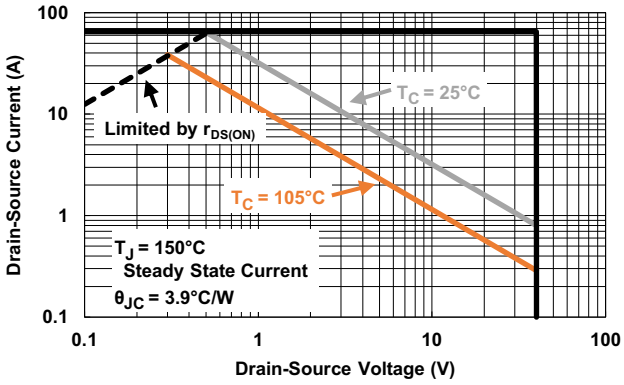


Figure 17. Safe Operating Area (Derated)

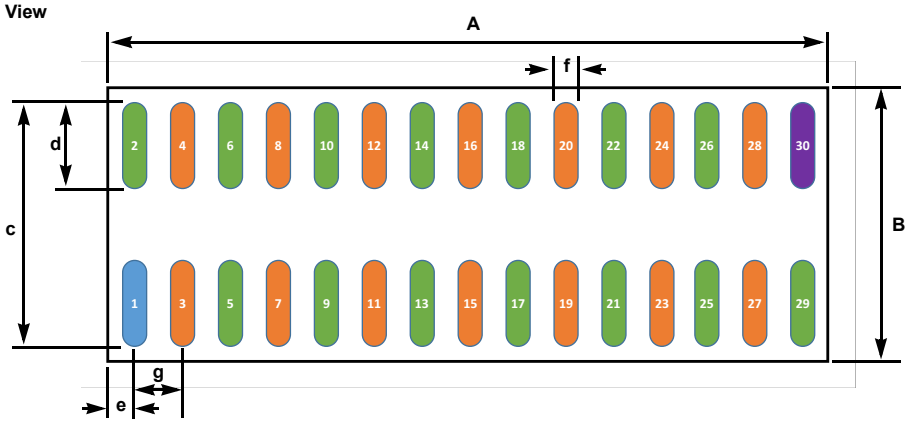
4. Die and Assembly Characteristics

Table 2. Die and Assembly Related Information

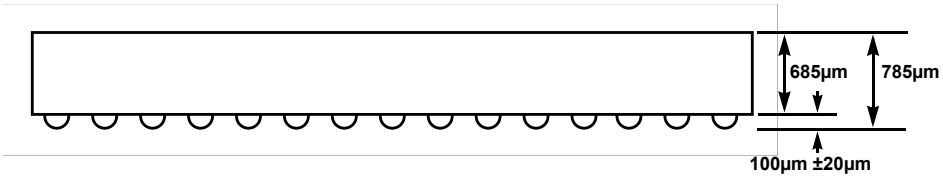
Die Information	
Dimensions	6050µm x 2300µm (238.19 mils x 90.55 mils) Thickness: 685µm (26.97 mils)

ISL70020SEH, ISL73020SEH

Solder Bump View



Side View



Color Key:

Pads in Green are the Source

Pads in Orange are the Drain

Pad in Blue is the Gate

Pad in Purple is the Substrate

Table 3. Dimensions

Dimension	Min (µm)	Nominal (µm)	Max (µm)
A	6020	6050	6080
B	2270	2300	2330
c	2047	2050	2053
d	717	720	723
e	210	225	240
f	195	200	205
g	400	400	400

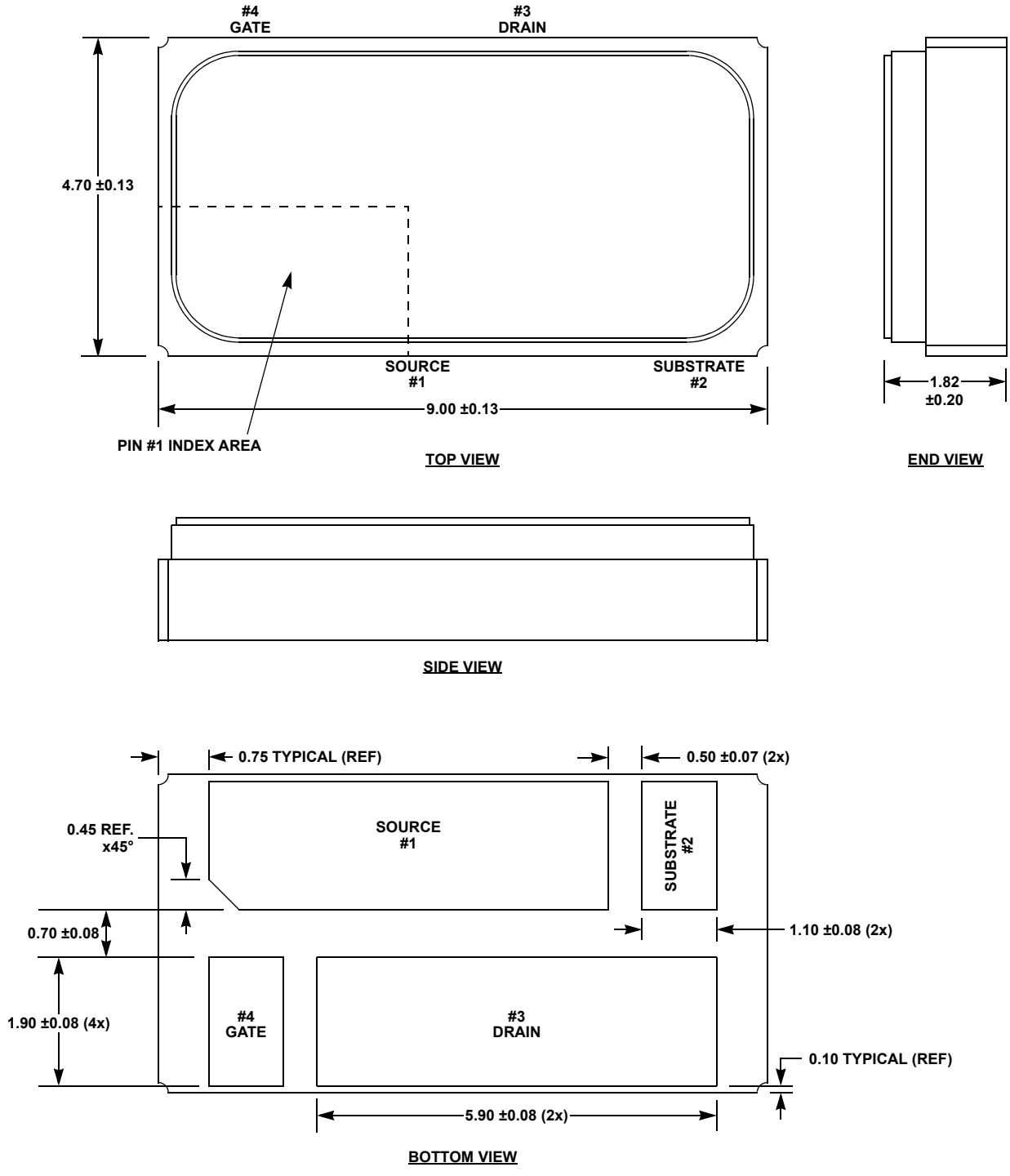
5. Revision History

Rev.	Date	Description
1.06	Mar 28, 2024	Clarified that LETs were calculated using a silicon target substrate.
1.05	May 30, 2023	Added screening Features bullet and subbullet. Updated Gate-to-Source Forward Leakage specifications typical from 0.1mA to 1mA and max from 0.5mA to 9mA. Updated Gate-to-Source Reverse Leakage specifications typical from -0.1mA to -0.1mA, removed max value, and added min value.
1.04	Apr 21, 2022	Updated Abs Max and Recommended Operating Conditions sections by removing the minimum column. Moved ESD Ratings to its own section. Removed Related Literature section.
1.03	Jan 28, 2021	Added Note 4.
1.02	Oct 26, 2020	Ordering Information table, changed: ISL73020SEHMX/SAMPLE to: ISL73020SEHX/SAMPLE ISL70020SEHMX/SAMPLE to: ISL70020SEHX/SAMPLE Added Note 2.
1.01	Nov 7, 2019	Added $r_{DS(ON)}$ specification for die only.
1.00	Oct 28, 2019	Initial release

6. Package Outline Drawing

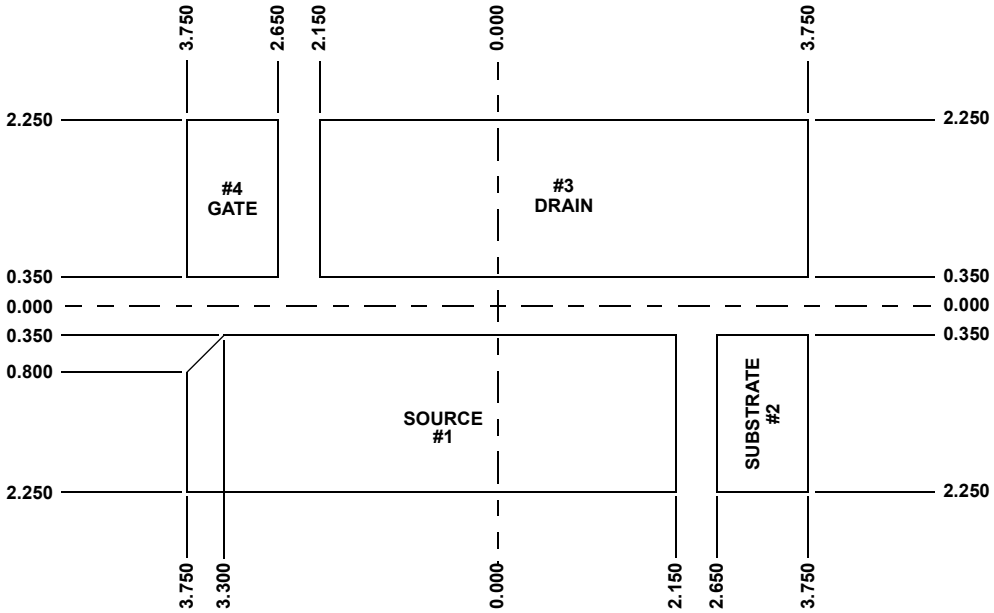
For the most recent package outline drawing, see J4.A.

J4.A
4 PIN 9.0mmx4.7mm HERMETIC SURFACE MOUNT PACKAGE
Rev 0, 2/16



Notes:

1. The corner shape (radius, chamfer, etc.) may vary at the manufacturers option from that shown on the drawing.
2. The package thickness dimension is the package height before being solder dipped.
3. Dimensions are in millimeters.



TYPICAL RECOMMENDED LAND PATTERN

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