

ISL6612A, ISL6613A

Advanced Synchronous Rectified Buck MOSFET Drivers with Pre-POR OVP

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The [ISL6612A](#) and [ISL6613A](#) are high frequency MOSFET drivers specifically designed to drive upper and lower power N-Channel MOSFETs in a synchronous rectified buck converter topology. These drivers combined with HIP63xx or ISL65xx Multi-Phase Buck PWM controllers and N-Channel MOSFETs form complete core-voltage regulator solutions for advanced microprocessors.

The ISL6612A drives the upper gate to 12V, while the lower gate can be independently driven over a range from 5V to 12V. The ISL6613A drives both upper and lower gates over a range of 5V to 12V. This drive-voltage provides the flexibility necessary to optimize applications involving trade-offs between gate charge and conduction losses.

An advanced adaptive zero shoot-through protection is integrated to prevent both the upper and lower MOSFETs from conducting simultaneously and to minimize the dead time. These products add an overvoltage protection feature operational before VCC exceeds its turn-on threshold, at which the PHASE node is connected to the gate of the low side MOSFET (LGATE). The output voltage of the converter is then limited by the threshold of the low side MOSFET, which provides some protection to the microprocessor if the upper MOSFET(s) is shorted during initial startup.

These drivers also feature a three-state PWM input which, working together with multi-phase PWM controllers, prevents a negative transient on the output voltage when the output is shut down. This feature eliminates the Schottky diode that is used in some systems for protecting the load from reversed output voltage events.

Features

- Pin-to-pin Compatible with HIP6601 SOIC family
- Dual MOSFET Drives for Synchronous Rectified Bridge
- Advanced Adaptive Zero Shoot-Through Protection
 - Body Diode Detection
 - Auto-zero of $r_{DS(ON)}$ Conduction Offset Effect
- Adjustable Gate Voltage (5V to 12V) for Optimal Efficiency
- 36V Internal Bootstrap Schottky Diode
- Bootstrap Capacitor Overcharging Prevention
- Supports High Switching Frequency (up to 2MHz)
 - 3A Sinking Current Capability
 - Fast Rise/Fall Times and Low Propagation Delays
- Three-State PWM Input for Output Stage Shutdown
- Three-State PWM Input Hysteresis for Applications with Power Sequencing Requirement
- Pre-POR Overvoltage Protection
- VCC Undervoltage Protection
- Expandable Bottom Copper Pad for Enhanced Heat Sinking
- Dual Flat No-Lead (DFN) Package
 - Near Chip-Scale Package Footprint; Improves PCB Efficiency and Thinner in Profile
- Pb-Free (RoHS Compliant)

Applications

- Core Regulators for Intel® and AMD® Microprocessors
- High Current DC/DC Converters
- High Frequency and High Efficiency VRM and VRD

Related Literature

For a full list of related documents, visit our website

- [ISL6612A](#), [ISL6613A](#) device pages

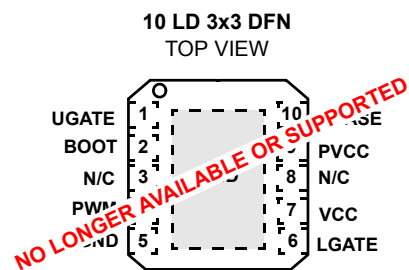
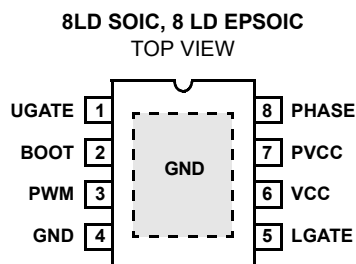
Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	TEMP. RANGE (°C)	TAPE AND REEL (UNITS) (Note 1)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL6612ACBZ	6612 ACBZ	0 to +85	-	8 Ld SOIC	M8.15
ISL6612ACBZ-T	6612 ACBZ	0 to +85	2.5k	8 Ld SOIC	M8.15
ISL6612ACBZA-T	6612 ACBZ	0 to +85	2.5k	8 Ld SOIC	M8.15
ISL6612ACRZ (No longer available, recommended replacement: ISL6612ACBZ-T)	12AZ	0 to +85	-	10 Ld 3x3 DFN	L10.3x3
ISL6612ACRZ-T (No longer available, recommended replacement: ISL6612ACBZ-T)	12AZ	0 to +85	6k	10 Ld 3x3 DFN	L10.3x3
ISL6612AECBZ(No longer available, recommended replacement: ISL6612ACBZ-T)	6612 AECBZ	0 to +85	-	8 Ld EPSONIC	M8.15B
ISL6612AECBZ-T (No longer available, recommended replacement: ISL6612ACBZ-T)	6612 AECBZ	0 to +85	2.5k	8 Ld EPSONIC	M8.15B
ISL6612AIBZ	6612 AIBZ	-40 to +85	-	8 Ld SOIC	M8.15
ISL6612AIBZ-T	6612 AIBZ	-40 to +85	2.5k	8 Ld SOIC	M8.15
ISL6613ACRZ (No longer available, recommended replacement: ISL6613BCRZ-T)	13AZ	0 to +85	-	10 Ld 3x3 DFN	L10.3x3
ISL6613ACRZ-T (No longer available, recommended replacement: ISL6613BCRZ-T)	13AZ	0 to +85	6k	10 Ld 3x3 DFN	L10.3x3
ISL6613AEIBZ	6613 AEIBZ	-40 to +85	-	8 Ld EPSONIC	M8.15B
ISL6613AEIBZ-T	6613 AEIBZ	-40 to +85	2.5k	8 Ld EPSONIC	M8.15B

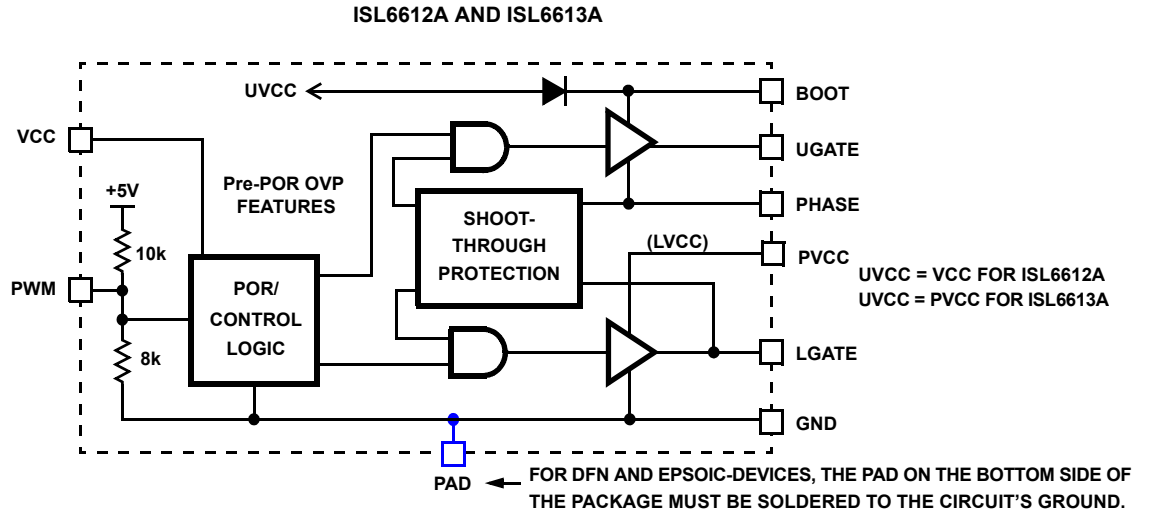
NOTES:

- See [TB347](#) for details about reel specifications.
- These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
- For Moisture Sensitivity Level (MSL), see the [ISL6612A](#), [ISL6613A](#) device pages. For more information about MSL, see [TB363](#).

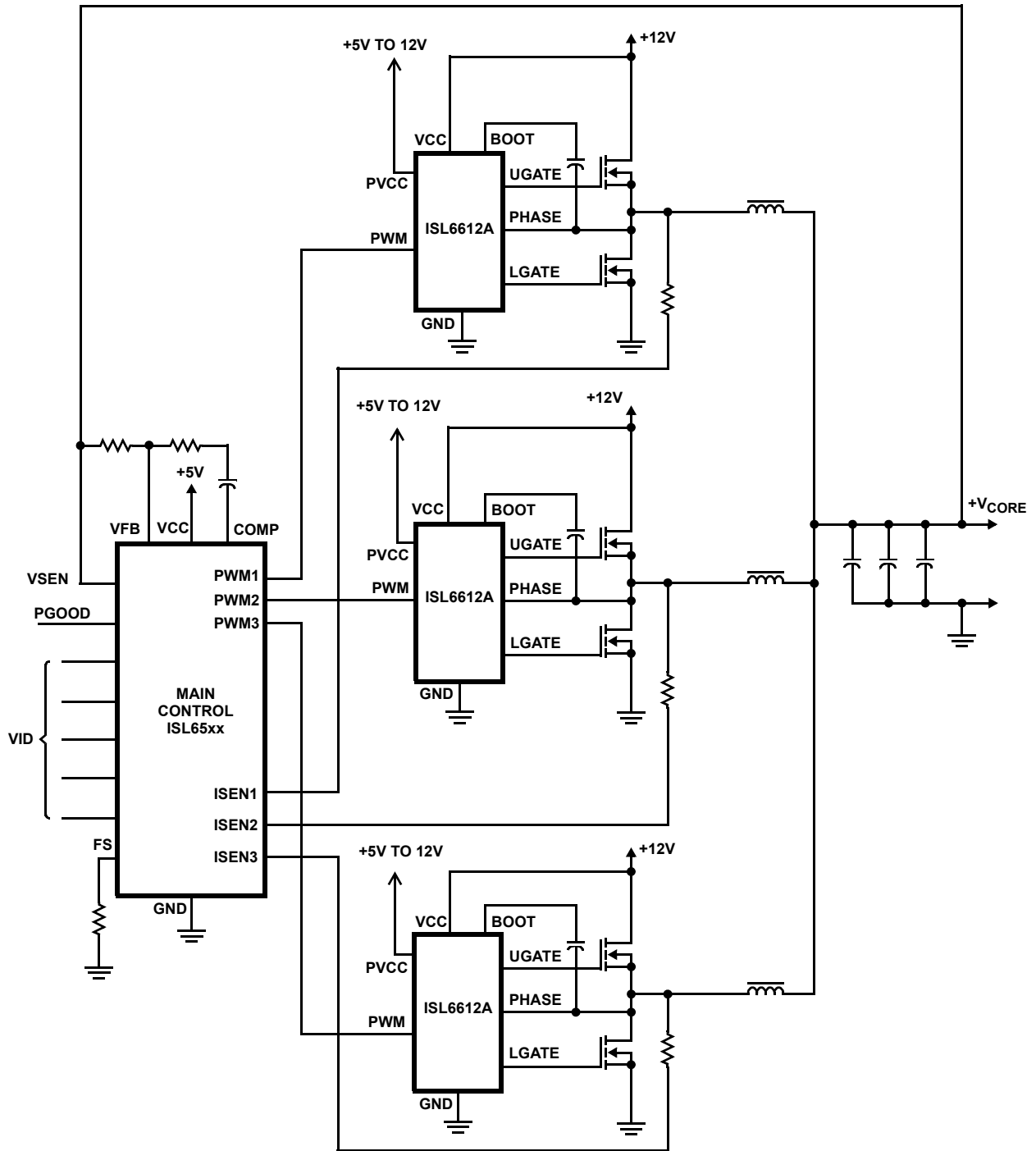
Pinouts



Block Diagram



Typical Application - 3 Channel Converter Using ISL65xx and ISL6612A Gate Drivers



Absolute Maximum Ratings

Supply Voltage (VCC)	15V
Supply Voltage (PVCC)	VCC + 0.3V
BOOT Voltage (V _{BOOT-GND})	36V
Input Voltage (V _{PWM})	GND - 0.3V to 7V
UGATE	V _{PHASE} - 0.3V _{DC} to V _{BOOT} + 0.3V
	V _{PHASE} - 3.5V (<100ns Pulse Width, 2μJ) to V _{BOOT} + 0.3V
LGATE	GND - 0.3V _{DC} to V _{PVCC} + 0.3V
	GND - 5V (<100ns Pulse Width, 2μJ) to V _{PVCC} + 0.3V
PHASE	GND - 0.3V _{DC} to 24V _{DC}
	GND - 8V (<400ns, 20μJ) to 31V (<200ns, V _{BOOT-GND} <36V)
ESD Rating	
Human Body Model	Class I JEDEC STD

Thermal Information

Thermal Resistance	θ _{JA} (°C/W)	θ _{JC} (°C/W)
SOIC Package (Note 4)	100	N/A
EPSON Package (Notes 5, 6)	50	7
DFN Package (Notes 5, 6)	48	7
Maximum Junction Temperature (Plastic Package)	+150°C	
Maximum Storage Temperature Range	-65°C to +150°C	
Maximum Lead Temperature (Soldering 10s)	+300°C (SOIC - Lead Tips Only)	
Pb-Free Reflow Profile	see TB493	

Recommended Operating Conditions

Ambient Temperature Range	-40°C to +85°C
Maximum Operating Junction Temperature	+125°C
Supply Voltage, VCC	12V ±10%
Supply Voltage Range, PVCC	5V to 12V ±10%

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

- θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air.
- θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. See [TB379](#).
- For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
VCC SUPPLY CURRENT						
Bias Supply Current	I _{VCC}	ISL6612A, f _{PWM} = 300kHz, V _{VCC} = 12V	-	7.2	-	mA
		ISL6613A, f _{PWM} = 300kHz, V _{VCC} = 12V	-	4.5	-	mA
	I _{VCC}	ISL6612A, f _{PWM} = 1MHz, V _{VCC} = 12V	-	11	-	mA
		ISL6613A, f _{PWM} = 1MHz, V _{VCC} = 12V	-	5	-	mA
Gate Drive Bias Current	I _{PVCC}	ISL6612A, f _{PWM} = 300kHz, V _{PVCC} = 12V	-	2.5	-	mA
		ISL6613A, f _{PWM} = 300kHz, V _{PVCC} = 12V	-	5.2	-	mA
	I _{PVCC}	ISL6612A, f _{PWM} = 1MHz, V _{PVCC} = 12V	-	7	-	mA
		ISL6613A, f _{PWM} = 1MHz, V _{PVCC} = 12V	-	13	-	mA
POWER-ON RESET AND ENABLE						
VCC Rising Threshold		T _A = 0°C to +85°C	9.35	9.80	10.00	V
VCC Rising Threshold		T _A = -40°C to +85°C	8.35	9.80	10.00	V
VCC Falling Threshold		T _A = 0°C to +85°C	7.35	7.60	8.00	V
VCC Falling Threshold		T _A = -40°C to +85°C	6.35	7.60	8.00	V
PWM INPUT (See “TIMING DIAGRAM” on page 7)						
Input Current	I _{PWM}	V _{PWM} = 5V	-	450	-	μA
		V _{PWM} = 0V	-	-400	-	μA
PWM Rising Threshold		VCC = 12V	-	3.00	-	V
PWM Falling Threshold		VCC = 12V	-	2.00	-	V
Typical Three-State Shutdown Window		VCC = 12V	1.80	-	2.40	V
Three-State Lower Gate Falling Threshold		VCC = 12V	-	1.50	-	V
Three-State Lower Gate Rising Threshold		VCC = 12V	-	1.00	-	V
Three-State Upper Gate Rising Threshold		VCC = 12V	-	3.20	-	V

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted. (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
Three-State Upper Gate Falling Threshold		VCC = 12V	-	2.60	-	V
Shutdown Holdoff Time	t _{TSSHD}		-	245	-	ns
UGATE Rise Time	t _{RU}	V _{PVCC} = 12V, 3nF Load, 10% to 90%	-	26	-	ns
LGATE Rise Time	t _{RL}	V _{PVCC} = 12V, 3nF Load, 10% to 90%	-	18	-	ns
UGATE Fall Time	t _{FU}	V _{PVCC} = 12V, 3nF Load, 90% to 10%	-	18	-	ns
LGATE Fall Time	t _{FL}	V _{PVCC} = 12V, 3nF Load, 90% to 10%	-	12	-	ns
UGATE Turn-On Propagation Delay (Note 7)	t _{PDHU}	V _{PVCC} = 12V, 3nF Load, Adaptive	-	10	-	ns
LGATE Turn-On Propagation Delay (Note 7)	t _{PDHL}	V _{PVCC} = 12V, 3nF Load, Adaptive	-	10	-	ns
UGATE Turn-Off Propagation Delay (Note 7)	t _{PDLU}	V _{PVCC} = 12V, 3nF Load	-	10	-	ns
LGATE Turn-Off Propagation Delay (Note 7)	t _{PDLL}	V _{PVCC} = 12V, 3nF Load	-	10	-	ns
LG/UG Three-State Propagation Delay (Note 7)	t _{PDTS}	V _{PVCC} = 12V, 3nF Load	-	10	-	ns
OUTPUT (Note 7)						
Upper Drive Source Current	I _{U_SOURCE}	V _{PVCC} = 12V, 3nF Load	-	1.25	-	A
Upper Drive Source Impedance	R _{U_SOURCE}	150mA Source Current	1.25	2.0	3.0	Ω
Upper Drive Sink Current	I _{U_SINK}	V _{PVCC} = 12V, 3nF Load	-	2	-	A
Upper Drive Transition Sink Impedance	R _{U_SINK_TR}	70ns With Respect To PWM Falling	-	1.3	2.2	Ω
Upper Drive DC Sink Impedance	R _{U_SINK_DC}	150mA Source Current	0.9	1.65	3.0	Ω
Lower Drive Source Current	I _{L_SOURCE}	V _{PVCC} = 12V, 3nF Load	-	2	-	A
Lower Drive Source Impedance	R _{L_SOURCE}	150mA Source Current	0.85	1.25	2.2	Ω
Lower Drive Sink Current	I _{L_SINK}	V _{PVCC} = 12V, 3nF Load	-	3	-	A
Lower Drive Sink Impedance	R _{L_SINK}	150mA Sink Current	0.60	0.80	1.35	Ω

NOTES:

- Limits should be considered typical and are not production tested.
- Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Functional Pin Description

PACKAGE PIN #	PIN		FUNCTION
	SOIC	DFN	
1	1	UGATE	Upper gate drive output. Connect to gate of high-side power N-Channel MOSFET.
2	2	BOOT	Floating bootstrap supply pin for the upper gate drive. Connect the bootstrap capacitor between this pin and the PHASE pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. See "Internal Bootstrap Device" on page 8 for guidance in choosing the capacitor value.
-	3, 8	N/C	No Connection.
3	4	PWM	The PWM signal is the control input for the driver. The PWM signal can enter three distinct states during operation, See "Three-State PWM Input" on page 7 for further details. Connect this pin to the PWM output of the controller.
4	5	GND	Bias and reference ground. All signals are referenced to this node. It is also the power ground return of the driver.
5	6	LGATE	Lower gate drive output. Connect to gate of the low-side power N-Channel MOSFET.
6	7	VCC	Connect this pin to a +12V bias supply. Place a high quality low ESR ceramic capacitor from this pin to GND.
7	9	PVCC	This pin supplies power to both upper and lower gate drives in ISL6613A; only the lower gate drive in ISL6612A. Its operating range is +5V to 12V. Place a high quality low ESR ceramic capacitor from this pin to GND.
8	10	PHASE	Connect this pin to the SOURCE of the upper MOSFET and the DRAIN of the lower MOSFET. This pin provides a return path for the upper gate drive.
9	11	PAD	Connect this pad to the power ground plane (GND) via thermally enhanced connection.

Description

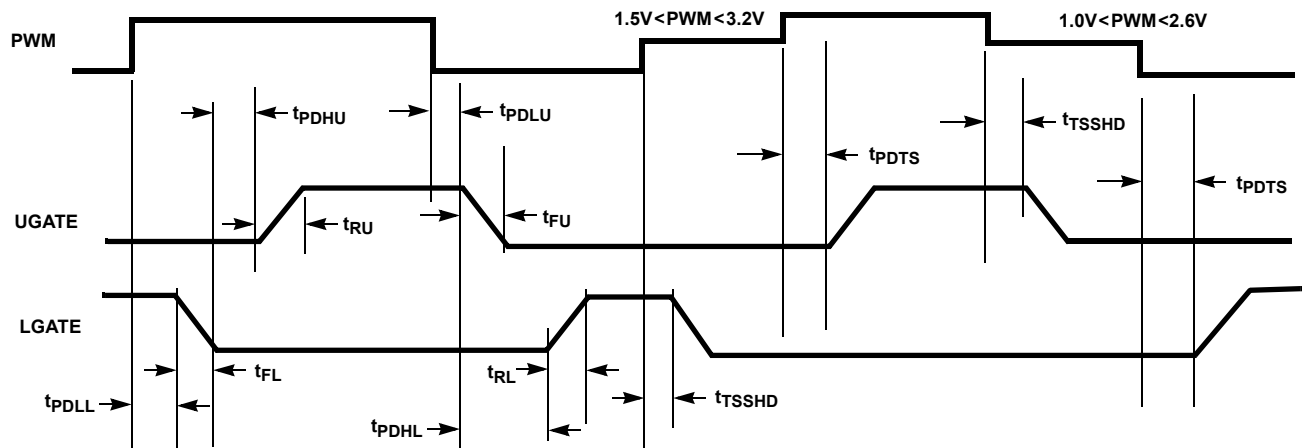


FIGURE 1. TIMING DIAGRAM

Operation

Designed for versatility and speed, the ISL6612A and ISL6613A MOSFET drivers control both high-side and low-side N-Channel FETs of a half-bridge power train from one externally provided PWM signal.

Prior to VCC exceeding its POR level, the Pre-POR overvoltage protection function is activated during initial startup; the upper gate (UGATE) is held low and the lower gate (LGATE), controlled by the Pre-POR overvoltage protection circuits, is connected to the PHASE. Once the VCC voltage surpasses the VCC Rising Threshold (See Electrical Specifications), the PWM signal takes control of gate transitions. A rising edge on PWM initiates the turn-off of the lower MOSFET (see Timing Diagram). After a short propagation delay [t_{PDLL}], the lower gate begins to fall. Typical fall times [t_{FL}] are provided in the Electrical Specifications section. Adaptive shoot-through circuitry monitors the PHASE voltage and determines the upper gate delay time [t_{PDHU}]. This prevents both the lower and upper MOSFETs from conducting simultaneously. Once this delay period is complete, the upper gate drive begins to rise [t_{RHU}] and the upper MOSFET turns on.

A falling transition on PWM results in the turn-off of the upper MOSFET and the turn-on of the lower MOSFET. A short propagation delay [t_{PDLU}] is encountered before the upper gate begins to fall [t_{FU}]. Again, the adaptive shoot-through circuitry determines the lower gate delay time, t_{PDHL} . The PHASE voltage and the UGATE voltage are monitored, and the lower gate is allowed to rise after PHASE drops below a level or the voltage of UGATE to PHASE reaches a level depending upon the current direction (See next section for details). The lower gate then rises [t_{RL}], turning on the lower MOSFET.

Advanced Adaptive Zero Shoot-Through Deadtime Control (Patent Pending)

These drivers incorporate a unique adaptive deadtime control technique to minimize deadtime, resulting in high efficiency from the reduced freewheeling time of the lower MOSFETs' body-diode conduction, and to prevent the upper and lower MOSFETs from conducting simultaneously. This is accomplished by ensuring either rising gate turns on its MOSFET with minimum and sufficient delay after the other has turned off.

During turn-off of the lower MOSFET, the PHASE voltage is monitored until it reaches a $-0.2V/+0.8V$ trip point for a forward/reverse current, at which time the UGATE is released to rise. An auto-zero comparator is used to correct the $r_{DS(ON)}$ drop in the phase voltage preventing from false detection of the $-0.2V$ phase level during $r_{DS(ON)}$ conduction period. In the case of zero current, the UGATE is released after 35ns delay of the LGATE dropping below 0.5V. During the phase detection, the disturbance of LGATE's falling transition on the PHASE node is blanked out to prevent falsely tripping. Once the PHASE is high, the advanced adaptive shoot-through circuitry monitors the PHASE and UGATE voltages during a PWM falling edge and the subsequent UGATE turn-off. If either the UGATE falls to less than 1.75V above the PHASE or the PHASE falls to less than +0.8V, the LGATE is released to turn on.

Three-State PWM Input

A unique feature of these drivers and the other Renesas drivers is the addition of a shutdown window to the PWM input. If the PWM signal enters and remains within the shutdown window for a set holdoff time, the driver outputs are disabled and both MOSFET gates are pulled and held low. The shutdown state is removed when the PWM signal moves outside the shutdown window. Otherwise, the PWM rising and falling thresholds (outlined in [Electrical](#)

[Specifications](#) on [page 5](#)) to determine when the lower and upper gates are enabled.

This feature helps prevent a negative transient on the output voltage when the output is shut down, eliminating the Schottky diode that is used in some systems for protecting the load from reversed output voltage events.

In addition, more than 400mV hysteresis also incorporates into the three-state shutdown window to eliminate PWM input oscillations due to the capacitive load seen by the PWM input through the body diode of the controller's PWM output when the power-up and/or power-down sequence of bias supplies of the driver and PWM controller are required.

Power-On Reset (POR) Function

During initial startup, the VCC voltage rise is monitored. Once the rising VCC voltage exceeds 9.8V (typically), operation of the driver is enabled and the PWM input signal takes control of the gate drives. If VCC drops below the falling threshold of 7.6V (typically), operation of the driver is disabled.

Pre-POR Overvoltage Protection

Prior to VCC exceeding its POR level, the upper gate is held low and the lower gate is controlled by the overvoltage protection circuits during initial startup. The PHASE is connected to the gate of the low side MOSFET (LGATE), which provides some protection to the microprocessor if the upper MOSFET(s) is shorted during initial startup. For complete protection, the low side MOSFET should have a gate threshold well below the maximum voltage rating of the load/microprocessor.

When VCC drops below its POR level, both gates pull low and the Pre-POR overvoltage protection circuits are not activated until VCC resets.

Internal Bootstrap Device

Both drivers feature an internal bootstrap schottky diode. Simply adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit. The bootstrap function is also designed to prevent the bootstrap capacitor from overcharging due to the large negative swing at the trailing-edge of the PHASE node. This reduces voltage stress on the boot to phase pins.

The bootstrap capacitor must have a maximum voltage rating above UVCC + 5V and its capacitance value can be chosen from the following equation:

$$C_{\text{BOOT_CAP}} \geq \frac{Q_{\text{GATE}}}{\Delta V_{\text{BOOT_CAP}}} \quad (\text{EQ. 1})$$

$$Q_{\text{GATE}} = \frac{Q_{\text{G1}} \cdot UVCC}{V_{\text{GS1}}} \cdot N_{\text{Q1}}$$

where Q_{G1} is the amount of gate charge per upper MOSFET at V_{GS1} gate-source voltage and N_{Q1} is the number of control

MOSFETs. The $\Delta V_{\text{BOOT_CAP}}$ term is defined as the allowable droop in the rail of the upper gate drive.

As an example, suppose two IRLR7821 FETs are chosen as the upper MOSFETs. The gate charge, Q_{G} , from the data sheet is 10nC at 4.5V (V_{GS}) gate-source voltage. Then the Q_{GATE} is calculated to be 53nC for UVCC (i.e. PVCC in ISL6613A, VCC in ISL6612A) = 12V. We will assume a 200mV droop in drive voltage over the PWM cycle. We find that a bootstrap capacitance of at least 0.267 μF is required.

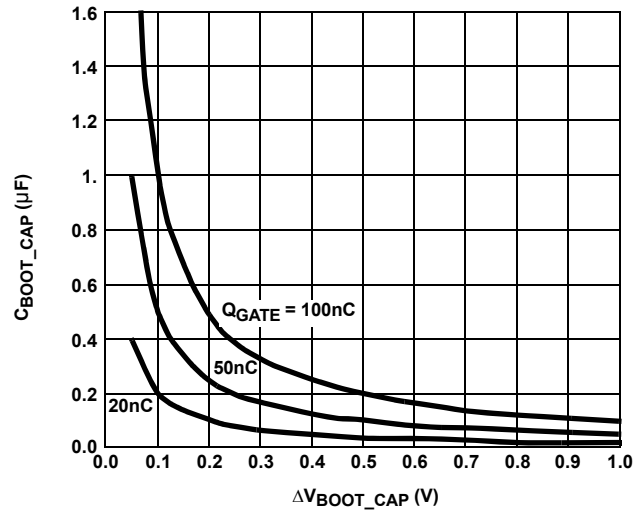


FIGURE 2. BOOTSTRAP CAPACITANCE vs BOOT RIPPLE VOLTAGE

Gate Drive Voltage Versatility

The ISL6612A and ISL6613A provide the user flexibility in choosing the gate drive voltage for efficiency optimization. The ISL6612A upper gate drive is fixed to VCC [+12V], but the lower drive rail can range from 12V down to 5V depending on what voltage is applied to PVCC. The ISL6613A ties the upper and lower drive rails together. Simply applying a voltage from 5V up to 12V on PVCC sets both gate drive rail voltages simultaneously.

Power Dissipation

Package power dissipation is mainly a function of the switching frequency (F_{SW}), the output drive impedance, the external gate resistance, and the selected MOSFET's internal gate resistance and total gate charge. Calculating the power dissipation in the driver for a desired application is critical to ensure safe operation. Exceeding the maximum allowable power dissipation level will push the IC beyond the maximum recommended operating junction temperature of +125°C. The maximum allowable IC power dissipation for the SO8 package is approximately 800mW at room temperature, while the power dissipation capacity in the EPSON and DFN packages, with an exposed heat escape pad, is more than 2W and 1.5W, respectively. Both EPSON and DFN packages are more suitable for high frequency applications. See Layout Considerations paragraph for thermal transfer improvement

suggestions. When designing the driver into an application, it is recommended that the following calculation is used to ensure safe operation at the desired frequency for thresholds outlined in the Electrical Specifications determine when the lower and upper gates are enabled.

the selected MOSFETs. The total gate drive power losses due to the gate charge of MOSFETs and the driver's internal circuitry and their corresponding average driver current can be estimated with [Equations 2](#) and [3](#), respectively,

$$P_{Qg_TOT} = P_{Qg_Q1} + P_{Qg_Q2} + I_Q \cdot VCC \quad (EQ. 2)$$

$$P_{Qg_Q1} = \frac{Q_{G1} \cdot UVCC^2}{V_{GS1}} \cdot F_{SW} \cdot N_{Q1}$$

$$P_{Qg_Q2} = \frac{Q_{G2} \cdot LVCC^2}{V_{GS2}} \cdot F_{SW} \cdot N_{Q2}$$

$$I_{DR} = \left(\frac{Q_{G1} \cdot UVCC \cdot N_{Q1}}{V_{GS1}} + \frac{Q_{G2} \cdot LVCC \cdot N_{Q2}}{V_{GS2}} \right) \cdot F_{SW} + I_Q \quad (EQ. 3)$$

where the gate charge (Q_{G1} and Q_{G2}) is defined at a particular gate to source voltage (V_{GS1} and V_{GS2}) in the corresponding MOSFET datasheet; I_Q is the driver's total quiescent current with no load at both drive outputs; N_{Q1} and N_{Q2} are number of upper and lower MOSFETs, respectively; $UVCC$ and $LVCC$ are the drive voltages for both upper and lower FETs, respectively. The $I_Q \cdot VCC$ product is the quiescent power of the driver without capacitive load and is typically 116mW at 300kHz.

The total gate drive power losses are dissipated among the resistive components along the transition path. The drive resistance dissipates a portion of the total gate drive power losses, the rest will be dissipated by the external gate resistors (R_{G1} and R_{G2}) and the internal gate resistors (R_{G11} and R_{G12}) of MOSFETs. [Figures 3](#) and [4](#) show the typical upper and lower gate drives turn-on transition path. The power dissipation on the driver can be roughly estimated as:

$$P_{DR} = P_{DR_UP} + P_{DR_LOW} + I_Q \cdot VCC \quad (EQ. 4)$$

$$P_{DR_UP} = \left(\frac{R_{HI1}}{R_{HI1} + R_{EXT1}} + \frac{R_{LO1}}{R_{LO1} + R_{EXT1}} \right) \cdot \frac{P_{Qg_Q1}}{2}$$

$$P_{DR_LOW} = \left(\frac{R_{HI2}}{R_{HI2} + R_{EXT2}} + \frac{R_{LO2}}{R_{LO2} + R_{EXT2}} \right) \cdot \frac{P_{Qg_Q2}}{2}$$

$$R_{EXT1} = R_{G1} + \frac{R_{G11}}{N_{Q1}} \quad R_{EXT2} = R_{G2} + \frac{R_{G12}}{N_{Q2}}$$

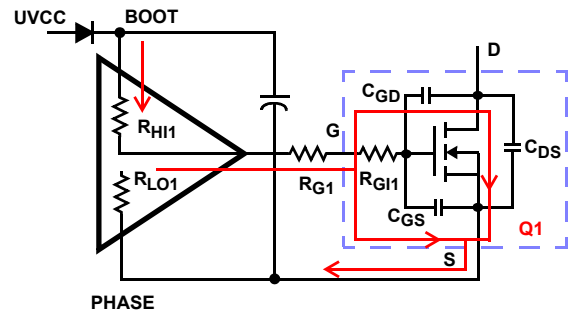


FIGURE 3. TYPICAL UPPER-GATE DRIVE TURN-ON PATH

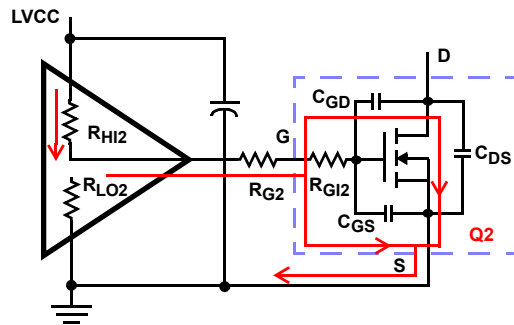


FIGURE 4. TYPICAL LOWER-GATE DRIVE TURN-ON PATH

Layout Considerations

For heat spreading, place copper underneath the IC whether it has an exposed pad or not. The copper area can be extended beyond the bottom area of the IC and/or connected to buried copper plane(s) with thermal vias. This combination of vias for vertical heat escape, extended copper plane, and buried planes for heat spreading allows the IC to achieve its full thermal potential.

Place each channel power component as close to each other as possible to reduce PCB copper losses and PCB parasitics: shortest distance between DRAINS of upper FETs and SOURCEs of lower FETs; shortest distance between DRAINS of lower FETs and the power ground. Thus, smaller amplitudes of positive and negative ringing are on the switching edges of the PHASE node. However, some space in between the power components is required for good airflow. The traces from the drivers to the FETs should be kept short and wide to reduce the inductance of the traces and to promote clean drive signals.

Revision History

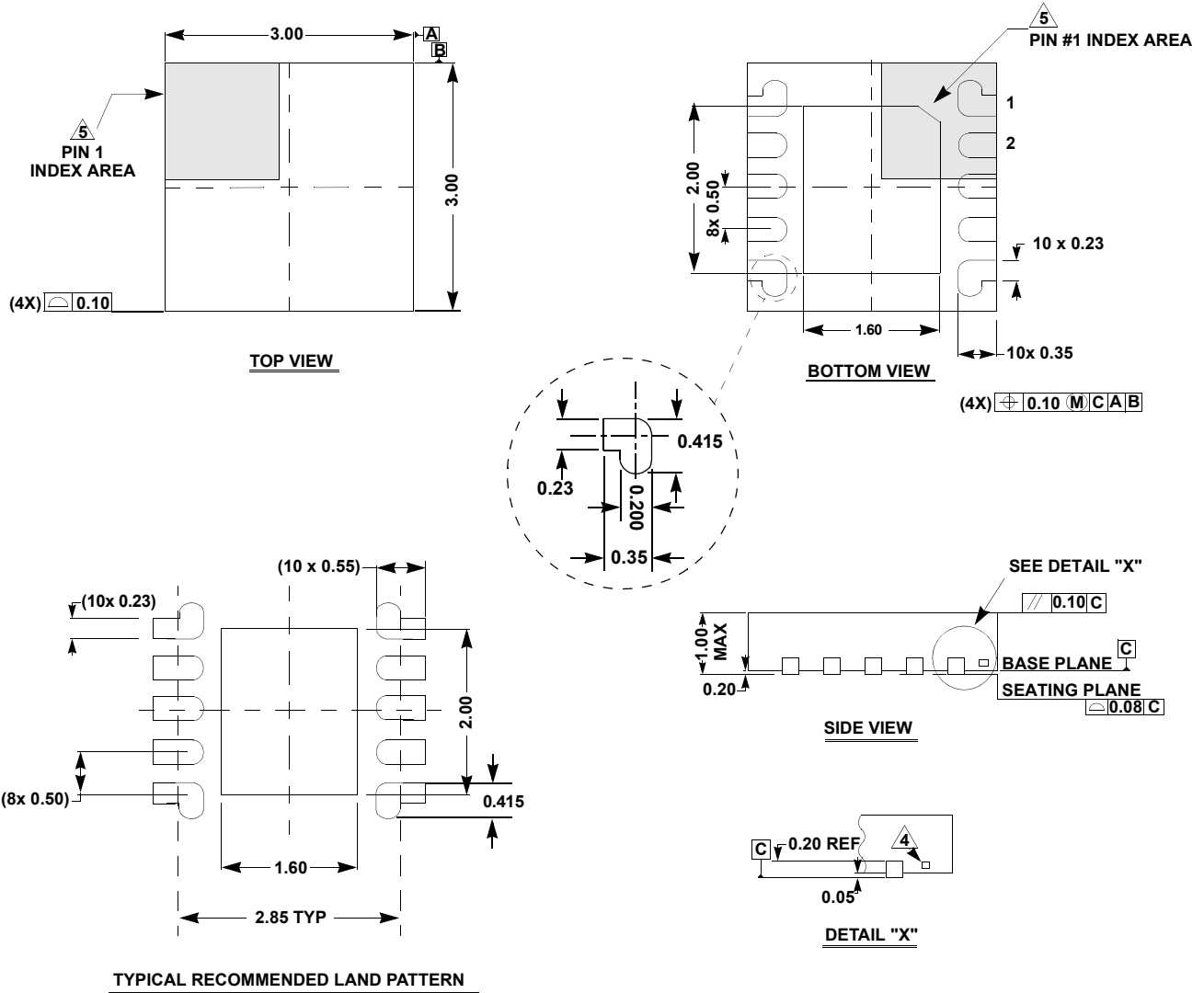
The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Aug 8, 2019	FN9159.8	<p>Updated Related Literature</p> <p>Updated Ordering information table removing retired parts, updating notes, and adding tape and reel column.</p> <p>Updated links throughout document.</p> <p>Added Revision History</p> <p>Updated POD L10.3x3 to the latest revision changes are as follows:</p> <ul style="list-style-type: none"> -Removed package outline and included center to center distance between lands on recommended land pattern. -Removed Note 4 "Dimension b applies to the metallized terminal and is measured between 0.18mm and 0.30mm from the terminal tip." since it is not applicable to this package. Renumbered notes accordingly. -Corrected L-shaped leads in Bottom view and land pattern so that they align with the rest of the leads (L shaped leads were shorter) -Added missing dimension 0.415 in Typical Recommended land pattern. -Shortened the e-pad rectangle on both the recommended land pattern and the package bottom view to line up with the centers of the corner pins. -Tiebar Note 4 updated: From: Tiebar shown (if present) is a non-functional feature. To: Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends). <p>Updated POD M8.15B to the latest revision changes are as follows:</p> <ul style="list-style-type: none"> -Replace the graphics with standard format (removing the dimension table). -Updated L Millimeter minimum in detail A from 0.41 to 0.406. <p>Updated the following in the Side View:</p> <ul style="list-style-type: none"> -Changed total package height Millimeter MIN and MAX values from: 1.43 MIN and 1.68 MAX to: 1.422 MIN and 1.700 MAX and Inches max from 0.066 to 0.067. -Changed A1 Inches MIN from: 0.001 to 0.0, and A1 Millimeters MIN from 0.03 to 0.0 <p>Updated POD M8.15 to the latest revision changes are as follows:</p> <ul style="list-style-type: none"> -Updated to new POD format by removing table and moving dimensions onto drawing and adding land pattern - Changed in Typical Recommended Land Pattern the following: 2.41(0.095) to 2.20(0.087) 0.76 (0.030) to 0.60(0.023) 0.200 to 5.20(0.205) -Changed Note 1 "1982" to "1994" <p>Updated disclaimer</p>

Package Outline Drawings

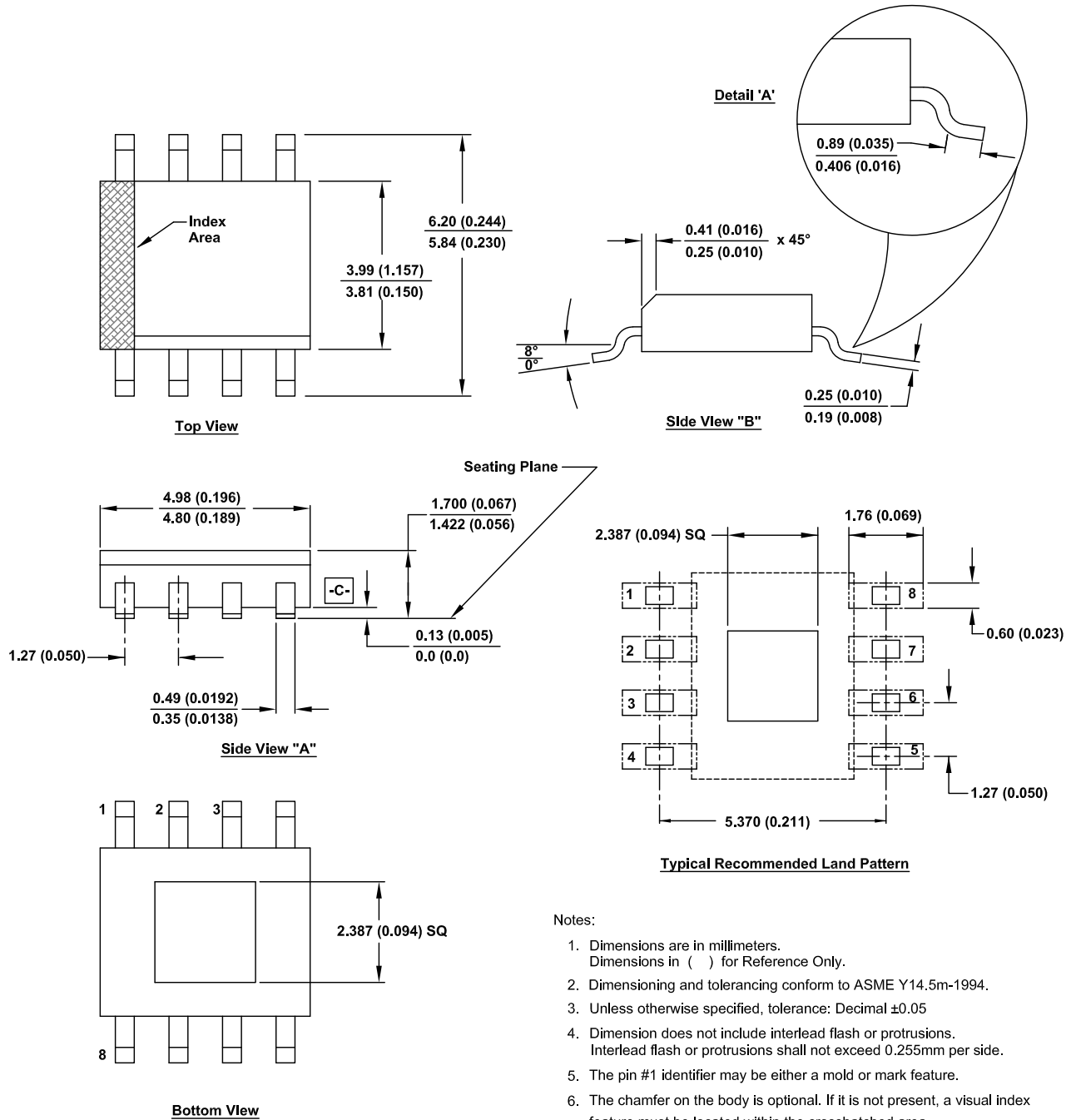
For the most recent package outline drawing, see [L10.3x3](#).

L10.3x3
 10 Lead Dual Flat Package (DFN)
 Rev 11, 3/15



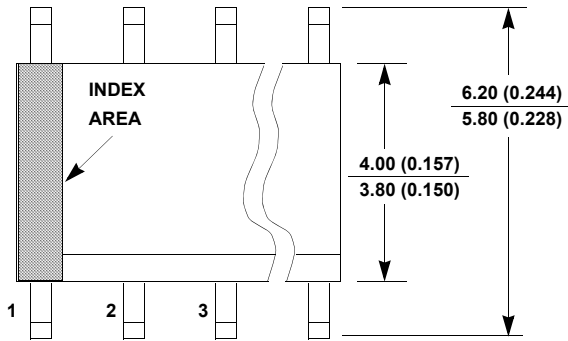
NOTES:

1. Dimensions are in millimeters.
 Dimensions in () for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
5. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

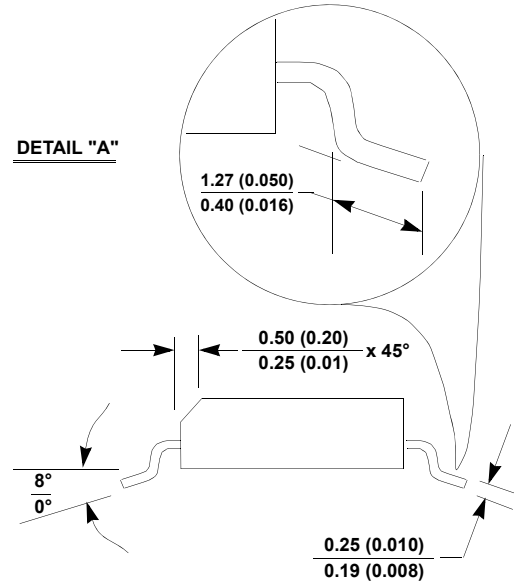


M8.15
 8 Lead Narrow Body Small Outline Plastic Package (SOIC)
 Rev 4, 1/12

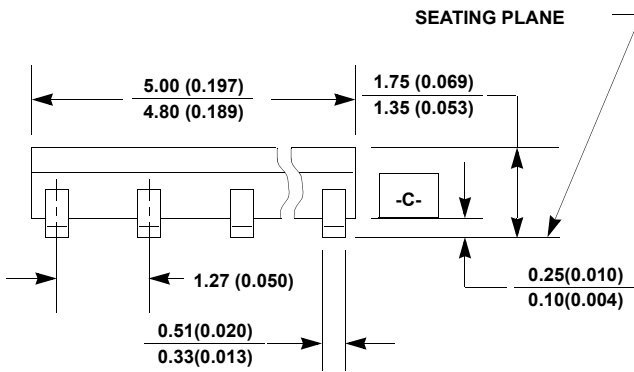
For the most recent package outline drawing, see [M8.15](#).



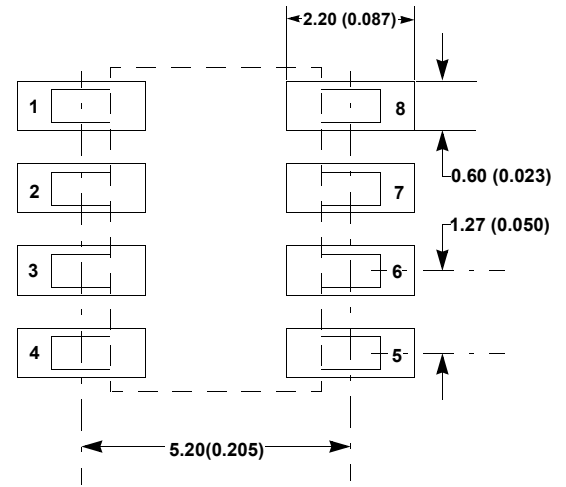
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

9. Dimensioning and tolerancing per ANSI Y14.5M-1994.
10. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
11. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
12. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
13. Terminal numbers are shown for reference only.
14. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
15. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
16. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

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