# 5-Bit VID Single-Phase Voltage Regulator with Current Monitor for GPU Core Power

The ISL6263C IC is a Single-Phase Synchronous-Buck PWM voltage regulator for GPU core power application. It features Intersil's Robust Ripple Regulator ($R^3$) Technology™. Integrated current monitor, differential remote sense amplifier, MOSFET driver and bootstrap diode result in smaller implementation area and lower component cost.

Intersil's $R^3$ Technology™ combines the best features of both fixed-frequency PWM and hysteretic PWM, delivering excellent light-load efficiency and superior load transient response by commanding variable switching frequency during the transitory event. For maximum conversion efficiency, the ISL6263C automatically enters diode emulation mode (DEM) when the inductor current attempts to flow negative. DEM is highly configurable and easy to set-up. A PWM filter can be enabled, which prevents the switching frequency from entering the audible spectrum as a result of extremely light load while in DEM.

The GPU core voltage can be dynamically programmed from 0.41200V to 1.28750V by the five VID input pins without requiring sequential stepping of the VID states. The ISL6263C requires only one capacitor for both the soft-start slew-rate and the dynamic VID slew-rate by internally connecting the SOFT pin to the appropriate current source. The voltage Kelvin sensing is accomplished with an integrated unity-gain true differential amplifier.

## Ordering Information

| PART NUMBER (Notes 2, 3) | PART MARKING | TEMP RANGE (°C) | PACKAGE (Pb-Free) | PKG. DWG. # |
|---|---|---|---|---|
| ISL6263CHRZ | ISL6263 CHRZ | -10 to +100 | 32 Ld 5x5 QFN | L32.5x5 |
| ISL6263CHRZ-T (Note 1) | ISL6263 CHRZ | -10 to +100 | 32 Ld 5x5 QFN | L32.5x5 |

NOTES:

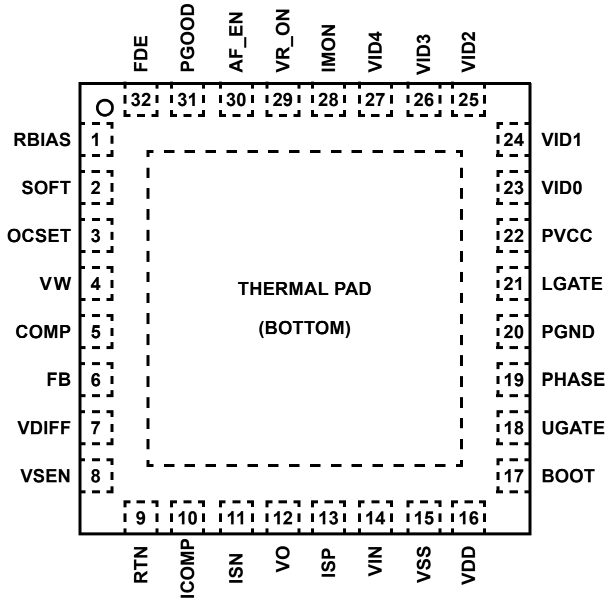
1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL6263C. For more information on MSL please see techbrief TB363.

## Features

- Precise Single-Phase Core Voltage Regulator
  - 0.5% System Accuracy 0°C to +100°C
  - Differential Remote GPU Die Voltage Sense
- Real-Time GPU Current Monitor Output
- Applications up to 25A
- Input Voltage Range: +5.0V to +25.0V
- Programmable PWM Frequency: 200kHz to 500kHz
- Pre-Biased Output Start-Up Capability
- 5-Bit Voltage Identification Input (VID)
  - 0.41200V to 1.28750V
  - 25.75mV Steps
  - Sequential or Non-Sequential VID Change On-the-Fly
- Configurable PWM Modes
  - Forced Continuous Conduction Mode
  - Automatic Entry and Exit of Diode Emulation Mode
  - Selectable Audible Frequency PWM Filter
- Integrated MOSFET Drivers and Bootstrap Diode
- Choice of Current Sense Schemes
  - Lossless Inductor DCR Current Sense
  - Precise Resistive Current Sense
- Overvoltage, Undervoltage and Overcurrent Protection
- Pb-Free (RoHS Compliant)

## Pinout

**ISL6263C**
**(32 LD 5x5 QFN)**
TOP VIEW



## Block Diagram

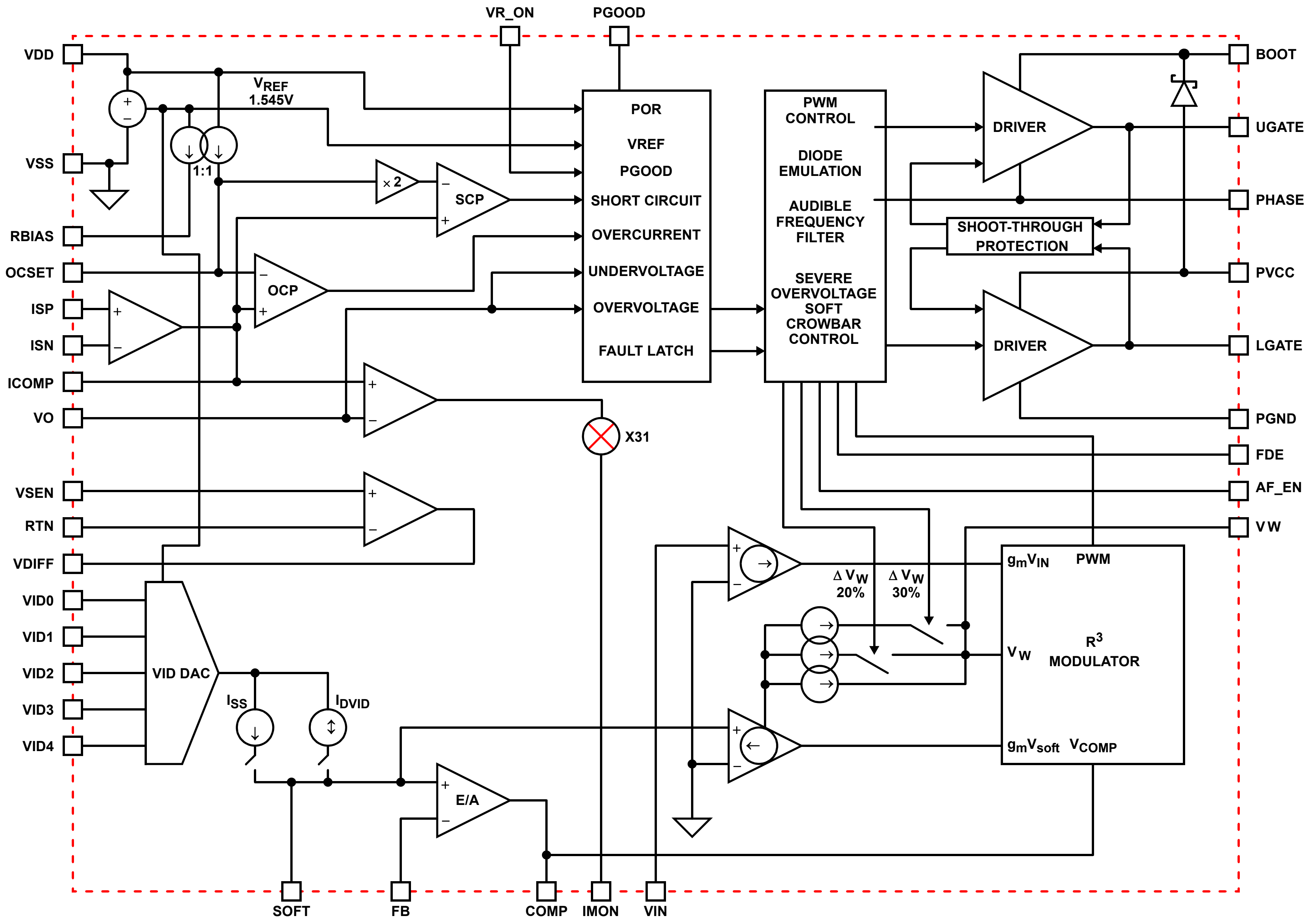


FIGURE 1. SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM OF THE ISL6263C

## Simplified Application Circuit for DCR Current Sense

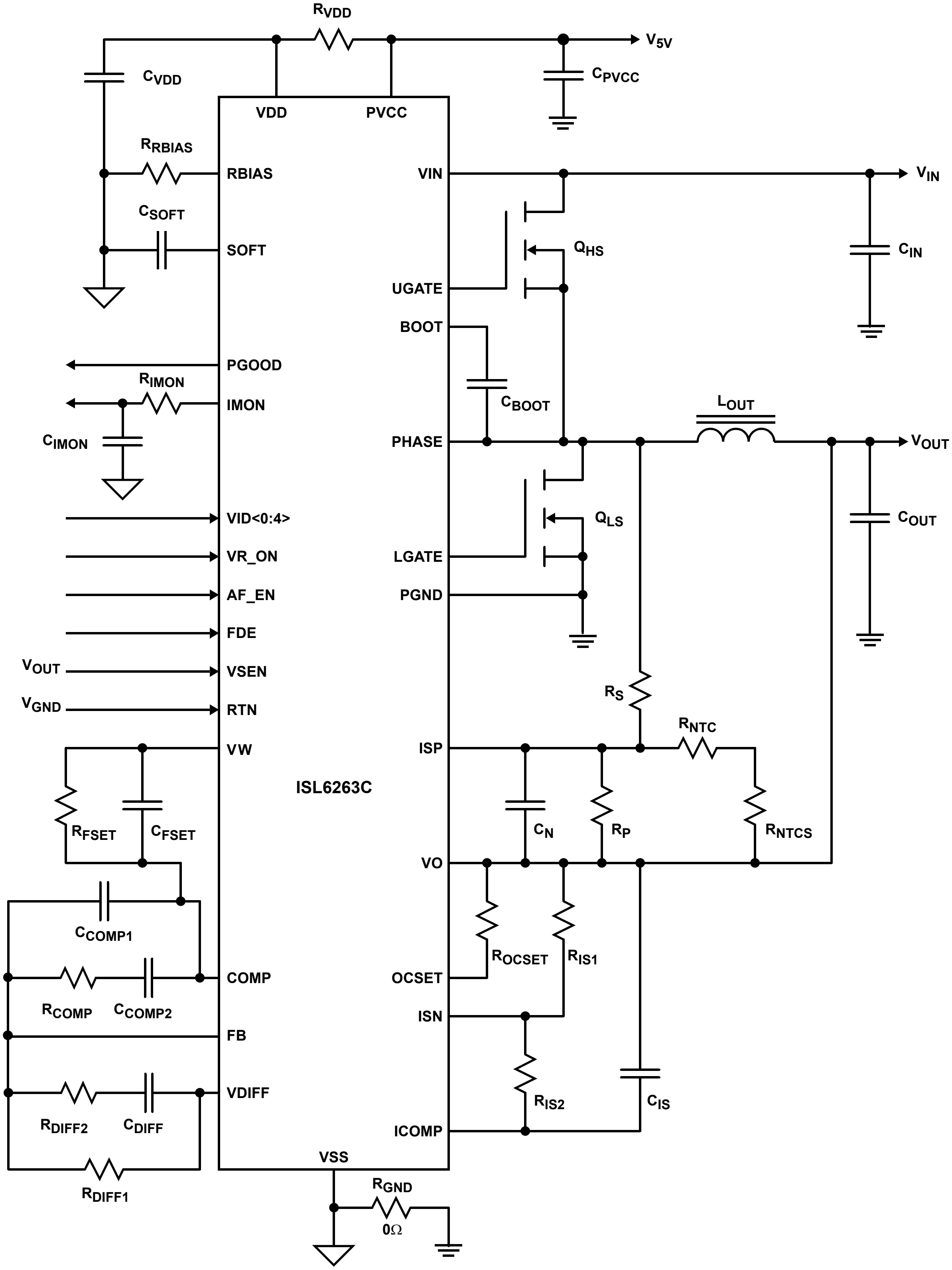


FIGURE 2. ISL6263C GPU CORE VOLTAGE REGULATOR SOLUTION WITH DCR CURRENT SENSE

## Simplified Application Circuit for Resistive Current Sense

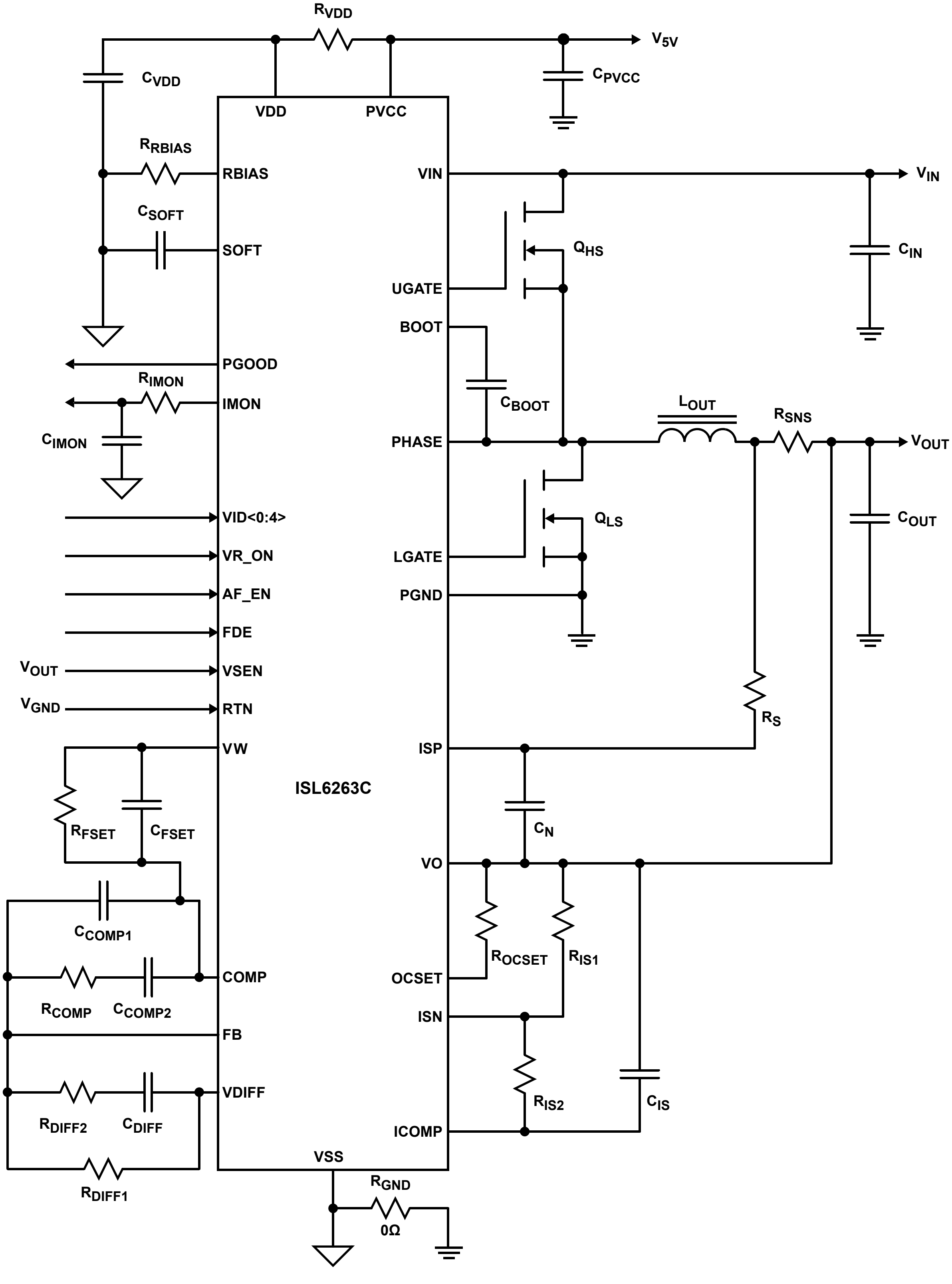


FIGURE 3. ISL6263C GPU CORE VOLTAGE REGULATOR SOLUTION WITH RESISTOR CURRENT SENSE

## Absolute Voltage Ratings

| | |
|---|---|
| VIN to VSS | -0.3V to +28V |
| VDD to VSS | -0.3V to +7.0V |
| PVCC to PGND | -0.3V to +7.0V |
| VSS to PGND | -0.3V to +0.3V |
| PHASE to VSS | (DC) -0.3V to +28V |
| | (<100ns Pulse Width, 10µJ) -5.0V |
| BOOT to PHASE | -0.3V to +7.0V |
| BOOT to VSS or PGND | -0.3V to +33V |
| UGATE | (DC) -0.3V to PHASE, BOOT +0.3V |
| | (<200ns Pulse Width, 20µJ) -4.0V |
| LGATE | (DC) -0.3V to PGND, PVCC +0.3V |
| | (<100ns Pulse Width, 4µJ) -2.0V |
| ALL Other Pins | -0.3V to VSS, VDD +0.3V |

## Thermal Information

| Thermal Resistance (Typical, Notes 4, 5) | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| 32 Ld QFN Package | 35 | 6 |

| | |
|---|---|
| Junction Temperature Range | -55°C to +150°C |
| Operating Temperature Range | -10°C to +100°C |
| Storage Temperature | -65°C to +150°C |
| Pb-Free Reflow Profile | see link below |

http://www.intersil.com/pbfree/Pb-FreeReflow.asp

## Recommended Operating Conditions

| | |
|---|---|
| Ambient Temperature Range | -10°C to +100°C |
| VIN to VSS | +5V to +25V |
| VDD to VSS | +5V ±5% |
| PVCC to PGND | +5V ±5% |
| FDE to VSS | 0V to +3.3V |

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTES:

4. $\theta_{JA}$ is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For $\theta_{JC}$, the "case temp" location is the center of the exposed metal pad on the package underside.

## Electrical Specifications

These specifications apply for $T_A$ = -10°C to +100°C, unless otherwise stated. All typical specifications $T_A$ = +25°C, $V_{DD}$ = 5V, PVCC = 5V. **Boldface limits apply over the operating temperature range, -10°C to +100°C.**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN (Note 6) | TYP | MAX (Note 6) | UNITS |
|---|---|---|---|---|---|---|
| **VIN** | | | | | | |
| VIN Input Resistance | $R_{VIN}$ | VR_ON = 3.3V | | 1.0 | | MΩ |
| VIN Shutdown Current | $I_{VIN\_SHDN}$ | VR_ON = 0V, $V_{IN}$ = 25V | | | **1.0** | µA |
| **VDD and PVCC** | | | | | | |
| VDD Input Bias Current | $I_{VDD}$ | VR_ON = 3.3V | | 2.7 | **3.3** | mA |
| VDD Shutdown Current | $I_{VDD\_SHDN}$ | VR_ON = 0V, $V_{DD}$ = 5.0V | | | **1.0** | µA |
| **VDD POR THRESHOLD** | | | | | | |
| Rising VDD POR Threshold Voltage | $V_{VDD\_THR}$ | | | 4.35 | **4.50** | V |
| Falling VDD POR Threshold Voltage | $V_{VDD\_THF}$ | | **3.85** | 4.10 | | V |
| **REGULATION** | | | | | | |
| Output Voltage Range | $V_{OUT\_MAX}$ | VID<4:0> = 00000 | | 1.28750 | | V |
| | $V_{OUT\_MIN}$ | VID<4:0> = 11111 | | 0.41200 | | V |
| VID Voltage Step | | VID<4:0> = 00000 to 11110 (1.28750V to 0.51500V) | | 25.75 | | mV/step |
| | | VID<4:0> = 11110 to 11111 (0.51500V to 0.41200V) | | 103 | | mV |
| System Accuracy | | VID = 1.28750V to 0.74675V<br>$T_A$ = 0°C to +100°C | **-0.5** | | **0.5** | % |
| | | VID = 0.72100V to 0.51500V<br>$T_A$ = 0°C to +100°C | **-1.0** | | **1.0** | % |
| | | VID = 0.41200<br>$T_A$ = 0°C to +100°C | **-3.0** | | **3.0** | % |

## Electrical Specifications

These specifications apply for $T_A$ = -10°C to +100°C, unless otherwise stated. All typical specifications $T_A$ = +25°C, $V_{DD}$ = 5V, PVCC = 5V. **Boldface limits apply over the operating temperature range, -10°C to +100°C. (Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN (Note 6) | TYP | MAX (Note 6) | UNITS |
|---|---|---|---|---|---|---|
| **PWM** | | | | | | |
| Nominal Frequency | $f_{SW}$ | $R_{FSET}$ = 7kΩ$V_{COMP}$ = 2V | **318** | 333 | **348** | kHz |
| Frequency Range | | | **200** | | **500** | kHz |
| Audio Filter Frequency | $f_{AF}$ | | | 28 | | kHz |
| **AMPLIFIERS** | | | | | | |
| Error Amplifier DC Gain (Note 7) | $A_{V0}$ | | | 90 | | dB |
| Error Amplifier Gain-Bandwidth Product (Note 3) | GBW | $C_L$ = 20pF | | 18 | | MHz |
| Error Amp Slew Rate (Note 7) | SR | $C_L$ = 20pF | | 5 | | V/µs |
| FB Input Bias Current | $I_{FB}$ | $V_{FB}$ = 1.28750V | | 10 | **150** | nA |
| Current Sense Amplifier Offset | $V_{ISENSE\_OFS}$ | | **-0.3** | | **0.3** | mV |
| RBIAS Voltage | $V_{RBIAS}$ | $R_{RBIAS}$ = 150kΩ | **1.495** | 1.515 | **1.535** | V |
| **SOFT-START CURRENT** | | | | | | |
| Soft-Start Current | $I_{SS}$ | | **-47** | -42 | **-37** | µA |
| Soft Dynamic VID Current | $I_{DVID}$ | \|SOFT - REF\|>100mV | **±180** | ±205 | **±230** | µA |
| **CURRENT MONITOR** | | | | | | |
| Current Monitor Output Voltage Range | $V_{IMON}$ | $V_{ICOMP}$ - $V_O$ = 40mV | **1.22** | 1.24 | **1.26** | V |
| | | $V_{ICOMP}$ - $V_O$ = 10mV | **0.285** | 0.310 | **0.335** | V |
| Current Monitor Maximum Output Voltage | $V_{IMONMAX}$ | | **3.1** | 3.4 | | V |
| Current Monitor Maximum Current Sinking Capability | | | **$V_{IMON}$/ 250Ω** | $V_{IMON}$/ 180Ω | **$V_{IMON}$/ 130Ω** | A |
| Current Monitor Sourcing Current | $I_{SC\_IMON}$ | $V_{ICOMP}$ - $V_O$ = 40mV | **2.0** | | | mA |
| Current Monitor Sinking Current | $I_{SK\_IMON}$ | $V_{ICOMP}$ - $V_O$ = 40mV | **2.0** | | | mA |
| Current Monitor Impedance (Note 7) | | $I_{IMON} \le I_{SK\_IMON}$, $I_{IMON} \le I_{SC\_IMON}$ | | 7 | | Ω |
| **GATE DRIVER** | | | | | | |
| UGATE Source Resistance (Note 7) | $R_{UGSRC}$ | 500mA Source Current | | 1.0 | **1.5** | Ω |
| UGATE Source Current (Note 7) | $I_{UGSRC}$ | $V_{UGATE\_PHASE}$ = 2.5V | | 2.0 | | A |
| UGATE Sink Resistance (Note 7) | $R_{UGSNK}$ | 500mA Sink Current | | 1.0 | **1.5** | Ω |
| UGATE Sink Current (Note 7) | $I_{UGSNK}$ | $V_{UGATE\_PHASE}$ = 2.5V | | 2.0 | | A |
| LGATE Source Resistance (Note 7) | $R_{LGSRC}$ | 500mA Source Current | | 1.0 | **1.5** | Ω |
| LGATE Source Current (Note 7) | $I_{LGSRC}$ | $V_{LGATE\_PGND}$ = 2.5V | | 2.0 | | A |
| LGATE Sink Resistance (Note 7) | $R_{LGSNK}$ | 500mA Sink Current | | 0.5 | **0.9** | Ω |
| LGATE Sink Current (Note 7) | $I_{LGSNK}$ | $V_{LGATE\_PGND}$ = 2.5V | | 4.0 | | A |
| UGATE Pull-Down Resistor | $R_{PD}$ | | | 1.1 | | kΩ |
| UGATE Turn-On Propagation Delay | $t_{PDRU}$ | $PV_{CC}$ = 5V, UGATE open | **20** | 30 | **44** | ns |
| LGATE Turn-On Propagation Delay | $t_{PDRL}$ | $PV_{CC}$ = 5V, LGATE open | **7** | 15 | **30** | ns |
| **BOOTSTRAP DIODE** | | | | | | |
| Forward Voltage | $V_F$ | $PV_{CC}$ = 5V, $I_F$ = 10mA | **0.56** | 0.69 | **0.76** | V |
| Reverse Leakage | $I_R$ | $V_R$ = 16V | | | **5.0** | µA |

## Electrical Specifications

These specifications apply for $T_A$ = -10°C to +100°C, unless otherwise stated. All typical specifications $T_A$ = +25°C, $V_{DD}$ = 5V, PVCC = 5V. **Boldface limits apply over the operating temperature range, -10°C to +100°C. (Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN (Note 6) | TYP | MAX (Note 6) | UNITS |
|---|---|---|---|---|---|---|
| **POWER GOOD and PROTECTION MONITOR** | | | | | | |
| PGOOD Low Voltage | $V_{PGOOD}$ | $I_{PGOOD}$ = 4mA | | 0.11 | **0.40** | V |
| PGOOD Leakage Current | $I_{PGOOD}$ | $V_{PGOOD}$ = 3.3V | **-1.0** | | **1.0** | µA |
| Overvoltage Threshold (VO-VSOFT) | $V_{OVP}$ | $V_O$ rising above $V_{SOFT}$ > 1ms | **155** | 195 | **235** | mV |
| Severe Overvoltage Threshold | $V_{OVPS}$ | $V_O$ rising above 1.55V reference > 0.5µs | **1.525** | 1.550 | **1.575** | V |
| OCSET Reference Current | $I_{OCSET}$ | $R_{RBIAS}$ = 150kΩ | **9.9** | 10.1 | **10.3** | µA |
| OCSET Voltage Threshold Offset | $V_{OCSET\_OFS}$ | $V_{ICOMP}$ rising above $V_{OCSET}$ > 120µs | **-3** | | **3** | mV |
| Undervoltage Threshold (VSOFT-VO) | $V_{UVF}$ | $V_O$ falling below $V_{SOFT}$ for > 1ms | **-360** | -300 | **-240** | mV |
| **CONTROL INPUTS** | | | | | | |
| VR_ON Input Low | $V_{VR\_ONL}$ | | | | **1** | V |
| VR_ON Input High | $V_{VR\_ONH}$ | | **2.3** | | | V |
| AF_EN Input Low | $V_{AF\_ENL}$ | | | | **1** | V |
| AF_EN Input High | $V_{AF\_ENH}$ | | **2.3** | | | V |
| VR_ON Leakage | $I_{VR\_ONL}$ | $V_{VR\_ON}$ = 0V | **-1.0** | 0 | | µA |
| | $I_{VR\_ONH}$ | $V_{VR\_ON}$ = 3.3V | | 0 | **1.0** | µA |
| AF_EN Leakage | $I_{AF\_ENL}$ | $V_{AF\_EN}$ = 0V | **-1.0** | 0 | | µA |
| | $I_{AF\_ENH}$ | $V_{AF\_EN}$ = 3.3V | | 0.45 | **1.0** | µA |
| VID<4:0> Input Low | $V_{VIDL}$ | | | | **0.4** | V |
| VID<4:0> Input High | $V_{VIDH}$ | | **0.7** | | | V |
| FDE Input Low | $V_{FDEL}$ | | | | **0.3** | V |
| FDE Input High | $V_{FDEH}$ | | **0.7** | | | V |
| VID<4:0> Leakage | $I_{VIDL}$ | $V_{VID}$ = 0V | **-1.0** | 0 | | µA |
| | $I_{VIDH}$ | $V_{VID}$ = 1.0V | | 0.45 | **1.0** | µA |
| FDE Leakage | $I_{FDEL}$ | $V_{FDE}$ = 0V | **-1.0** | 0 | | µA |
| | $I_{FDEH}$ | $V_{FDE}$ = 1.0V | | 0.45 | **1.0** | µA |

NOTES:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
7. Limits established by characterization and are not production tested.

## Functional Pin Descriptions

**RBIAS (Pin 1) -** Sets the internal 10µA current reference. Connect a 150kΩ ±1% resistor from RBIAS to VSS.

**SOFT (Pin 2) -** Sets the output voltage slew-rate. Connect an X5R or X7R ceramic capacitor from SOFT to VSS. The SOFT pin is the non-inverting input of the error amplifier.

**OCSET (Pin 3) -** Sets the overcurrent threshold. Connect a resistor from OCSET to VO.

**VW (Pin 4) -** Sets the static PWM switching frequency in continuous conduction mode. Connect a resistor from VW to COMP.

**COMP (Pin 5) -** Connects to the output of the control loop error amplifier.

**FB (Pin 6) -** Connects to the inverting input of the control loop error amplifier.

**VDIFF (Pin 7) -** Connects to the output of the VDIFF differential amplifier. Together with the FB pin, it is used for the output voltage feedback.

**VSEN (Pin 8) -** This is the $V_{OUT}$ input of the GPU processor Kelvin connection. Connects internally to the non-inverting inputs of the VDIFF differential amplifier.

**RTN (Pin 9) -** This is the $V_{GND}$ input of the GPU processor Kelvin connection. Connects internally to the inverting inputs of the VDIFF differential amplifier.

**ICOMP (Pin 10) -** Connects to the output of the differential current sense amplifier and to the non-inverting inputs of the overcurrent comparator. Used for output current monitor and overcurrent protection.

**ISN (Pin 11) -** This is the feedback of the current sense amplifier. Connects internally to the inverting input of the current sense amplifier. Used for output current sense.

**VO (Pin 12) -** Connects to the inverting inputs of the VDIFF differential amplifier.

**ISP (Pin 13) -** Connects to the non-inverting input of the current sense amplifier. Used for output current sense.

**VIN (Pin 14) -** Connects to the $R^3$ PWM modulator providing input voltage feed-forward. For optimum input voltage transient response, connect near the drain of the high-side MOSFETs.

**VSS (Pin 15) -** Analog ground.

**VDD (Pin 16) -** Input power supply for the IC. Connect to +5VDC and decouple with at least a 1µF MLCC capacitor from the VDD pin to the VSS pin.

**BOOT (Pin 17) -** Input power supply for the high-side MOSFET gate driver. Connect an MLCC bootstrap capacitor from the BOOT pin to the PHASE pin.

**UGATE (Pin 18) -** High-side MOSFET gate driver output. Connect to the gate of the high-side MOSFET.

**PHASE (Pin 19) -** Current return path for the UGATE high-side MOSFET gate driver. Detects the polarity of the PHASE node voltage for diode emulation. Connect the PHASE pin to the drains of the low-side MOSFETs.

**PGND (Pin 20) -** Current return path for the LGATE low-side MOSFET gate driver. The PGND pin only conducts current when LGATE pulls down. Connect the PGND pin to the sources of the low-side MOSFETs.

**LGATE (Pin 21) -** Low-side MOSFET gate driver output. Connect to the gate of the low-side MOSFET.

**PVCC (Pin 22) -** Input power supply for the low-side MOSFET gate driver, and the high-side MOSFET gate driver, via the internal bootstrap diode connected between the PVCC and BOOT pins. Connect to +5VDC and decouple with at least 1µF of an MLCC capacitor from the PVCC pin to the PGND pin.

**VID0:VID4 (Pin 23:Pin 27) -** Voltage identification inputs. VID0 input is the least significant bit (LSB) and VID4 input is the most significant bit (MSB).

**IMON (Pin 28) -** A voltage signal proportional to the output current of the converter.

**VR_ON (Pin 29) -** A high logic signal on this pin enables the converter and a low logic signal disables the converter.

**AF_EN (Pin 30) -** Used in conjunction with VID0:VID4 and FDE pins to program the diode-emulation and audio filter behavior. Refer to Table 2.

**PGOOD (Pin 31) -** The PGOOD pin is an open-drain output that indicates when the converter is able to supply regulated voltage. Connect the PGOOD pin to a maximum of 5V through a pull-up resistor.

**FDE (Pin 32) -** Used in conjunction with VID0:VID4 and AF_EN pins to program the diode-emulation and audio filter behavior. Refer to Table 2.

**BOTTOM -** Connects to substrate. Electrically isolated but should be connected to VSS. Requires best practical thermal coupling to PCB.

## Theory of Operation

### The $R^3$ Modulator

The heart of the ISL6263C is Intersil's Robust-Ripple-Regulator ($R^3$) Technology™. The $R^3$ modulator is a hybrid of fixed frequency PWM control, and variable frequency hysteretic control that will simultaneously affect the PWM switching frequency and PWM duty cycle in response to input voltage and output load transients.

The term "Ripple" in the name "Robust-Ripple-Regulator" refers to the synthesized voltage-ripple signal $V_R$ that appears across the internal ripple-capacitor $C_R$. The $V_R$ signal is a representation of the output inductor ripple current. Transconductance amplifiers measuring the input voltage of the converter and the output set-point voltage $V_{SOFT}$, together produce the voltage-ripple signal $V_R$.

A voltage window signal $V_W$ is created across the VW and COMP pins by sourcing a current proportional to $g_mV_{SOFT}$ through a parallel network consisting of resistor $R_{FSET}$ and capacitor $C_{FSET}$. The synthesized voltage-ripple signal $V_R$ along with similar companion signals are converted into PWM pulses.

The PWM frequency is proportional to the difference in amplitude between $V_W$ and $V_{COMP}$. Operating on these large-amplitude, low noise synthesized signals allows the ISL6263C to achieve lower output ripple and lower phase jitter than either conventional hysteretic or fixed frequency PWM controllers. Unlike conventional hysteretic converters, the ISL6263C has an error amplifier that allows the controller to maintain tight voltage regulation accuracy throughout the VID range from 0.41200V to 1.28750V.

### Voltage Programming

The output voltage $V_{OUT}$ is regulated to the SOFT pin voltage, $V_{SOFT}$, which is determined by the DAC output. The DAC output voltage is programmed by the external five VID pins. Refer to Table 1 for the VID voltage programming specification.

### Power-On Reset

The ISL6263C is disabled until the voltage at the VDD pin has increased above the rising VDD power-on reset (POR) $V_{DD\_THR}$ threshold voltage. The controller will become disabled when the voltage at the VDD pin decreases below the falling POR $V_{DD\_THF}$ threshold voltage.

### Start-Up Timing

Figure 4 shows the ISL6263C start-up timing. Once VDD has ramped above $V_{DD\_THR}$, the controller can be enabled by pulling the VR_ON pin voltage above the input-high threshold $V_{VR\_ONH}$. Approximately 100µs later, the soft-start capacitor $C_{SOFT}$ begins slewing to the designated VID set-point as it is charged by the soft-start current source $I_{SS}$. The $V_{OUT}$ output voltage of the converter follows the $V_{SOFT}$ voltage ramp to within 10% of the VID set-point then counts 13 switching cycles, then changes the open-drain output of the PGOOD pin to high impedance. During soft-start, the regulator always operates in continuous conduction mode (CCM).

**TABLE 1. VID AND DAC TRUTH TABLE**

| GPU MODE | VID4 | VID3 | VID2 | VID1 | VID0 | $V_{SOFT}$ (DAC) (V) |
|---|---|---|---|---|---|---|
| GPU MODE 1 | - | - | - | - | - | 0 |
| | 0 | 0 | 0 | 0 | 0 | 1.28750 |
| | 0 | 0 | 0 | 0 | 1 | 1.26175 |
| | 0 | 0 | 0 | 1 | 0 | 1.23600 |
| | 0 | 0 | 0 | 1 | 1 | 1.21025 |
| | 0 | 0 | 1 | 0 | 0 | 1.18450 |
| | 0 | 0 | 1 | 0 | 1 | 1.15875 |
| | 0 | 0 | 1 | 1 | 0 | 1.13300 |
| | 0 | 0 | 1 | 1 | 1 | 1.10725 |
| | 0 | 1 | 0 | 0 | 0 | 1.08150 |
| | 0 | 1 | 0 | 0 | 1 | 1.05575 |
| | 0 | 1 | 0 | 1 | 0 | 1.03000 |
| | 0 | 1 | 0 | 1 | 1 | 1.00425 |
| | 0 | 1 | 1 | 0 | 0 | 0.97850 |
| | 0 | 1 | 1 | 0 | 1 | 0.95275 |
| | 0 | 1 | 1 | 1 | 0 | 0.92700 |
| | 0 | 1 | 1 | 1 | 1 | 0.90125 |
| | 1 | 0 | 0 | 0 | 0 | 0.87550 |
| | 1 | 0 | 0 | 0 | 1 | 0.84975 |
| GPU MODE 2 | 1 | 0 | 0 | 1 | 0 | 0.82400 |
| | 1 | 0 | 0 | 1 | 1 | 0.79825 |
| | 1 | 0 | 1 | 0 | 0 | 0.77250 |
| | 1 | 0 | 1 | 0 | 1 | 0.74675 |
| | 1 | 0 | 1 | 1 | 0 | 0.72100 |
| | 1 | 0 | 1 | 1 | 1 | 0.69525 |
| | 1 | 1 | 0 | 0 | 0 | 0.66950 |
| | 1 | 1 | 0 | 0 | 1 | 0.64375 |
| | 1 | 1 | 0 | 1 | 0 | 0.61800 |
| | 1 | 1 | 0 | 1 | 1 | 0.59225 |
| | 1 | 1 | 1 | 0 | 0 | 0.56650 |
| | 1 | 1 | 1 | 0 | 1 | 0.54075 |
| | 1 | 1 | 1 | 1 | 0 | 0.51500 |
| | 1 | 1 | 1 | 1 | 1 | 0.41200 |

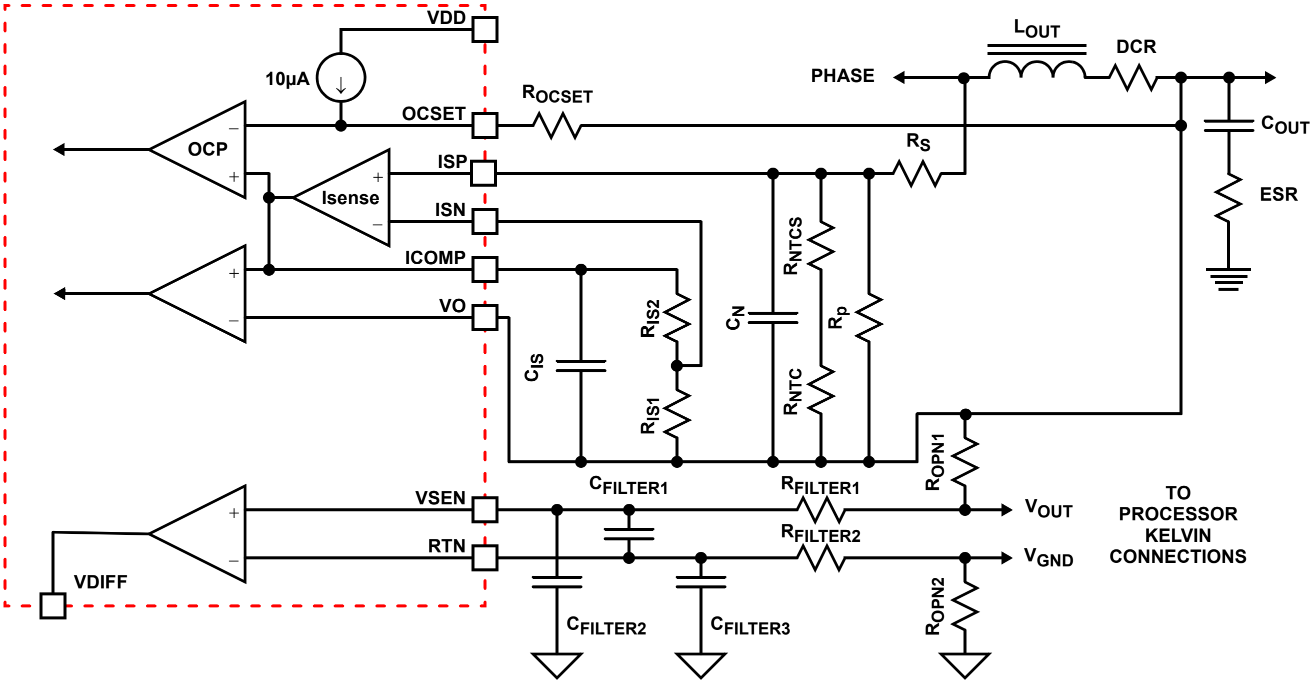


**FIGURE 5. SIMPLIFIED GPU KELVIN SENSE AND INDUCTOR DCR CURRENT SENSE**

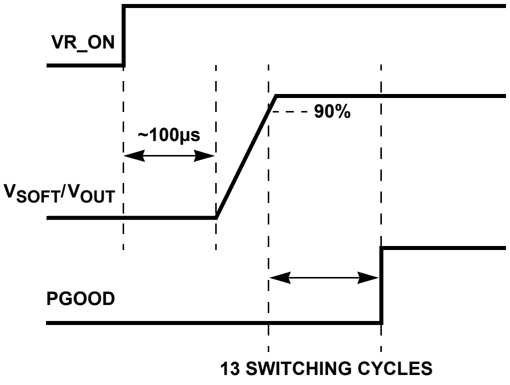


**FIGURE 4. ISL6263C START-UP TIMING**

## Static Regulation

The output voltage $V_{OUT}$ will be regulated to the value set by the VID inputs per Table 1. A true differential amplifier connected to the VSEN and RTN pins implements processor Kelvin sense for precise core voltage regulation at the GPU voltage sense points.

The ISL6263C can accommodate DCR current sense or discrete resistor current sense. The DCR current sense uses the intrinsic series resistance of the output inductor, as shown in the application circuit of Figure 2. The discrete resistor current sense uses a shunt resistor in series with the output inductor, as shown in the application circuit in Figure 3. In both cases, the signal is fed to the non-inverting input of the current sense amplifier at the ISP pin, where it is measured differentially with respect to the output voltage of the converter at the VO pin and amplified. The voltage at the ICOMP pin minus the output voltage measured at the VO pin, is proportional to the total inductor current. This information is used for overcurrent protection and current monitoring. It is important to note that this current measurement should not be confused with the synthetic current ripple information created within the $R^3$ modulator.

When using inductor DCR current sense, an NTC compensation network is optional to compensate the positive temperature coefficient of the copper winding, thus maintaining the current sense accuracy.

## Processor Kelvin Voltage Sense

The remote voltage sense input pins VSEN and RTN of the ISL6263C are to be terminated at the die of the GPU. Kelvin sense allows the voltage regulator to tightly control the processor voltage at the die, compensating for various resistive voltage drops in the power delivery path.

Since the voltage feedback is sensed at the processor die, removing the GPU will open the voltage feedback path of the regulator, causing the output voltage to rise towards VIN. The ISL6263C will shut down when the voltage between the VO and VSS pins exceeds the severe overvoltage protection threshold $V_{OVPS}$ of 1.55V. To prevent this issue from occurring, it is recommended to install resistors $R_{OPN1}$ and $R_{OPN2}$, as shown in Figure 5. These resistors provide voltage feedback from the regulator local output in the absence of the GPU. These resistors should be in the range of 20Ω to 100Ω.

### High Efficiency Diode Emulation Mode

The ISL6263C operates in continuous-conduction-mode (CCM) during heavy load for minimum conduction loss by forcing the low-side MOSFET to operate as a synchronous rectifier. An improvement in light-load efficiency is achieved by allowing the converter to operate in diode-emulation mode (DEM) where the low-side MOSFET behaves as a smart-diode, forcing the device to block negative inductor current flow.

Positive-going inductor current flows from either the source of the high-side MOSFET, or the drain of the low-side MOSFET. Negative-going inductor current flows into the source of the high-side MOSFET, or into the drain of the low-side MOSFET. When the low-side MOSFET conducts positive inductor current, the phase voltage will be negative with respect to the VSS pin. Conversely, when the low-side MOSFET conducts negative inductor current, the phase voltage will be positive with respect to the VSS pin. Negative inductor current occurs when the output DC load current is less than ½ the inductor ripple current. Sinking negative inductor current through the low-side MOSFET lowers efficiency through unnecessary conduction losses. Efficiency can be further improved with a reduction of unnecessary switching losses by reducing the PWM frequency. The PWM frequency can be configured to automatically make a step-reduction upon entering DEM by forcing a step-increase of the window voltage $V_W$. The window voltage can be configured to increase approximately 30%, 50%, or not at all. The characteristic PWM frequency reduction, coincident with decreasing load, is accelerated by the step-increase of the window voltage.

The converter will enter DEM after detecting three consecutive PWM pulses with negative inductor current. The negative inductor current is detected during the time that the high-side MOSFET gate driver output UGATE is low, with the exception of a brief blanking period. The voltage between the PHASE pin and VSS pin is monitored by a comparator that latches upon detection of positive phase voltage. The converter will return to CCM after detecting three consecutive PWM pulses with positive inductor current.

The inductor current is considered positive if the phase comparator has not been latched while UGATE is low.

Because the switching frequency in DEM is a function of load current, very light load condition can produce frequencies well into the audio band. To eliminate this audible noise, an audio filter can be enabled that briefly turns on the low-side MOSFET gate driver LGATE approximately every 35µs.

The DEM and audio filter operation are programmed by the AF_EN and FDE pins in conjunction with VID0:VID4 according to Table 2.

TABLE 2. DIODE EMULATION MODE and AUDIO FILTER

| GPU MODE (VID code) | FDE | AF_EN | DEM STATUS | VOLTAGE WINDOW | AUDIO FILTER |
|---|---|---|---|---|---|
| MODE 1 | 0 | - | DISABLED | NOM | - |
| | 1 | - | ENABLED | 130% NOM | - |
| MODE 2 | - | 0 | ENABLED | 150% NOM | - |
| | 1 | 1 | ENABLED | 130% NOM | - |
| | 0 | 1 | ENABLED | 130% NOM | ENABLED |

Smooth mode transitions are facilitated by the $R^3$ modulator, which correctly maintains the internally synthesized ripple current information throughout mode transitions.

### Current Monitor

The ISL6263C features a current monitor output. The voltage between the IMON and VSS pins is proportional to the output inductor current. The output inductor current is proportional to the voltage between the ICOMP and VO pins. The IMON pin has source and sink capability for close tracking of transient current events. The current monitor output is expressed in Equation 1:

$$V_{IMON} = (V_{ICOMP} - V_O) \cdot 31 \quad \text{(EQ. 1)}$$

### Protection

The ISL6263C provides overcurrent protection (OCP), overvoltage protection (OVP), and undervoltage protection (UVP), as shown in Table 3.

Overcurrent protection is tied to the current sense amplifier. Given the overcurrent set point $I_{OC}$, the maximum voltage at ICOMP pin $V_{ICOMP(max)}$ (which is the voltage when OCP happens) can be determined by the current sense network (explained in “Inductor DCR Current Sense” on page 14 and “Resistor Current Sense” on page 15). During start-up, the ICOMP pin must fall 25mV below the OCSET pin to reset the overcurrent comparator, which requires $(V_{ICOMP(max)} - V_O) > 25mV$.

The OCP threshold detector is checked every 15µs and will increment a counter if the OCP threshold is exceeded, conversely the counter will be decremented if the load current is below the OCP threshold. The counter will latch an OCP fault when the counter reaches eight. The fastest OCP response for overcurrent levels that are no more than 2.5 times the OCP threshold is 120µs, which is eight counts at 15µs each. The ISL6263C protects against hard shorts by latching an OCP fault within 2µs for overcurrent levels exceeding 2.5 times the OCP threshold.

The overcurrent threshold is determined by the resistor $R_{OCSET}$ between OCSET pin and VO pin. The value of $R_{OCSET}$ is calculated in Equation 2:

$$R_{OCSET} = \frac{V_{ICOMP(max)} - V_O}{10\mu A} \quad \text{(EQ. 2)}$$

For example, choose $V_{ICOMP(max)}$ - $V_O$ = 80mV. $R_{OCSET}$ can use a 8.06kΩ resistor, according to Equation 2.

UVP and OVP are independent of the OCP. If the output voltage measured on the VO pin is less than +300mV below the voltage on the SOFT pin for longer than 1ms, the controller will latch a UVP fault. If the output voltage measured on the VO pin is >195mV above the voltage on the SOFT pin for longer than 1ms, the controller will latch an OVP fault. Keep in mind that $V_{SOFT}$ will equal the voltage level commanded by the VID states only after the soft-start capacitor $C_{SOFT}$ has slewed to the VID DAC output voltage. The UVP and OVP detection circuits act on static and dynamic $V_{SOFT}$ voltage.

When an OCP, OVP, or UVP fault has been latched, PGOOD becomes a low impedance and the gate driver outputs UGATE and LGATE are pulled low. The energy stored in the inductor is dissipated as current flows through the low-side MOSFET body diode. The controller will remain latched in the fault state until the VR_ON pin has been pulled below the falling VR_ON threshold voltage $V_{VR\_ONL}$ or until VDD has gone below the falling POR threshold voltage $V_{VDD\_THF}$.

A severe-overvoltage protection fault occurs immediately after the voltage between the VO and VSS pins exceed the rising severe-overvoltage threshold $V_{OVPS}$ which is 1.545V, the same reference voltage used by the VID DAC. The ISL6263C will latch UGATE and PGOOD low but unlike other protective faults, LGATE remains high until the voltage between VO and VSS falls below approximately 0.77V, at which time LGATE is pulled low. The LGATE pin will continue to switch high and low at 1.545V and 0.77V until VDD has gone below the falling POR threshold voltage $V_{VDD\_THF}$. This provides maximum protection against a shorted high-side MOSFET while preventing the output voltage from ringing below ground. The severe-overvoltage fault circuit can be triggered after another fault has already been latched.

**TABLE 3. FAULT PROTECTION SUMMARY OF ISL6263C**

| FAULT TYPE | FAULT DURATION PRIOR TO PROTECTION | PROTECTION ACTIONS | FAULT RESET |
|---|---|---|---|
| Overcurrent | 120µs | LGATE, UGATE, and PGOOD latched low | Cycle VR_ON or VDD |
| Short Circuit | <2µs | LGATE, UGATE, and PGOOD latched low | Cycle VR_ON or VDD |
| Overvoltage (+195mV) between VO pin and SOFT pin | 1ms | LGATE, UGATE, and PGOOD latched low | Cycle VR_ON or VDD |
| Severe Overvoltage (+1.55V) between VO pin and VSS pin | Immediately | UGATE, and PGOOD latched low, LGATE toggles ON when VO > 1.55V OFF when VO < 0.77V until fault reset | Cycle VDD only |
| Undervoltage (-300mV) between VO pin and SOFT pin | 1ms | LGATE, UGATE, and PGOOD latched low | Cycle VR_ON or VDD |

### Gate-Driver Outputs LGATE and UGATE

The ISL6263C has internal high-side and low-side N-Channel MOSFET gate-drivers. The LGATE driver is optimized for low duty-cycle applications where the low-side MOSFET conduction losses are dominant. The LGATE pull-down resistance is very low in order to clamp the gate-source voltage of the MOSFET below the $V_{GS(th)}$ at turn-off. The current transient through the low-side gate at turn-off can be considerable due to the characteristic large switching charge of a low $r_{DS(ON)}$ MOSFET.

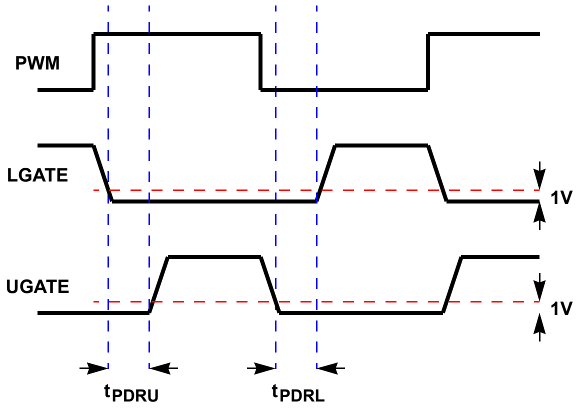


FIGURE 6. GATE DRIVER TIMING DIAGRAM

Adaptive shoot-through protection prevents the gate-driver outputs from going high until the opposite gate-driver output has fallen below approximately 1V. The UGATE turn-on propagation delay $t_{PDRU}$ and LGATE turn-on propagation delay $t_{PDRL}$ are found in the “Electrical Specifications” table on page 6. The power for the LGATE gate-driver is sourced directly from the PVCC pin. The power for the UGATE gate-driver is sourced from a boot-strap capacitor connected across the BOOT and PHASE pins. The boot capacitor is charged from PVCC through an internal boot-strap diode each time the low-side MOSFET turns on, pulling the PHASE pin low.

### Internal Bootstrap Diode

The ISL6263C has an integrated boot-strap Schottky diode connected from the PVCC pin to the BOOT pin. Simply adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit.

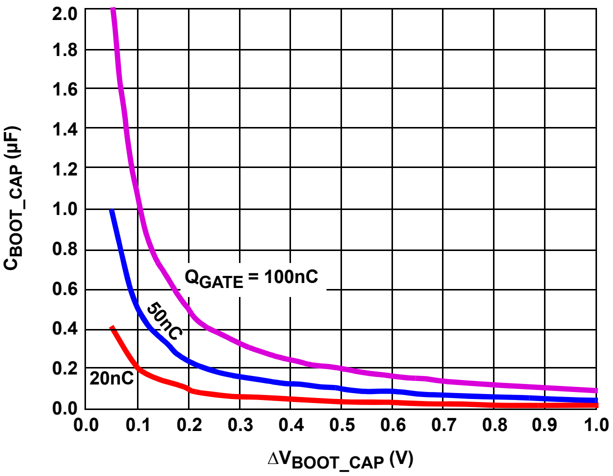


FIGURE 7. BOOTSTRAP CAPACITANCE vs BOOT RIPPLE VOLTAGE

The minimum value of the bootstrap capacitor can be calculated using Equation 3:

$$C_{BOOT} \geq \frac{Q_{GATE}}{\Delta V_{BOOT}} \qquad \text{(EQ. 3)}$$

where $Q_{GATE}$ is the amount of gate charge required to fully charge the gate of the upper MOSFET. The $\Delta V_{BOOT}$ term is defined as the allowable droop in the rail of the upper drive.

As an example, suppose an upper MOSFET has a gate charge, $Q_{GATE}$, of 25nC at 5V and also assume the droop in the drive voltage at the end of a PWM cycle is 200mV. One will find that a bootstrap capacitance of at least 0.125µF is required. The next larger standard value capacitance is 0.15µF. A good quality ceramic capacitor is recommended.

### Soft-Start and Soft Dynamic VID Slew Rates

The output voltage of the converter tracks $V_{SOFT,}$ the voltage across the SOFT and VSS pins. Shown in Figure 1, the SOFT pin is connected to the output of the VID DAC through the unidirectional soft-start current source $I_{SS}$ or the bidirectional soft-dynamic VID current source $I_{DVID}$, and the non-inverting input of the error amplifier. Current is sourced from the SOFT pin when $I_{SS}$ is active. The SOFT pin can both source and sink current when $I_{DVID}$ is active. The soft-start capacitor $C_{SOFT}$ changes voltage at a rate proportional to $I_{SS}$ or $I_{DVID}$. The ISL6263C automatically selects $I_{SS}$ for the soft-start sequence so that the inrush current through the output capacitors is maintained below the OCP threshold. Once soft-start has completed, $I_{DVID}$ is automatically selected for output voltage changes commanded by the VID inputs, charging $C_{SOFT}$ when the output voltage is commanded to rise, and discharging $C_{SOFT}$ when the output voltage is commanded to fall.

The GPU voltage regulator may require a minimum voltage slew rate, which will be guaranteed by the value of $C_{SOFT}$. For example, if the regulator requires 10mV/µs slew rate, the value of $C_{SOFT}$ can be calculated using Equation 4:

$$C_{SOFT} = \frac{I_{DVIDmin}}{\left(\frac{10mV}{\mu s}\right)} = \frac{180\mu A}{10K} = 0.018\mu F \qquad \text{(EQ. 4)}$$

$I_{DVID}$ is the soft-dynamic VID current source, and its minimum value is specified in the “Electrical Specifications” table on page 5. Choosing the next lower standard component value of 0.015µF will guarantee 10mV/µs slew rate. This choice of $C_{SOFT}$ controls the startup slew-rate as well. One should expect the output voltage during soft-start to slew to the voltage commanded by the VID settings at a nominal rate given by Equation 5:

$$\frac{dV_{SOFT}}{dt} = \frac{I_{SS}}{C_{SOFT}} = \frac{42\mu A}{0.015\mu F} \approx \frac{2.8mV}{\mu s} \qquad \text{(EQ. 5)}$$

Note that the slew rate is the average rate of change between the initial and final voltage values.

It is worth it to mention that the surge current charges the output capacitors when the output voltage is commanded to rise. This surge current could be high enough to trigger the OC protection circuit if the voltage slew rate is too high, or/and the output capacitance is too large. The overcurrent set point should guarantee the VID code transition successful.

### RBIAS Current Reference

The RBIAS pin is internally connected to a 1.545V reference through a 3kΩ resistance. A bias current is established by connecting a ±1% tolerance, 150kΩ resistor between the RBIAS and VSS pins. This bias current is mirrored, creating the reference current $I_{OCSET}$ that is sourced from the OCSET pin. Do not connect any other components to this pin, as they will have a negative impact on the performance of the IC.

### Setting the PWM Switching Frequency

The $R^3$ modulator scheme is not a fixed-frequency architecture, lacking a fixed-frequency clock signal to produce PWM. The switching frequency increases during the application of a load to improve transient performance. The static PWM frequency varies slightly depending on the input voltage, output voltage, and output current, but this variation is normally less than 10% in continuous conduction mode.

Refer to Figure 2 and find that resistor $R_{FSET}$ is connected between the VW and COMP pins. A current is sourced from VW through $R_{FSET}$ creating the synthetic ripple window voltage signal $V_W$, which determines the PWM switching frequency. The relationship between the resistance of $R_{FSET}$

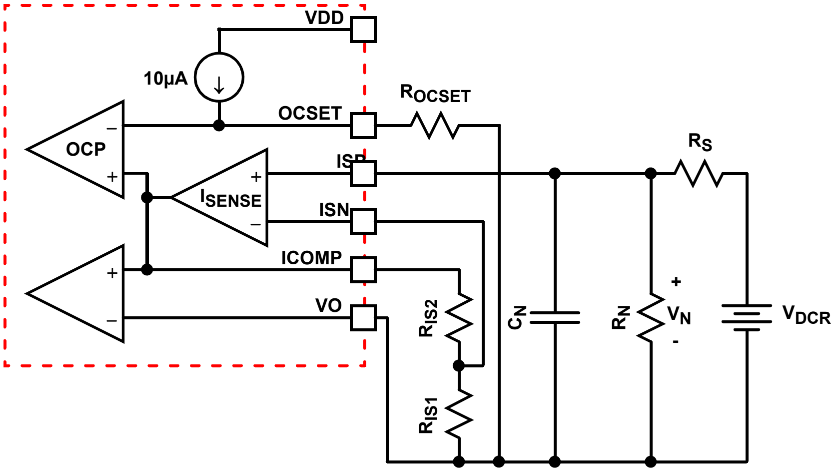


FIGURE 8. EQUIVALENT MODEL OF CURRENT SENSE USING INDUCTOR DCR CURRENT SENSE

and the switching frequency in CCM is approximated using Equation 6:

$$R_{FSET} = \frac{(t - 0.5 \times 10^{-6})}{400 \times 10^{-12}} \quad \text{(EQ. 6)}$$

t is the switching period. For example, the value of $R_{FSET}$ for 300kHz operation is approximated using Equation 7:

$$7.1 \times 10^{3} = \frac{(3.33 \times 10^{-6} - 0.5 \times 10^{-6})}{400 \times 10^{-12}} \quad \text{(EQ. 7)}$$

This relationship only applies to operation in constant conduction mode because the PWM frequency naturally decreases as the load decreases while in diode emulation mode.

### *Inductor DCR Current Sense*

ISL6263C provides the option of using the inductor DCR for current sense. To maintain the current sense accuracy, an NTC compensation network is optional when using DCR sense. The process to compensate the DCR resistance variation takes several iterative steps. Figure 2 shows the DCR sense method. Figure 8 shows the simplified model of the current sense circuitry. The inductor DC current $I_O$ generates a DC voltage drop on the inductor DCR. Equation 8 gives this relationship:

$$V_{DCR} = I_O \cdot DCR \quad \text{(EQ. 8)}$$

An R-C network senses the voltage across the inductor to get the inductor current information. $R_N$ represents the equivalent resistance of $R_P$ and the optional NTC network consisting of $R_{NTC}$ and $R_{NTCS}$. $R_N$ is temperature T dependent and is given by Equation 9:

$$R_N(T) = \frac{(R_{NTC} + R_{NTCS}) \cdot R_P}{R_{NTC} + R_{NTCS} + R_P} \quad \text{(EQ. 9)}$$

If the NTC network is not used, simply set $R_N(T) = R_P$.

Sensing the time varying inductor current accurately requires that the parallel R-C network time constant match the inductor L/DCR time constant. Equation 10 shows this relationship:

$$\frac{L}{DCR} = \left(\frac{R_N(T) \cdot R_S}{R_N(T) + R_S}\right) \cdot C_N \quad \text{(EQ. 10)}$$

Solution of $C_N$ yields:

$$C_N = \frac{\left(\frac{L}{DCR}\right)}{\left(\frac{R_N(T) \cdot R_S}{R_N(T) + R_S}\right)} \quad \text{(EQ. 11)}$$

The first step is to adjust $R_N(T)$ and $R_S$ such that the correct current information appears between the ISP and VO pins even at light loads. Assume $V_N$ is the voltage drop across $R_N(T)$. The $V_N$ to $V_{DCR}$ gain $G_1(T)$ provides a reasonable amount of light load signal from which to derive the current information. $G_1(T)$ is given by Equation 12:

$$G_1(T) = \frac{R_N(T)}{R_N(T) + R_S} \quad \text{(EQ. 12)}$$

The gain of the current sense amplifier circuit is expressed in Equation 13:

$$K_{ISENSE} = 1 + \frac{R_{IS2}}{R_{IS1}} \quad \text{(EQ. 13)}$$

The current sense amplifier output voltage is given by Equation 14:

$$V_{ICOMP} = V_O + V_N \cdot K_{ISENSE} \quad \text{(EQ. 14)}$$

The inductor DCR is a function of temperature T and is approximated using Equation 15:

$$DCR(T) = DCR(+25°C) \cdot (1 + 0.00393 \cdot T - (+25°C)) \quad \text{(EQ. 15)}$$

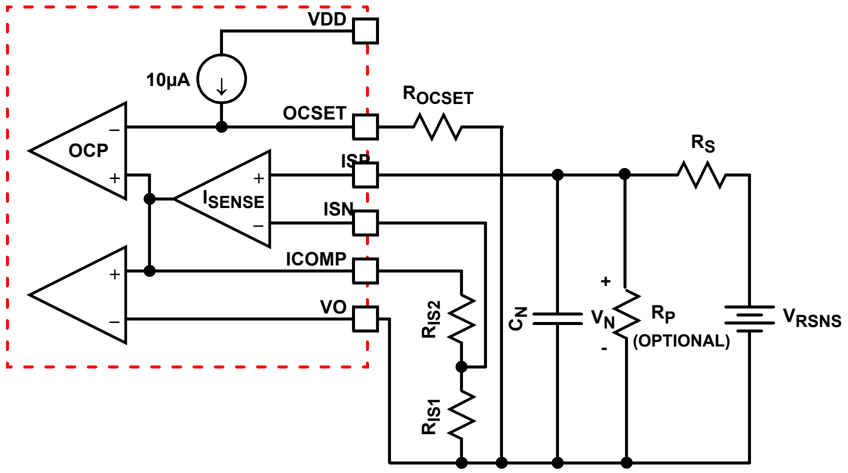


FIGURE 9. EQUIVALENT MODEL OF CURRENT SENSE USING DISCRETE RESISTOR CURRENT SENSE

0.00393 is the temperature coefficient of the copper. To make $V_{ICOMP}$ independent of the inductor temperature, the NTC characteristic is desired to satisfy:

$$G_1(T)\cdot(1+0.00393\cdot T-(+25°C)) \cong G_{1target} \qquad \text{(EQ. 16)}$$

where $G_{1target}$ is the desired ratio of $V_N/V_{DCR}$. Therefore, the temperature characteristics $G_1$, which determines parameters selection, is described by Equation 17:

$$G_1(T) = \frac{G_{1target}}{1+0.00393\cdot(T-(+25°C))} \qquad \text{(EQ. 17)}$$

It is recommended to begin the DCR current sense design using the $R_{NTC}$, $R_{NTCS}$, and $R_P$ component values of the evaluation board available from Intersil.

Given the inductor DCR and the overcurrent set point $I_{OC}$, the maximum voltage of ICOMP pin is determined by Equation 18:

$$V_{ICOMP(max)} - V_O = I_{OC}\cdot DCR(25°C)\cdot\frac{R_N(+25°C)}{R_N(+25°C)+R_S}\cdot\left(1+\frac{R_{IS2}}{R_{IS1}}\right) \qquad \text{(EQ. 18)}$$

$R_N$, $R_S$, $R_{IS1}$, $R_{IS2}$ should be adjusted to meet the requirement ($V_{ICOMP(max)}$ - $V_O$) > 25mV and the time constant matching according to Equation 10.

The effectiveness of the $R_N$ network is sensitive to the coupling coefficient between the NTC thermistor and the inductor. The NTC thermistor should be placed in the closet proximity of the inductor.

### *Resistor Current Sense*

Figure 3 shows a detailed schematic using discrete resistor sense of the inductor current. Figure 9 shows the equivalent circuit. Since the current sense resistor voltage represents the actual inductor current information, $R_S$ and $C_N$ simply provide noise filtering. A low ESL sense resistor is strongly recommended for $R_{SNS}$ because this parameter is the most significant source of noise that affects discrete resistor sense. It is recommended to start out using 100Ω for $R_S$ and 47pF for $C_N$. Since the current sense resistance changes very little with temperature, the NTC network is not needed for thermal compensation. Discrete resistor sense design follows the same approach as DCR sense. The voltage on the current sense resistor is given by Equation 19:

$$V_{RSNS} = I_O\cdot R_{SNS} \qquad \text{(EQ. 19)}$$

It is optional to parallel a resistor $R_P$ to form a voltage divider with $R_S$ to obtain more flexibility. Assume the voltage across $R_P$ is $V_N$, which is given by Equation 20:

$$V_N = V_{RSNS}\cdot\frac{R_P}{R_S+R_P} \qquad \text{(EQ. 20)}$$

The current sense amplifier output voltage $V_{ICOMP}$ is given by Equation 21:

$$V_{ICOMP} = V_O+V_N\cdot\left(1+\frac{R_{IS2}}{R_{IS1}}\right) \qquad \text{(EQ. 21)}$$

Given an current sense resistor $R_{SNS}$ and the overcurrent set point $I_{OC}$, the maximum voltage of ICOMP pin is determined by Equation 22:

$$V_{ICOMP(max)} - V_O = I_{OC}\cdot R_{SNS}\cdot\frac{R_P}{R_S+R_P}\cdot\left(1+\frac{R_{IS2}}{R_{IS1}}\right) \qquad \text{(EQ. 22)}$$

If $R_P$ is not used, the maximum voltage of ICOMP pin is determined by Equation 23:

$$V_{ICOMP(max)} - V_O = I_{OC}\cdot R_{SNS}\cdot\left(1+\frac{R_{IS2}}{R_{IS1}}\right) \qquad \text{(EQ. 23)}$$

$R_S$, $R_P$, $R_{IS1}$, $R_{IS2}$ should be adjusted to meet the requirement ($V_{ICOMP(max)}$ - $V_O$) > 25mV.

The current sense traces should be routed directly to the current sense resistor pads for accurate measurement. However, due to layout imperfection, the calculated $R_{IS2}$ may still need slight adjustment to achieve optimum load line slope. It is recommended to adjust $R_{IS2}$ after the system has achieved thermal equilibrium at full load.

### Dynamic Mode of Operation - Compensation Parameters

Intersil provides a spreadsheet to calculate the compensator parameters. Caution needs to be used in choosing the input resistor to the FB pin. Excessively high resistance will cause an error to the output voltage regulation due to the bias current flowing through the FB pin. It is recommended to keep this resistor below 3kΩ.

## Layout Considerations

As a general rule, power should be on the bottom layer of the PCB and weak analog or logic signals are on the top layer of the PCB. The ground-plane layer should be adjacent to the top layer to provide shielding.

### Inductor Current Sense and the NTC Placement

It is crucial that the inductor current be sensed directly at the PCB pads of the sense element, be it DCR sensed or discrete resistor sensed. The effect of the NTC on the inductor DCR thermal drift is directly proportional to its thermal coupling with the inductor and thus, the physical proximity to it.

### Signal Ground and Power Ground

The ground plane layer should have a single point connection to the analog ground at the VSS pin. The VSS island should be located under the IC package along with the weak analog traces and components. The paddle on the bottom of the ISL6263C QFN package is not electrically connected to the IC, however, it is recommended to make a good thermal connection to the VSS island using several vias. Connect the input capacitors, the output capacitors, and the source of the lower MOSFETs to the power ground plane.

### LGATE, PVCC, and PGND

PGND is the return path for the pull-down of the LGATE low-side MOSFET gate driver. Ideally, PGND should be connected to the source of the low-side MOSFET with a low-resistance, low-inductance path. The LGATE trace should be routed in parallel with the trace from the PGND pin. These two traces should be short, wide, and away from other traces because of the high peak current and extremely fast dv/dt. PVCC should be decoupled to PGND with a ceramic capacitor physically located as close as practical to the IC pins.

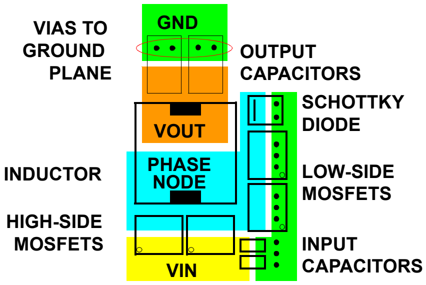


FIGURE 10. TYPICAL POWER COMPONENT PLACEMENT

### UGATE, BOOT, and PHASE

PHASE is the return path for the entire UGATE high-side MOSFET gate driver. The layout for these signals require similar treatment, but to a greater extent, than those for LGATE, PVCC, and PGND. These signals swing from approximately VIN to VSS and are more likely to couple into other signals.

### VSEN and RTN

These traces should be laid out as noise sensitive. For optimum load line regulation performance, the traces connecting these two pins to the Kelvin sense leads of the processor should be laid out away from rapidly rising voltage nodes, (switching nodes) and other noisy traces. The filter capacitors $C_{FILTER1}$, $C_{FILTER2}$, and $C_{FILTER3}$ used in conjunction with filter resistors $R_{FILTER1}$ and $R_{FILTER2}$ form common mode and differential mode filters, as shown in Figure 8. The noise environment of the application and actual board layout conditions will drive the extent of filter complexity. The maximum recommended resistance for $R_{FILTER1}$ and $R_{FILTER2}$ is approximately 10Ω to avoid interaction with the 50kΩ input resistance of the remote sense differential amplifier. The physical location of these resistors is not as critical as the filter capacitors. Typical capacitance values for $C_{FILTER1}$, $C_{FILTER2}$, and $C_{FILTER3}$ range between 330pF to 1000pF and should be placed near the IC.

### RBIAS

The resistor $R_{RBIAS}$ should be placed in close proximity to the ISL6263C using a noise-free current return path to the VSS pin.

### IMON, SOFT, OCSET, V W, COMP, FB, VDIFF, ICOMP, ISP, ISN and VO

The traces and components associated with these pins require close proximity to the IC as well as close proximity to each other. This section of the converter circuit needs to be located above the island of analog ground with the single-point connection to the VSS pin.

### Resistor $R_S$

Resistor $R_S$ is preferably located near the boundary between the power ground and the island of analog ground connected to the VSS pin.

### VID<0:4>, AF_EN, PGOOD, and VR_ON

These are logic signals that do not require special attention.

### FDE

This logic signal should be treated as noise sensitive and should be routed away from rapidly rising voltage nodes, (switching nodes) and other noisy traces.

### VIN

The VIN signal should be connected near the drain of the high-side MOSFET.

### Copper Size for the Phase Node

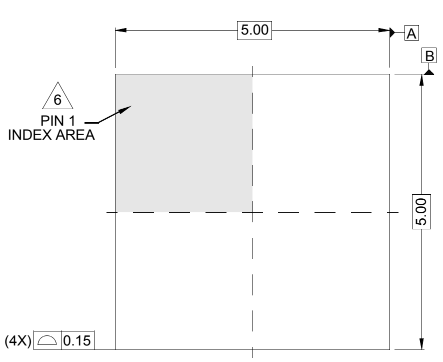
The parasitic capacitance and parasitic inductance of the phase node should be kept very low to minimize ringing. It is best to limit the size of the PHASE node copper in strict accordance with the current and thermal management of the application. An MLCC should be connected directly across the drain of the high-side MOSFET and the source of the low-side MOSFET to suppress turn-off voltage spikes.

# Package Outline Drawing

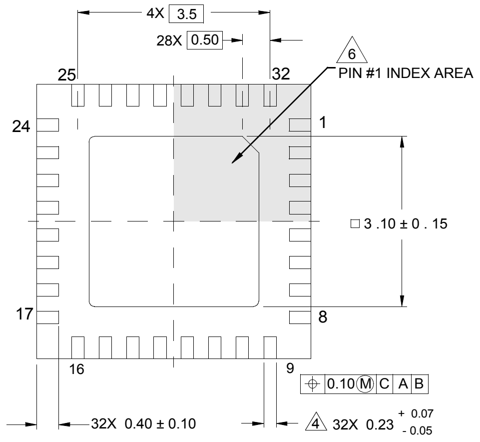
## L32.5x5

**32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE**

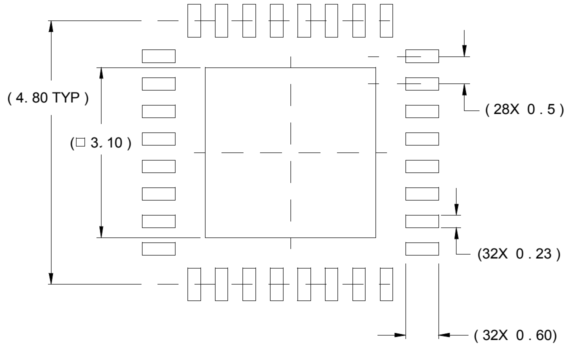
**Rev 2, 02/07**



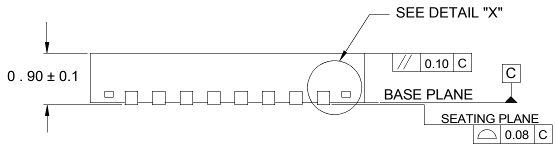
TOP VIEW



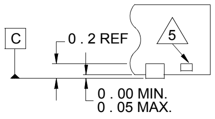
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.