ISL59451

Triple 4:1 DC Restored Single Supply Video Multiplexing Amplifier

FN6253
Rev 0.00
September 24, 2007

The ISL59451 is a 4-input, single-supply triple video multiplexer. It features a DC restore function that makes it ideally suited for single-supply AC-coupled component video applications where amplifier headroom is a concern.

When logic “0” is applied to $\overline{\text{CLAMP}}$, the sample-hold amplifier loop is closed and the DC level of the amplifier output is set to the corresponding reference level. This can occur during sync, or at any time that a black level is expected. When logic “1” is applied to $\overline{\text{CLAMP}}$, the clamp is disabled and the correcting voltage is stored on each video amplifier’s input coupling capacitor. This DC reference condition is maintained during the active video period. The restored DC voltage level can be adjusted over a range of 0V to +3V using external reference voltages applied to the REF_G and REF_RB pins.

The device features a TTL/CMOS logic compatible gain select pin (AV2) of x1 or x2. When HIZ is pulled high, the outputs are put into high-impedance states and the video inputs are disconnected. This is an essential feature for power sensitive applications. The ISL59451 also features channel-switching at pixel rates to allow for video overlays.

The ISL59451 operates from a single +5V supply and is ideal for +5V systems when used with sync separators such as the EL1883. The red and blue channels share a common reference pin (REF_RB) which can also be used to adjust chroma offsets in YPbPr systems. The green channel has a separate reference pin (REF_G), which can be used to accommodate sync-on-green or luma.

The ISL59451 is comes in a 32 Ld QFN package and is specified for operation over the -40°C to +85°C extended temperature range.

Ordering Information

PART NUMBER (Note)	PART MARKING	PACKAGE (Pb-Free)	PKG. DWG. #
ISL59451IRZ	ISL594 51IRZ	32 Ld 5x5 QFN	L32.5x5
ISL59451IRZ-T7*	ISL594 51IRZ	32 Ld 5x5 QFN	L32.5x5

*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

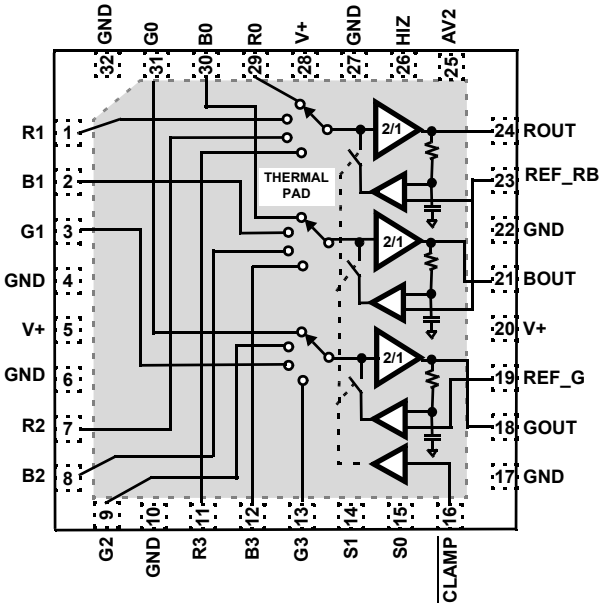
- Complete Video Level DC Restoration System
- 250MHz Bandwidth (GAIN = 1)
- +5V Single Supply Operation
- Capable of Pixel Rate Channel Switching
- TTL/CMOS Compatible Keyed Clamp Control
- High Impedance Output Setting
- 150Ω Output Load Capability for Video Cable Driving
- Ideal for RGB/YPbPr/S-Video/Composite Video Signals
- Pb-Free (RoHS Compliant)

Applications

- SDTVs and HDTVs
- Set-Top Boxes
- Video Overlay
- Security Video
- Broadcast Video Equipment

Pinout

ISL59451
(32 LD QFN)
TOP VIEW



Exposed Thermal Pad (Gray Area) must be connected to GND.

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage (V+ to GND) 5.5V
Input Voltage to GND . . . . . .GND - 0.5V to V+ +0.5V
Voltage between HIZ, $\overline{CLAMP}$, AV2, REF_ and GND
. . . . . .GND - 0.5;V+ +0.5V
Supply Turn-on Slew Rate 1V/µs
Digital and Analog Input Current (Note 1) 50mA
Output Current (Continuous) 50mA
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7). . . .2500V
Machine Model 300V

Thermal Information

Storage Temperature Range . . . . . .-65°C to +150°C
Ambient Operating Temperature . . . . . .-40°C to +85°C
Operating Junction Temperature . . . . . .-40°C to +125°C
Power Dissipation . . . . . .See Curves
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

1. If an input signal is applied before the supplies are powered up, the input current must be limited to these maximum values.
2. Parts are 100% tested at +25°C. Over-temperature limits established by characterization and are not production tested.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V+ = +5V, GND = 0V, T_A = +25°C, R_L = 150Ω to GND, REF_G = 0.5V, REF_RB = 1.2V, $\overline{CLAMP}$ = 2.0V, S1 = S0 = AV2 = HIZ = 0.8V, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNIT
DC CHARACTERISTICS						
V+	Supply Voltage		4.5	5.0	5.5	V
$+I_S$ Enabled	Enabled Supply Current	No load, V_{IN} = 2.2V, HIZ = 0.8V		45	75	mA
$+I_S$ Disabled	Disabled Supply Current	No load, V_{IN} = 2.2V, HIZ = 2.0V		3	5	mA
V_{SHIFT}	Input to Output Level Shift (V_{IN} - V_{OUT})	DC-coupled inputs, V_{IN} = 2V, GAIN = 1	1.2	1.6	2	V
I_B	Input Bias Current	V_{IN} = 2.2V, No Load	-1	0	1	µA
R_{OUT_DIS}	Disabled Output Resistance (DC)	HIZ = 2.0V	1.4	2	2.6	kΩ
A_V	Voltage Gain	AV2 = 0.8V, GAIN = 1	0.98	1	1.02	V/V
		AV2 = 2.0V, GAIN = 2	1.95	2.00	2.05	V/V
$PSRR_{DC}$	DC Power Supply Rejection Ratio	V+ = 4.5V to 5.5V, $\overline{CLAMP}$ = 2.0V, V_{IN} = 2.0V	40	50		dB
		V+ = 4.5V to 5.5V, $\overline{CLAMP}$ = 0.8V, inputs floating	50	65		dB
OUTPUT AMPLIFIERS						
V_{OUT+}	Maximum Output High Level	R_L = 150Ω, V_{IN} = 4V, GAIN = 2	3.5			V
V_{OUT-}	Minimum Output Low Level	R_L = 150Ω,V_{IN} = 0.8V, GAIN = 2			15	mV
I_{SC}	Short Circuit Current	Sourcing, V_{IN} = 4V, R_L = 10Ω to GND, GAIN = 2		125		mA
		Sinking, V_{IN} = 0V, R_L = 10Ω to +3V		57		mA
DC RESTORE SECTION						
$V_{CLAMP-OS}$	Output Clamp Accuracy (V_{OUT} - V_{REF_RB})	REF_RB = 1.2V, $\overline{CLAMP}$ = 0.8V	-15	-4	+10	mV
	Output Clamp Accuracy (V_{OUT} - V_{REF_G})	REF_G = 0.5V, $\overline{CLAMP}$ = 0.8V	-15	-3	+10	mV
I_{CLAMP}	Positive Restore Clamp Current	V_{IN} = 0V, $\overline{CLAMP}$ = 0.8V, Sourcing	500	860	1100	µA
	Negative Restore Clamp Current	V_{IN} = 4V, $\overline{CLAMP}$ = 0.8V, Sinking	150	290	500	µA
I_{B_VREF}	Reference Input Bias Current	REF_G = 0.5V or 1.2V, $V_{\overline{CLAMP}}$ = 0.8V	-2	-0.4	+0.5	µA
		REF_RB = 0.5V or 1.2V, $V_{\overline{CLAMP}}$ = 0.8V	-3	-0.9	+0.5	µA

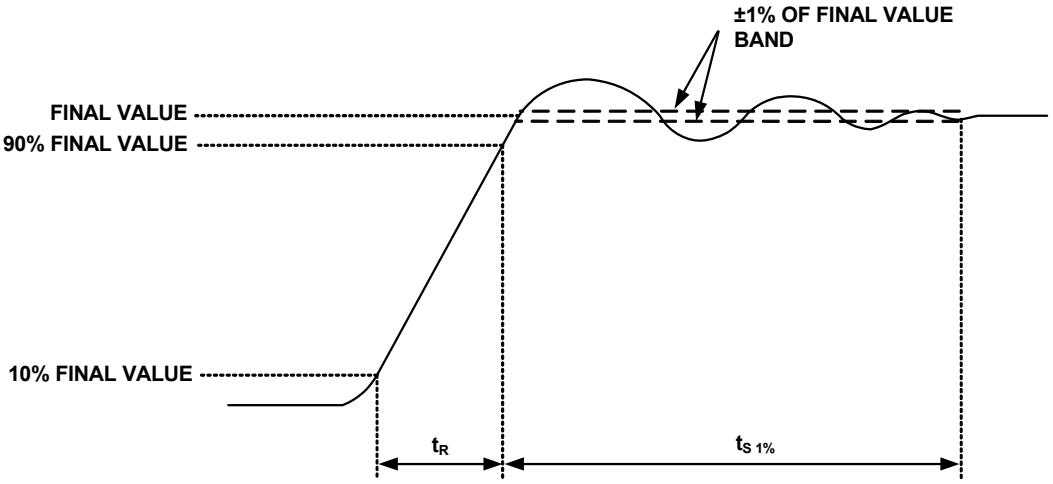
Electrical Specifications V+ = +5V, GND = 0V, T_A = +25°C, R_L = 150Ω to GND, REF_G = 0.5V, REF_RB = 1.2V, $\overline{CLAMP}$ = 2.0V, S1 = S0 = AV2 = HIZ = 0.8V, unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNIT
LOGIC ($\overline{CLAMP}$, AV2, HIZ, S1, S0)						
V_{IH}	Input High Voltage (HIGH)		2			V
V_{IL}	Input Low Voltage (LOW)				0.8	V
I_{IH}	Input High Current (Logic Inputs)	S1 = S0 = $\overline{CLAMP}$ = 5V (no pull-up or pull-down)	-1	0	+1	µA
		AV2 = HIZ= 5V (300kΩ internal pull-downs)	8	17	34	µA
I_{IL}	Input Low Current (Logic Inputs)	S1 = S0 = $\overline{CLAMP}$ = 0V (no pull-up or pull-down)	-1	0	+1	µA
		AV2 = HIZ= 5V (300kΩ internal pull-downs)	-1	0	+1	µA
AC GENERAL						
PSRR	Power Supply Rejection Ratio	V_{IN} = 2.0V, f = 10kHz to 10MHz, V+ = $5V_{DC}$ + $100mV_{P-P}$ sine wave		50		dB
X_{TALK}	Channel-to-Channel Crosstalk (ROUT/BOUT to Green Input)	f = 10MHz, V_{IN} = $0.7V_{P-P}$; (GAIN = 1)		60		dB
		f = 10MHz, V_{IN} = $0.7V_{P-P}$; (GAIN = 2)		55		dB
OFF_{CH_ISO}	De-Selected Channel Isolation (any de-selected output to driven input)	f = 10MHz, Ch-Ch Off Isolation V_{IN} = $0.7V_{P-P}$; (GAIN = 1)		94		dB
		f = 10MHz, Ch-Ch Off Isolation V_{IN} = $0.7V_{P-P}$; (GAIN = 2)		89		dB
dG	Differential Gain Error	R_L = 150		0.0025		%
dP	Differential Phase Error	R_L = 150		0.08		°
BW	Small Signal -3dB Bandwidth	V_{OUT} = $0.2V_{P-P}$; R_L = 150Ω, C_L = 0.6pF (GAIN = 1)		240		MHz
		V_{OUT} = $0.2V_{P-P}$; R_L = 150Ω, C_L = 0.6pF (GAIN = 2)		200		MHz
	Large Signal -3dB Bandwidth	V_{OUT} = $1.4V_{P-P}$; R_L = 150Ω, C_L = 0.6pF (GAIN = 1)		210		MHz
		V_{OUT} = $1.4V_{P-P}$; R_L = 150Ω, C_L = 0.6pF (GAIN = 2)		200		MHz
BW_0.1	0.1dB Bandwidth	V_{OUT} = $1.4V_{P-P}$; R_L = 150Ω, C_L = 0.6pF (GAIN = 1)		30		MHz
		V_{OUT} = $1.4V_{P-P}$; R_L = 150Ω, C_L = 0.6pF (GAIN = 2)		30		MHz
SR+	Positive Slew Rate	V_{IN} = 1.8 to 2.8V, time = 10% to 90%, R_L = 150Ω, GAIN = 1		500		V/µs
		V_{IN} = 1.8 to 2.3V, time = 10% to 90%, R_L = 150Ω, GAIN = 2		930		V/µs
SR-	Negative Slew Rate	V_{IN} = 2.8 to 1.8V, time = 90% to 10%, R_L = 150Ω, GAIN = 1		300		V/µs
		V_{IN} = 2.3 to 1.8V, time = 90% to 10%, R_L = 150Ω, GAIN = 2		600		V/µs
TRANSIENT RESPONSE						
t_R	Rise Time 10% to 90%	V_{OUT} = $0.7V_{P-P}$; R_L = 150Ω, C_L = 2.1pF, GAIN = 1		1.3		ns
		V_{OUT} = $1.4V_{P-P}$; R_L = 150Ω, C_L = 2.1pF, GAIN = 2		2		ns
t_F	Fall Time 90% to 10%	V_{OUT} = $0.7V_{P-P}$; R_L = 150Ω, C_L = 2.1pF, GAIN = 1		2.6		ns
		V_{OUT} = $1.4V_{P-P}$; R_L = 150Ω, C_L = 2.1pF, GAIN = 2		2.3		ns
$t_{S\ 1\%}$	Settling Time to 1%	V_{OUT} = $1V_{P-P}$; R_L = 150Ω, C_L = 2.1pF, GAIN = 1, time from 90% crossing to 1% of final value		2		ns
		V_{OUT} = $1V_{P-P}$; R_L = 150Ω, C_L = 2.1pF, GAIN = 2, time from 90% crossing to 1% of final value		4		ns

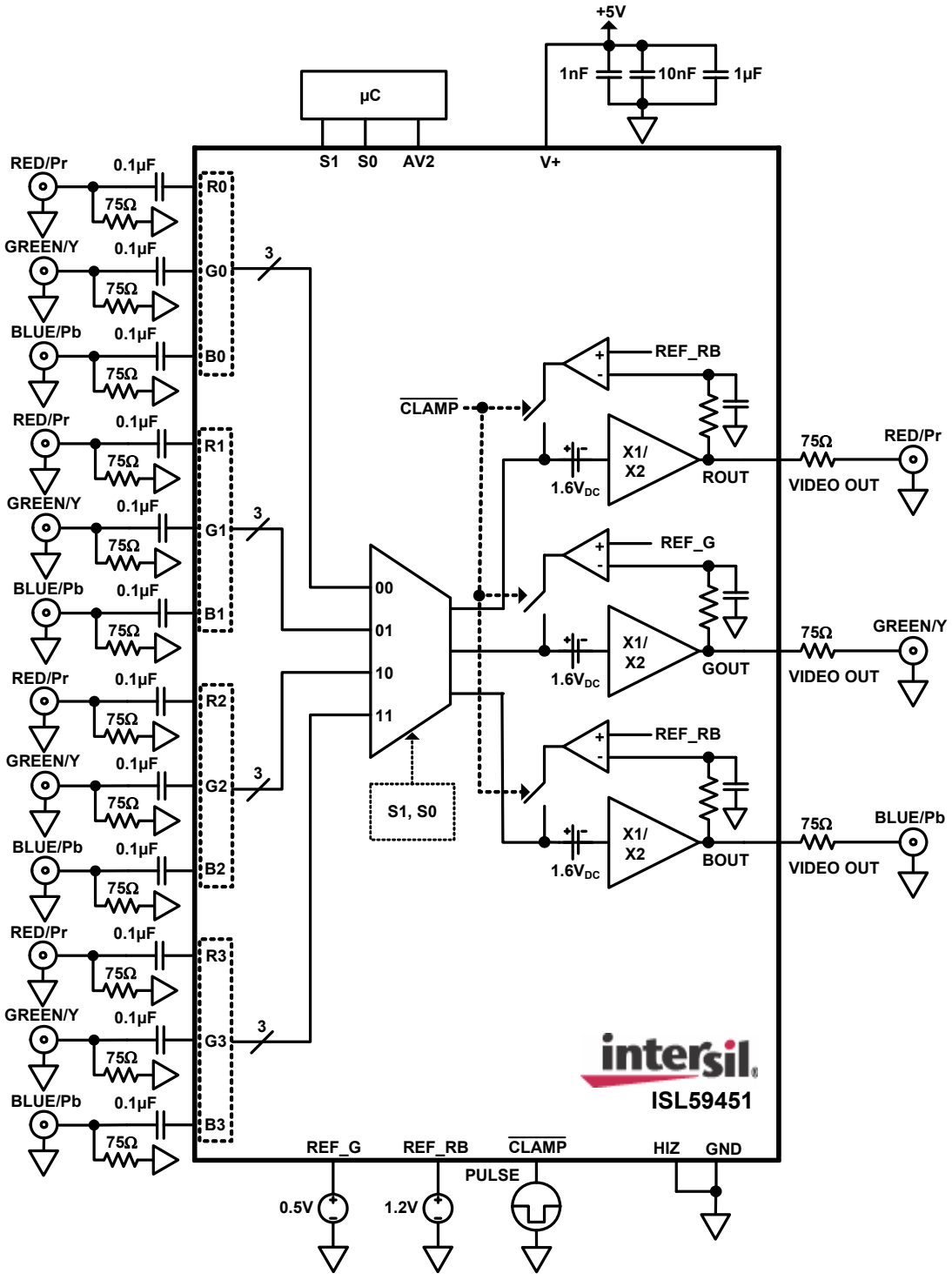
Electrical Specifications V+ = +5V, GND = 0V, T_A = +25°C, R_L = 150Ω to GND, REF_G = 0.5V, REF_RB = 1.2V, $\overline{CLAMP}$ = 2.0V, S1 = S0 = AV2 = HIZ = 0.8V, unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNIT
SWITCHING CHARACTERISTICS						
V_{GLITCH}	HIZ High to Low Switching Glitch	V_{IN} = 1V, R_L = 150Ω; C_L = 2.1pF, GAIN = 1		500		mV_{P-P}
		V_{IN} = 1V, R_L = 150Ω; C_L = 2.1pF, GAIN = 2		300		mV_{P-P}
t_{SW-L-H}	Channel Switching Delay Time Low to High	1.2V logic threshold to 10% movement of analog output		3		ns
t_{SW-H-L}	Channel Switching Delay Time High to Low	1.2V logic threshold to 10% movement of analog output		4		ns
$t_{HIZ-L-H}$	HIZ Switching Delay Time Low to High	1.2V logic threshold to 10% movement of analog output		25		ns
$t_{HIZ-H-L}$	HIZ Switching Delay Time High to Low	1.2V logic threshold to 10% movement of analog output		220		ns
tpd	Propagation Delay	10% input to 10% output		2.5		ns
t_{HE}	Time to Enable $\overline{CLAMP}$	$\overline{CLAMP}$ = LOW to settled output		40		ns
t_{HD}	Time to Disable $\overline{CLAMP}$	$\overline{CLAMP}$ = HIGH to settled output		20		ns

Settling Time Diagram



Typical Application Circuit



Typical Performance Curves V_{CC} = +5V, R_L = 150Ω to GND, T_A = +25°C, unless otherwise specified.

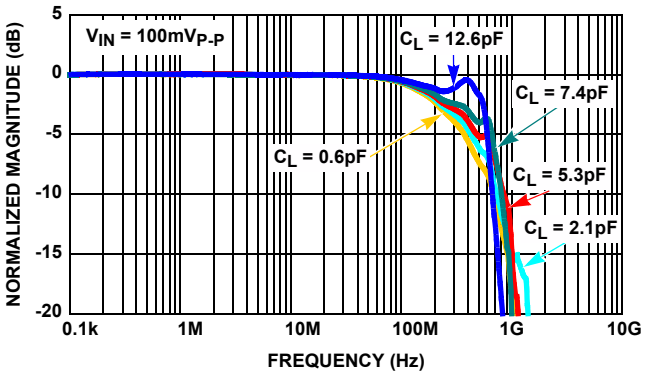


FIGURE 1. SMALL SIGNAL GAIN vs FREQUENCY vs C_L INTO 150Ω LOAD, GAIN = 1

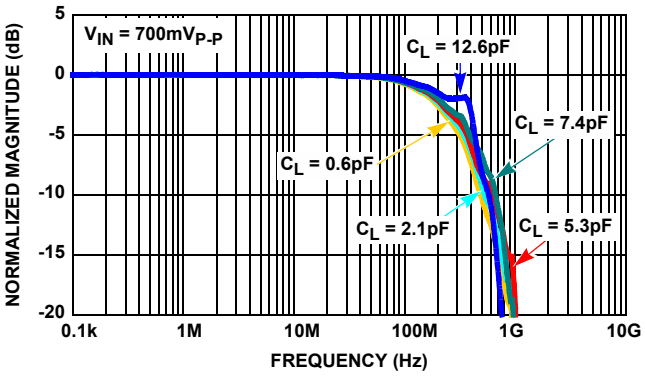


FIGURE 2. LARGE SIGNAL GAIN vs FREQUENCY vs C_L INTO 150Ω LOAD, GAIN = 1

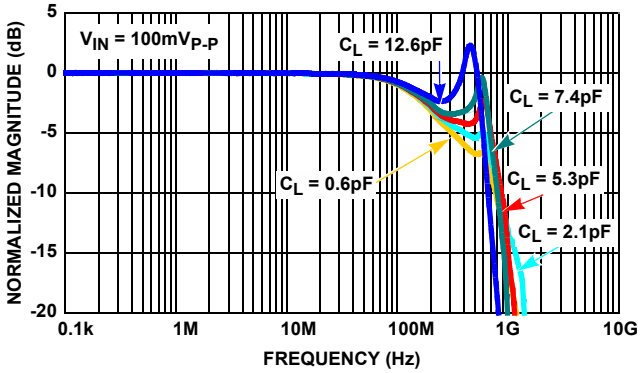


FIGURE 3. SMALL SIGNAL GAIN vs FREQUENCY vs C_L INTO 150Ω LOAD, GAIN = 2

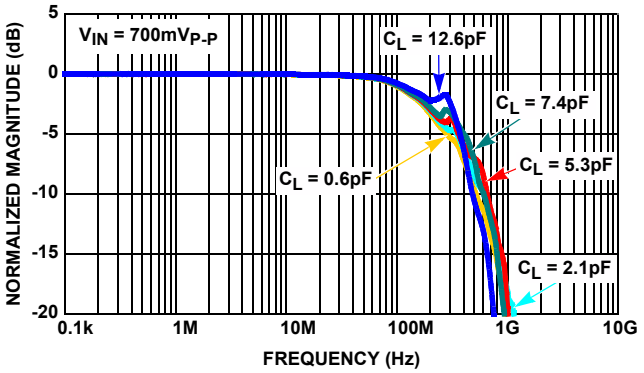


FIGURE 4. LARGE SIGNAL GAIN vs FREQUENCY vs C_L INTO 150Ω LOAD, GAIN = 2

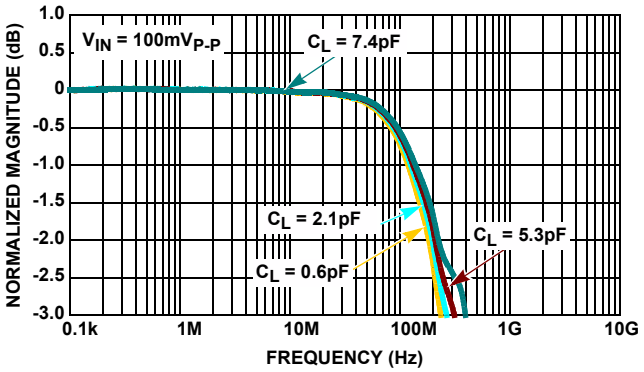


FIGURE 5. SMALL SIGNAL GAIN FLATNESS, GAIN = 1

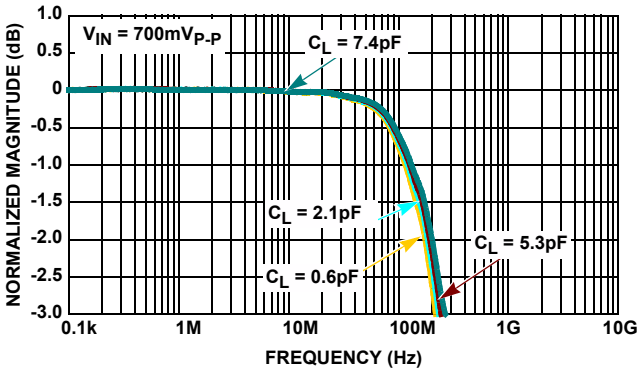


FIGURE 6. LARGE SIGNAL GAIN FLATNESS, GAIN = 1

Typical Performance Curves V_{CC} = +5V, R_L = 150Ω to GND, T_A = +25°C, unless otherwise specified. **(Continued)**

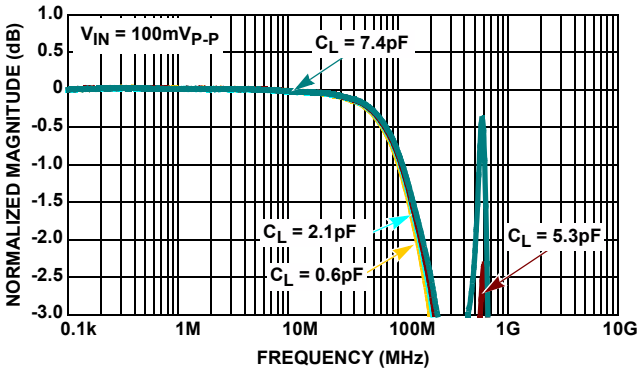


FIGURE 7. SMALL SIGNAL GAIN FLATNESS, GAIN = 2

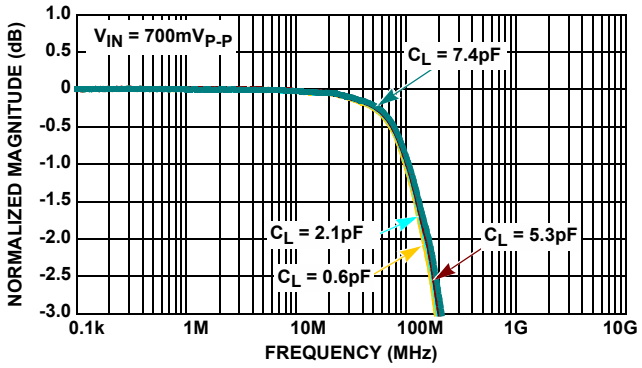


FIGURE 8. LARGE SIGNAL GAIN FLATNESS, GAIN = 2

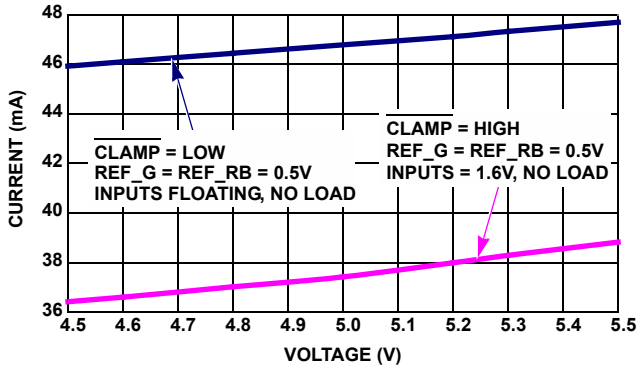


FIGURE 9. SUPPLY CURRENT vs SUPPLY VOLTAGE

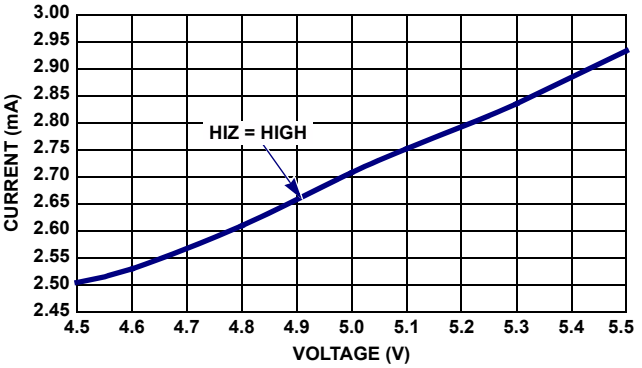


FIGURE 10. DISABLED SUPPLY CURRENT vs SUPPLY VOLTAGE

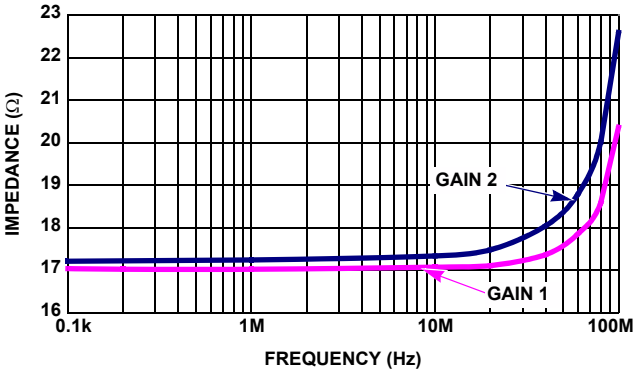


FIGURE 11. Z_{OUT} vs FREQUENCY - ENABLED

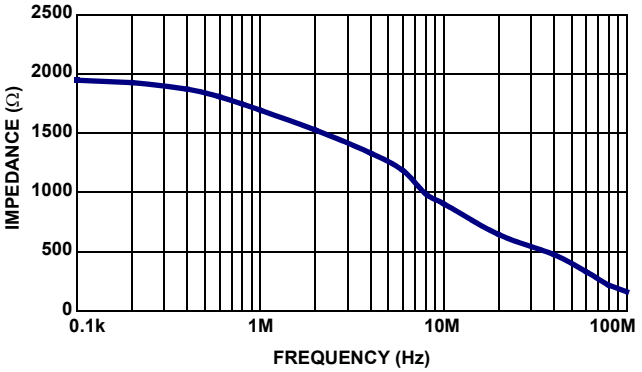


FIGURE 12. Z_{OUT} vs FREQUENCY - DISABLED

Typical Performance Curves V_{CC} = +5V, R_L = 150Ω to GND, T_A = +25°C, unless otherwise specified. **(Continued)**

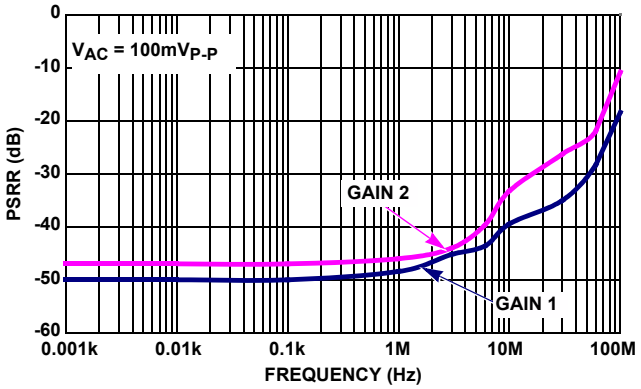


FIGURE 13. PSRR vs FREQUENCY

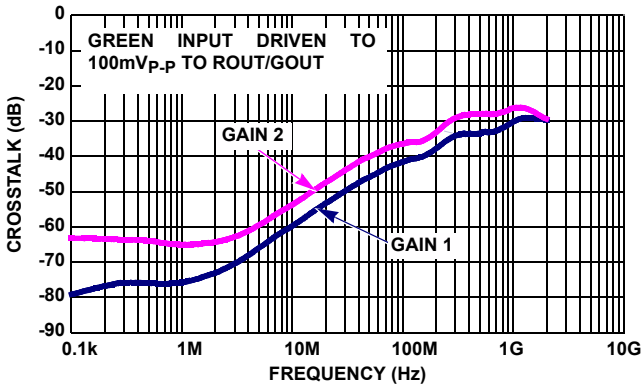


FIGURE 14. ACTIVE CHANNEL CROSSTALK

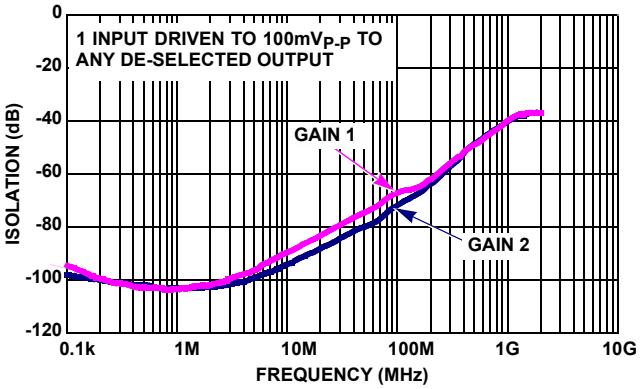


FIGURE 15. DE-SELECTED CHANNEL OFF ISOLATION

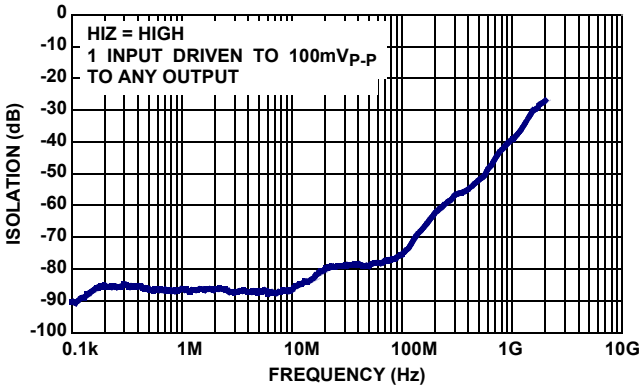


FIGURE 16. DISABLED ISOLATION

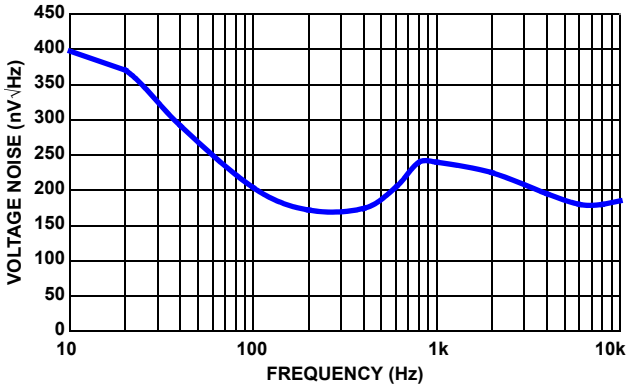


FIGURE 17. INPUT REFERRED NOISE vs FREQUENCY

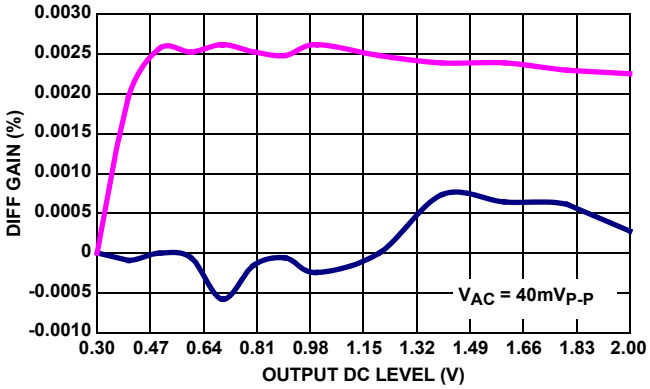


FIGURE 18. DIFFERENTIAL GAIN; f_O = 3.58MHz, R_L = 150Ω

Typical Performance Curves V_{CC} = +5V, R_L = 150Ω to GND, T_A = +25°C, unless otherwise specified. **(Continued)**

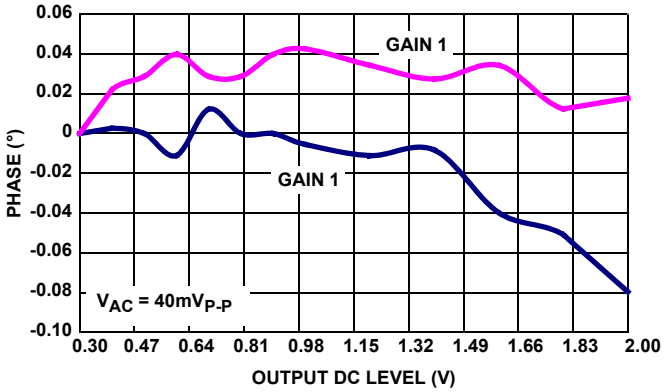


FIGURE 19. DIFFERENTIAL PHASE; f_O = 3.58MHz, R_L = 150Ω

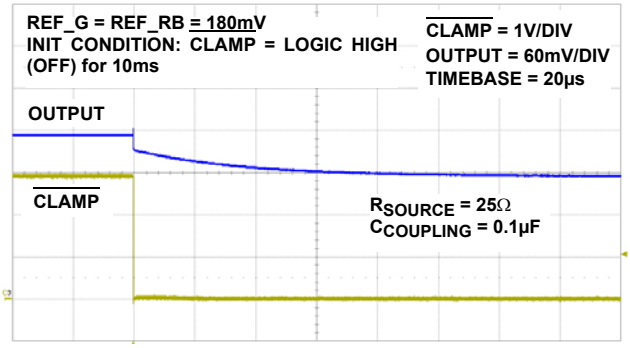


FIGURE 20. DC RESTORE SETTLING TIME

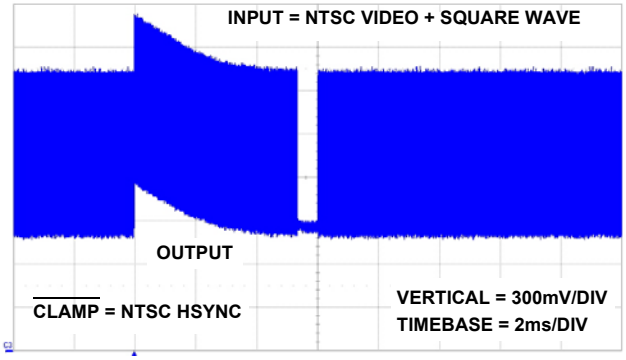


FIGURE 21. RESPONSE TO +300mV DC STEP ON INPUT (SEE FIGURE 36)

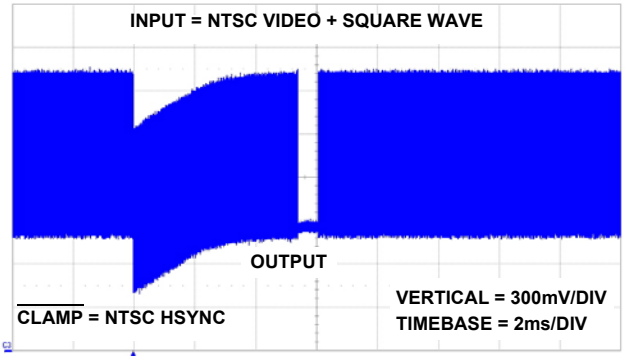


FIGURE 22. RESPONSE TO -300mV DC STEP ON INPUT (SEE FIGURE 36)

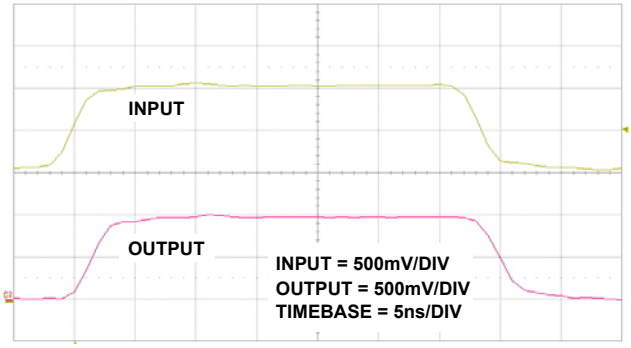


FIGURE 23. PULSE RESPONSE, GAIN = 1

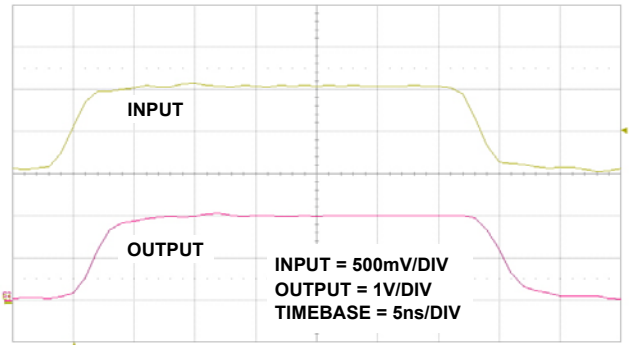


FIGURE 24. PULSE RESPONSE, GAIN = 2

Typical Performance Curves V_{CC} = +5V, R_L = 150Ω to GND, T_A = +25°C, unless otherwise specified. **(Continued)**

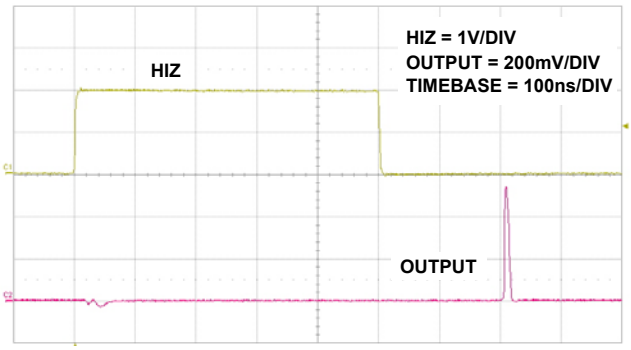


FIGURE 25. HIZ SWITCHING GLITCH, V_{IN} = 0V, GAIN = 1

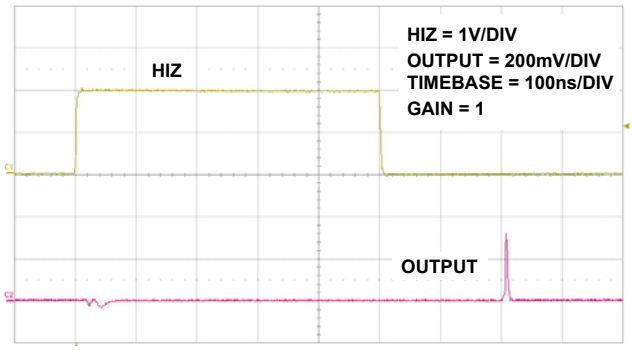


FIGURE 26. HIZ SWITCHING GLITCH, V_{IN} = 0V, GAIN = 2

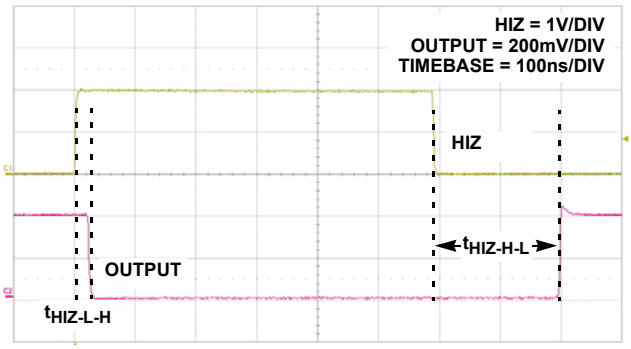


FIGURE 27. HIZ SWITCH TIMING, V_{IN} = 1V_{DC}

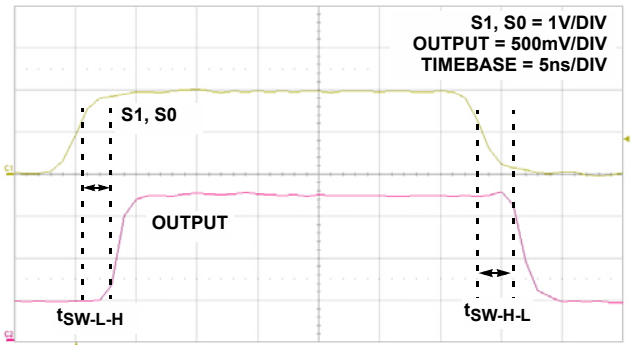


FIGURE 28. CHANNEL TO CHANNEL SWITCHING TIME, V_{IN} = 1V_{DC}

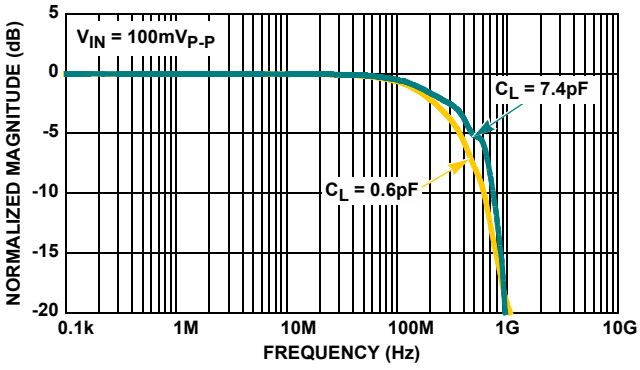


FIGURE 29. SMALL SIGNAL GAIN vs FREQUENCY vs C_L INTO 75Ω LOAD, GAIN = 1

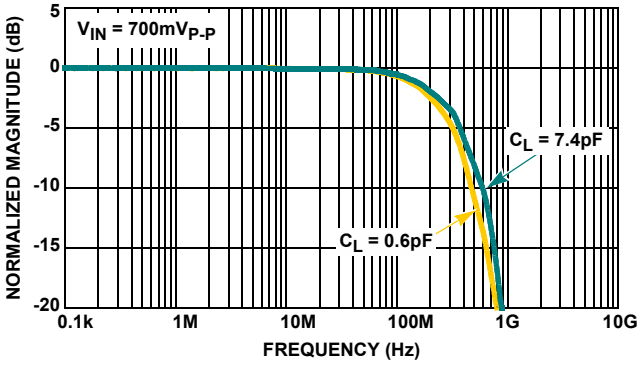


FIGURE 30. LARGE SIGNAL GAIN vs FREQUENCY vs C_L INTO 75Ω LOAD, GAIN = 2

Typical Performance Curves V_{CC} = +5V, R_L = 150Ω to GND, T_A = +25°C, unless otherwise specified. **(Continued)**

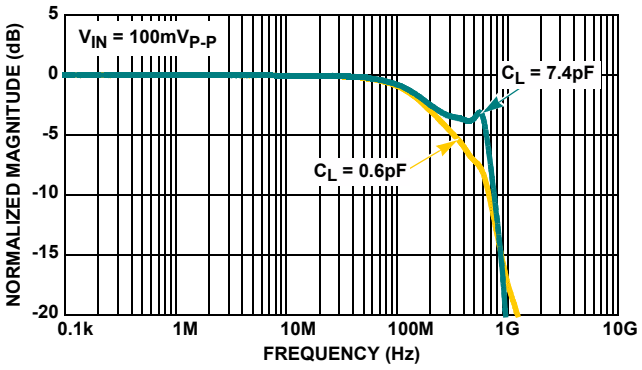


FIGURE 31. SMALL SIGNAL GAIN vs FREQUENCY vs C_L INTO 75Ω LOAD, GAIN = 2

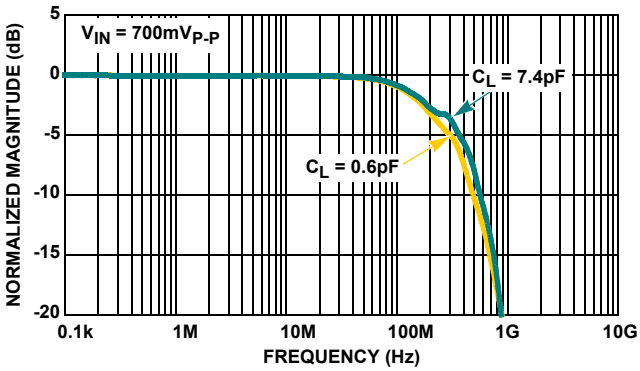


FIGURE 32. LARGE SIGNAL GAIN vs FREQUENCY vs C_L INTO 75Ω LOAD, GAIN = 2

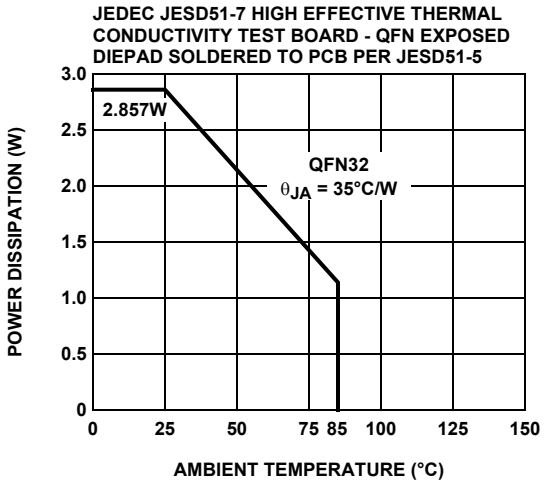


FIGURE 33. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

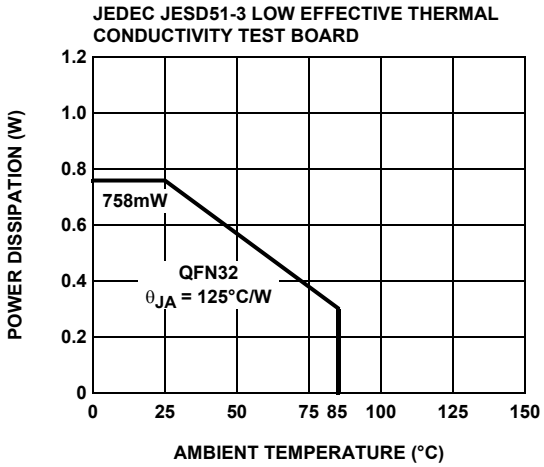


FIGURE 34. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Functional Block Diagram

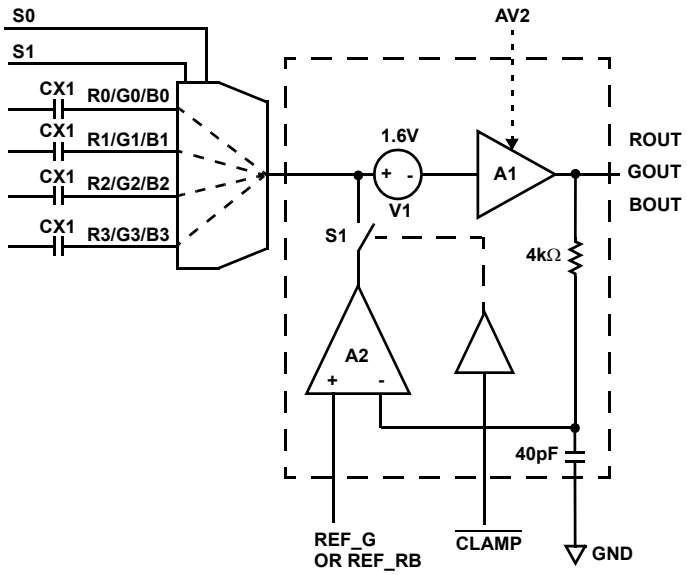


TABLE 1. CHANNEL SELECT LOGIC TABLE

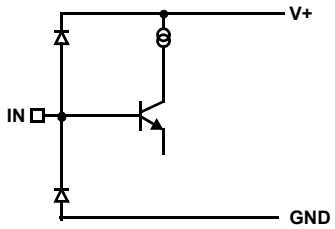
S1	S0	HIZ	OUTPUT
0	0	0	R0, G0, B0
0	1	0	R1, G1, B1
1	0	0	R2, G2, B2
1	1	0	R3, G3, B3
X	X	1	High Impedance, Inputs Disconnected

Pin Descriptions

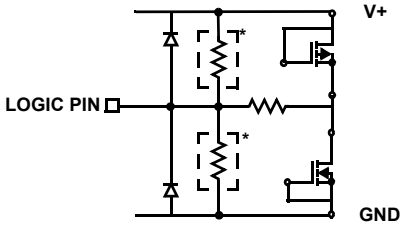
ISL59451 (32 LD QFN)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
1	R1	Circuit 1	Channel 1 Red/Pr/Chroma Input
2	B1	Circuit 1	Channel 1 Blue/Pb/Chroma Input
3	G1	Circuit 1	Channel 1 Green/Luma Input
4, 6, 10, 17, 22, 27, 32	GND	Circuit 4	Ground
5, 20, 28	V+	Circuit 4	Positive Supply. Bypass to GND with 0.01µF and 1nF capacitors.
7	R2	Circuit 1	Channel 2 Red/Pr/Chroma Input
8	B2	Circuit 1	Channel 2 Blue/Pb/Chroma Input
9	G2	Circuit 1	Channel 2 Green/Luma Input
11	R3	Circuit 1	Channel 3 Red/Pr/Chroma Input
12	B3	Circuit 1	Channel 3 Blue/Pb/Chroma Input
13	G3	Circuit 1	Channel 3 Green/Luma Input
14	S1	Circuit 2	Channel selection pin MSB (binary logic code). This pin does not have internal pull-up or pull-down resistors.
15	S0	Circuit 2	Channel selection pin. LSB (binary logic code). This pin does not have internal pull-up or pull-down resistors.
16	$\overline{\text{CLAMP}}$	Circuit 2	Clamp/Store Logic Input. Logic ‘0’ selects the clamp DC restore state, logic ‘1’ selects the hold state. This pin does not have internal pull-up or pull-down resistors.
18	GOUT	Circuit 3	Green/Luma Output
19	REF_G		Green/Luma Reference. Green/Luma channel offset by this voltage during DC restore state. Reference voltage range is 0 to +3.0V.
21	BOUT	Circuit 3	Blue Output
23	REF_RB		Red and Blue Reference. Red and blue channels offset by this voltage during DC restore state. Reference voltage range is 0 to +3.0V.
24	ROUT	Circuit 3	Red Output
25	AV2	Circuit 2	Gain Set. Set to logic high for gain of x2 (+6dB), or set to logic low for a gain of x1 (+0dB). If left floating, an internal pull-down resistor pulls this pin low (300kΩ pull-down).

Pin Descriptions (Continued)

ISL59451 (32 LD QFN)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
26	HIZ	Circuit 2	Output disable (active high). Internal pull-down resistor ensures the device will be active with no connection to this pin. A logic high puts the outputs in a high impedance state. Use this state to control logic when more than one MUX-amp share the same video output line. During high impedance state, there is a 2kΩ pull-down present at each output. If left floating, an internal pull-down resistor pulls this pin low (300kΩ pull-down).
29	R0	Circuit 1	Channel 0 Red/Pr/Chroma Input
30	B0	Circuit 1	Channel 0 Blue/Pb/Chroma Input
31	G0	Circuit 1	Channel 0 Green/Luma Input
-	EP		Exposed Pad. Connect to GND

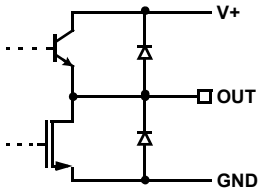


CIRCUIT 1

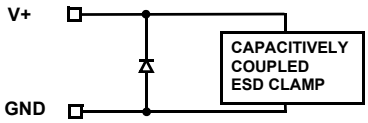


CIRCUIT 2

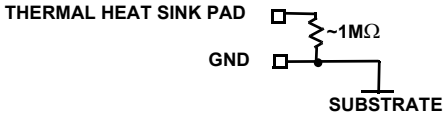
*Not Always Present.
Refer to "Pin Description"



CIRCUIT 3



CIRCUIT 4



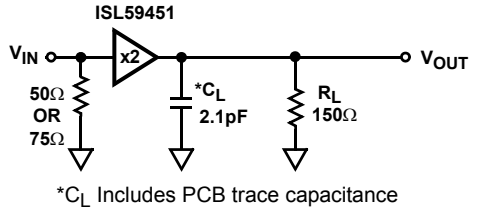


FIGURE 35A. TEST CIRCUIT WITH OPTIMAL OUTPUT LOAD

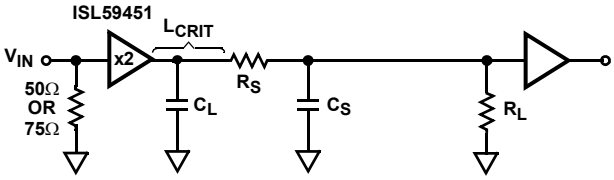


FIGURE 35B. INTER-STAGE APPLICATION CIRCUIT

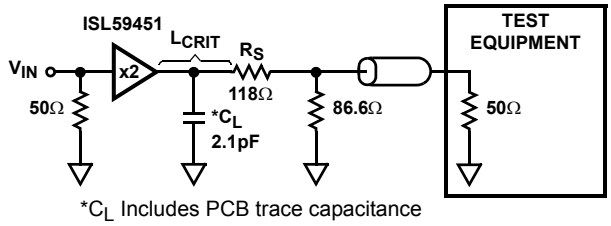


FIGURE 35C. 150Ω TEST CIRCUIT WITH 50Ω LOAD

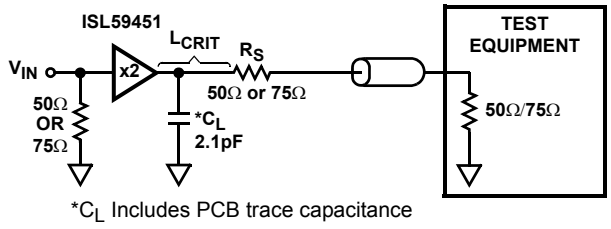


FIGURE 35D. BACKLOADED TEST CIRCUIT FOR 50Ω/75Ω VIDEO CABLE APPLICATION

FIGURE 35. AC TEST CIRCUITS

AC Test Circuits

Figures 35A and 35B illustrate the optimum output load for testing AC performance at 150Ω loads. Figure 35C illustrates how to use the optimal 150Ω load for a 50Ω cable. Figure 35D illustrates the optimum output load for 50Ω and 75Ω cable-driving.

Application Information

General

The ISL59451 triple 4:1 MUX video driver features single +5V supply operation, high bandwidth and TTL/CMOS logic compatible gain select (AV2) of x1 (0dB) or x2 (+6dB). It also includes a DC restore function to set the blanking level of the output signal.

The ISL59451 implements the video DC-restore function with a high performance gain-adjustable video amplifier and a nulling, sample-hold amplifier to establish a user defined DC reference voltage at the video amplifier output. A detailed description of the DC-restore function implemented in the ISL59451 can be found in application note AN1089, EL4089 and EL4390 DC-Restored Video Amplifier. The ISL59451 performs the same function with the exception that it is designed for single supply operation. Each of the three output channels feature DC restore functionality.

Video Amplifier Operation

(refer to "Functional Block Diagram" on page 12)

The ISL59451 video amplifier (A1) is a voltage-feed, high performance video amplifier designed for +5V operation. The output stage is capable of swinging to within 15mV of the negative rail. The differential input stage contains an internal voltage reference that positions the non-inverting input DC level (V1) to ~1.6V higher than ground. This offset ensures that the amplifier input DC level is maintained within the common mode input voltage range. The amplifier non-inverting gain is given in Equation 1.

$$V_{OUT} = (V_{IN+} - 1.6V) \bullet \left(1 + \frac{R_F}{R_G}\right) \quad \text{(EQ. 1)}$$

DC-Restore Amplifier

(refer to "Functional Block Diagram" on page 12)

The DC-restore circuit contains a voltage reference amplifier and an analog switch function that closes the DC-restore loop under control of the $\overline{\text{CLAMP}}$ logic input. The A2 amplifier output stage operates in a current-feedback mode with a source capability of 860µA (Typ).

A logic "0" at the CLAMP input closes switch S1, which closes the DC-restore loop. The video input AC coupling capacitor, CX1, acts as a DC hold capacitor (through the 75Ω termination resistor) to average the current-source output of amplifier A2. When the DC-restore loop has reached equilibrium, the DC voltage stored on CX1 will be the value required to set the voltages at A1 (V_{OUT}) and A2 (V_{IN+}) according to Equations 2 and 3:

$$V_{OUT}(DC) = V_{REF} \quad \text{(EQ. 2)}$$

$$V_{IN+} = V_{OUT}(DC) + 1.6V \quad \text{(EQ. 3)}$$

Therefore, if V_{REF} is set to 0V (GND); V_{OUT} = 15mV, and the DC voltage stored on CX1 is ~1.6V.

The CX1 capacitor value is chosen from the system requirements. A typical DC-restore application using an NTSC video horizontal sync to drive the $\overline{CLAMP}$ pin will result in a 62µs hold time. The typical input bias current to the video amplifier is 1.2µA, so for a 62µs hold time, and a 0.01µF capacitor, the output voltage drift is 7.5mV in one line. The restore amplifier can provide a typical source current of 860µA to charge capacitor CX1, so with a 1.2µs sampling time, the output can be corrected by 36mV in each line.

Using a smaller value of CX1 increases both the voltage that can be corrected, as well as the droop while being held. Likewise, using a larger value of CX1, reduces the correction and droop voltages. A sample of charging and droop rates are shown in Table 2.

TABLE 2. TABLE OF CHARGE STORAGE CAPACITOR VS DROOP CHARGING RATES (NOTE)

CAP VALUE (nF)	DROOP IN 62µs (mV)	CHARGE IN 1.2µs (mV)	CHARGE IN 4µs (mV)
10	7.5	103	344
33	2.3	32.5	103
100	0.75	10.3	34

$$V_{DROOP} = \frac{I_B}{\text{CAP Value}} \times (\text{Line Time} - \text{Sample Time}) \quad \text{(EQ. 4)}$$

$$V_{CHARGE} = \frac{I_{CLAMP}}{\text{CAP Value}} \times (\text{Sample Time}) \quad \text{(EQ. 5)}$$

Figure 36 shows the test setup for measuring the DC Restore's response to an input DC step shown in Figures 21 and 22.

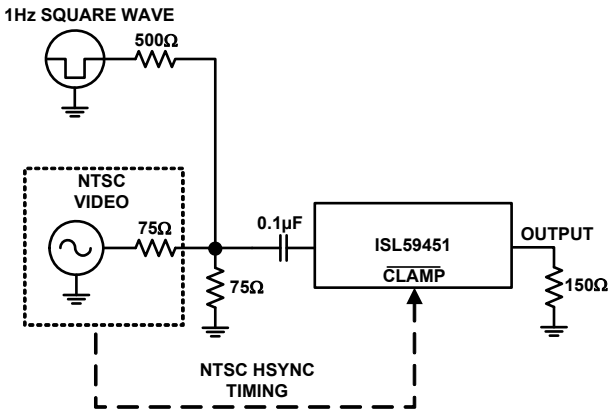


FIGURE 36. DC STEP RESPONSE

AC Design Considerations

High speed current-feed amplifiers are sensitive to capacitance at the inverting input and output terminals. Capacitance at the output terminal increases gain peaking and overshoot. The AC response of the ISL59451 is optimized for a total output capacitance of 2.1pF with a load of 150Ω (Figure 35A). When PCB trace capacitance and component capacitance exceed 2pF, overshoot becomes strongly dependent on the input pulse amplitude and slew rate. Increasing levels of output capacitance reduce stability, resulting in increased overshoot and settling time.

PC board trace length (L_{CRIT}) should be kept to a minimum in order to minimize output capacitance. At 500MHz, trace lengths approaching 1" begin exhibiting transmission line behavior and may cause excessive ringing if controlled impedance traces are not used. Figure 35B shows the optimum inter-stage circuit when the total output trace length is less than the critical length of the highest signal frequency.

As a general rule of thumb the trace lengths should be less than one-tenth of the wavelength of the highest frequency component in the signal. Equation 6 shows an approximate way to calculate L_{CRIT} in meters.

$$L_{CRIT} \leq \frac{c}{10 \times f_{MAX} \times \sqrt{\varepsilon_R}} \quad \text{(EQ. 6)}$$

c = speed of light (3 x 10^8 m/s)

f_{MAX} = maximum frequency component

ε_R = relative dielectric of board material (e.g. FR4 = 4.2)

For applications where inter-stage distances are long but pulse response is not critical, capacitor C_S can be added to low values of R_S to form a low-pass filter to dampen pulse overshoot. This approach avoids the need for the large gain correction required by the -6dB attenuation of the back-loaded controlled impedance interconnect. Load resistor R_L is still required but can be 500Ω or greater, resulting in a much smaller attenuation factor.

For applications where pulse response is critical and where inter-stage distances exceed L_{CRIT}, the circuit shown in Figure 35C is recommended. Resistor R_S constrains the capacitance seen by the amplifier output to the trace capacitance betweeen the output pin and the resistor. Therefore, R_S should be placed as close to the ISL59451 output pin as possible. For inter-stage distances much greater than L_{CRIT}, the back-loaded circuit shown in Figure 35D should be used with controlled impedance PCB lines, with R_S and R_L equal to the controlled impedance.

Control Signals

S0, S1, HIZ, $\overline{CLAMP}$, and AV2 are binary coded, TTL/CMOS compatible control inputs. The S0, S1 pins select the inputs. All three amplifiers are switched simultaneously from their respective inputs. When HIZ is pulled high, it puts the outputs in a high-impedance state and disconnects the video inputs. $\overline{CLAMP}$ enables and disables the DC restore circuitry. For control signal rise and fall times less than 10ns, the use of termination resistors on the control lines close to the part may be necessary to prevent reflections and to minimize transients

coupled to the output. See Table 1 for the S1, S0 selection states.

High-Impedance State

An internal pull-down resistor ensures the device will be active with no connection to the HIZ pin. The HIZ state is established within approximately 25ns by placing a logic high (>2V) on the HIZ pin. If the HIZ state is selected, the output impedance is ~2000Ω (Figure 6). The supply current during this state is reduced to ~3mA.

Limiting the Output Current

No output short circuit current limit exists on these parts. All applications need to limit the output current to less than 50mA. Adequate thermal heat sinking of the parts is also required.

PC Board Layout

The AC performance of this circuit depends greatly on the care taken in designing the PC board. The following are recommendations to achieve optimum high frequency performance from your PC board.

- Use low inductance components, such as chip resistors and chip capacitors whenever possible.
- Minimize signal trace lengths. Trace inductance and capacitance can easily limit circuit performance. Avoid sharp corners; use rounded corners when possible. Vias in the signal lines add inductance at high frequency and should be avoided. PCB traces longer than 1" begin to exhibit transmission line characteristics with signal rise/fall times of 1ns or less. To maintain frequency performance with longer traces, use striplines.
- Match channel-to-channel analog I/O trace lengths and layout symmetry. This will minimize propagation delay mismatches.
- All signal I/O lines should be routed over continuous ground planes (i.e. no split planes or PCB gaps under these lines).
- Put the proper termination resistors in their optimum location as close to the device as possible.
- When testing, use good quality connectors and cables, matching cable types and keeping cable lengths to a minimum.
- Decouple well, using aminimum of 2 power supply decoupling capacitors (1000pF, 0.01µF), placed as close to the devices as possible. Avoid vias between the capacitor and the device because vias adds unwanted inductance. Larger caps can be farther away. When vias are required in a layout, they should be routed as far away from the device as possible.

The QFN Package Requires Additional PCB Layout Rules for the Thermal Pad

The thermal pad is electrically connected to GND through the high resistance IC substrate. Its primary function is to provide heat sinking for the IC.

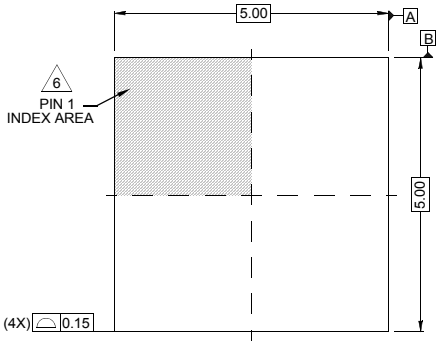
Maximum AC performance is achieved if the thermal pad is attached to a dedicated decoupled layer in a multi-layered PC board. In cases where a dedicated layer is not possible, AC performance may be reduced at upper frequencies.

- The thermal pad requirements are proportional to power dissipation and ambient temperature. A dedicated layer (oftern the ground plane) eliminates the need for individual thermal pad area. When a dedicated layer is not possible, a 1”x1” pad area is sufficient for an ISL59451 dissipating 0.5W at +50°C ambient. Pad area requirements should be evaluated according to the maximum ambient temperature, the maximum supply current (including worst case signals + loads), and the thermal characteristic of the PCB.

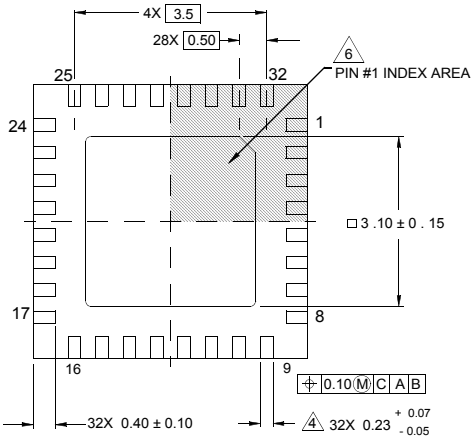
Package Outline Drawing

L32.5x5

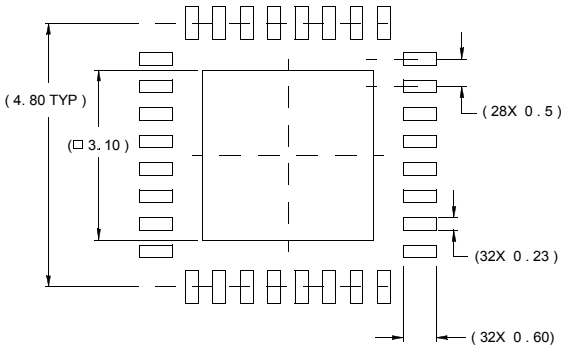
32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 02/07



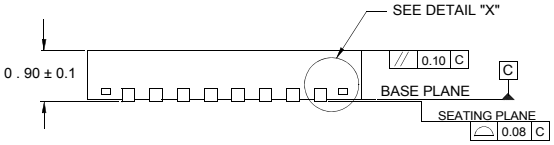
TOP VIEW



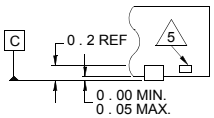
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.