ISL55211

Wideband, Low Noise, Low Distortion, Fixed Gain, Differential Amplifier

FN7868
Rev 0.00
June 21, 2011

The ISL55211 is a wideband, differential input to differential output amplifier offering 3 possible internal gain settings. Using fixed 500Ω internal feedback resistors, the amplifier may be configured for a differential gain of 2, 4 or 5V/V depending on which combination of input pins are connected to the signal source. Internal feedback capacitors controls the signal bandwidth to be a constant 1.4GHz in all gain settings.

Ideally suited for AC-coupled data acquisition applications, the output DC common mode voltage is controlled through an external V_{CM} pin or left to default to 1.2V above the negative supply pin. Where the differential signal source is AC-coupled, the input common mode voltage will equal the output common mode voltage.

Intended for very high dynamic range ADC interface applications, the ISL55211 offers 5600V/µs differential slew rate, <12nV/√Hz output noise, and >100dBc SFDR to >100MHz for $2V_{P-P}$ 2-tone 3rd order intermodulation. Its balanced architecture effectively suppresses even order distortion terms - an important issue for very wide band 1st Nyquist zone ADC interface applications. Minimum gain operation of 2V/V (6dB) with <1dB peaking ensures stable performance over-temperature. It's ultra high differential slew rate of 5600V/µs provides adequate performance margin for large signal application through 500MHz.

The ISL55211 requires only a single 3.3V (max. 4.2V) power supply and 35mA quiescent current, providing a very low power solution (115mW). Further power savings are possible using the optional power shutdown control - where the quiescent current can be reduced to <0.4mA. A companion device, the ISL55210, offers similar performance where the feedback and gain resistors are external. Both are available in a 16 Ld TQFN (Pb-free) package and are specified for operation over the -40°C to +85°C ambient temperature range.

Features

- 3 Fixed Gain Options . . . . . 2, 4, or 5V/V
- Constant Bandwidth Over Gain 1.4GHz
- Differential Slew Rate 5,600V/µs
- $2V_{P-P}$, 2-tone IM3 (200Ω) 100MHz . . . . . -103dBc
- Low Differential Output Noise (Gain 5V/V) . . . . . <12nV/√Hz
- Supply Voltage Range . . . . . 3.0V to 4.2V
- Quiescent Power (3.3V Supply) 115mW

Applications

- Low Power, High Dynamic Range ADC Interface
- Differential Mixer Output Amplifier
- SAW Filter Pre/Post Driver
- Fixed Gain Coax Receiver

Related Devices

- ISL55210 - External Gain Set Version
- ISLA112P50 - 12-bit, 500MSPS ADC (<500mW)
- ISLA214P50 - 14-bit, 500MSPS ADC (<850mW)

Related Literature

- AN1649 - "Designer's guide to the ISL55210 and ISL55211 Evaluation Boards"

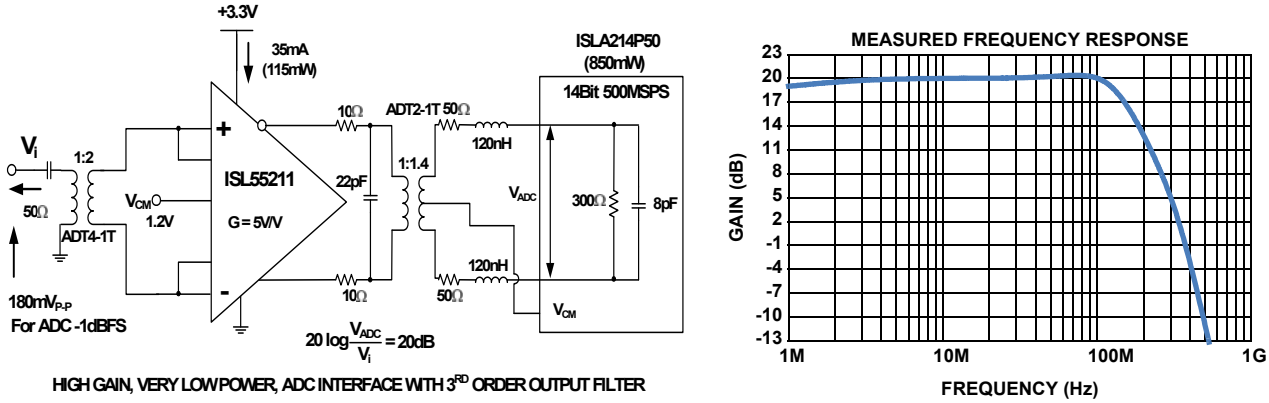
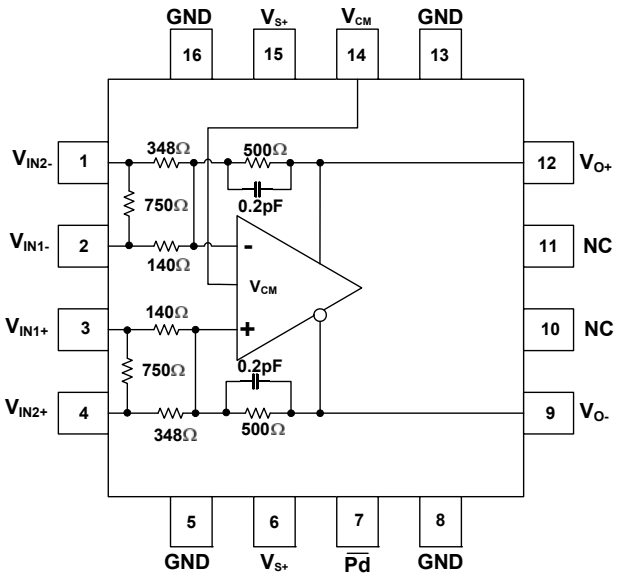


FIGURE 1. TYPICAL APPLICATION CIRCUIT

Pin Configuration

ISL55211
(3x3 16 LD TQFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	V_{IN2-}	Balanced Differential Input for Av = 6dB, strapped to V_{IN1-} for Av = 14dB
2	V_{IN1-}	Balanced Differential Input for Av = 12dB, strapped to V_{IN2-} for Av = 14dB
3	V_{IN1+}	Balanced Differential Input for Av = 12dB, strapped to V_{IN2+} for Av = 14dB
4	V_{IN2+}	Balanced Differential Input for Av = 6dB, strapped to V_{IN1+} for Av = 14dB
5, 8, 13, 16	GND	Supply Ground (thermal pad electrically connected)
6, 15	V_{S+}	Positive Power Supply (3.0V~4.2V)
7	Pd	Power-down: $\overline{Pd}$ = logic low. Puts part into low power mode; $\overline{Pd}$ = logic high or open for normal operation
9	V_{O-}	Inverting Amplifier Output
10, 11	NC	No Internal Connection
12	V_{O+}	Non-Inverting Amplifier Output
14	V_{CM}	Common-mode Voltage Input

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL55211IRTZ	5211	-40 to +85	16 Ld 3x3 TQFN	L16.3x3D
ISL55211IRTZ-EVAL1Z	Evaluation Board			

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL55211. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage from V_{S+} to GND 4.5V
Input Voltage . . . . . V_{S+} +0.3V to GND-0.3V
Power Dissipation . . . . . See Thermal Conditions Section
ESD Rating
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) 3500V
Machine Model (Per EIAJ ED-4701 Method C-111) 250V
Charged Device Model 1500V
Latch up (Per JESD-78; Class II; Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld TQFN Package (Notes 4, 5)	63	16.5

Storage Temperature . . . . . -65°C to +125°C
Max. Continuous Operating Junction Temperature . . . . . +135°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Ambient Operating Temperature . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

V_{S+} = +3.3V Test Conditions: G = 12dB, V_{CM} = open, V_O = $2V_{P-P}$, R_L = 200Ω differential, T_A = +25°C, differential input, differential output, input and output referenced to internal default V_{CM} (1.2V nominal) unless otherwise specified.

PARAMETER	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT	TESTED
AC PERFORMANCE						
Small-Signal Bandwidth (4-port S parameter, Test Circuit 2)	G = 6dB, V_O = $100mV_{P-P}$		1.6		GHz	
	G = 12dB, V_O = $100mV_{P-P}$		1.4		GHz	
	G = 14dB, V_O = $100mV_{P-P}$		1.4		GHz	
Bandwidth for 0.1-dB Flatness	G = 12dB, V_O = $2V_{P-P}$ (Figure 17)		150		MHz	
Large-Signal Bandwidth	G = 12dB, V_O = $2V_{P-P}$		1.2		GHz	
Gain Accuracy	G = 6dB, R_L = Open	1.96	2	2.04	V/V	*
	G = 12dB, R_L = Open	3.88	4	4.12	V/V	*
	G = 14dB, R_L = Open	4.8	5	5.2	V/V	
Slew Rate (Differential)	2-V step (simulated)		5,600		V/µs	
Differential Rise/Fall Time			0.22		ns	
2nd-order Harmonic Distortion, Test Circuit 1, 15dB Gain	f = 20MHz, V_O = $2V_{P-P}$		-110		dBc	
	f = 50MHz, V_O = $2V_{P-P}$		-98		dBc	
	f = 100MHz, V_O = $2V_{P-P}$		-85		dBc	
3rd-order Harmonic Distortion, Test Circuit 1, 15dB Gain	f = 20MHz, V_O = $2V_{P-P}$		-120		dBc	
	f = 50MHz, V_O = $2V_{P-P}$		-110		dBc	
	f = 100MHz, V_O = $2V_{P-P}$		-100		dBc	
2nd-order Intermodulation Distortion, Test Circuit 1, 15dB Gain	f_C = 70MHz, 200kHz spacing ($2V_{P-P}$ envelope)		-89		dBc	
	f_C = 140MHz, 200kHz spacing ($2V_{P-P}$ envelope)		-78		dBc	
3rd-order Intermodulation Distortion, Test Circuit 1, 15dB Gain	f_C = 70MHz, 200kHz spacing ($2V_{P-P}$ envelope)		-104		dBc	
	f_C = 140MHz, 200kHz spacing ($2V_{P-P}$ envelope)		-92		dBc	
Output Voltage Noise	Test Circuit 1, total gain 15dB, ADT2-1T		11.2		$nV/\sqrt{Hz}$	
DC PERFORMANCE (Internal Nodes)						
Input Offset Voltage	T_A = +25°C	-1.4	±0.1	+1.4	mV	*
	T_A = -40°C to +85°C	-1.6	±0.1	+1.6	mV	

Electrical Specifications V_{S+} = +3.3V Test Conditions: G = 12dB, V_{CM} = open, V_O = $2V_{P-P}$, R_L = 200Ω differential, T_A = +25°C, differential input, differential output, input and output referenced to internal default V_{CM} (1.2V nominal) unless otherwise specified. **(Continued)**

PARAMETER	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT	TESTED
Average Offset Voltage Drift	T_A = -40°C to +85°C		±3		µV/°C	
Input Bias Current	T_A = +25°C, positive current into the pin		+50	+120	µA	*
	T_A = -40°C to +85°C		+50	+140	µA	
Average Bias Current Drift	T_A = -40°C to +85°C		200		nA/°C	
Input Offset Current	T_A = +25°C	-5	±1	+5	µA	*
	T_A = -40°C to +85°C	-6		+6	µA	
Average Offset Current Drift	T_A = -40°C to +85°C		±8		nA/°C	
INPUT						
Common-mode Input Range High	Internal Nodes			1.7	V	*
Common-mode Input Range Low	Internal Nodes	1.1			V	*
Common-mode Rejection Ratio	f < 10MHz, common mode to differential output	56	75		dB	*
Differential Input Impedance	V_{IN1-} Connected to V_{IN2-} V_{IN1+} Connected to V_{IN2+}		200		Ω	
OUTPUT (Pins 9 AND 12)						
Maximum Output Voltage	Each output (with 200Ω differential load) Linear Operation	2.15	2.35		V	*
Minimum Output Voltage			0.45	0.63	V	*
Differential Output Voltage Swing	T_A = +25°C	3.04	3.8		V_{P-P}	*
	T_A = -40°C to +85°C	2.95			V	
Differential Output Current Drive	R_L = 10Ω [sourcing or sinking]	40	45		mA	*
Closed-loop Output Impedance	f < 10MHz, differential		0.6		Ω	
OUTPUT COMMON-MODE VOLTAGE CONTROL (Pin 14)						
Small-signal Bandwidth	From V_{CM} pin to Output V_{CM}		30		MHz	
Slew Rate	Rising/Falling		150		V/µs	
Gain	V_{CM} input pin 1.0V to 1.4V	0.995	0.999		V/V	*
Output Common-Mode Offset from CM Input		-8	±1	+8	mV	*
CM Default Voltage	Output V_{CM} with V_{CM} pin floating	1.18	1.2	1.22	V	*
CM Input Bias Current	At control pin		2		µA	
CM Input Voltage Range	At control pin	0.9		1.9	V	*
CM Input Impedance	At control pin		15 ‖ 50		kΩ ‖ pF	
POWER SUPPLY						
Specified Operation Voltage		3	3.3	4.2	V	*
Quiescent Current	T_A = +25°, V_{S+} = 3.3V, V_{S-} = 0V	33	35	37	mA	*
	T_A = -40°C to +85°C	30.5	35	39.5	mA	
Power-supply Rejection (PSRR) V_{S+}	3.0V to 4.5V range f < 10MHz [PSRR to differential output]	50	67		dB	*
POWER-DOWN (Pin 7)	Referenced to GND					
Enable Voltage Threshold	Assured on above 1.55V		1.3	1.55	V	*
Disable Voltage Threshold	Assured off below 0.54V	0.54	0.7		V	*

Electrical Specifications

V_{S+} = +3.3V Test Conditions: G = 12dB, V_{CM} = open, V_O = $2V_{P-P}$, R_L = 200Ω differential, T_A = +25°C, differential input, differential output, input and output referenced to internal default V_{CM} (1.2V nominal) unless otherwise specified. **(Continued)**

PARAMETER	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT	TESTED
Power-down Quiescent Current	T_A = +25°C	0.2	0.3	0.4	mA	*
	T_A = -40°C to +85°C	0.15		0.45	mA	
Input Bias Current	$\overline{PD}$ = 0V, current positive into pin	-5	1	+5	µA	
Input Impedance			2 || 5		MΩ || pF	
Turn-on Time Delay	Measured to output on		200		ns	
Turn-off Time Delay	Measured to output off		400		ns	

NOTE:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

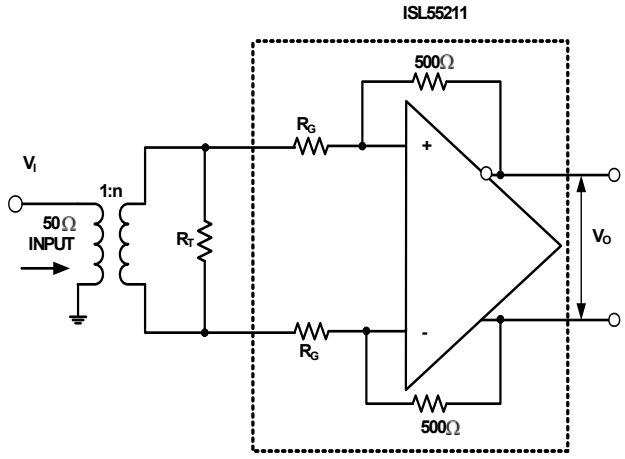


FIGURE 2. INTENDED CONFIGURATION

TABLE 1. ISL55211 INTENDED TRANSFORMER + INTERNAL GAIN SETTINGS

INPUT XFMR TURNS RATIO	INTERNAL R_G VALUE (Ω)	GAIN (V/V) V_O/V_I	GAIN (dB) V_O/V_I	R_T VALUE (Ω) TO GET 50Ω MATCH
1:1.4	250	2.8	9	122
1:1.4	125	5.6	15	162
1:1.4	100	7	17	192
1:2	250	4	12	333
1:2	125	8	18	1020
1:2	100	10	20	Open

Typical Performance Curves V_{S+} = 3.3V, $T_A \approx +25°C$, unless otherwise noted.

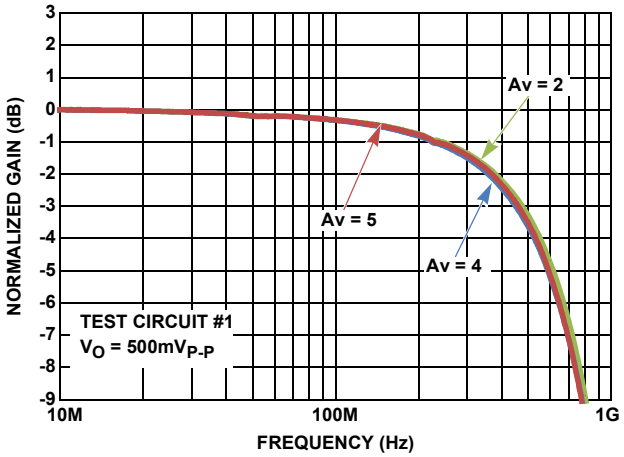


FIGURE 3. SMALL SIGNAL FREQUENCY RESPONSE WITH ADT2-1T INPUT TRANSFORMER

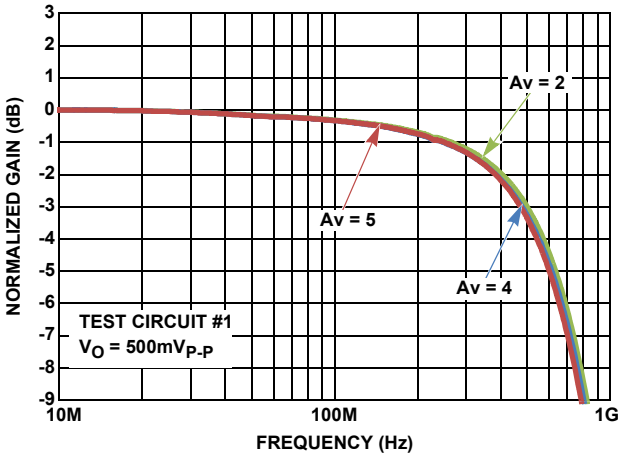


FIGURE 4. SMALL SIGNAL FREQUENCY RESPONSE WITH ADT4-1WT INPUT TRANSFORMER

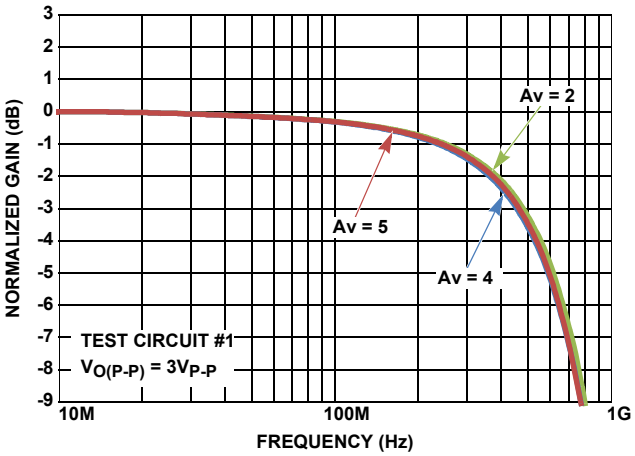


FIGURE 5. LARGE SIGNAL FREQUENCY RESPONSE WITH ADT2-1T INPUT TRANSFORMER

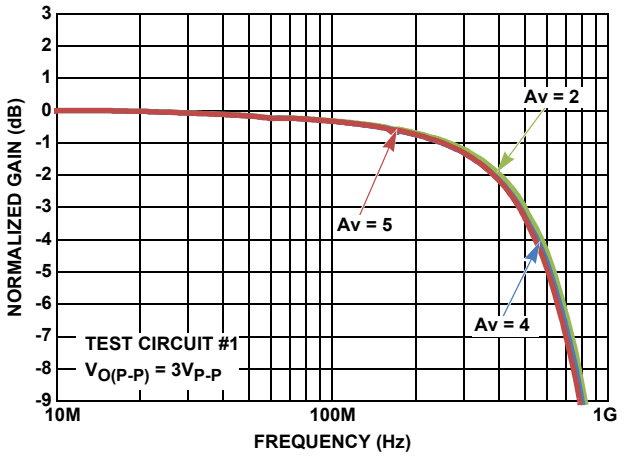


FIGURE 6. LARGE SIGNAL FREQUENCY RESPONSE WITH ADT4-1WT INPUT TRANSFORMER

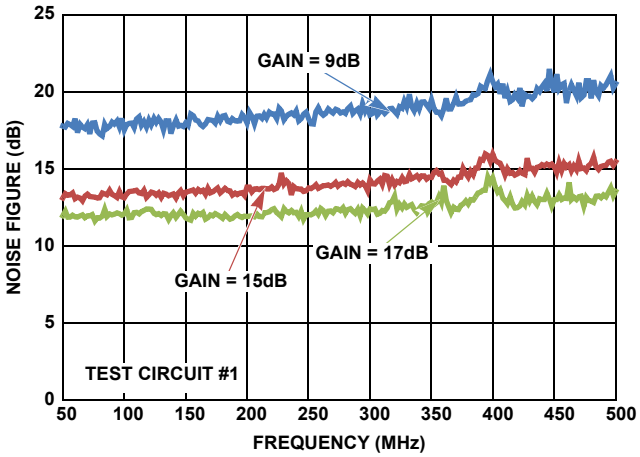


FIGURE 7. NOISE FIGURE WITH ADT2-1T INPUT TRANSFORMER

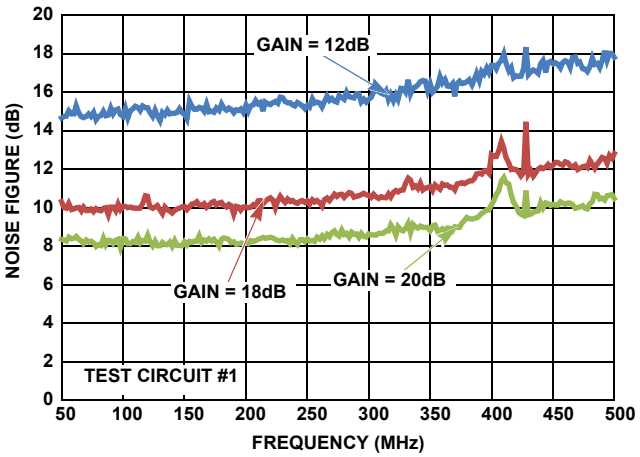


FIGURE 8. NOISE FIGURE WITH ADT4-1WT INPUT TRANSFORMER

Typical Performance Curves V_{S+} = 3.3V, $T_A \approx +25°C$, unless otherwise noted. (Continued)

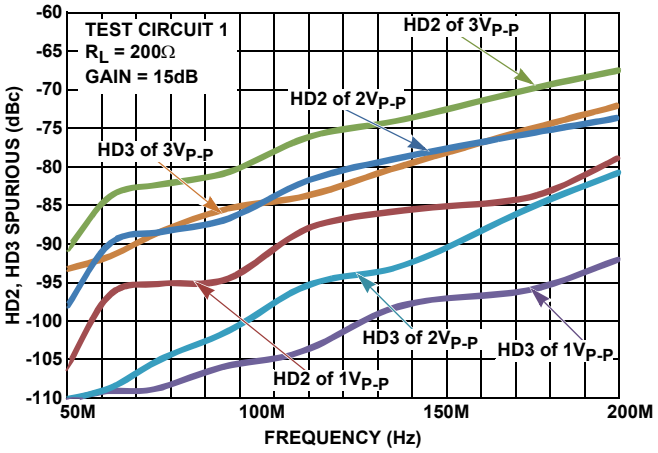


FIGURE 9. HD2, HD3 vs OUTPUT SWING

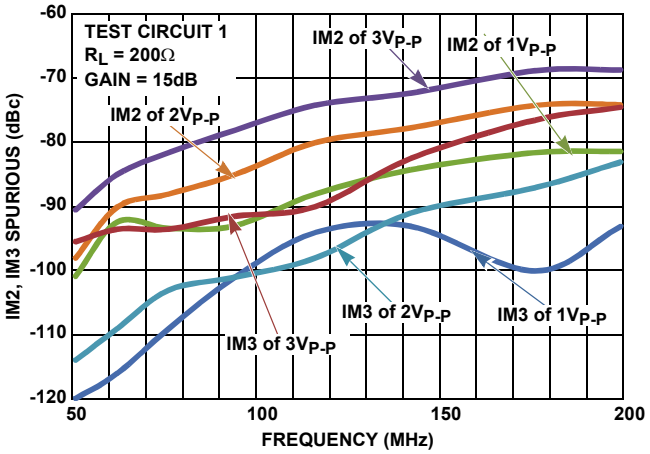


FIGURE 10. IM2 AND IM3 vs OUTPUT SWING

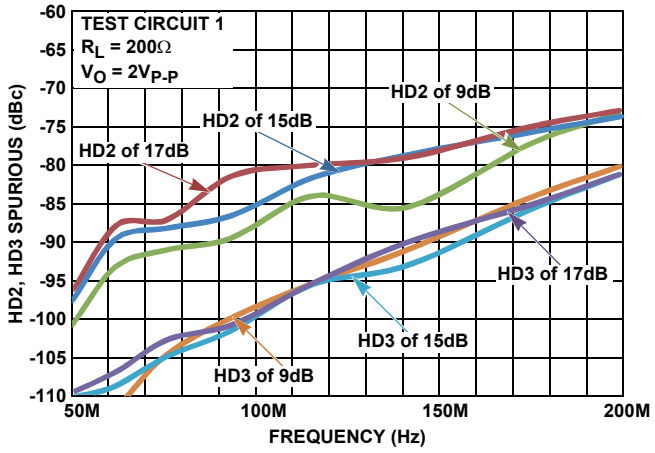


FIGURE 11. HD2, HD3 vs GAIN

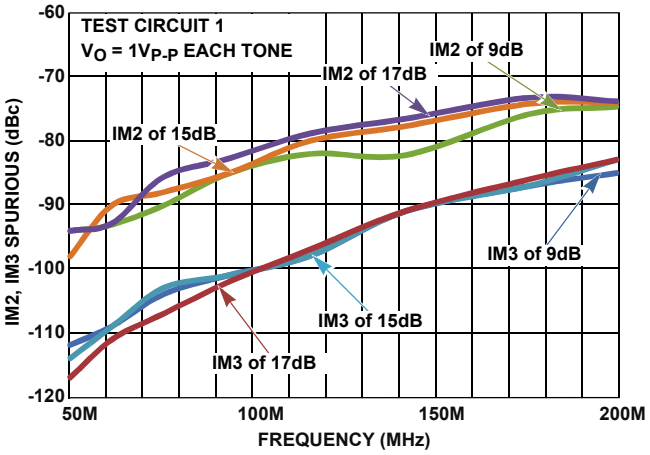


FIGURE 12. IM2 AND IM3 vs GAIN

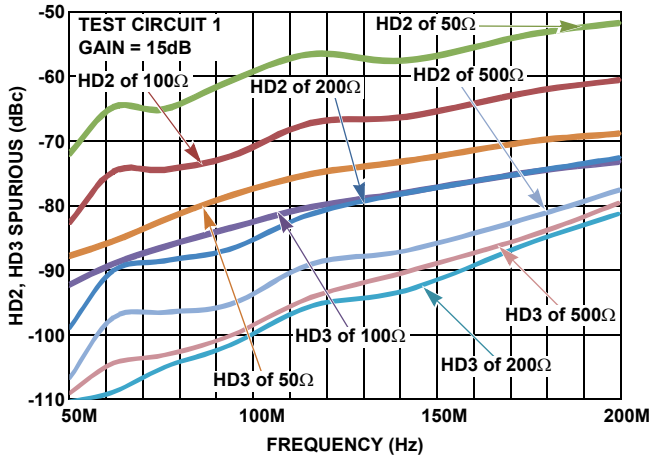


FIGURE 13. HD2, HD3 vs DIFFERENTIAL LOAD

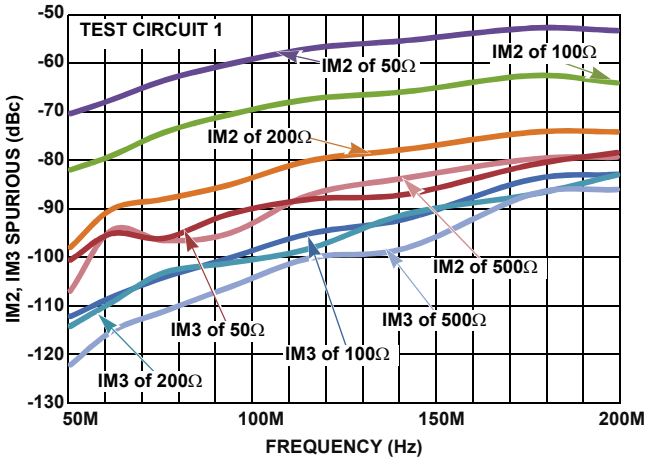


FIGURE 14. IM2, IM3 vs DIFFERENTIAL LOAD

Typical Performance Curves V_{S+} = 3.3V, $T_A \approx +25°C$, unless otherwise noted. (Continued)

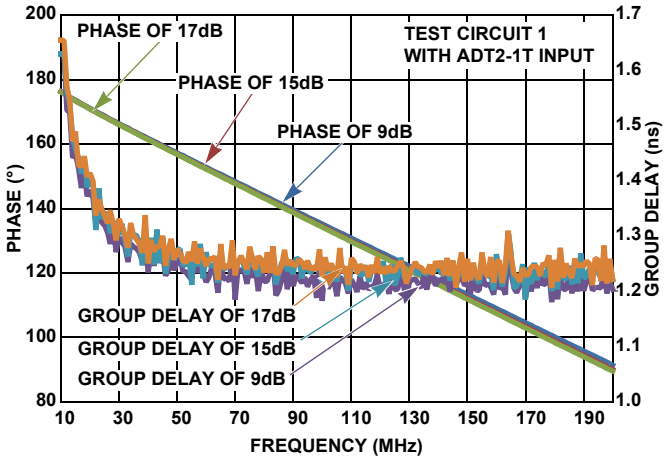


FIGURE 15. PHASE AND GROUP DELAY vs GAIN

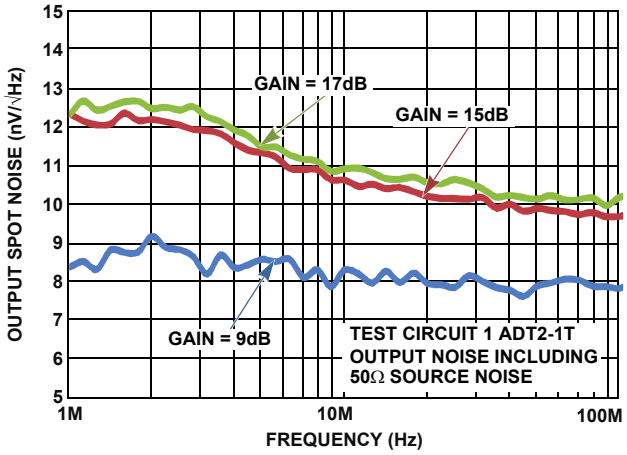


FIGURE 16. DIFFERENTIAL OUTPUT NOISE vs GAIN

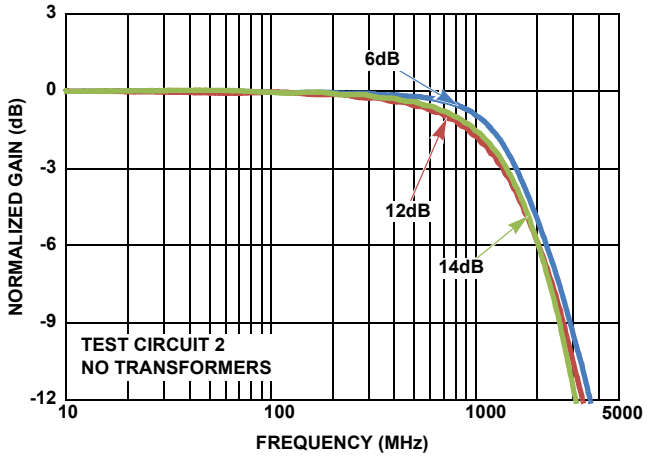


FIGURE 17. SMALL SIGNAL FREQUENCY RESPONSE

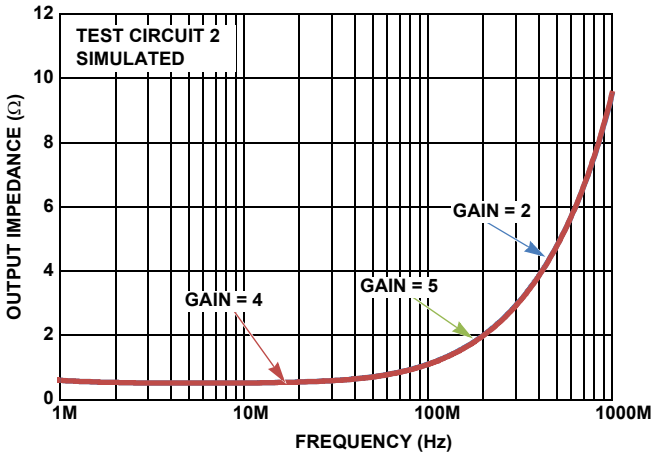


FIGURE 18. DIFFERENTIAL OUTPUT IMPEDANCE

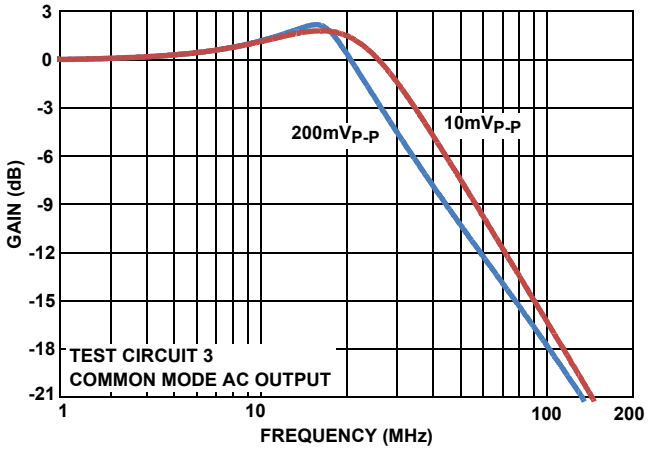


FIGURE 19. V_{CM} PIN INPUT FREQUENCY RESPONSE TO OUTPUT COMMON MODE

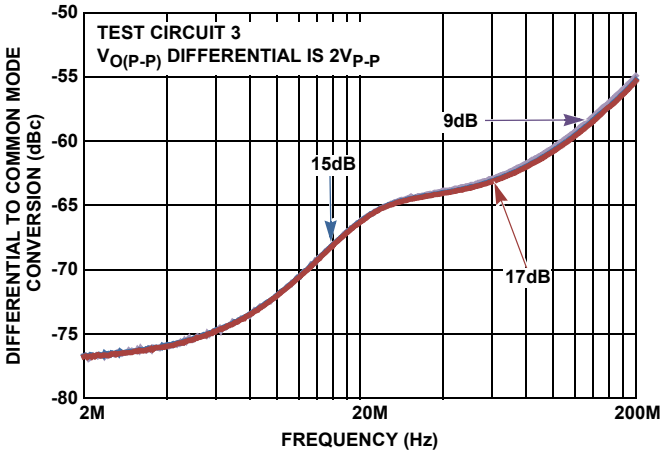


FIGURE 20. OUTPUT BALANCE ERROR

Typical Performance Curves V_{S+} = 3.3V, $T_A \approx +25°C$, unless otherwise noted. (Continued)

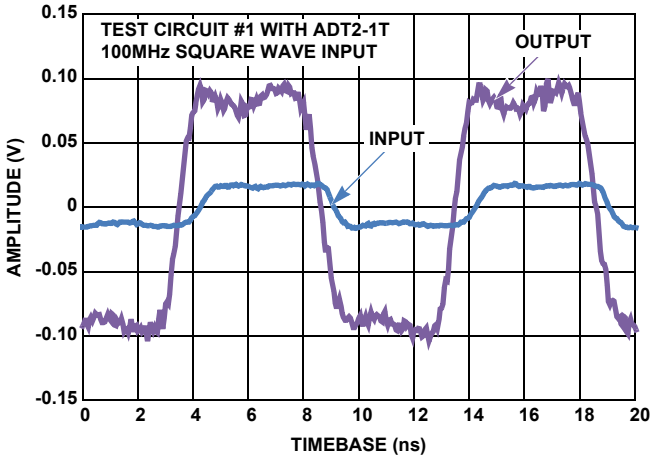


FIGURE 21. SMALL SIGNAL STEP RESPONSE

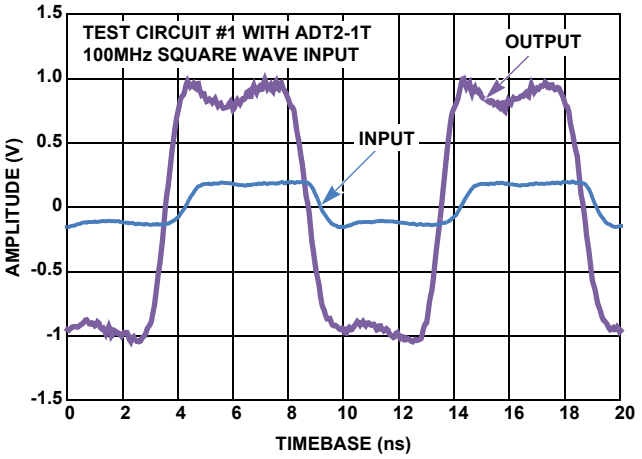


FIGURE 22. LARGE SIGNAL RESPONSE

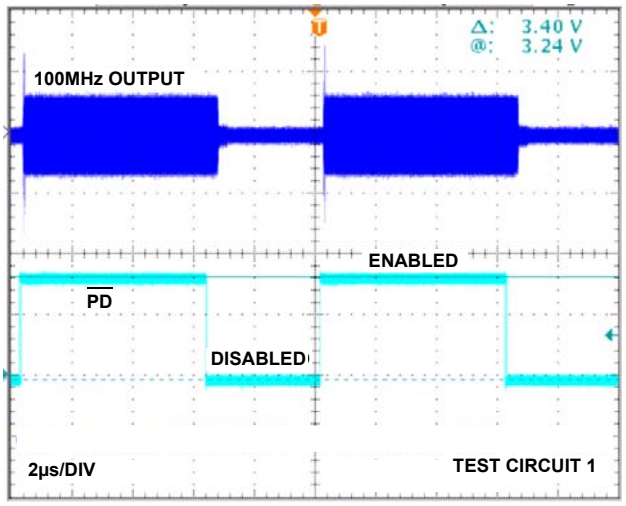


FIGURE 23. ENABLE/DISABLE TIMES (2µs/DIV)

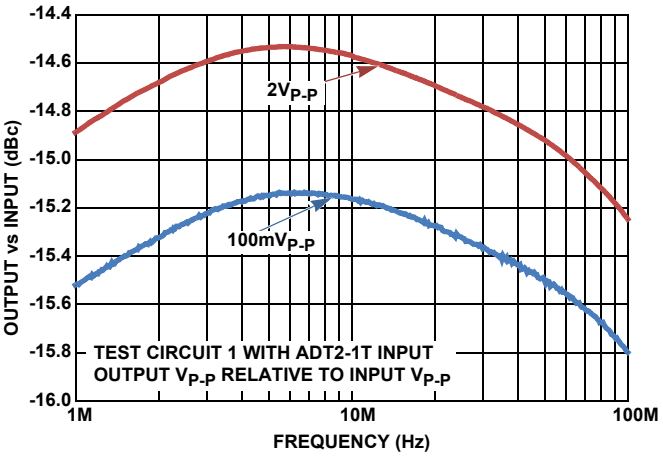


FIGURE 24. SHUTDOWN FEED-THROUGH

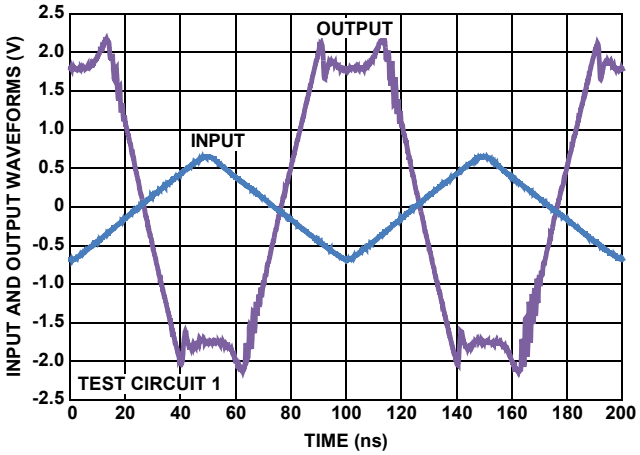


FIGURE 25. OVERDRIVE RECOVERY

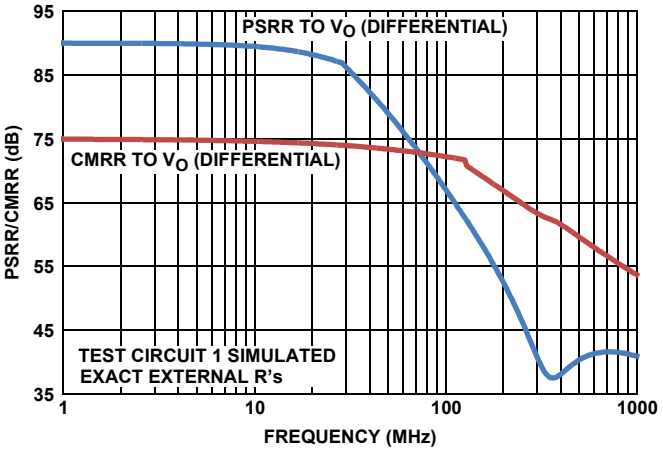


FIGURE 26. PSRR/CMRR TO DIFFERENTIAL V_O

Typical Performance Curves V_{S+} = 3.3V, $T_A \approx +25°C$, unless otherwise noted. **(Continued)**

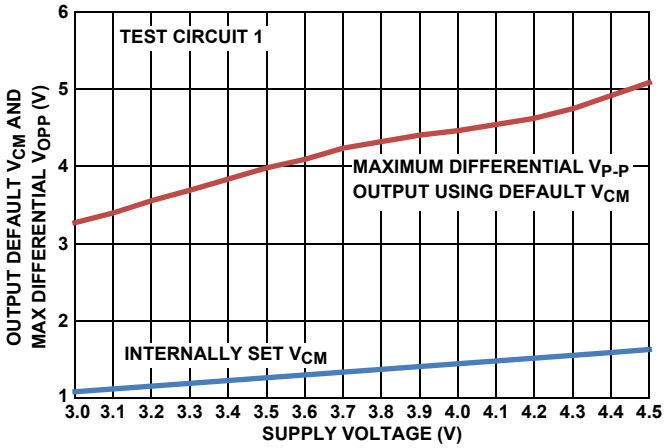


FIGURE 27. DEFAULT V_{CM} AND MAX V_{OPP} vs SUPPLY VOLTAGE

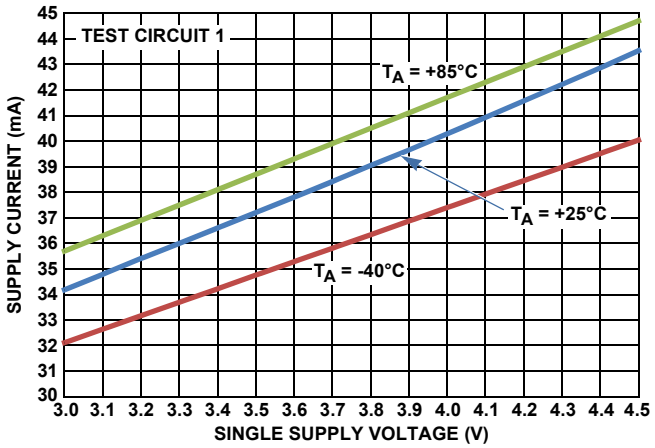


FIGURE 28. SUPPLY CURRENT vs SUPPLY VOLTAGE

Applications

Basic Operation

The ISL55211 is a very wideband, voltage feedback based, differential amplifier including an output common mode control loop and optional power shutdown feature. Intended for very low distortion differential signal driving, this internally fixed gain device provides 3 possible gain settings by simply picking the input side connections as shown in Table 1. Including internal compensation, the ISL55211 holds a constant bandwidth over gain settings. Most applications are intended for AC-coupled I/O using a single 3.3V supply and an input transformer. The internal resistor values have been scaled up slightly to require an external termination element along with the two internal resistors where a 50Ω differential input match is desired. This does increase the output noise slightly but narrows up the input VSWR tolerance and lowers the added loading of the feedback resistors improving SFDR.

Where DC-coupled differential I/O operation is desired, the ISL55211 can be connected directly to the source as long as the internal input common mode range limits are observed (1.1V to 1.7V for a 3.3V single supply operation). For a DC-coupled, single to differential requirement, consider the ISL55210. This device is an external resistor version of the ISL55211 where the flexibility in the external resistors will enable single to differential operation. For a ground referenced input signal, this will require a negative supply when using the ISL55210.

Most applications behave as a differential inverting op amp design. There is therefore an input gain resistor on each side of the inputs that must be driven. The 3 possible connections to the two pairs of input pins will give a 100Ω, 125Ω, or 250Ω input resistor on each side. Combined with the two input turns ratio's shown in Table 1, gives a 9dB to 20dB operating gain range in approximately 3dB steps.

The device can be powered down to < 400µA supply current using the optional disable pin. To operate normally, this pin should be asserted high using a simple logic gate to $+V_{CC}$ or tied high through a 10kΩ resistor to $+V_{CC}$. When disabled, the power dissipation drops to < 1mW but, due to the inverting op amp type architecture, the input signal will feed-forward through the feedback and gain resistors giving limited isolation.

Application and Characterization Circuits

Test Circuit 1 of Figure 29 forms a starting point for many of the characterization curves for the ISL55211. Since most lab sources and measurement devices are single-ended, this circuit converts to differential at the input through a wideband transformer and would also be a typical application circuit coming from a single-ended source. Assuming the source is a 50Ω impedance, the internal R_G resistors and external R_T are set to provide both the input termination and the gain. Since the inverting summing nodes act as virtual ground points for AC signal analysis, the total termination impedance across the input transformer secondary will be $(2*R_G)||R_T$. Setting this equal to n^2*R_S will give a matched input impedance inside the bandwidth of the transformer (where "n" is the turns ratio). The amplifier gain is fixed by the selected input R_G element and the internal 500Ω feedback resistors. While the ISL55211 is internally a Voltage Feedback Design (VFA) to give the lowest possible noise, internal compensation caps hold the bandwidth over gain setting approximately constant at 1.4GHz. For wider small signal bandwidth at lower gains, consider the ISL55210, which provides >2.2GHz at a gain of 12dB.

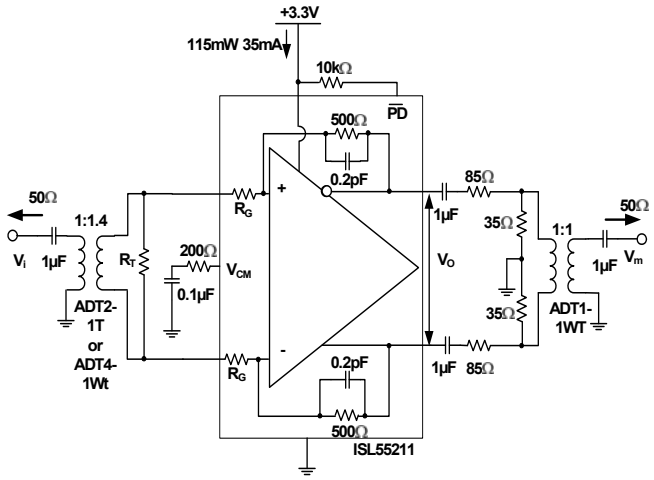


FIGURE 29. TEST CIRCUIT 1

Working with a transformer coupled input as shown in Figure 29, or with two DC blocking caps from a differential source, means the output common mode voltage set by either the default internal V_{CM} setting, or a voltage applied to the V_{CM} control pin, will also appear as the input common mode voltage. This provides a very easy way to control the ISL55211 I/O common mode operating voltages for an AC-coupled signal path. The internal common mode loop holds the output pins to V_{CM} and, since there is no DC path for an I_{CM} current back towards the input in Figure 29, that V_{CM} setting will also appear as the input common mode voltage. It is useful, for this reason, to leave any input transformer secondary centertap unconnected. The internally set V_{CM} voltage is referenced from the negative supply pin. With a single 3.3V supply, it is very close to 1.2V but will change with total supply voltage across the device as shown in Figure 27.

Most of the characterization curves starting with Figure 29 then get different gains by changing the connections to the two pairs of input R_G connections, as shown on the pin configuration drawing on page 2. Two input turns ratios are intended for Test Circuit 1; either a 1:1.4 turns ratio (ohms ratio of 2) or a 1:2 turns ratio (ohm ratio of 4). The specific transformers shown in Figure 29 are representative of broadband RF transformers but alternate devices and manufacturers of these turns ratio devices are certainly applicable. The output side of this test circuit presents a differential 200Ω load while converting the differential to single-ended through a resistive attenuator and a 1:1 transformer. This inserts approximately a 17dB insertion loss that is removed to report the characteristic curves. For load tests below the 200Ω shown in Figure 29, a simple added shunt resistor is placed across the output pins. For loads > 200Ω, the series and shunt load R's are adjusted to show that total load (including the 50Ω measurement load reflected through the 1:1 output measurement port transformer) and provide an apparent 50Ω differential source to that transformer. This output side transformer is for measurement purposes only and is not necessary for final applications circuits. There are output interface designs that do benefit from a transformer as part of the signal path as shown in Figure 1. In that case, the 1:1:4 output side transformer becomes part of a filter design and recovers the filter insertion loss from the amplifier output pins to the ADC inputs.

Where just the amplifier is tested, a 4-port network analyzer is used and the very simple test circuit of Figure 30 is implemented. This is used to measure the differential S21 curves vs gain of Figure 17 and as a simulation circuit for the differential output impedance vs gain of Figure 18. Changing the gain is a simple matter of adjusting the connections to the four input R_G connections resistors, as shown in Table 1. This circuit depends on the two AC-coupled source 50Ω of the 4 port network analyzer and presents an AC-coupled differential 100Ω load to the amplifier as the input impedance of the remaining two ports of the network analyzer.

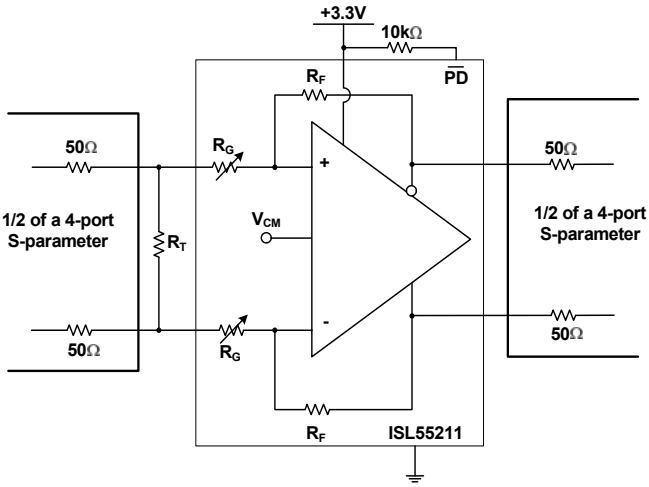


FIGURE 30. TEST CIRCUIT 2 4-PORT S-PARAMETER MEASUREMENTS

Using this measurement allows the small single bandwidth of just the ISL55211 to be exposed. Many of the other measurements are using I/O transformers that are limiting the apparent bandwidth to a reduced level. Figure 17 shows the 3 normalized differential S21 curves for the possible internal gains of 9dB, 14dB and 15dB. The small signal bandwidth is remaining nearly constant at 1.4GHz due to the internal capacitive feedback network.

The closed loop differential output impedance of Figure 18 is simulated using Figure 30 in ADS. This shows a relatively low output impedance (< 1Ω through 100MHz) constant with signal gain setting. Typical FDA outputs show a closed loop output impedance that increases with signal gain setting. The ISL55211 holds a more constant response due to internal design elements unique to this device.

Common mode output measurements are made using the circuit in Figure 31. Here, the outputs are summed together through two 100Ω resistors (still a 200Ω differential load) to a center point where the average, or common mode, output voltage may be sensed. This is coupled through a 1µF DC blocking capacitor and measured using 50Ω test equipment. The common mode source impedance for this circuit is the parallel combination of the 2-100Ω elements, or 50Ω. Figure 19 uses this circuit to measure the small and large signal response from the V_{CM} control pin to the output common mode. This pin includes an internal 50pF capacitor on the default bias network (to filter supply noise when there is no connection to this pin), which bandlimits the response to approximately 30MHz. This is far lower than the actual bandwidth of the common mode loop. Figure 20 uses this output

CM measurement circuit with a large signal ($2V_{P-P}$) differential output voltage (generated through the Vi path of Figure 31) to measure the differential to common mode conversion - often called the "Output Balance Error" for an FDA.

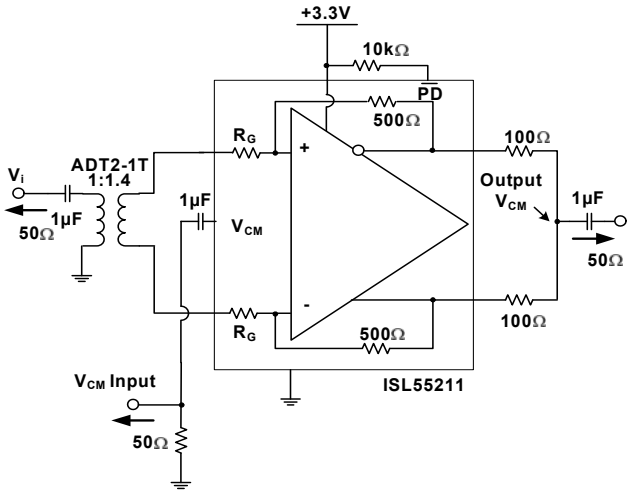


FIGURE 31. TEST CIRCUIT #3 COMMON MODE AC OUTPUT MEASUREMENTS

Single Supply, Input Transformer Coupled, Design Considerations

The characterization circuit of Figure 29 shows one possible input stage interface that offers several advantages. Where AC coupling is adequate, the circuit of Figure 29 simplifies the input common mode voltage control. If the source coming into this stage is single-ended, the input transformer provides a zero power conversion to differential. The two gain resistors (R_G in Figure 29) provide both a portion of the input termination impedance and the gain element for the amplifier. For 50Ω systems, these R_G resistors are too high with the turns ratios shown in Figure 29 to provide the full match and an external R_T resistor is required. This R_T element goes away at the highest gain setting using a 1:2 input turns ratio transformer.

It is also possible to adapt this circuit to other input characteristic impedances. Figure 32 shows a 75Ω example similar to Figure 2 while Table 2 shows the necessary external R values and resulting gains.

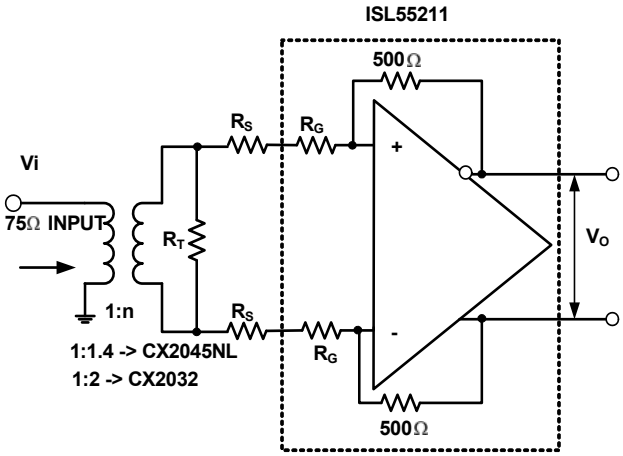


FIGURE 32. 75Ω IMPEDANCE IMPLEMENTATIONS

Here, the sum of the two internal R_G resistors at the higher two gain settings is too low to retain a match for the 1:2 input step up case. There, a pair of external series resistors are added to get the total differential input impedance up to 300Ω on the secondary side of the transformer and the R_T element goes to infinity. These two conditions are not particularly useful but Figure 32 shows how to implement the full range of internal conditions with the two turns ratios considered in Table 2. Figure 32 also shows a pair of alternate input transformer types from Pulse Engineering particularly suitable to the 75Ω case.

TABLE 2. EXTERNAL RESISTORS FOR A 75Ω INPUT IMPEDANCE DESIGN

ISL55211 INTENDED TRANSFORMER + INTERNAL GAIN SETTINGS					
INPUT XFMR TURNS RATIO	INTERNAL R_G VALUE (Ω)	GAIN (V/V) V_O/V_I	GAIN (dB) V_O/V_I	EXTERNAL R_T VALUE (Ω)	EXTERNAL R_S VALUE (Ω)
1:1.4	250	2.8	9	214	0
1:1.4	125	5.6	15	375	0
1:1.4	100	7	17	600	0
1:2	250	4	12	750	0
1:2	125	6.7	16.5	Open	25
1:2	100	6.7	16.5	Open	50

This input interface also simplifies the input common mode control. The V_{CM} pin controls the output common mode voltage. In most DC-coupled FDA applications, the input common mode voltage is determined by both this output common mode and the source signal. In a configuration like Figure 29, there is no path for a common mode current to flow from output to input, so the input common mode voltage equals the output. A similar effect could be achieved with just two blocking caps on the two R_G resistors. A DC-coupled, single to differential, configuration will also have a common mode input that is moving with the input signal. Converting to just a differential signal at the amplifier, as in Figure 29, removes any input signal related artifacts from the input common mode making the ISL55211 behave as a differential only VFA amplifier. There is only a very small differential error signal at the inputs set by the loop gain, as in a

normal single-ended VFA application, but no common mode signal related terms.

The examples shown are using the transformer to convert from single to differential. However, if the source is already differential, these same transformer input circuits can drive the transformer differentially still providing impedance scaling if needed and common mode rejection for both DC and AC common mode issues. A good example would be differential mixer outputs or SAW filter outputs. Those differential sources could also be connected into the ISL55211 R_G resistors through blocking caps as well eliminating the input transformer. The AC termination impedance for the differential source will then be the sum of the two R_G resistors when simple blocking caps are used.

Amplifier I/O Range Limits

The ISL55211 is intended principally to give the lowest IM3 performance on the lowest power for a differential I/O application. The amplifier will work DC coupled and over a relatively wide supply range of 3.0V to 4.2V supplies. The outputs have both a differential and common mode operating range limits while the input pins internal to the ISL55211 have a common mode voltage operating range. For single supply operation, the -Vs pins are at ground as is the exposed metal pad on the underside of the package. The ISL55211 can operate split supply where then -Vs will be a negative supply voltage and the exposed metal pad is either connected to this negative supply or left unconnected on an insulating board layer.

Briefly, the I/O and V_{CM} limits are as follows:

1. Maximum V_{CM} setting = -Vs +2V
2. Input common mode operating range (internal summing junction pints of the ISL55211) of -Vs + 1.1V or to output V_{CM} + 0.5V
3. Output V_O minimum (on each side) is either -Vs + 0.3V or output V_{CM} - 0.9V
4. Output V_O maximum (on each side) is +Vs - 1.5V

The output swing limits are often asymmetrical around the V_{CM} voltage. The maximum single-ended swings are set by these two limits - $V_{O(MIN)}$ is either -Vs + 0.3V or V_{CM} - 0.9V, whichever is less. So for instance, on a single 3.3V supply with the default V_{CM} voltage of 1.2V, these two limits give the same result and the output pins can swing down to 0.3V above -Vs (= 0V). If, however, the V_{CM} pin is raised to 1.5V, then the minimum output voltage will become 1.5V - 0.9V = 0.6V.

$V_{O(MAX)}$ is set by a headroom limit to the positive supply to be $-V_{O(MAX)}$ = +Vs - 1.5V. Again, on a 3.3V single supply and the default 1.2V V_{CM} setting, this means the maximum referenced to ground output pin voltages can be 3.3V - 1.5V = +1.8V or 0.6V above the default V_{CM} voltage.

Using these default conditions, and the maximum positive excursion of 0.6V above the 1.2V output V_{CM} setting, the maximum differential V_{P-P} swing will be 4x this 0.6V single-ended limit or $2.4V_{P-P}$. Where +Vs is increased, the limit then becomes the 0.9V below V_{CM}, but then the absolute maximum differential V_{P-P} is then 4 x 0.9V to $3.6V_{P-P}$. So for instance, to get this maximum output swing, increase the supply voltage until +Vs - 1.5V > V_{CM} + 0.9V. If we assume a V_{CM} voltage of 1.3V for instance, then 1.3V + 0.9V + 1.5V = 3.7V will give an unclipped $3.6V_{P-P}$ output capability. The V_{P-P} reported in Figure 27 is an asymmetrically clipped maximum swing. Going 10% above this 3.7V target to 4.1V will be within the recommended operating range and give some tolerancing headroom that would also suggest the V_{CM} voltage be moved up to approximately 1.5V, which coincides with the default output V_{CM} from Figure 27. Operating at +4.1V single supply in a Figure 29 type configuration will give the maximum linear differential output swing of $3.6V_{P-P}$.

The differential inputs internal to the ISL55211 also have operating range limits relative to the supply voltages. Operating in an AC-coupled circuit like Figure 29 will produce an input common mode voltage equal to the outputs. The inputs can operate with full linearity with this V_{CM} voltage down to 1.1V above the -Vs supply. On the default 1.2V output V_{CM} on +3.3V supplies this gives a 100mV guardband on the input V_{CM} voltages. Overriding the default V_{CM} by applying a control voltage to the V_{CM} pin should be done with care in going towards the negative supply due to this limit. On the + side, the maximum input V_{CM} above the -Vs supply is 2V so there is more room to move the output V_{CM} up than down from the default value.

Power Supply, Shutdown, and Thermal Considerations

The ISL55211 is intended for single supply operation from 3.0V to 4.2V with an absolute maximum setting of 4.5V. The 3.3V supply current is trimmed to be nominally 35mA at +25°C ambient. Figure 28 shows the supply current for nominal +25°C and -40°C to +85°C operation over the specified maximum supply range. The input stage is biased from an internal voltage reference from the negative supply giving the exceptional 90dB low frequency PSRR shown in Figure 26.

Since the input stage bias is from a re-regulated internal supply, a simple approach to single +5V operation can be supported as shown in Figure 33. Here, a simple IR drop from the +5V supply will bring the operating supply voltage for the ISL55211 into its allowed range. Figure 33 shows example calculations for the voltage range at the ISL55211 +Vs pin assuming a ±5% tolerance on the +5V supply and a 35mA to 55mA range on the total supply current. Considering the 34mA to 44mA quiescent current range from Figure 28 over the -40°C to +85°C ambient, and the 3.4V to 4.4V supply voltage range assumed here, this is designing for a 1mA to 11mA average load current, which should be adequate for most intended application loads. Good supply decoupling at the device pins is required for this simple solution to still provide exceptional HD performance.

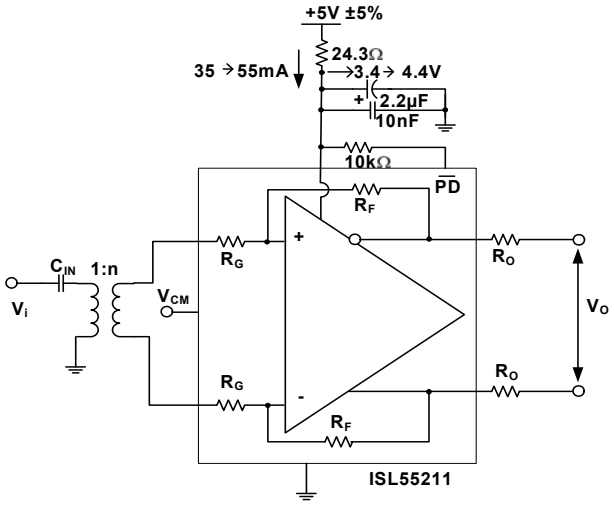


FIGURE 33. OPERATING FROM A SINGLE +5V SUPPLY

The ISL55211 includes a power shutdown feature that can be used to reduce system power dissipation when signal path operation is not required. This pin ($\overline{Pd}$) is referenced to -Vs and must be asserted low to activate the shutdown feature. When not used, a 10kΩ external resistor to +Vs should be used to assert a high level at this pin. Digital control on this pin can be either an open collector output (using that 10kΩ pull-up) or a CMOS logic line running off the same +Vs as the amplifier. For split supply operation, the $\overline{Pd}$ pins must be pulled to below -Vs + 0.54V to disable.

Since the ISL55211 operates as a differential inverting op amp, there is only modest signal path isolation when disabled, as shown in Figure 24. The inputs include 2 pairs of back to back low capacitance diodes intended to protect any subsequent devices from large input signals during shutdown. Those diodes limit the maximum overdrive voltage across the input to approximately 1.0V in each polarity. The internal R_G resistors of Test Circuit 1 limit the current into those diodes under this condition.

The supply current in shutdown does not reduce to zero as internal circuitry is still active to hold the output common mode voltage at the V_{CM} voltage even during shutdown. This is intended to hold the ISL55211 outputs near the desired common mode output level during shutdown. This improves the turn on characteristic and keeps those output voltages in a safe range for downstream circuitry.

The very low internal power dissipation of the ISL55211, along with the excellent thermal conductivity of the TQFN package when the exposed metal pad is tied to a conductive plate, reduces the T_J rise above ambient to very modest levels. Assuming a nominal 115mW dissipation and using the 63°C/W measured thermal impedance from Junction to ambient, gives a rise of only 0.115*63 = 7.2°C. Operation at elevated ambient temperatures is easily supported given this very low internal rise to junction.

The maximum internal junction temperatures would occur at maximum supply voltage, +85°C maximum ambient operating, and where the TQFN exposed pad is not tied to a conductive layer. Where the TQFN must be mounted with an insulating layer to the exposed metal plate, such as in a split supply application, device measurements show an increased thermal impedance junction to ambient of +120°C/W. Using this, and a maximum quiescent internal power on 4.5V absolute maximum, which shows 45mA for +85°C maximum operating ambient from Figure 27, we get 4.5V*45mA*+120°C/W = +24°C rise above +85°C or approximately +109°C operating T_J maximum - still well below the specified Absolute Maximum operating junction temperature of +135°C.

Noise Analysis

The decompensated voltage feedback design of the ISL55211 provides very low input voltage and current noise. Based on the ISL55210, these internal noise terms are 0.85nV/√Hz differential voltage noise and a 5pA/√Hz current noise term on each side. Since the ISL55211 is an internally fixed gain version, these internal noise terms will produce only a few set of output noise values. Figure 34 shows the analysis model for just the ISL55211 with no input transformer while Table 3 shows the resulting output and input referred differential spot noise voltages using Equation 1.

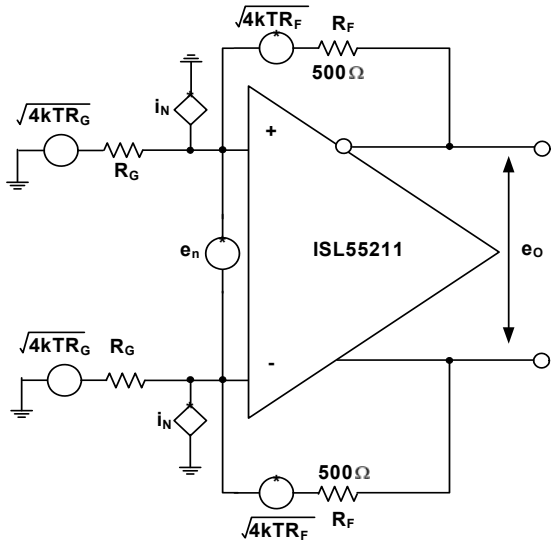


FIGURE 34. AMPLIFIER ONLY NOISE MODEL

With equal feedback and gain resistors, the total output noise expression becomes very simple. This is shown as Equation 1.

$$e_0\sqrt{(e_N{*}NG)^2+2(i_NR_F)^2+2(4kTR_FNG)} \quad \text{(EQ. 1)}$$

The NG term in this equation is the Noise Gain = 1 + R_F/R_G. The last term in Equation 1 captures both the R_F and R_G resistor noise terms. Table 3 evaluates this expression for the 3 possible internal gains with a fixed 500Ω internal feedback. nV/√HZ

TABLE 3. OUTPUT AND INPUT SPOT NOISE FROM EQUATION 1 FOR THE 3 GAINS OF THE ISL55211

R_G (Ω)	GAIN V/V	NOISE GAIN V/V	INPUT REFERRED	
			E_O nV/√Hz	E_{NI} nV/√Hz
250	2	3	8.19	4.09
125	4	5	10.51	2.63
100	5	6	11.60	2.32

TABLE 4. OUTPUT NOISE AND INPUT REFERRED EQUIVALENT NOISE FOR THE TRANSFORMER COUPLED INPUT

ISL55211 INTENDED TRANSFORMER + INTERNAL GAIN SETTINGS						NOISE GAIN V/V	INPUT REFERRED	
INPUT XFMR TURNS RATIO	INTERNAL R_G VALUE (Ω)	GAIN (V/V) V_O/V_I	GAIN (dB) V_O/V_I	EXTERNAL R_T VALUE (Ω)	TOTAL GAIN RESISTOR FOR NG (Ω)		E_O nV/√Hz	E_{NI} nV/√Hz
1:1.4	250	2.8	9	122	277.48	2.80	7.94	2.834811
1:1.4	125	5.6	15	162	155.92	4.21	9.62	1.718338
1:1.4	100	7	17	192	132.88	4.76	10.25	1.46452
1:2	250	4	12	333	312.48	2.60	7.68	1.920066
1:2	125	8	18	1020	208.61	3.40	8.67	1.083876
1:2	100	10	20	100[8]	200.00	3.50	8.79	0.879492

Adding an input transformer can improve the input referred noise by adding a noiseless voltage gain. Starting from Test Circuit 1 of Figure 29, and assuming the source shows a matched broadband source R_S that will be matched by the input referred parallel combination of $2*R_G||R_T$, a noise gain analysis circuit can be developed as shown in Figure 35.

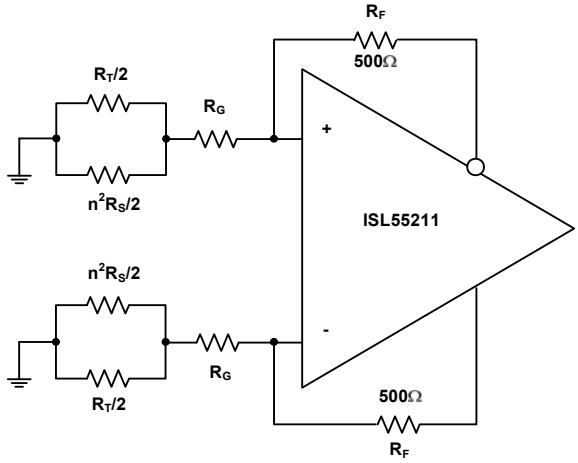


FIGURE 35. NOISE GAIN MODEL FOR THE TRANSFORMER COUPLED INPUT CIRCUIT OF FIGURE 29

Stepping through the 3 gain settings with two input transformers will allow the noise gain to be calculated for the circuit of Figure 35, which is all that is needed in Equation 1 to arrive at an output differential noise (since R_F is fixed at 500Ω). Doing this gives Table 4.

The signal gain is taken from the input of the transformer for this analysis and shows the total input referred noise going below 0.9nV at the highest gain setting here. While this analysis is including the approximate 0.9nV noise of a 50Ω source R, that noise is assumed to be divided down by 2 to the input of the transformer, which explains the total input referred noise showing up as less than just a 50Ω resistor. The total output differential noise goes below 9nV/√Hz at the higher gains settings using this input transformer technique. For even lower noise, consider the ISL55210 where the input R_T element is generally not required. In that case, simply setting R_G to the desired input Z and adjusting R_F to the desired gain will give an output noise that is slightly lower than shown previously for the same input transformer due to the removal of the R_T element.

Driving Cap and Filter Loads

Most applications will drive a resistive or filter load. The ISL55211 is robust to direct capacitive load on the outputs up to approximately 10pF. For frequency response flatness, it is best to avoid any output pin capacitance as much as possible - as the capacitance increases, the high frequency portion of the ISL55211 (>1GHz) response will start to show considerable peaking. No oscillations were observed up through 10pF load on each output.

For AC-coupled applications, an output network that is a small series resistor (10 to 50Ω) into a blocking capacitor is preferred. This series resistor will isolate parasitic capacitance to ground from the internally closed loop output stage of the amplifier and de-que the self resonance of the blocking capacitors. Once the output stage sees this resistive element first, the remaining part of a passive filter design can be done without fear of amplifier instability.

Driving ADC's

Many of the intended applications for the ISL55211 are as a low power, very high dynamic range, last stage interface to high performance ADC's. The lowest power ADC's, such as the ISLA214P50 shown on the front page, include an innovative "Femto-Charge™" internal architecture that eliminates op amps from the ADC design and only passes signal charge from stage to stage. This greatly reduces the required quiescent power for these ADC's but then that signal charge has to be provided by the external circuit at the two input pins. This appears on an ADC like the ISLA112P50 as a clock rate dependent common mode input current that must be supplied by the interface circuit. At 500MHz, this DC current is 1.3mA on each input for the 14-bit ISLA214P50.

Most interfaces will also include an interstage noise power bandlimiting filter between the amplifier and the ADC. This filter needs to be designed considering the loading of the amplifier, any V_{CM} level shifting that needs to take place, the filter shape, and this Icm issue into the ADC input pins. Here are 4 example topologies suitable for different situations.

1. AC-coupled, broadband RLC interstage filter design. This approach lets the amplifier operate at its desired output common mode, then provides the ADC common mode voltage and current through a bias path as part of the filters designs last stage R values. The V_b is set to include the IR loss from that voltage to the ADC inputs due to the I_{CM} current.

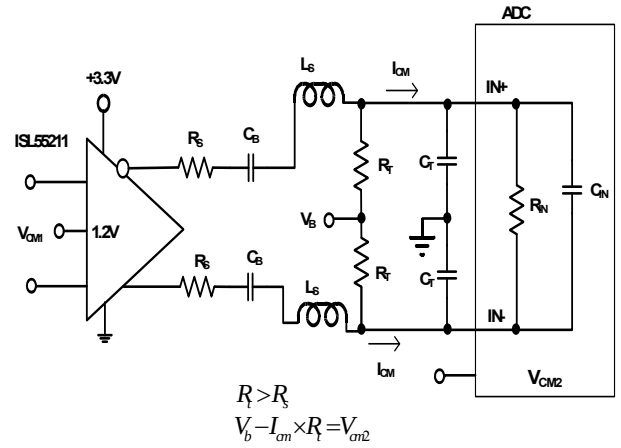


FIGURE 36. AC- COUPLED BROADBAND RLC INTERSTAGE FILTER DESIGN

2. AC-coupled, higher frequency range interstage filter design. This design replaces the R_T resistors in Figure 35 with large valued inductors and implements the filter just using shunt resistors at the end of the RLC filter. In this case, the ADC V_{CM} can be tied to the centerpoint of the bias path inductors (very much like a Bias-T) to provide the common mode voltage and current to the ADC inputs. These bias inductors do limit the low frequency end of the operation where, with 1µH values, operation from 10MHz to 200MHz is supported using the approach of Figure 37.

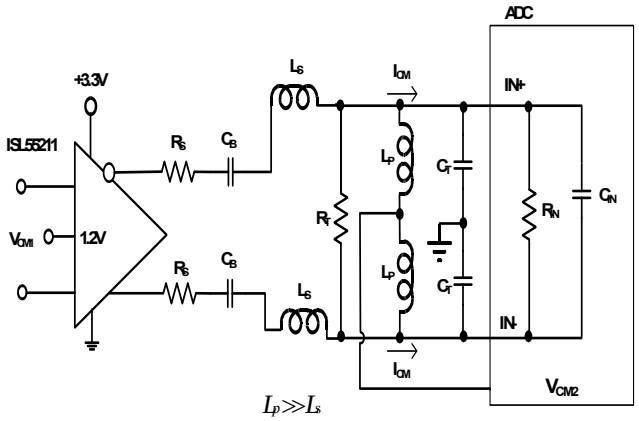


FIGURE 37. AC-COUPLED, HIGHER FREQUENCY RLC INTERSTAGE FILTER DESIGN

3. AC-coupled with output side transformer. This design includes an output side transformer, very similar to ADC characterization circuits. This approach allows a slightly lower amplifier output swing (if N>1 is used) and very easy 2nd or 3rd order low pass responses to be implemented. It also provides the I_{CM} and V_{CM} bias to the ADC through the transformer centertap. This approach would be attractive for higher ADC input swing targets and more aggressive noise power bandwidth control needs. Figure 1 on page 1 is an example showing this approach.

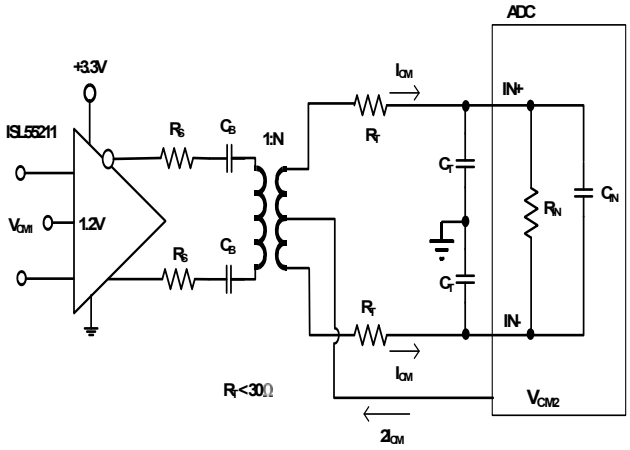


FIGURE 38. AC-COUPLED WITH OUTPUT SIDE TRANSFORMER

4. DC-coupled with ADC V_{CM} and I_{CM} provided from the amplifier. Here, DC to very high frequency interstage low pass filter can be provided. Again, the R_S element must be low to reduce the IR drop from the V_{CM} of the converter, which now shows up on the output of the ISL55211, to the ADC input pins.

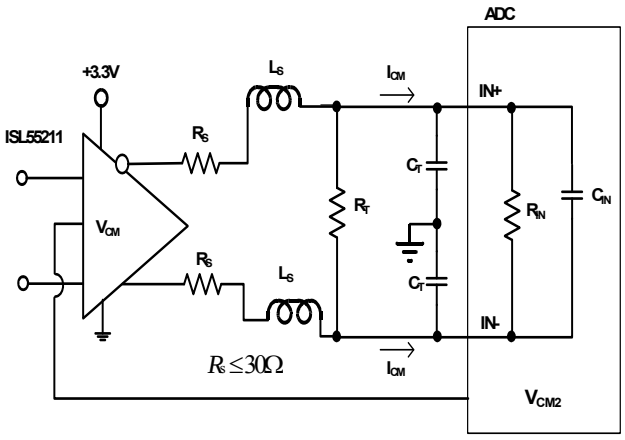


FIGURE 39. DC-COUPLED WITH A V_{CM} VOLTAGE FROM THE ADC

Layout Considerations

The ISL55211 pinout is organized to isolate signal I/O along one axis of the package with ground, power and control pins on the other axis. Ground and power should be planes coming into the upper and lower sides of the package (see “Pin Configuration” on page 2). The signal I/O should be laid out as tight as possible.

The ground pins and package backside metal contact should be connected into a good ground plane. The power supply should have both a large values electrolytic cap to ground, then a high frequency ferrite beads, then 0.01µF SMD ceramic caps at the supply pins. Some improvement in HD2 performance may be experienced by placing and X2Y cap between the two Vs+ pins and ground underneath the package on the board back side. This is 3 terminal device that is included in the Evaluation board layout.

Evaluation Board (Rev. C)

Test circuit 1 (Figure 29) is implemented on an Evaluation Board available from Intersil. This board includes a number of optional features that not populated as the board is delivered. The full Evaluation circuit is shown in Figure 40 where unloaded (optional) elements are shown in green.

The nominal supply voltage for the board and device is a single 3.3V supply. From this, the ISL55210, ISL55211 generates an internal common mode voltage of approximately 1.2V. That voltage can be overridden by populating the two resistors and potentiometer shown as R_{19} to R_{21} above.

The primary test purpose for this board is to implement different interstage differential passive filters intended for the ADC interface along with the ADC input impedances. The board is delivered with only the output R's loaded to give a 200Ω differential load. This is done using the two 85Ω resistors as R9 and R_{10}, then the 4 0Ω elements (R_{10}, R_{12}, R_{24}, and R_{25}) and finally the two shunt elements R_{13} and R_{14} set to 35.5Ω. Including the 50Ω measurement load on the output side of the 1:1 transformer reflecting in parallel with the two 35Ω resistors takes the nominal AC shunt impedance to 71Ω||50Ω = 29.3Ω. This adds to the two 85Ω series output elements to give a total load across the amplifier outputs of 170Ω + 29.3Ω = 199.3Ω.

To test a particular ADC interface RLC filter and converter input impedance, replace R_{11} and R_{12} with RF chip inductors, load C_{10} and C_{11} with the specified ADC input capacitance and R_{26} with the specified ADC differential input R. With these loaded, the remaining resistive elements (R_{24}, R_{25}, R_{13}, R_{14}) are set to hit a desired total parallel impedance to implement the desired filter (must be < than the ADC input differential R since that sits in parallel with any "external" elements) and achieve a 250Ω source looking into each side of the tap point transformer.

This Evaluation board includes a user's manual showing a number of example circuits and tested results and is available on the Intersil web site on the ISL55211 Product Information Page.

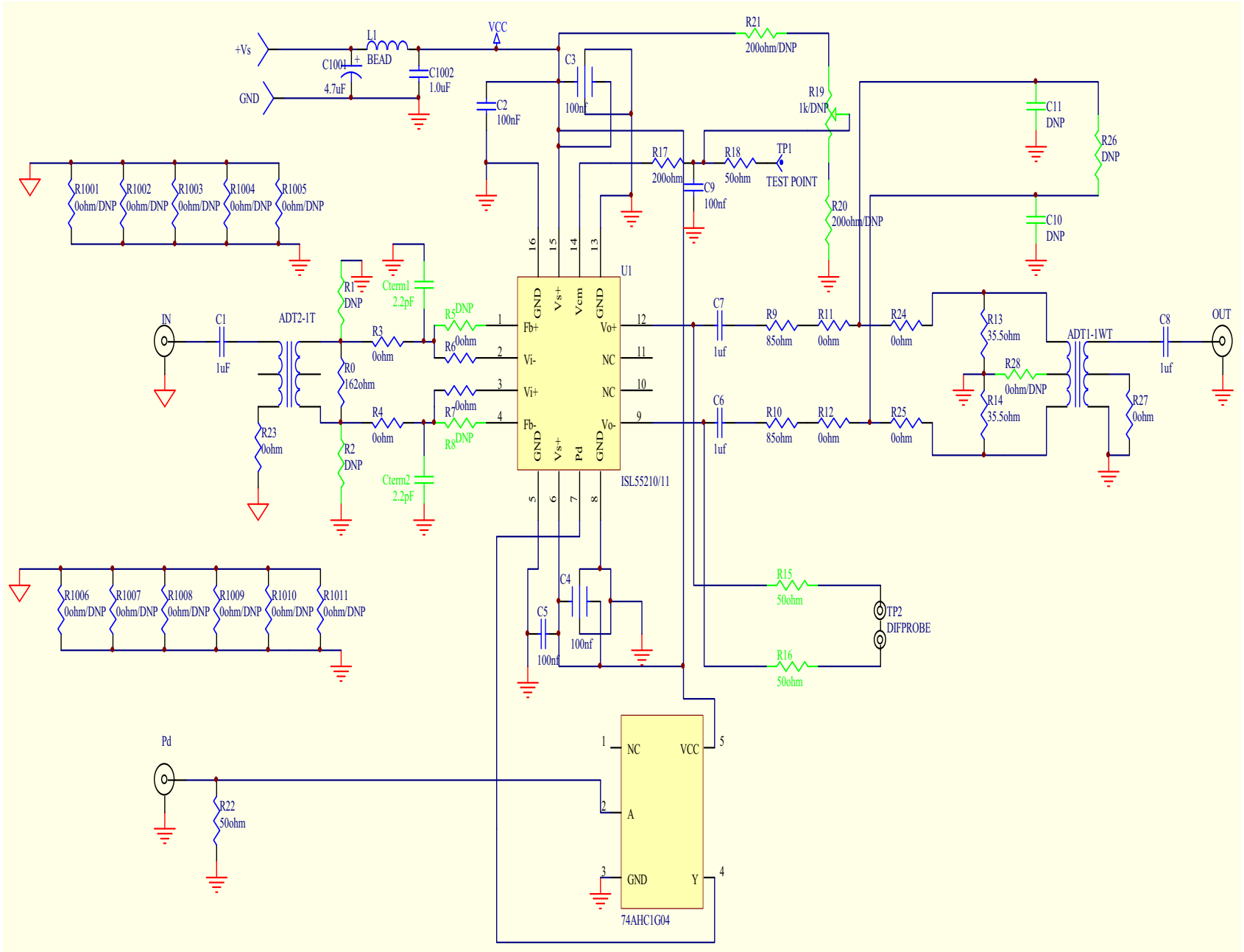


FIGURE 40. ISL55210, ISL55211 SINGLE INPUT TRANSFORMER EVALUATION BOARD REV C

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
June 21, 2011	FN7868.0	Initial Release

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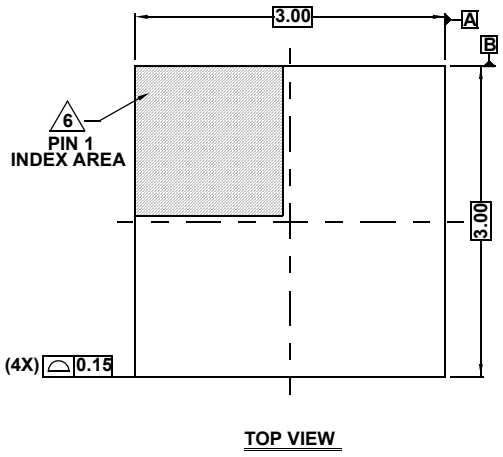
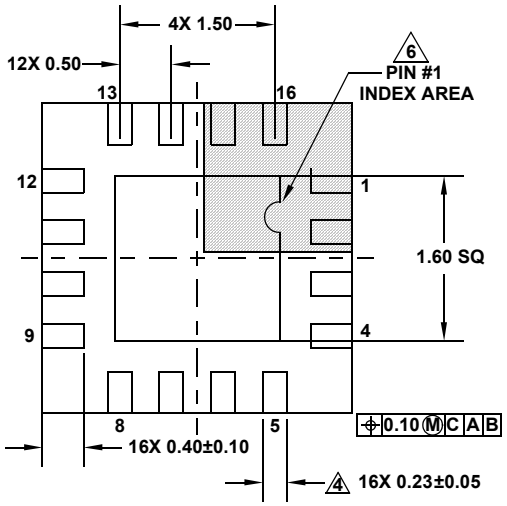
Package Outline Drawing

L16.3x3D

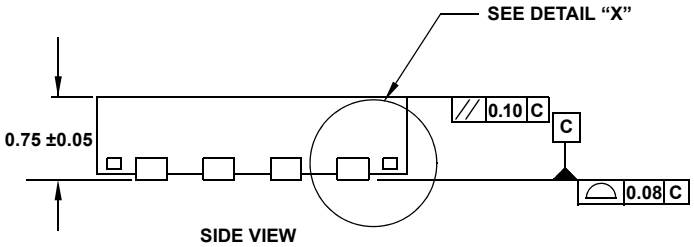
16 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 3/10



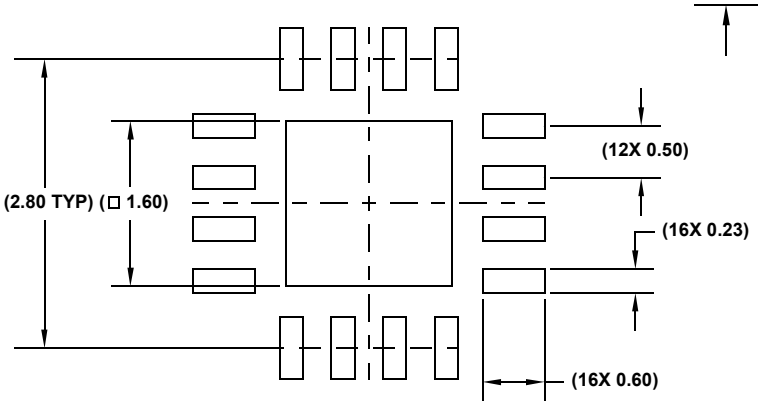
TOP VIEW



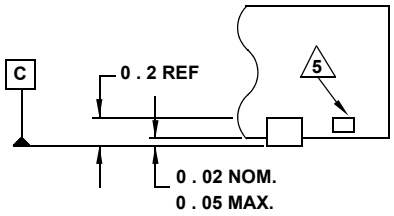
BOTTOM VIEW



SIDE VIEW



TYPICAL RECOMMENDED LAND PATTERN



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.25mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. JEDEC reference drawing: MO-220 WEED.