

ISL54214

USB 2.0 High-Speed x 2 Channels/Stereo Audio Dual SP3T
(Dual 3 to 1 Multiplexer)

FN6816
Rev 3.00
June 28, 2010

The Intersil ISL54214 is a single supply dual SP3T analog switch that operates from a single supply in the range of 2.7V to 4.6V. It was designed to multiplex between audio stereo signals and two different USB 2.0 high speed differential data signals. The audio channels allow signal swings below ground, allowing the multiplexing of the voice and data signals through a common headphone connector in Personal Media Players and other portable battery powered devices.

The audio switch cells can pass $\pm 1V$ ground referenced audio signals with very low distortion ($< 0.03\%$ THD+N when driving 5mW into 32Ω loads). The USB switch cells have very low ON capacitance (8pF) and high bandwidth to pass USB high speed signals (480Mbps) with minimal edge and phase distortion.

The ISL54214 is available in a tiny 12 Ld 2.2mmx1.4mm ultra-thin QFN and 12 Ld 3mmx3mm TQFN packages. It operates over a temperature range of -40 to $+85^\circ C$.

Related Literature

- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"

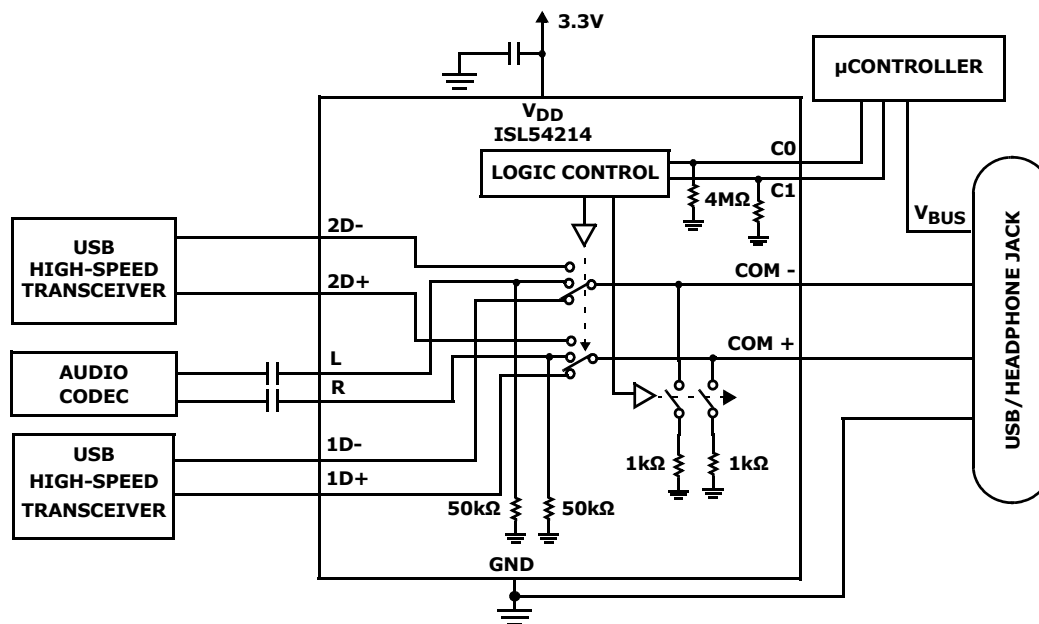
Features

- High Speed (480Mbps) and Full Speed (12Mbps) Signaling Capability per USB 2.0
- Low Distortion Negative Signal Capability Audio Switches
- Power OFF Protection
- COM Pins Overvoltage Tolerant to 5.5V
- Low Distortion Headphone Audio Signals - 0.03% THD+N at 5mW into 32Ω Load
- -98dB cross-talk (100kHz)
- 95.5dB OFF-Isolation (100kHz)
- 2.7V to 4.6V Single Supply Operation (V_{DD})
- 700MHz of -3dB Bandwidth USB Switches
- Available in Tiny 12 Ld μ TQFN and TQFN Packages
- Compliant with USB 2.0 Short Circuit Requirements Without Additional External Components
- Pb-Free (RoHS Compliant)

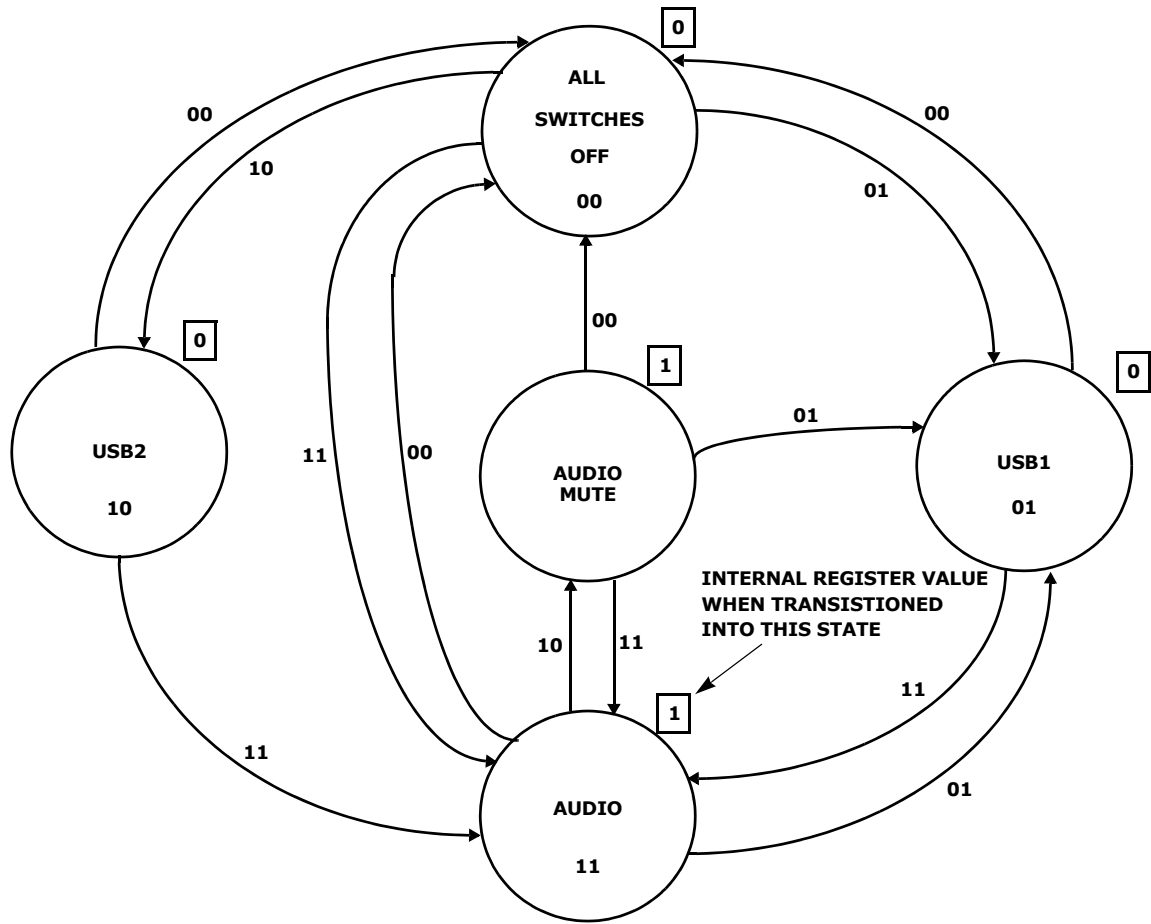
Applications

- MP3 and other Personal Media Players
- Cellular/Mobile Phone

Application Block Diagram



State Diagram

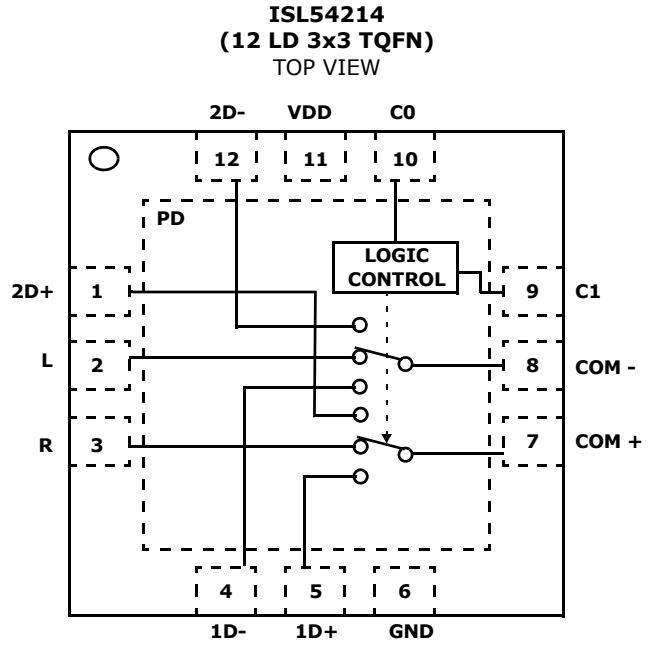
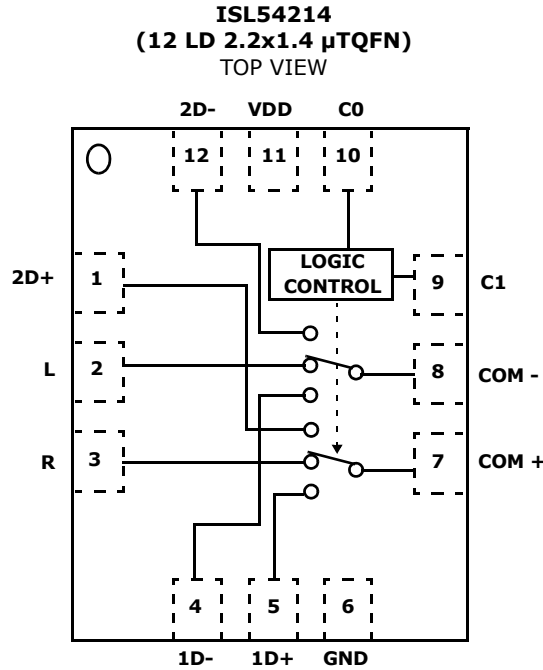


Truth Table

CURRENT CODE		LAST CODE		MODE	SHUNT SWITCHES		REGISTER
C1	C0	C1	C0		1kΩ COM SHUNTS		
0	0	X	X	ALL SWITCHES OFF	OFF	0	
0	1	X	X	USB1	OFF	0	
1	0	0	0	USB2	OFF	0	
1	0	0	1	USB2	OFF	0	
1	0	1	0	USB2	OFF	0	
1	1	X	X	AUDIO	OFF	1	
1	0	1	0	MUTE	ON	1	
1	0	1	1	MUTE	ON	1	

C0, C1: Logic "0" when ≤ 0.5V or float, Logic "1" when ≥ 1.4V with V_{DD} in range of 2.7V to 3.6V.

Pin Configurations



NOTE:

- ISL54214 Switches Shown for C1 = Logic "1" and C0 = Logic "1". The R and L 50kΩ pull-down resistors, C1 and C0 4MΩ pull-down resistors and COM- and COM+ 1kΩ Shunts are not shown.

Pin Descriptions

μTQFN	TQFN	NAME	FUNCTION
1	1	2D+	USB2 Differential Input
2	2	L	Audio Left Input
3	3	R	Audio Right Input
4	4	1D-	USB1 Differential Input
5	5	1D+	USB1 Differential Input
6	6	GND	Ground Connection
7	7	COM+	Voice and Data Common Pin

Pin Descriptions (Continued)

μTQFN	TQFN	NAME	FUNCTION
8	8	COM-	Voice and Data Common Pin
9	9	C1	Digital Control Input
10	10	C0	Digital Control Input
11	11	VDD	Power Supply
12	12	2D-	USB2 Differential Input
-	-	PD	Thermal Pad. Tie to Ground or Float (TQFN only)

Ordering Information

PART NUMBER (Note 5)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL54214IRUZ-T (Note 2, 3)	GJ	-40 to +85	12 Ld 2.2mmx1.4mm μ TQFN (Tape and Reel)	L12.2.2x1.4A
ISL54214IRTZ (Note 4)	4214	-40 to +85	12 Ld 3mmx3mm TQFN	L12.3x3A
ISL54214IRTZ-T (Notes 2, 4)	4214	-40 to +85	12 Ld 3mmx3mm TQFN (Tape and Reel)	L12.3x3A
ISL54214EVAL1Z	Evaluation Board			

NOTES:

- Please refer to [TB347](#) for details on reel specifications.
- These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
- These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
- For Moisture Sensitivity Level (MSL), please see device information page for [ISL54214](#). For more information on MSL please see techbrief [TB363](#).

Absolute Maximum Ratings

V_{DD} to GND	-0.3V to 5.5V
Input Voltages	
1D+, 1D-, L, R, 2D+, 2D-	-2V to 5.5V
C0, C1 (Note 6)	-0.3V to 5.5V
Output Voltages	
COM-, COM+	-2V to 5.5V
Continuous Current (L, R)	±60mA
Peak Current (L, R)	
(Pulsed 1ms, 10% Duty Cycle, Max)	±120mA
Continuous Current (1D-, 1D+, 2D-, 2D+)	±40mA
Peak Current (1D-, 1D+, 2D-, 2D+)	
(Pulsed 1ms, 10% Duty Cycle, Max)	±100mA
ESD Rating:	
Human Body Model	>5kV
Machine Model	>500V
Charged Device Model	>2kV
Latch-up Tested per JEDEC; Class II Level A	at 85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

- Signals on C1 and C0 exceeding GND by specified amount are clamped. Limit current to maximum current ratings.
- θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
- For θ_{JC} , the "case temp" location is taken at the package top center.
- θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
- For θ_{JC} , the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications - 2.7V to 3.6V Supply Test Conditions: $V_{DD} = +3.0V$, GND = 0V, V_{COH} , $V_{C1H} = 1.4V$, V_{COL} , $V_{C1L} = 0.5V$, (Note 11), Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 12, 13)	TYP	MAX (Notes 12, 13)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Audio Switches (L, R)						
Analog Signal Range, V_{ANALOG}	$V_{DD} = 3.0V$ to 3.6V, Audio Mode (C0 = V_{DD} , C1 = V_{DD})	Full	-1.5	-	1.5	V
ON-Resistance, r_{ON}	$V_{DD} = 3.0V$, Audio Mode (C0 = 1.4V, C1 = 1.4V), $I_{COMx} = 60mA$, V_L or $V_R = -0.85V$ to 0.85V, (See Figure 3, Note 15)	+25	-	2.3	2.8	Ω
		Full	-	-	3.4	Ω
r_{ON} Matching Between Channels, Δr_{ON}	$V_{DD} = 3.0V$, Audio Mode (C0 = 1.4V, C1 = 1.4V), $I_{COMx} = 60mA$, V_L or $V_R =$ Voltage at max r_{ON} over signal range of -0.85V to 0.85V, (Notes 15, 16)	+25	-	0.04	0.25	Ω
		Full	-	-	0.26	Ω
r_{ON} Flatness, $r_{FLAT(ON)}$	$V_{DD} = 3.0V$, Audio Mode (C0 = 1.4V, C1 = 1.4V), $I_{COMx} = 60mA$, V_L or $V_R = -0.85V$ to 0.85V, (Notes 14, 15)	+25	-	0.03	0.05	Ω
		Full	-	-	0.07	Ω
USB/DATA Switches (1D+, 1D-, 2D+, 2D-)						
Analog Signal Range, V_{ANALOG}	$V_{DD} = 2.7V$ to 4.6V, USB1 mode (C0 = 0V, C1 = V_{DD}) or USB2 Mode (C0 = V_{DD} , C1 = 0V)	Full	-1	-	V_{DD}	V
ON-Resistance, r_{ON}	$V_{DD} = 2.7V$, USB1 mode (C0 = 0.5V, C1 = 1.4V) or USB2 Mode (C0 = 1.4V, C1 = 0.5V), $I_{COMx} = 40mA$, V_{D+} or $V_{D-} = 0V$ to 400mV (See Figure 4, Note 15)	25	-	6.2	8	Ω
		Full	-	-	10	Ω
r_{ON} Matching Between Channels, Δr_{ON}	$V_{DD} = 2.7V$, USB1 mode (C0 = 0.5V, C1 = 1.4V) or USB2 Mode (C0 = 1.4V, C1 = 0.5V), $I_{COMx} = 40mA$, V_{D+} or $V_{D-} =$ Voltage at max r_{ON} , (Notes 15, 16)	25	-	0.08	0.5	Ω
		Full	-	-	0.55	Ω

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
12 Ld μ TQFN Package (Note 7, 8)	155	90
12 Ld TQFN Package (Notes 9, 10)	58	1.0
Maximum Junction Temperature (Plastic Package)	+150°C	
Maximum Storage Temperature Range	-65°C to +150°C	
Pb-Free Reflow Profile	see link below	
	http://www.intersil.com/pbfree/Pb-FreeReflow.asp	

Operating Conditions

Temperature Range	-40°C to +85°C
Supply Voltage Range	2.7V to 4.6V

Electrical Specifications - 2.7V to 3.6V Supply Test Conditions: $V_{DD} = +3.0V$, $GND = 0V$, V_{C0H} , $V_{C1H} = 1.4V$, V_{C0L} , $V_{C1L} = 0.5V$, (Note 11), Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 12, 13)	TYP	MAX (Notes 12, 13)	UNITS
r_{ON} Flatness, $r_{FLAT(ON)}$	$V_{DD} = 2.7V$, USB1 mode ($C0 = 0.5V$, $C1 = 1.4V$) or USB2 Mode ($C0 = 1.4V$, $C1 = 0.5V$), $I_{COMx} = 40mA$, V_{D+} or $V_{D-} = 0V$ to $400mV$, (Notes 14, 15)	25	-	0.26	1	Ω
		Full	-	-	1.2	Ω
ON-Resistance, r_{ON}	$V_{DD} = 3.3V$, USB1 mode ($C0 = 0.5V$, $C1 = 1.4V$) or USB2 Mode ($C0 = 1.4V$, $C1 = 0.5V$), $I_{COMx} = 40mA$, V_{D+} or $V_{D-} = 3.3V$ (See Figure 4, Note 15)	+25	-	9.8	20	Ω
		Full	-	-	25	Ω
OFF Leakage Current, $I_{D+(OFF)}$ or $I_{D-(OFF)}$	$V_{DD} = 3.6V$, All OFF Mode ($C0 = 0.5V$, $C1 = 0.5V$), V_{COM-} or $V_{COM+} = 0.5V$, $0V$, V_{D+} or $V_{D-} = 0V$, $0.5V$, $L = R = float$	25	-15	0.11	15	nA
		Full	-20	-	20	nA
ON Leakage Current, I_{DX}	$V_{DD} = 3.3V$, USB1 mode ($C0 = 0.5V$, $C1 = 1.4V$) or USB2 Mode ($C0 = 1.4V$, $C1 = 0.5V$), V_{D+} or $V_{D-} = 2.7V$, $COM- = COM+ = Float$, L and $R = float$	25	-20	2.4	20	nA
		Full	-25	-	25	nA
DPDT DYNAMIC CHARACTERISTICS						
All OFF to USB or USB to All OFF Address Transition Time, t_{TRANS}	$V_{DD} = 2.7V$, $R_L = 50\Omega$, $C_L = 10pF$, (see Figure 1)	25	-	175	-	ns
Audio to USB1 Address Transition Time, t_{TRANS}	$V_{DD} = 2.7V$, $R_L = 50\Omega$, $C_L = 10pF$, (see Figure 1)	25	-	12	-	μs
Break-Before-Make Time Delay, t_D	$V_{DD} = 3.6V$, $R_L = 50\Omega$, $C_L = 10pF$, (see Figure 2)	25	-	52	-	ns
Skew, ($t_{SKEWOUT} - t_{SKEWIN}$)	$V_{DD} = 3.0V$, USB1 mode ($C0 = 0V$, $C1 = V_{DD}$) or USB2 Mode ($C0 = V_{DD}$, $C1 = 0V$), $R_L = 45\Omega$, $C_L = 10pF$, $t_R = t_F = 500ps$ at 480Mbps, (Duty Cycle = 50%) (see Figure 7)	25	-	75	-	ps
Total Jitter, t_j	$V_{DD} = 3.0V$, USB1 mode ($C0 = 0V$, $C1 = V_{DD}$) or USB2 Mode ($C0 = V_{DD}$, $C1 = 0V$), $R_L = 50\Omega$, $C_L = 10pF$, $t_R = t_F = 500ps$ at 480Mbps	25	-	210	-	ps
Rise/Fall Degradation (Propagation Delay), t_{PD}	$V_{DD} = 3.0V$, USB1 mode ($C0 = 0V$, $C1 = V_{DD}$) or USB2 Mode ($C0 = V_{DD}$, $C1 = 0V$), $R_L = 45\Omega$, $C_L = 10pF$, (see Figure 7)	25	-	250	-	ps
Audio Crosstalk R to COM-, L to COM+	$V_{DD} = 3.0V$, Audio Mode ($C0 = V_{DD}$, $C1 = V_{DD}$), $R_L = 32\Omega$, $f = 20Hz$ to $20kHz$, V_R or $V_L = 0.707V_{RMS}$ (see Figure 6)	25	-	-88	-	dB
Crosstalk (Audio to USB, USB to Audio)	$V_{DD} = 3.0V$, $R_L = 50\Omega$, $f = 100kHz$	25	-	-98	-	dB
OFF-Isolation	$V_{DD} = 3.0V$, $R_L = 50\Omega$, $f = 100kHz$	25	-	95.5	-	dB
Audio OFF-Isolation (All OFF Mode)	$V_{DD} = 3.0V$, $C0 = 0V$, $C1 = 0V$, $R_L = 32\Omega$, $f = 20Hz$ to $20kHz$	25	-	115	-	dB
Audio OFF-Isolation (Mute Mode)	$V_{DD} = 3.0V$, $C1 = V_{DD}$, $C0 = 0V$, $R_L = 32\Omega$, $f = 20Hz$ to $20kHz$	25	-	105	-	dB
Audio OFF-Isolation (Mute Mode)	$V_{DD} = 3.0V$, $C1 = V_{DD}$, $C0 = 0V$, $R_L = 20k\Omega$, $f = 20Hz$ to $20kHz$	25	-	77	-	dB
Total Harmonic Distortion	$f = 20Hz$ to $20kHz$, $V_{DD} = 3.0V$, $C0 = V_{DD}$, $C1 = V_{DD}$, L or $R = 0.707V_{RMS}$ ($2 V_{p-p}$), $R_L = 32\Omega$	25	-	0.045	-	%
Total Harmonic Distortion	$f = 20Hz$ to $20kHz$, $V_{DD} = 3.0V$, $C0 = V_{DD}$, $C1 = V_{DD}$, $5mW$ into $R_L = 32\Omega$	25	-	0.025	-	%
USB Switch -3dB Bandwidth	Signal = $0dBm$, $0.2VDC$ offset, $R_L = 50\Omega$, $C_L = 5pF$	25	-	700	-	MHz
Audio Switch -3dB Bandwidth	Signal = $0dBm$, $R_L = 50\Omega$, $C_L = 5pF$	25	-	330	-	MHz

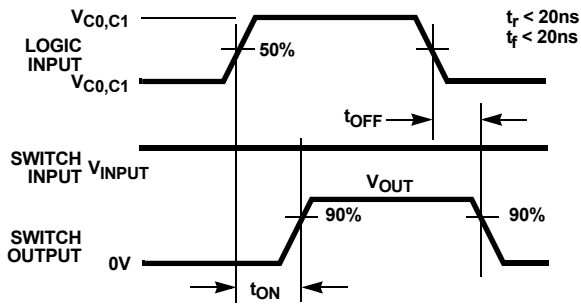
Electrical Specifications - 2.7V to 3.6V Supply Test Conditions: $V_{DD} = +3.0V$, $GND = 0V$, V_{C0H} , $V_{C1H} = 1.4V$, V_{C0L} , $V_{C1L} = 0.5V$, (Note 11), Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 12, 13)	TYP	MAX (Notes 12, 13)	UNITS
1D+/1D- OFF Capacitance, C_{1D+OFF} , C_{1D-OFF}	$f = 1MHz$, $V_{DD} = 3.0V$, $C0 = V_{DD}$, $C1 = V_{DD}$, V_{D-} or $V_{D+} = V_{COMx} = 0V$, (see Figure 5)	25	-	3	-	pF
L/R OFF Capacitance, C_{LOFF} , C_{ROFF}	$f = 1MHz$, $V_{DD} = 3.0V$, $C0 = 0V$, $C1 = V_{DD}$, L or R = $COMx = 0V$, (see Figure 5)	25	-	5	-	pF
2D+/2D- OFF Capacitance, C_{2D+OFF} , C_{2D-OFF}	$f = 1MHz$, $V_{DD} = 3.3V$, $C0 = V_{DD}$, $C1 = V_{DD}$, Tx or Rx = $COMx = 0V$, (See Figure 5)	25	-	3	-	pF
COM ON Capacitance, $C_{COM-(ON)}$, $C_{COM+(ON)}$	$f = 1MHz$, $V_{DD} = 3.0V$, USB Mode ($C0 = 0V$, $C1 = V_{DD}$), D- or D+ = $COMx = 0V$, (see Figure 5)	25	-	8	-	pF
POWER SUPPLY CHARACTERISTICS						
Power Supply Range, V_{DD}		Full	2.7		4.6	V
Positive Supply Current, I_{DD} (ALL OFF Mode)	$V_{DD} = 3.6V$, $C1 = GND$, $C0 = GND$	25	-	6.2	8	μA
		Full	-	-	15	μA
Positive Supply Current, I_{DD} (USB1 Mode)	$V_{DD} = 3.6V$, $C1 = GND$, $C0 = V_{DD}$	25	-	6.5	8	μA
		Full	-	-	15	μA
Positive Supply Current, I_{DD} (USB2 Mode)	$V_{DD} = 3.6V$, $C1 = V_{DD}$, $C0 = GND$	25	-	6.2	8	μA
		Full	-	-	15	μA
Positive Supply Current, I_{DD} (Audio Mode)	$V_{DD} = 3.6V$, Audio Mode ($C0 = C1 = V_{DD}$)	25	-	9	14	μA
		Full	-	-	20	μA
Positive Supply Current, I_{DD} (MUTE Mode)	$V_{DD} = 3.6V$, $C1 = V_{DD}$, $C0 = GND$	25	-	6.6	8	μA
		Full	-	-	15	μA
Power OFF $COMx$ Current, I_{COMx}	$V_{DD} = 0V$, $C0 = C1 = \text{Float}$, $COMx = 5.25V$	25	-	-	4	μA
Power OFF Logic Current, I_{C0} , I_{C1}	$V_{DD} = 0V$, $C0 = C1 = 5.25V$	25	-	11	-	μA
Power OFF D+/D- Current, I_{XD+} , I_{XD-}	$V_{DD} = 0V$, $C0 = C1 = \text{Float}$, $XD- = XD+ = 5.25V$	25	-	5	-	μA
DIGITAL INPUT CHARACTERISTICS						
$C0$, $C1$ Voltage Low, V_{C0L} , V_{C1L}	$V_{DD} = 2.7V$ to $3.6V$	Full	-	-	0.5	V
$C0$, $C1$ Voltage High, V_{C0H} , V_{C1H}	$V_{DD} = 2.7V$ to $3.6V$	Full	1.4	-	5.25	V
$C0$, $C1$ Input Current, I_{C0L} , I_{C1L}	$V_{DD} = 3.6V$, $C0 = C1 = 0V$ or Float	Full	-50	6.2	50	nA
$C0$, $C1$ Input Current, I_{C0H} , I_{C1H}	$V_{DD} = 3.6V$, $C0 = C1 = 3.6V$	Full	-2	1.6	2	μA
$C0$, $C1$ Pull-Down Resistor, R_{Cx}	$V_{DD} = 3.6V$, $C0 = C1 = 3.6V$, Measure current into $C0$ or $C1$ pin and calculate resistance value.	Full	-	4	-	M Ω

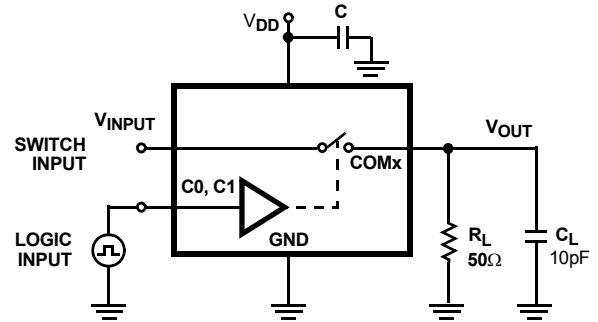
NOTES:

- V_{logic} = Input voltage to perform proper function.
- The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
- Flatness is defined as the difference between maximum and minimum value of on-resistance over the specified analog signal range.
- Limits established by characterization and are not production tested.
- r_{ON} matching between channels is calculated by subtracting the channel with the highest max r_{ON} value from the channel with lowest max r_{ON} value, between L and R or between 1D+ and 1D- or between 2D+ and 2D-.

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.



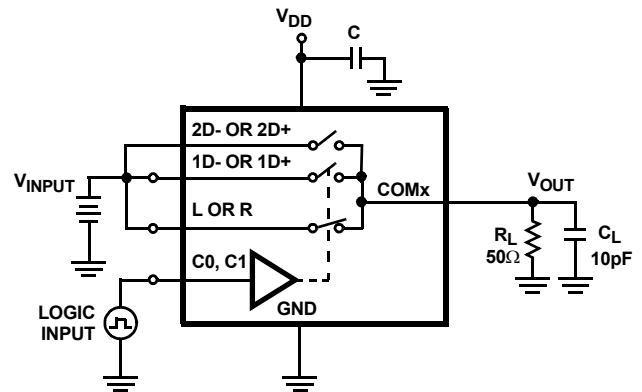
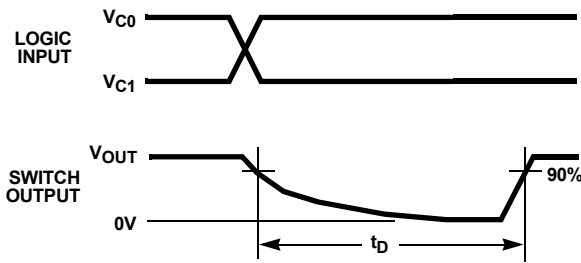
Repeat test for all switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(INPUT)} \frac{R_L}{R_L + r_{ON}}$$

FIGURE 1A. ADDRESS t_{TRANS} MEASUREMENT POINTS

FIGURE 1B. ADDRESS t_{TRANS} TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

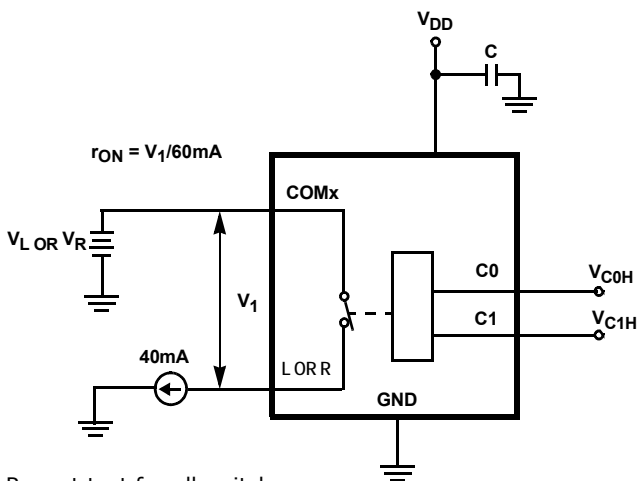


Repeat test for all switches. C_L includes fixture and stray capacitance.

FIGURE 2A. MEASUREMENT POINTS

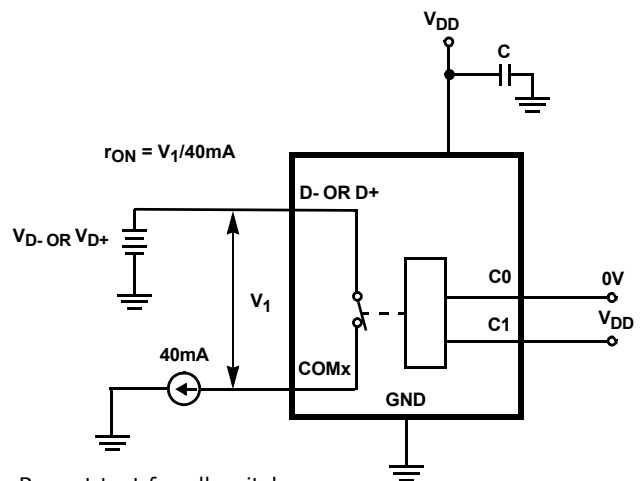
FIGURE 2B. TEST CIRCUIT

FIGURE 2. BREAK-BEFORE-MAKE TIME



Repeat test for all switches.

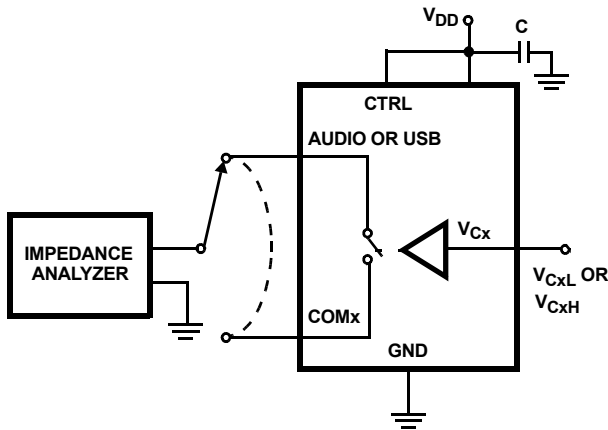
FIGURE 3. AUDIO r_{ON} TEST CIRCUIT



Repeat test for all switches.

FIGURE 4. USB r_{ON} TEST CIRCUIT

Test Circuits and Waveforms (Continued)



Repeat test for all switches.

FIGURE 5. CAPACITANCE TEST CIRCUIT

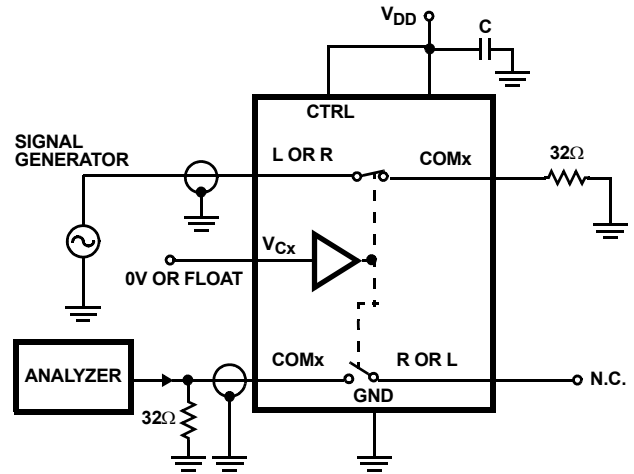


FIGURE 6. AUDIO CROSSTALK TEST CIRCUIT

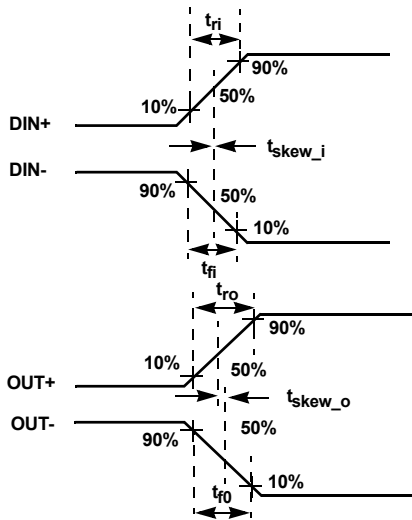
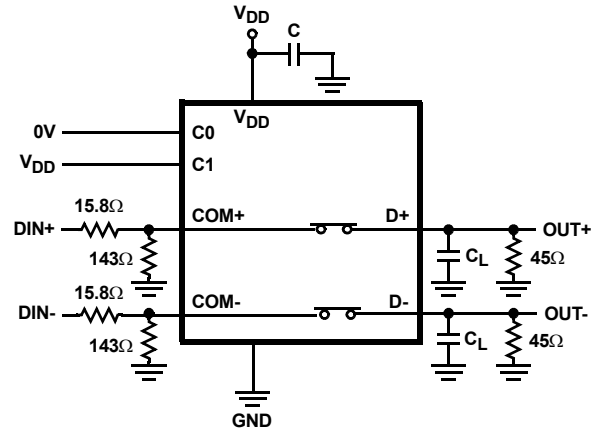


FIGURE 7A. MEASUREMENT POINTS

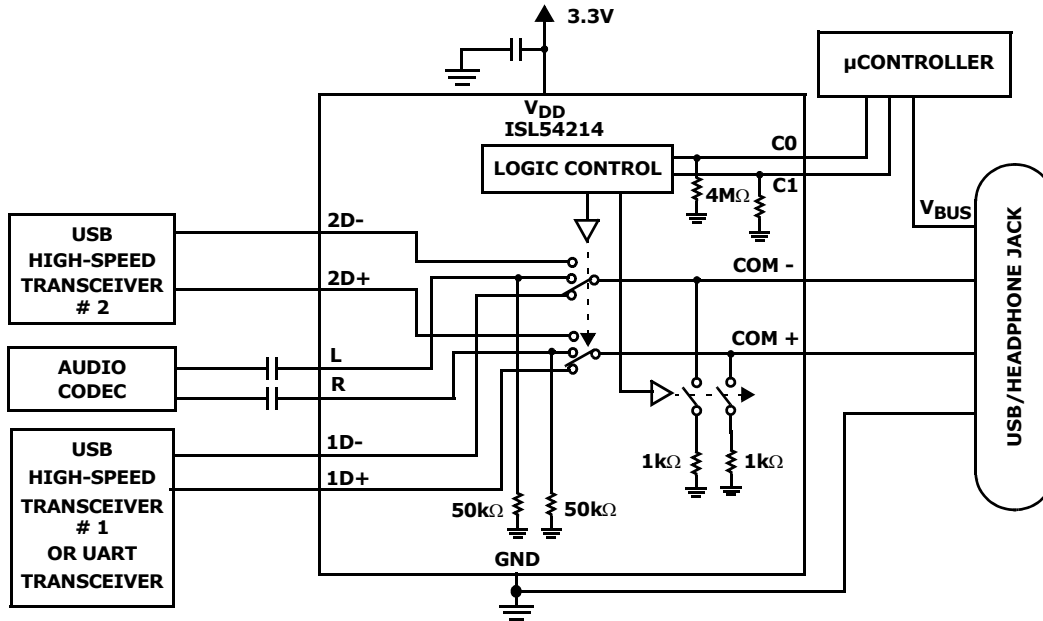


$|t_{ro} - t_{ri}|$ Delay Due to Switch for Rising Input and Rising Output Signals.
 $|t_{fo} - t_{fi}|$ Delay Due to Switch for Falling Input and Falling Output Signals.
 $|t_{skew_o}|$ Change in Skew through the Switch for Output Signals.
 $|t_{skew_i}|$ Change in Skew through the Switch for Input Signals.

FIGURE 7B. TEST CIRCUIT

FIGURE 7. SKEW TEST

Application Block Diagrams



Detailed Description

The ISL54214 device consists of dual SP3T (single pole/triple throw) analog switches. It operates from a single DC power supply in the range of 2.7V to 4.6V. It was designed to function as differential 3 to 1 multiplexer to select between two different USB differential data signals and audio L and R stereo signals. Its offered in tiny μ TQFN and TQFN packages for use in MP3 players, PDAs, cellphones, and other personal media players.

A device consists of two 2.3Ω audio switches and four 6.2Ω USB switches. The audio switches can accept signals that swing below ground. They were designed to pass audio left and right stereo signals, that are ground referenced, with minimal distortion. The USB switches were designed to pass high-speed USB differential data signals with minimal edge and phase distortion.

The ISL54214 was specifically designed for MP3 players, personal media players and cellphone applications that need to combine the stereo audio and USB channels into a single shared connector, thereby saving space and component cost. The Typical application block diagram of this functionality is previously shown.

The ISL54214 contains two logic control pins (C1 and C0) that determine the state of the device. The part has the following five states or modes of operation: All SWITCHES OFF; USB1; USB2; Audio; and Audio Mute. These states are discussed in detail in "Logic Control" on page 11.

A detailed description of the various types of switches is provided in the following sections.

Audio Switches

The two audio switches (L, R) are 2.3Ω switches that can pass signals that swing below ground.

Over a signal range of $\pm 1V$ ($0.707V_{RMS}$) with $V_{DD} > 2.7V$, these switches have an extremely low r_{ON} resistance variation. They can pass ground referenced audio signals with very low distortion ($< 0.05\%$ THD+N) when delivering $15.6mW$ into a 32Ω headphone speaker load. See Figures 16, 17, 18, 19 and 20 THD+N performance curves.

Crosstalk between the L and R audio switches over the frequency range of 20Hz to 20kHz when driving a 32Ω load is $< -88dB$. These switches have excellent off-isolation $> 105dB$ over the audio band when connected to 32Ω loads and $77dB$ when connected to $20k\Omega$ loads (In Audio Mute mode). See Figures 21 and 22 in "Typical Performance Curves" section.

The audio drivers should be connected at the L and R side of the switch (pins 2 and 3) and the speaker loads should be connected at the COM side of the switch (pins 7 and 8).

The audio switches are active (turned ON) whenever the C1 and C0 logic pins are logic "1" (High).

USB Switches

The four USB switches (1D+, 1D-, 2D+, 2D-) are 6.2Ω bidirectional switches that were specifically designed to pass high-speed USB differential data signals in the range of 0V to 400mV. The switches have low capacitance and high bandwidth to pass USB high-speed signals (480Mbps) with minimum edge and phase distortion to meet USB 2.0 signal quality specifications. See Figures 23 and 24 for the high-speed eye pattern taken with the switch in the signal path.

These switches can also swing rail-to-rail and pass USB full-speed signals (12Mbps) with minimal distortion. See Figure 25 for the full-speed eye pattern taken with the switch in the signal path.

The maximum normal operating signal range for the USB switches is from -1V to V_{DD} . The signal voltage at D- and D+ should not be allowed to exceed the V_{DD} voltage rail or go below ground by more than -1V for normal operation.

However, in the event that the USB 5.25V V_{BUS} voltage is shorted to one or both of the COM pins, the ISL54214 has fault protection circuitry to prevent damage to the ISL54214 part. The fault circuitry allows the signal pins (COM-, COM+, 1D-, 1D+, 2D-, 2D+, L and R) to be driven up to 5.25V while the V_{DD} supply voltage is in the range of 0V to 4.6V. This fault condition causes no stress to the IC. In addition, when V_{DD} is at 0V (ground), all switches are OFF and the fault voltage is isolated from the other side of the switch. When V_{DD} is in the range of 2.7V to 4.6V, the fault voltage will pass through to the output of an active switch channel. Note: During the fault condition normal operation is not guaranteed until the fault condition is removed.

The USB (1D+ and 1D-) switches are active (turned ON) whenever the C1 is logic "0" (Low) and C0 is logic "1" (High). The USB (2D+ and 2D-) switches are active (turned ON) whenever the C1 is logic "1" (High) and C0 is logic "0" (Low) provided the last state was not the Audio or Audio Mute state.

ISL54214 Operation

The discussion that follows will discuss using the ISL54214 in the "Application Block Diagrams" on page 10.

LOGIC CONTROL

The state of the ISL54214 device is determined by the voltage at the C1 pin (pin 9) and the C0 pin (pin 10). The part has five states or modes of operation. The All SWITCHES OFF mode, USB1 mode, USB2 mode, Audio mode and Audio Mute mode. Refer to the "Truth Table" on page 2 and "State Diagram" on page 2.

The C1 pin and C0 pin are internally pulled low through 4M Ω resistors to ground and can be tri-stated or left floating.

The C1 pin and C0 pin can be driven with a voltage that is higher than the V_{DD} supply voltage. They can be driven up to 5.25V with the V_{DD} supply in the range of 2.7V to 4.6V. Driving the logic higher than the supply rail will cause the logic current to increase. With $V_{DD} = 2.7V$ and $V_{LOGIC} = 5.25V$, I_{LOGIC} current is approximately 5.5 μ A.

Logic Control Voltage Levels

With V_{DD} in the range of 2.7V to 3.6V the logic levels are: C1, C0 = Logic "0" (Low) when $\leq 0.5V$ or Floating. C1, C0 = Logic "1" (High) when $\geq 1.4V$

ALL SWITCHES OFF Mode

If the C1 pin = Logic "0" and C0 pin = Logic "0" the part will be in the ALL SWITCHES OFF mode. In this mode, the 2D- and 2D+ USB switches, the L and R audio switches and the 1D- and 1D+ USB switches will be OFF (high impedance).

The 1k Ω shunts on the COM side will be disconnected (OFF).

It is recommended that when transitioning from USB1 to USB2 or from USB2 to USB1 that you always pass through the All Switches OFF state.

Audio Mode

If the C1 pin = Logic "1" and C0 pin = Logic "1", the part will be in the Audio mode. In Audio mode, the L (left) and R (right) 2.3 Ω audio switches are ON, the 1D- and 1D+ 6.2 Ω USB switches and 2D- and 2D+ 6.2 Ω USB switches will be OFF (high impedance).

The 1k Ω shunts on the COM side of the switch will be disconnected (OFF).

When a headphone is plugged into the common connector, the μ controller will drive the C1 and C0 logic pins "High" putting the part in the audio mode. In the Audio mode, the audio drivers of the player can drive the headphones and play music.

USB1 Mode

If the C1 pin = Logic "0" and C0 pin = Logic "1" the part will go into USB1 mode. In USB1 mode, the 1D- and 1D+ 6.2 Ω switches are ON and the L and R 2.3 Ω audio switches and 2D- and 2D+ 6.2 Ω USB switches will be OFF (high impedance).

The 1k Ω COM shunt resistors will be disconnected (OFF).

When a USB cable from a computer or USB hub is connected at the common connector, the μ controller will route the incoming USB signal to USB transceiver section #1 by taking the C1 pin "Low" and the C0 pin "High" putting the ISL54214 part into the USB1 mode. In USB1 mode the computer or USB hub transceiver and the MP3 player or cellphone USB transceiver #1 are connected and digital data will be able to be transmit back and forth.

USB2 Mode

If the C1 = Logic "1" and C0 pin = Logic "0" the part will be in the USB2 mode provided that the last state was not the Audio or Audio Mute state. In the USB2 mode, the 2D- and 2D+ 6.2 Ω USB switches will be ON and audio switches and the 1D- and 1D+ USB switches will be OFF (high impedance).

The 1k Ω COM shunt resistors will be disconnected (OFF).

When a USB cable from a computer or USB hub is connected at the common connector, the μ controller will route the incoming USB signal to USB transceiver section #2 by taking the C1 pin "High" and the C0 pin "Low" putting the ISL54214 part into the USB2 mode. In USB2

mode, the computer or USB hub transceiver and the MP3 player or cellphone USB transceiver #2 are connected and digital data will be able to be transmit back and forth.

Audio MUTE Mode

If the C1 pin = Logic "1" and C0 pin = Logic "0", the part will be in the Audio Mute mode provided that the last state was the Audio state. In the Audio Mute mode, the 2D- and 2D+ USB switches, the L and R audio switches and the 1D- and 1D+ USB switches will be OFF (high impedance).

The 1kΩ COM shunt resistors will be connected (ON). The 1kΩ shunts provide 77dB of off-isolation when driving 10kΩ to 20kΩ amplifier inputs.

The 1kΩ COM shunt resistors are active (ON) only when in the Audio Mute mode.

Logic Control Timing Between C1 and C0

The ISL54214 has a unique logic control architecture. The part has five different logic states but only two external logic control pins, C1 and C0. Refer to the "State Diagram" on page 2 and "Truth Table" on page 2.

The following state transitions require both C1 and C0 logic control bits to change their logic levels in unison:

- All OFF (C1 = 0, C0 = 0) -----> Audio (C1 = 1, C0 = 1)
- Audio (C1 = 1, C0 = 1) -----> All OFF (C1 = 0, C0 = 0)
- Audio Mute (C1 = 1, C0 = 0) -----> USB1 (C1 = 0, C0 = 1)

The delay time between these bits must be < 100ns to ensure that you directly move between these states without momentarily transitioning to one of the other states.

For example, if you are going from the "All OFF" state to the "Audio" state and C0 does not go high until 100nS after C1 went high you will momentarily transition to the "USB2" state. Any signals connected at the USB2 signal lines will momentarily get passed through to the COM outputs.

Delay time between C1 and C0 must be < 100ns and should be controlled by logic control drivers with well behaved monotonic transitions from High to Low and Low to High and with typical logic family rise and fall times of 1ns to 6ns.

POWER

The power supply connected at VDD (pin 11) provides power to the ISL54214 part. Its voltage should be kept in the range of 2.7V to 4.6V. In a typical application, VDD will be in the range of 2.7V to 4.3V and will be connected to the battery or LDO of the MP3 player or cellphone.

A 0.01μF or 0.1μF decoupling capacitor should be connected from the VDD pin to ground to filter out any power supply noise from entering the part. The capacitor should be located as close to the VDD pin as possible.

Typical Performance Curves $T_A = +25^\circ\text{C}$, Unless Otherwise Specified.

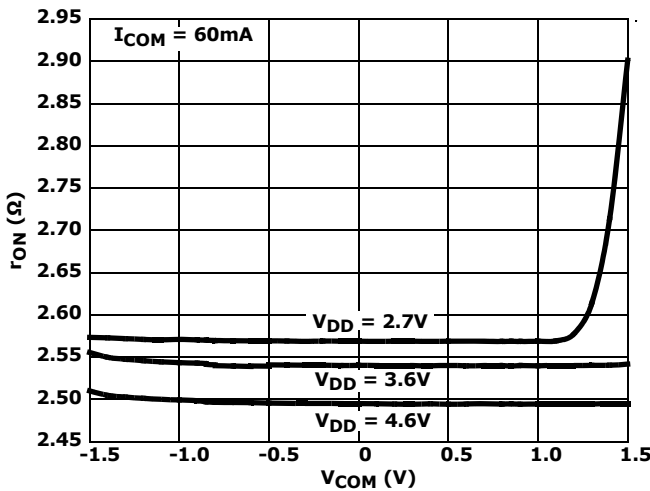


FIGURE 8. AUDIO ON-RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

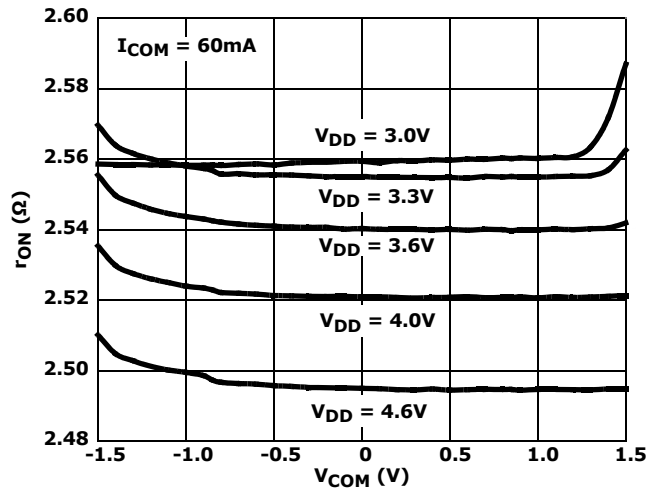


FIGURE 9. AUDIO ON-RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

Typical Performance Curves $T_A = +25^\circ\text{C}$, Unless Otherwise Specified. (Continued)

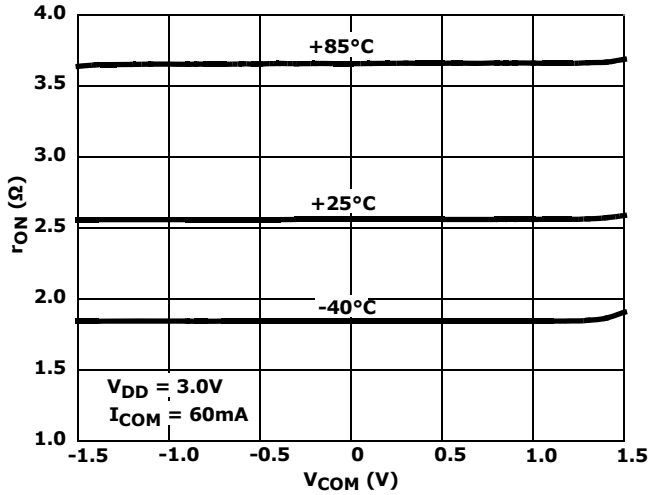


FIGURE 10. AUDIO ON-RESISTANCE vs SWITCH VOLTAGE vs TEMPERATURE

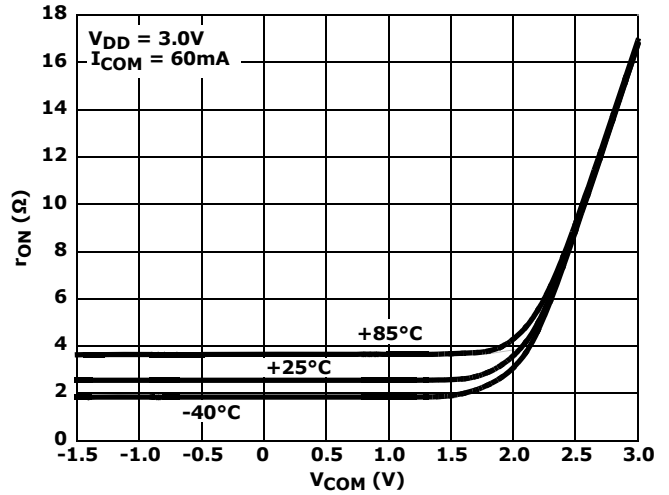


FIGURE 11. AUDIO ON-RESISTANCE vs SWITCH VOLTAGE vs TEMPERATURE

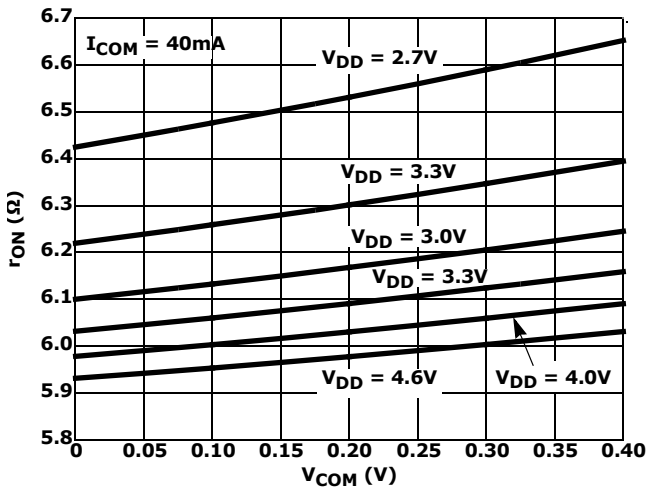


FIGURE 12. USB ON-RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

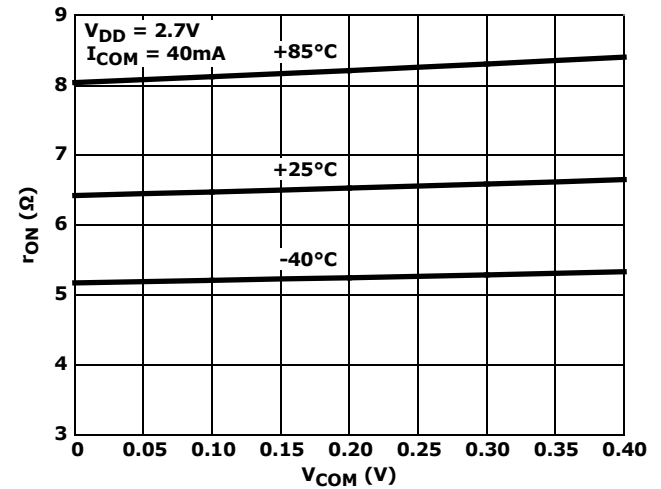


FIGURE 13. USB ON-RESISTANCE vs SWITCH VOLTAGE vs TEMPERATURE

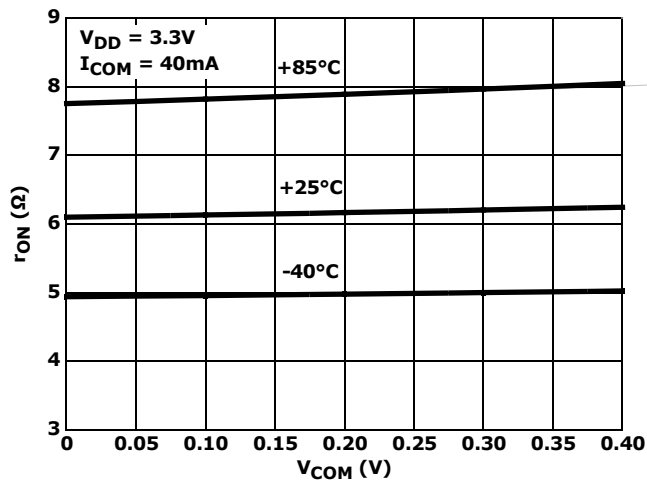


FIGURE 14. USB ON-RESISTANCE vs SWITCH VOLTAGE vs TEMPERATURE

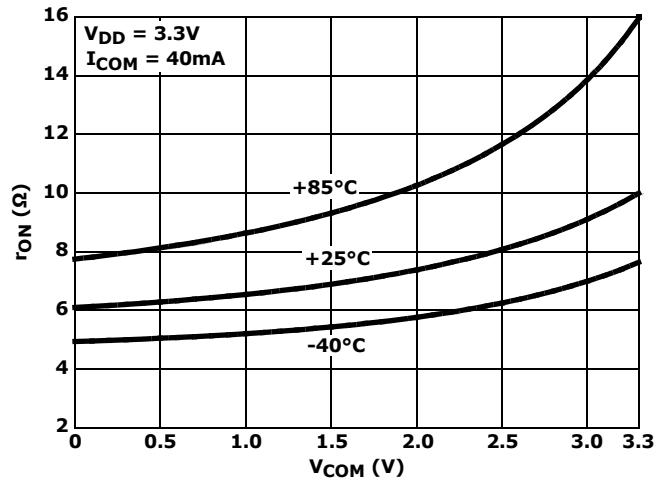


FIGURE 15. USB ON-RESISTANCE vs SWITCH VOLTAGE vs TEMPERATURE

Typical Performance Curves $T_A = +25^\circ\text{C}$, Unless Otherwise Specified. (Continued)

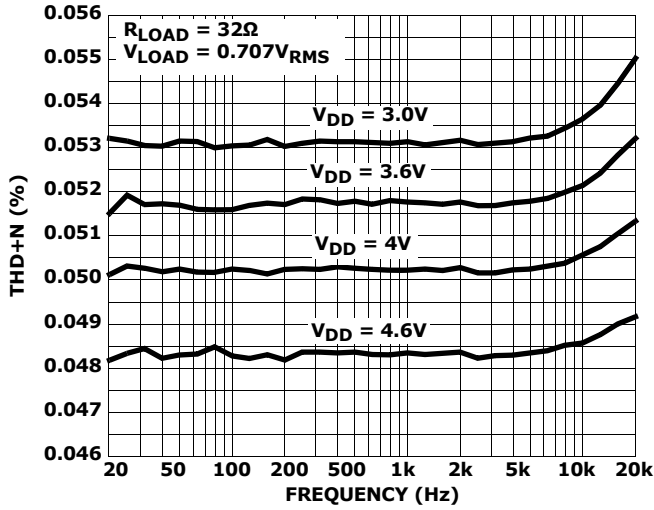


FIGURE 16. THD+N vs SUPPLY VOLTAGE vs FREQUENCY

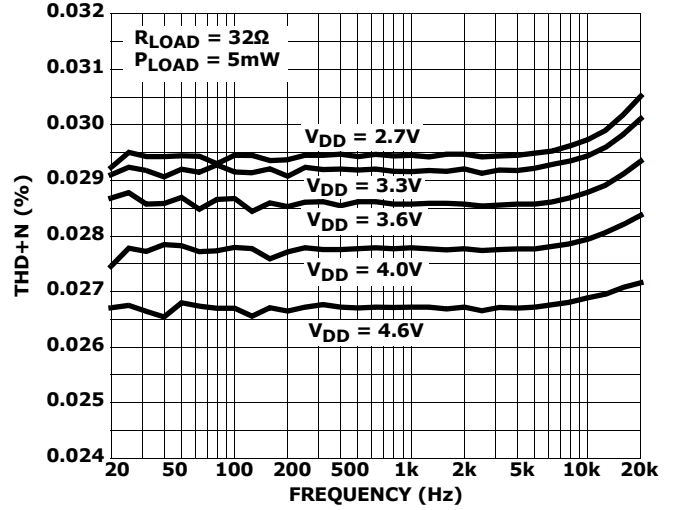


FIGURE 17. THD+N vs SUPPLY VOLTAGE vs FREQUENCY

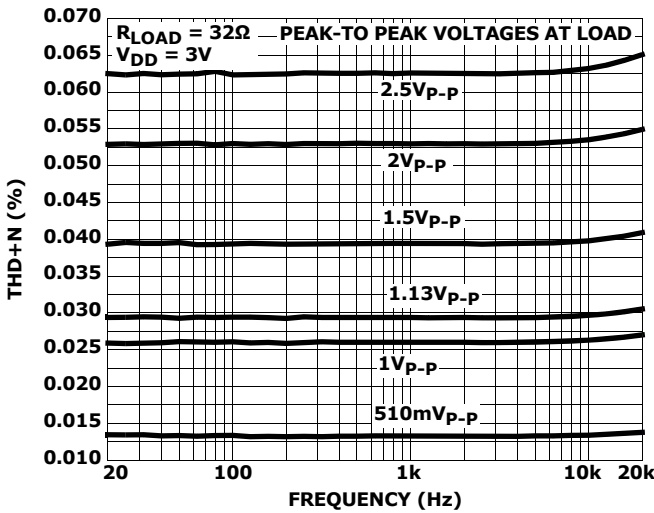


FIGURE 18. THD+N vs SIGNAL LEVELS vs FREQUENCY

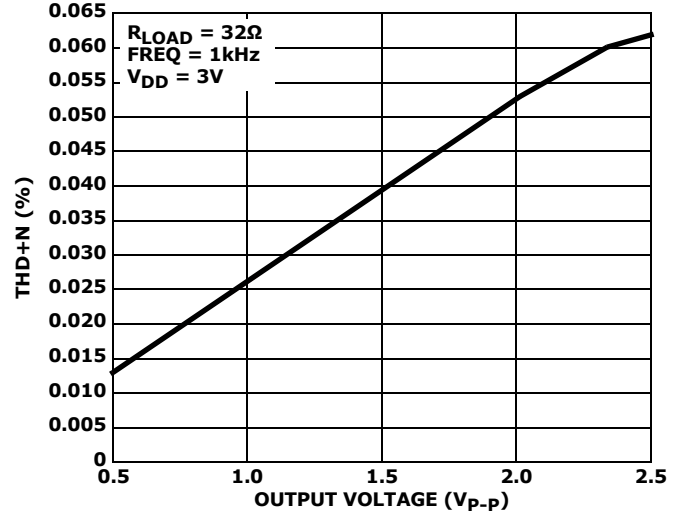


FIGURE 19. THD+N vs OUTPUT VOLTAGE

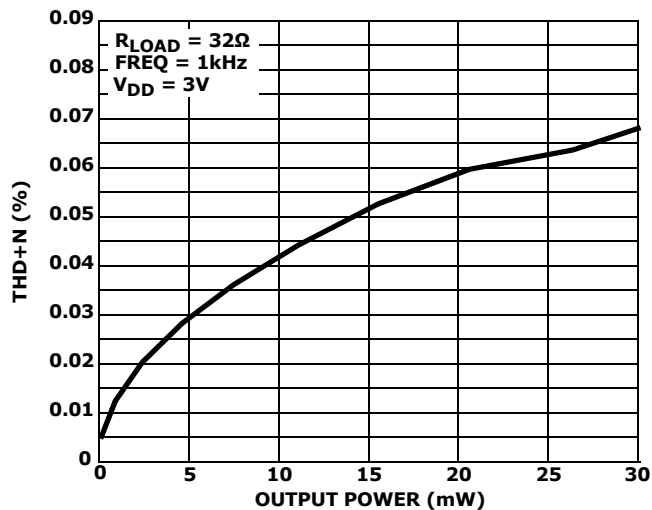


FIGURE 20. THD+N vs OUTPUT POWER

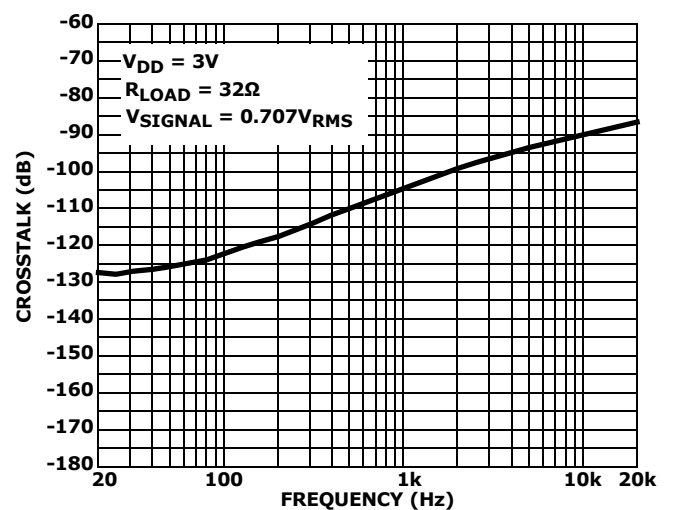


FIGURE 21. AUDIO CHANNEL-TO-CHANNEL CROSSTALK

Typical Performance Curves $T_A = +25^\circ\text{C}$, Unless Otherwise Specified. (Continued)

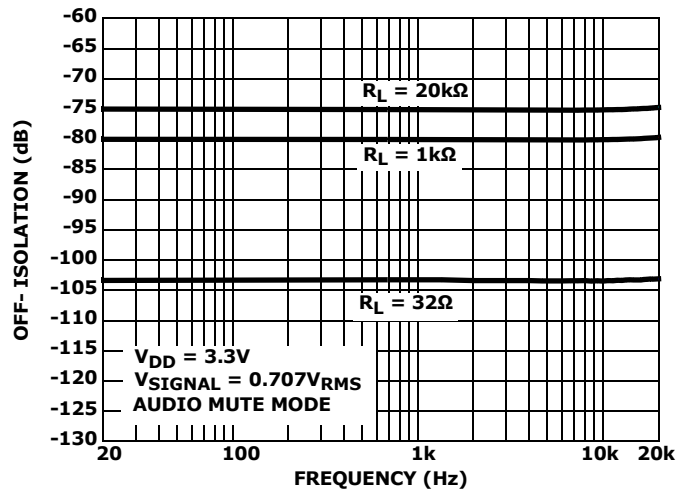


FIGURE 22. OFF-ISOLATION AUDIO SWITCH vs LOADING vs FREQUENCY

Typical Performance Curves $T_A = +25^\circ\text{C}$, Unless Otherwise Specified. (Continued)

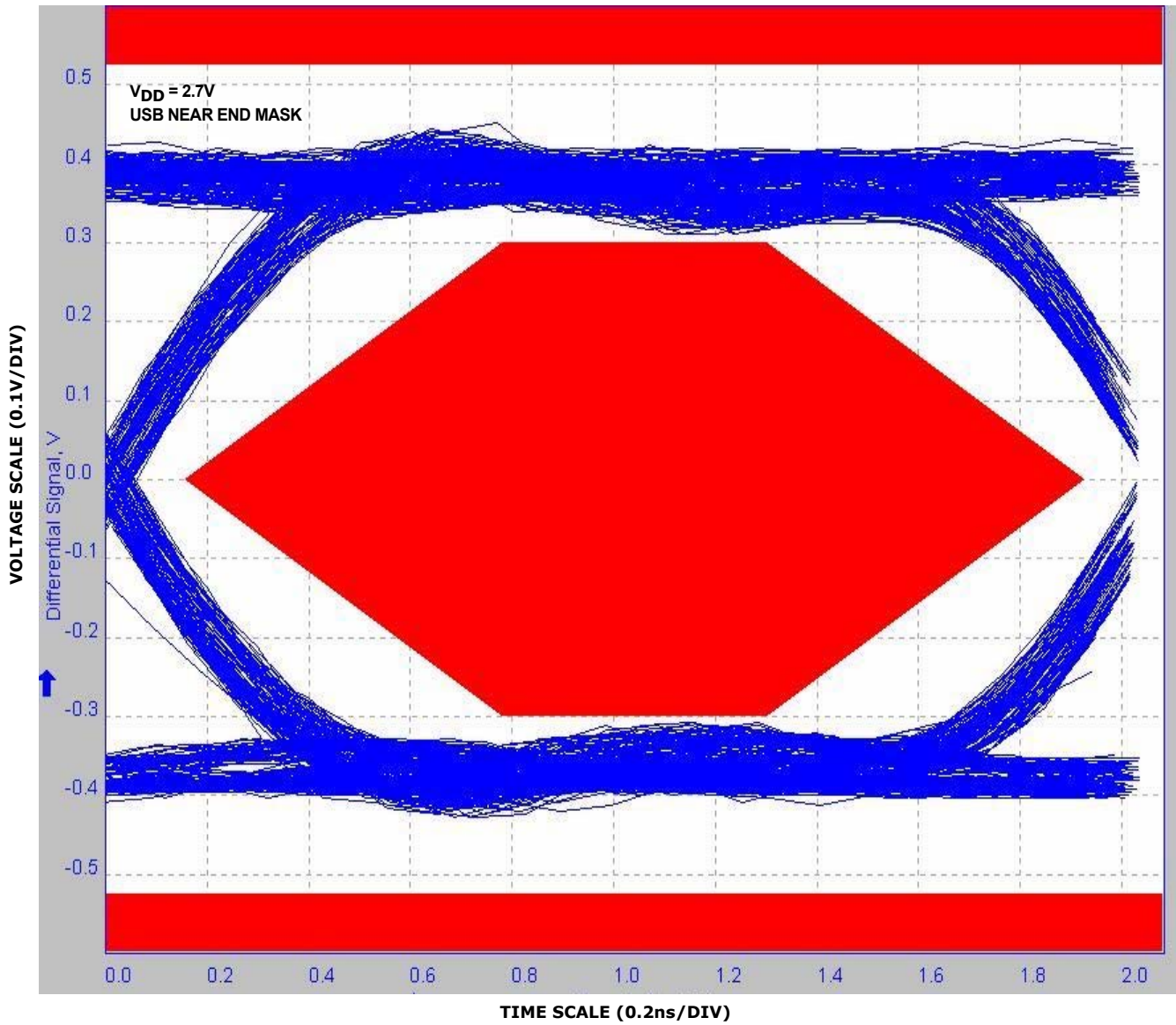


FIGURE 23. EYE PATTERN: 480Mbps WITH USB SWITCHES IN THE SIGNAL PATH

Typical Performance Curves $T_A = +25^\circ\text{C}$, Unless Otherwise Specified. (Continued)

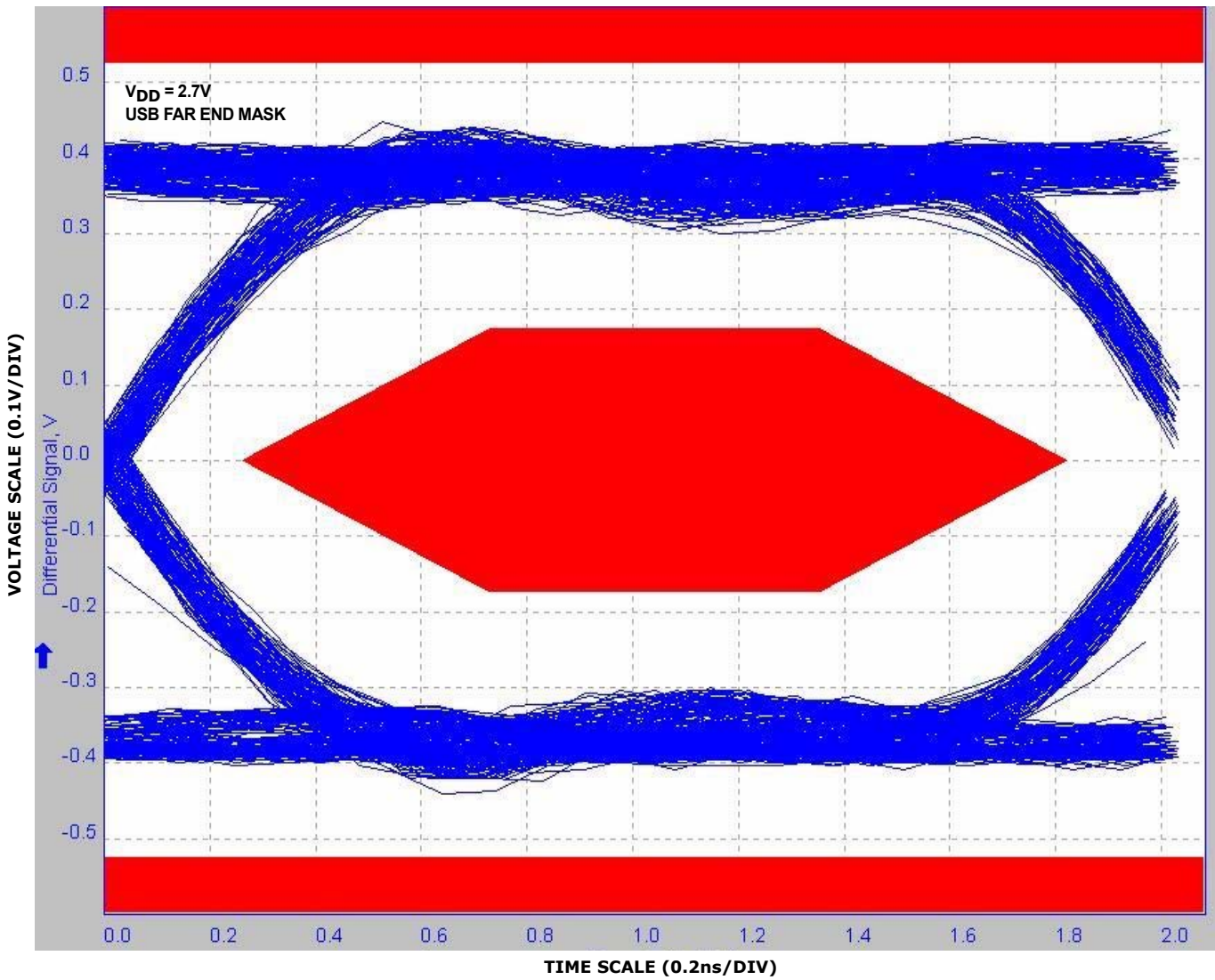


FIGURE 24. EYE PATTERN: 480Mbps WITH USB SWITCHES IN THE SIGNAL PATH

Typical Performance Curves $T_A = +25^\circ\text{C}$, Unless Otherwise Specified. (Continued)

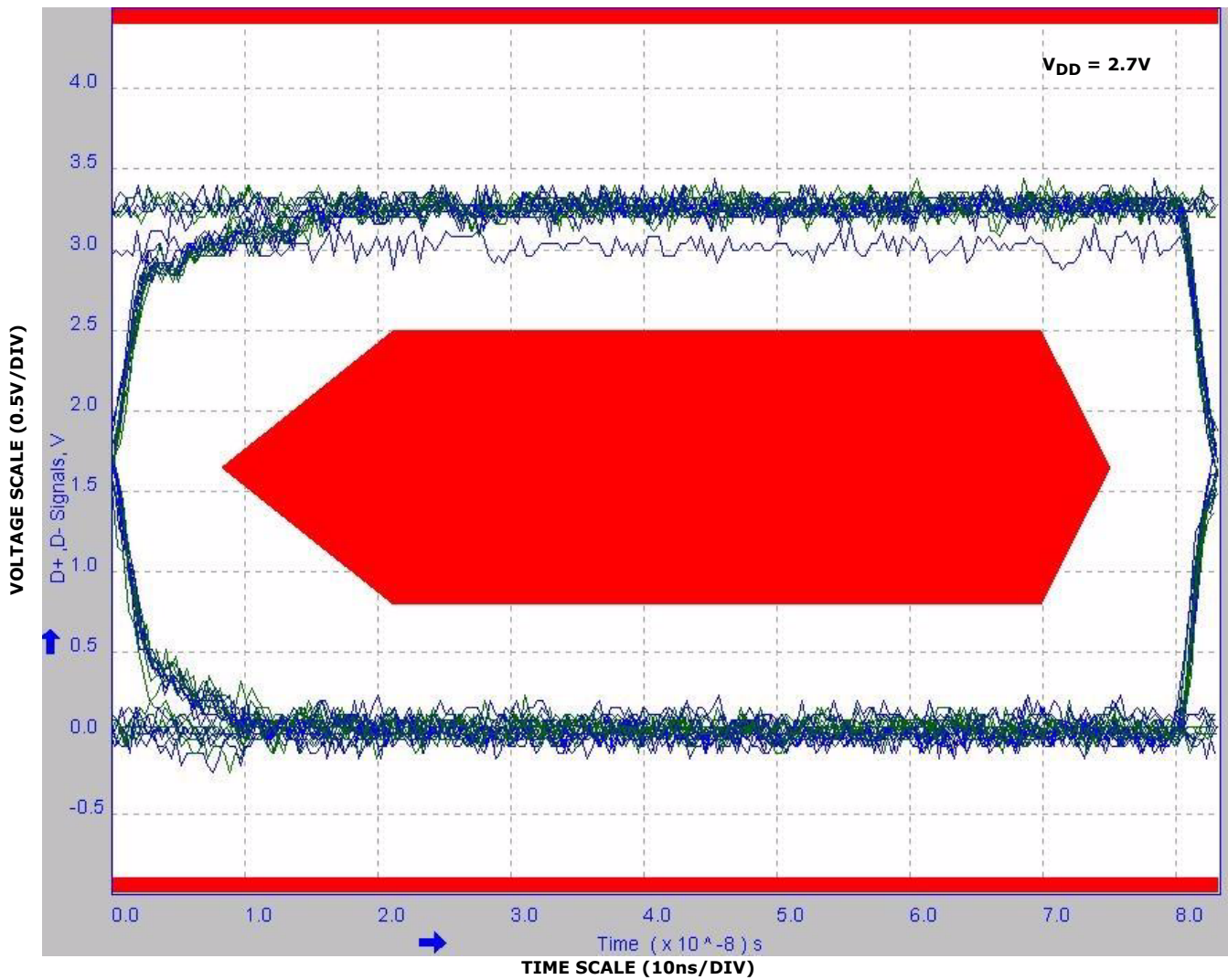


FIGURE 25. EYE PATTERN: 12Mbps USB SIGNAL WITH USB SWITCHES IN THE SIGNAL PATH

Typical Performance Curves $T_A = +25^\circ\text{C}$, Unless Otherwise Specified. (Continued)

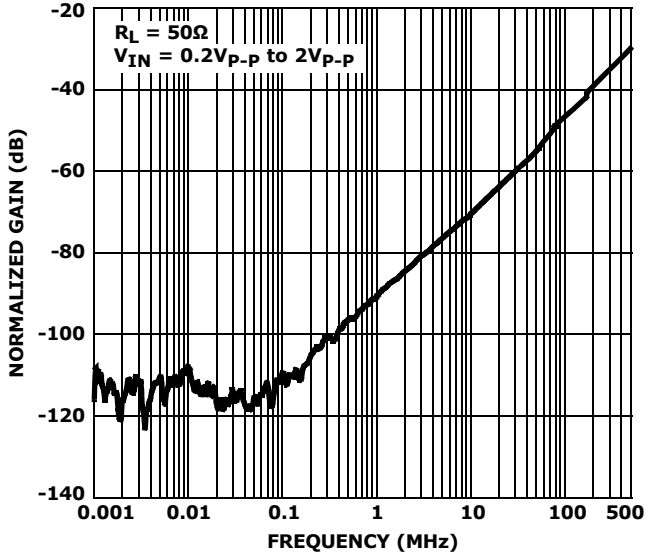


FIGURE 26. OFF-ISOLATION USB SWITCHES

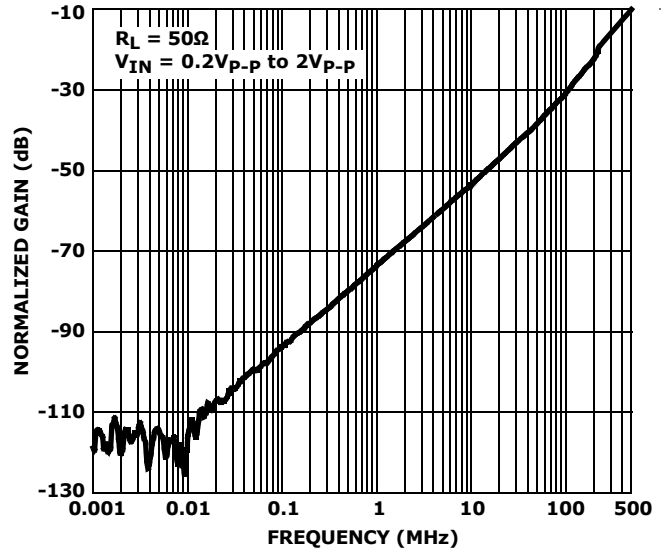


FIGURE 27. OFF-ISOLATION AUDIO SWITCHES

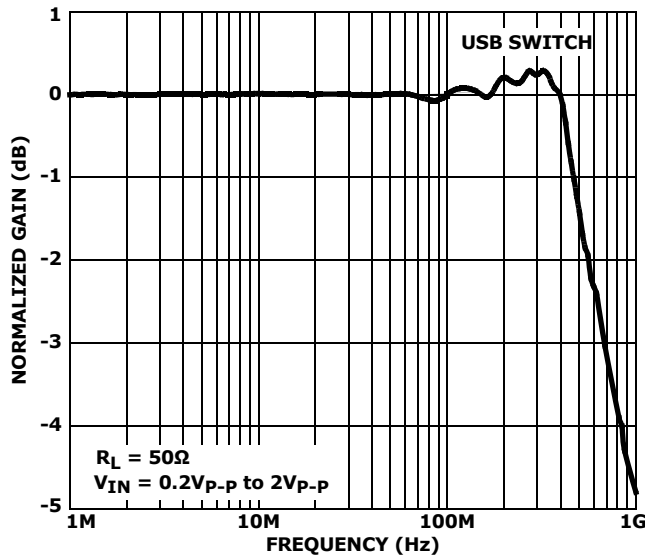


FIGURE 28. FREQUENCY RESPONSE

Die Characteristics

SUBSTRATE AND TQFN THERMAL PAD POTENTIAL (POWERED UP):

GND

TRANSISTOR COUNT:

837

PROCESS:

Submicron CMOS

Revision History

DATE	REVISION	CHANGE
6/1/10	FN6816.3	Converted to new Intersil template. Added Revision History table and Products sections. On page 3 , added separate pin configuration diagrams for the uTQFN and TQFN parts. On page 3, updated the pin description table to show the thermal pad. On page 5, in ABS section added latch-up level. On page 7, Changed I _{COMx} current limit for 25°C from: 1μA, to: 4μA. Under "Thermal Information" on page 5 for the μTQFN, added theta JC TOP value of 90C/W, along with appropriate foot note for theta JC as measured on top of package.

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL54214

To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at <http://rel.intersil.com/reports/search.php>

© Copyright Intersil Americas LLC 2008-2010. All Rights Reserved.
 All trademarks and registered trademarks are the property of their respective owners.

For additional products, see www.intersil.com/en/products.html

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at www.intersil.com/en/support/qualandreliability.html

Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

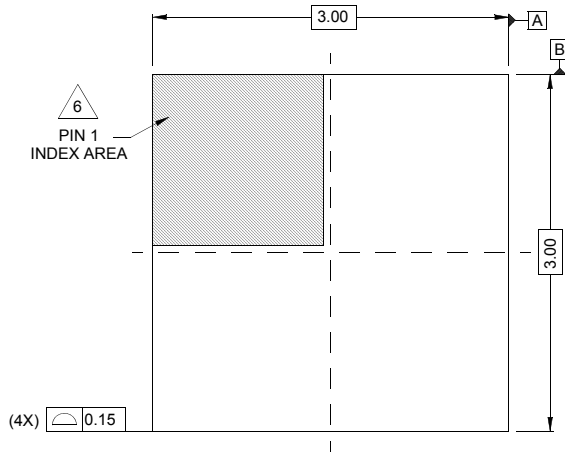
For information regarding Intersil Corporation and its products, see www.intersil.com

Package Outline Drawing

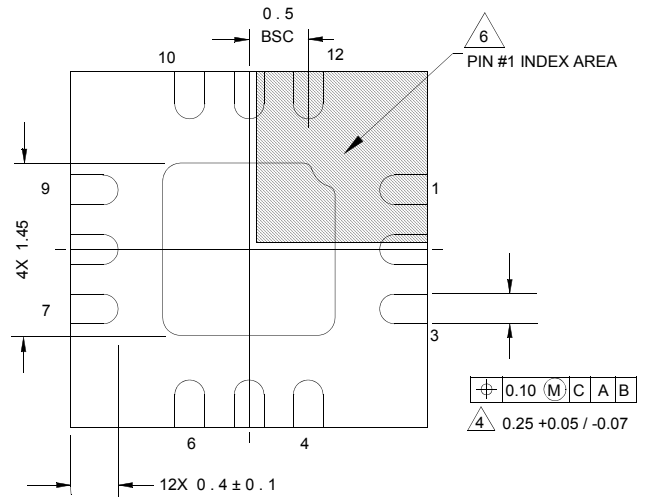
L12.3x3A

12 LEAD THIN QUAD FLAT NO LEAD PLASTIC PACKAGE

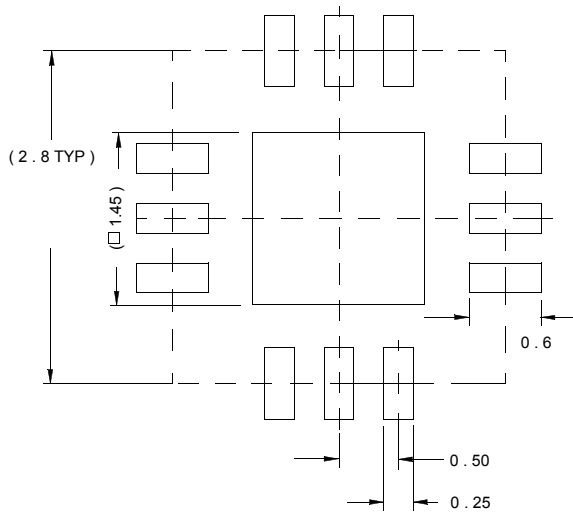
Rev 0, 09/07



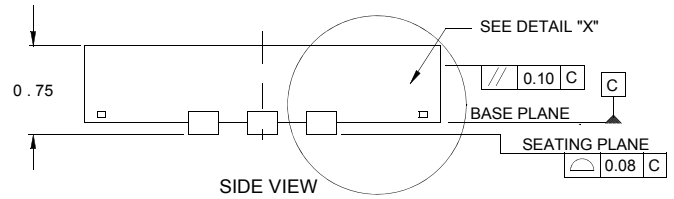
TOP VIEW



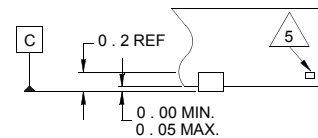
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW

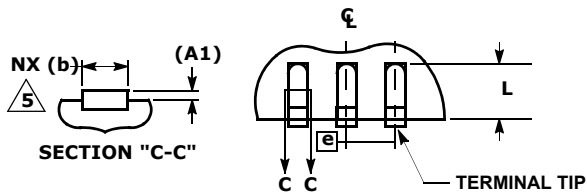
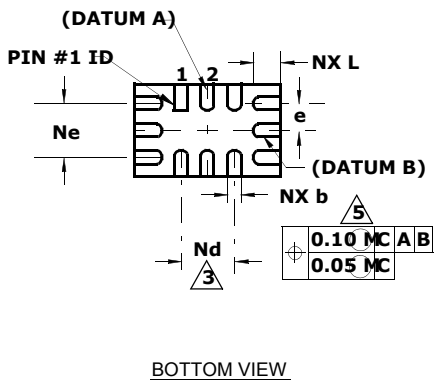
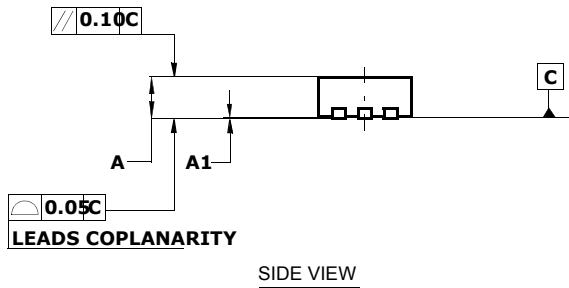
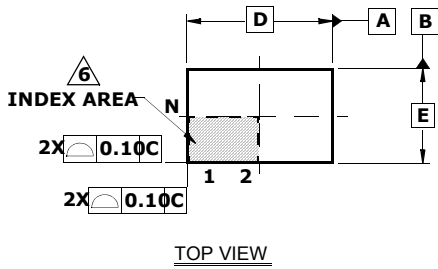


DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
Dimensions in () for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.18mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

Ultra Thin Quad Flat No-Lead Plastic Package (UTQFN)



L12.2.2x1.4A

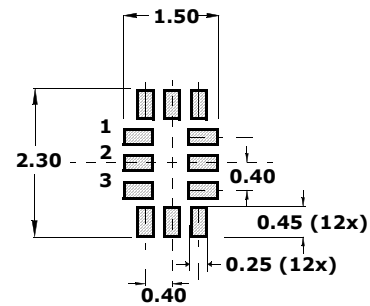
12 LEAD ULTRA THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.45	0.50	0.55	-
A1	-	-	0.05	-
A3	0.127 REF			-
b	0.15	0.20	0.25	5
D	2.15	2.20	2.25	-
E	1.35	1.40	1.45	-
e	0.40 BSC			-
k	0.20	-	-	-
L	0.35	0.40	0.45	-
N	12			2
Nd	3			3
Ne	3			3
θ	0	-	12	4

Rev. 0 12/06

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on D and E side, respectively.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Maximum package warpage is 0.05mm.
8. Maximum allowable burrs is 0.076mm in all directions.
9. Same as JEDEC MO-255UABD except:
No lead-pull-back, "A" MIN dimension = 0.45 not 0.50mm
"L" MAX dimension = 0.45 not 0.42mm.
10. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.



TYPICAL RECOMMENDED LAND PATTERN