

## ISL3282EMRTEP

±16.5kV ESD Protected, 16Mbps, with Active Low Rx EN, RS-485/422 Receiver

### Description

The **ISL3282EMRTEP** is a ±16.5kV IEC61000 ESD protected, 3.0V to 5.5V powered, single receiver that meets both the RS-485 and RS-422 standards for balanced communication. This receiver has very low bus currents (+125µA/-100µA), so it presents a true “1/8 unit load” to the RS-485 bus. This allows up to 256 receivers on the network without violating the RS-485 specification’s 32 unit load maximum and without using repeaters.

Receiver inputs feature a “Full Fail-Safe” design, which ensures a logic high Rx output if Rx inputs are floating, shorted, or terminated but undriven.

The ISL3282EMRTEP includes an active low enable pin and is offered in the Military Temperature range (-55°C to +125°C).

A 26% smaller footprint is available with the TDFN package. This device also features a logic supply pin ( $V_L$ ) that sets the  $V_{OH}$  level of the RO output (and the switching points of the RE/ $\overline{RE}$  input) to be compatible with another supply voltage in mixed voltage systems.

### Device Information

The specifications for an Enhanced Product (EP) device are defined in a Vendor Item Drawing (VID), which is controlled by the Defense Logistics Agency (DLA). “Hot-links” to the applicable VID and other supporting application information are provided on our website.

### Applications

- Clock distribution
- High node count systems
- Space constrained systems
- Security camera networks
- Building environmental control/lighting systems
- Industrial/process control networks

### Features

- Specifications per DLA VID V62/10601
- Full military temperature electrical performance from -55°C to +125°C
- NiPdAu-Ag Lead finish (Sn-free, Pb-free) (ISL3282EMRTEPZ-TK only)
- Controlled baseline with one wafer fabrication site and one assembly/test site
- Full homogeneous lot processing in wafer fab
- No combination of wafer fabrication lots in assembly
- Full traceability through assembly and test by date/trace code assignment
- Enhanced process change notification
- Enhanced obsolescence management
- Eliminates need for up-screening a COTS component
- ±16.5kV IEC61000 ESD protection on RS-485 inputs
- Class 3 ESD level on all other pins: >5kV HBM
- Wide supply range: 3.0V to 5.5V
- Specified for +125°C operation
- Logic supply pin ( $V_L$ ) eases operation in mixed supply systems
- Full fail-safe (open, short, terminated/undriven)
- True 1/8 unit load allows up to 256 devices on the bus
- High data rates: up to 16Mbps
- Low quiescent supply current: 500µA (max.)
- Very low shutdown supply current: 20µA (max.)
- -7V to +12V common-mode input voltage range
- Tri-statable Rx available (active low or high EN input)
- 5V tolerant logic inputs when  $V_{CC} \leq 5V$

Table 1. Summary of Features

Part Number	Function	Data Rate (Mbps)	# Devices on Bus	RX Enable?	$V_L$ Pin?	Quiescent $I_{CC}$ (µA)	Low-Power Shutdown?	Lead Count
ISL3282EMRTEP	1 Rx	16	256	Active Low	Yes	350	Yes	8-TDFN

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# 1. Overview

## 1.1 Typical Operating Circuits

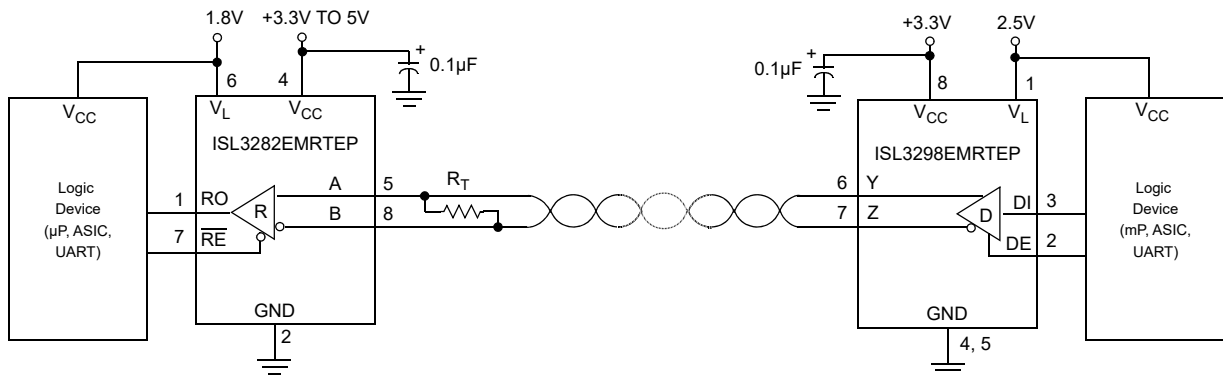


Figure 1. Network with V<sub>L</sub> Pin for Interface to Lower Voltage Logic Devices

Figure 2. Truth Table

Receiving		
Inputs		Output
$\overline{\text{RE}}$	A - B	RO
0	$\geq -0.05\text{V}$	1
0	$\leq -0.2\text{V}$	0
0	Inputs Open/Shorted	1
1	X	High-Z*

## 2. Pin Information

### 2.1 Pin Assignments

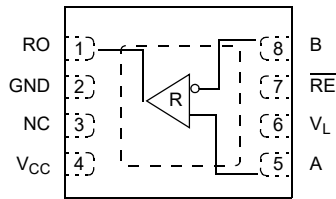


Figure 3. Pin Assignments - Top View

### 2.2 Pin Descriptions

Pin Number	Pin Name	Function
1	RO	Receiver output: If $A - B \geq -50\text{mV}$ , RO is high; If $A - B \leq -200\text{mV}$ , RO is low; RO = High if A and B are unconnected (floating) or shorted.
7	$\overline{\text{RE}}$	Receiver output enable. RO is enabled when $\overline{\text{RE}}$ is low; RO is high impedance when $\overline{\text{RE}}$ is high. If the Rx enable function is not used, connect $\overline{\text{RE}}$ directly to GND. $\overline{\text{RE}}$ is internally pulled high.
2	GND	Ground connection. This is also the potential of the TDFN thermal pad.
5	A	$\pm 16.5\text{kV}$ IEC61000 ESD Protected RS-485, RS-422 level, non-inverting receiver input.
8	B	$\pm 16.5\text{kV}$ IEC61000 ESD Protected RS-485, RS-422 level, inverting receiver input.
4	$V_{\text{CC}}$	System power supply input (3.0V to 5.5V). On devices with a $V_{\text{L}}$ pin, power-up $V_{\text{CC}}$ first.
6	$V_{\text{L}}$	Logic-level supply, which sets the $V_{\text{IL}}/V_{\text{IH}}$ levels for the $\overline{\text{RE}}$ pin, and sets the $V_{\text{OH}}$ level of the RO output. Power-up this supply after $V_{\text{CC}}$ , and keep $V_{\text{L}} \leq V_{\text{CC}}$ .
3	NC	No Connection

### 3. Typical Performance Curves

$C_L = 15\text{pF}$ ,  $T_A = +25^\circ\text{C}$ ; unless otherwise specified.

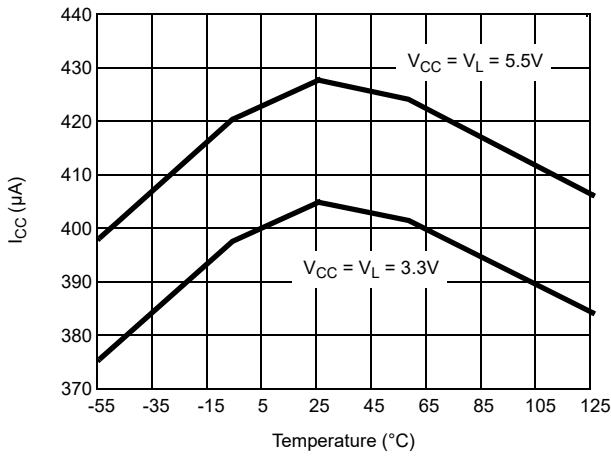


Figure 4. Supply Current vs Temperature

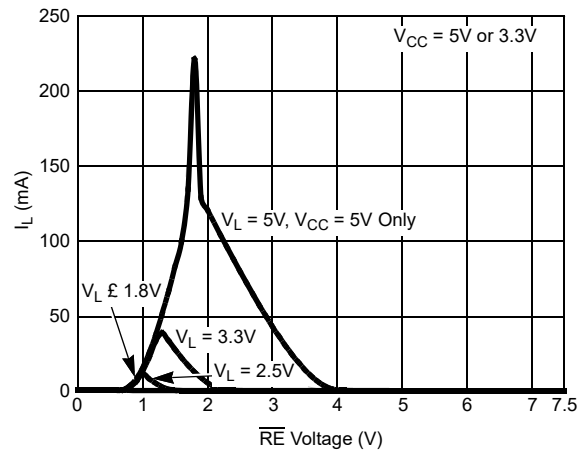


Figure 5.  $V_L$  Supply Current vs Enable Pin Voltage

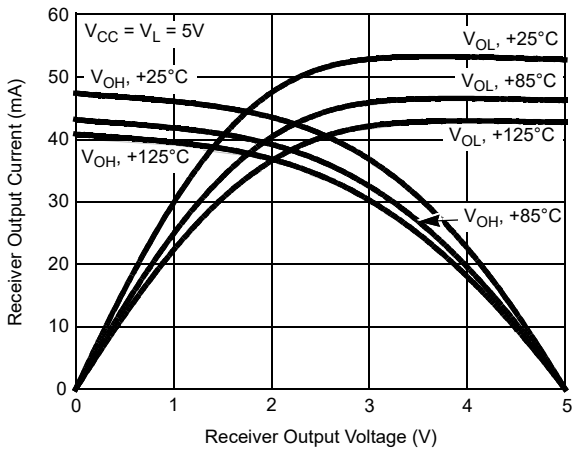


Figure 6. Receiver Output Current vs Receiver Output Voltage

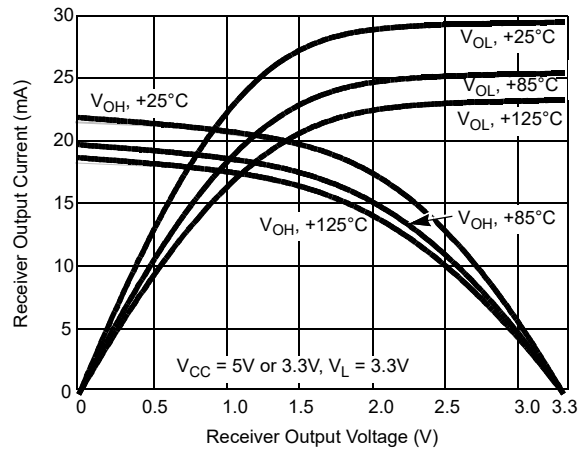


Figure 7. Receiver Output Current vs Receiver Output Voltage

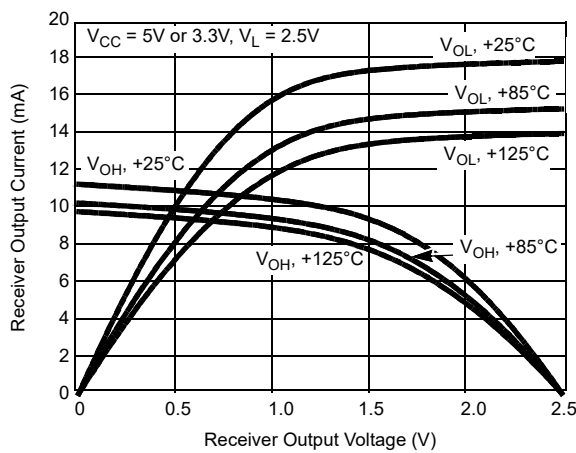


Figure 8. Receiver Output Current vs Receiver Output Voltage

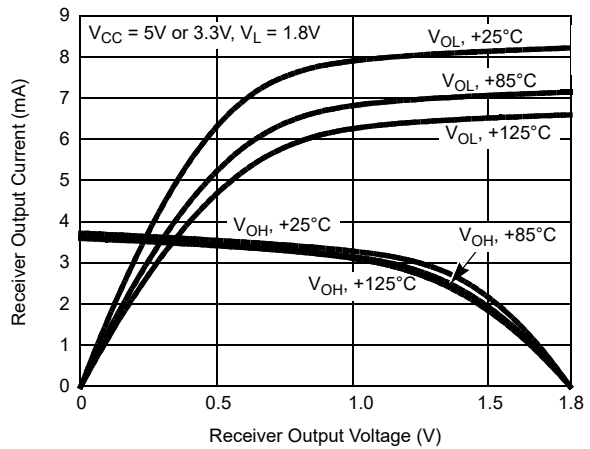


Figure 9. Receiver Output Current vs Receiver Output Voltage

$C_L = 15\text{pF}$ ,  $T_A = +25^\circ\text{C}$ ; unless otherwise specified. (Cont.)

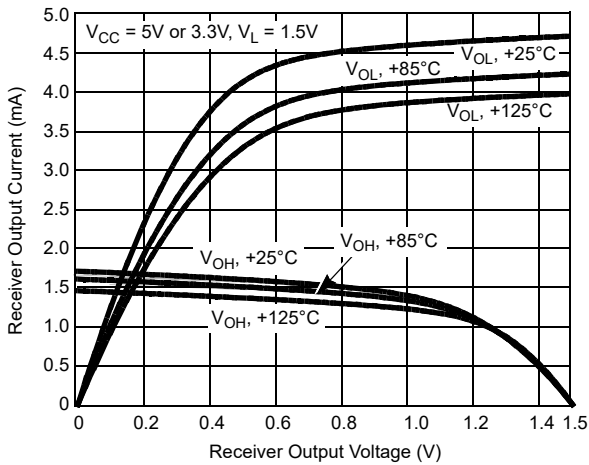


Figure 10. Receiver Output Current vs Receiver Output Voltage

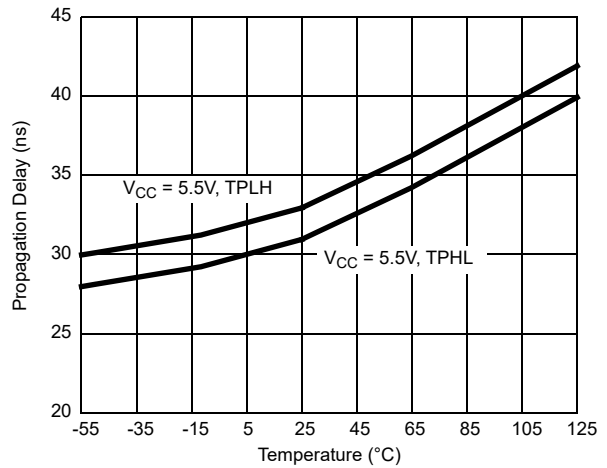


Figure 11. Receiver Propagation Delay vs Temperature

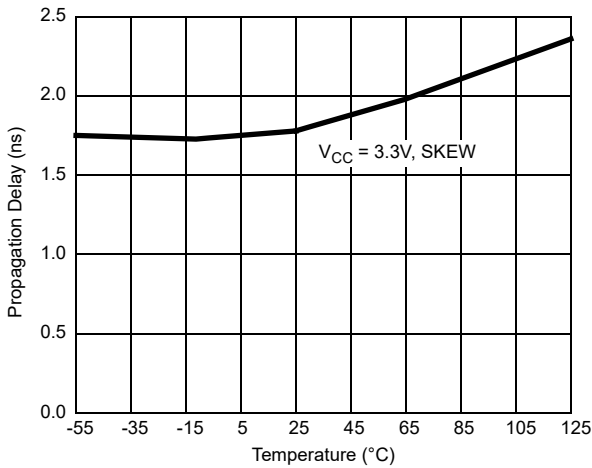


Figure 12. Receiver Skew vs Temperature

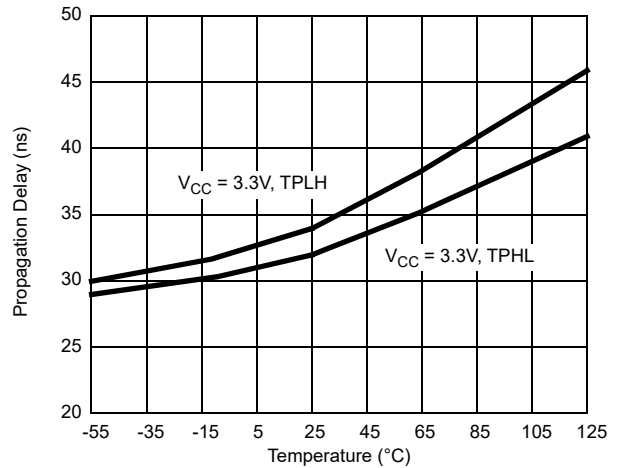


Figure 13. Receiver Propagation Delay vs Temperature

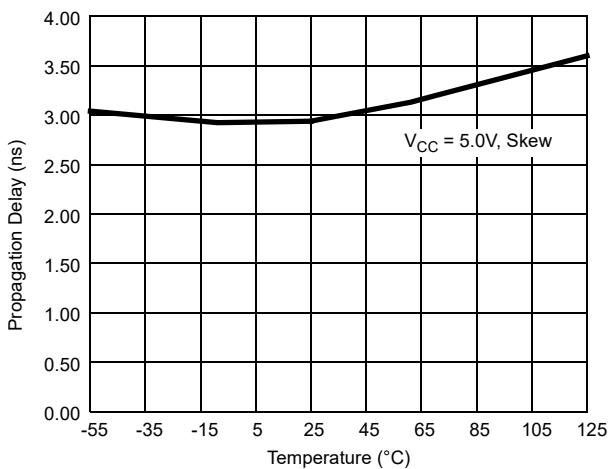


Figure 14. Receiver Skew vs Temperature

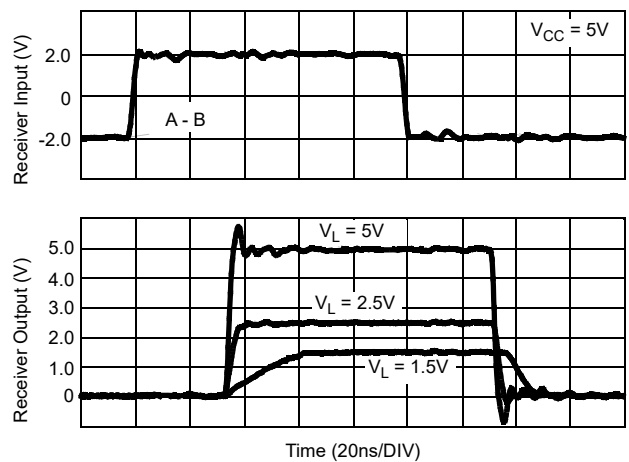


Figure 15. Receiver Waveforms

$C_L = 15\text{pF}$ ,  $T_A = +25^\circ\text{C}$ ; unless otherwise specified. (Cont.)

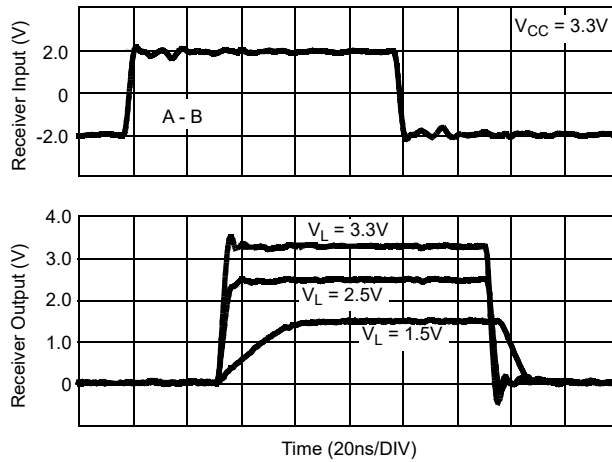
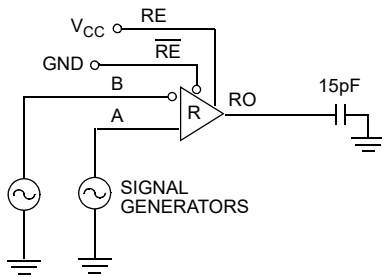
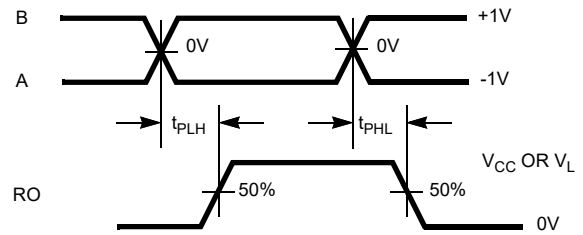


Figure 16. Receiver Waveforms

### 3.1 Test Circuits and Waveforms

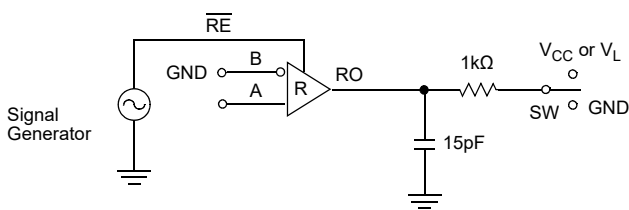


Test Circuit

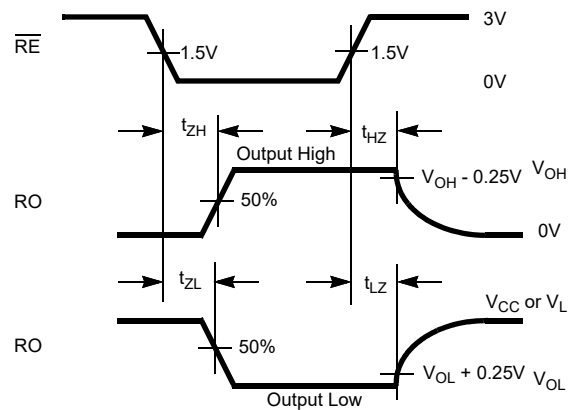


Measurement Points

Figure 17. Receiver Propagation Delay and Data Rate



Test Circuit



Measurement Points

Figure 18. Receiver Enable and Disable Times

Parameter	A (V)	SW
$t_{HZ}$	+1.5	GND
$t_{LZ}$	-1.5	$V_{CC}$ or $V_L$
$t_{ZH}$	+1.5	GND
$t_{ZL}$	-1.5	$V_{CC}$ or $V_L$

## 4. Application Information

RS-485 and RS-422 are differential (balanced) data transmission standards for use in long haul or noisy environments. RS-422 is a subset of RS-485, so RS-485 transceivers are also RS-422 compliant. RS-422 is a point-to-multipoint (multidrop) standard, which allows only one driver and up to 10 (assuming one unit load devices) receivers on each bus. RS-485 is a true multipoint standard, which allows up to 32 one unit load devices (any combination of drivers and receivers) on each bus.

Another important advantage of RS-485 is the extended Common-Mode Range (CMR), which specifies that the driver outputs and receiver inputs withstand signals that range from +12V to -7V. RS-422 and RS-485 are intended for runs as long as 4000', so the wide CMR is necessary to handle ground potential differences, as well as voltages induced in the cable by external fields.

### 4.1 Receiver Features

This device utilizes a differential input receiver for maximum noise immunity and common-mode rejection. Input sensitivity is better than  $\pm 200\text{mV}$ , as required by the RS-422 and RS-485 specifications.

Receiver input resistance of  $96\text{k}\Omega$  surpasses the RS-422 specification of  $4\text{k}\Omega$  and is eight times the RS-485 "Unit Load (UL)" requirement of  $12\text{k}\Omega$  minimum. Thus, these products are known as "one-eighth UL" transceivers and there can be up to 256 of these devices on a network while still complying with the RS-485 loading specification.

Receiver inputs function with common-mode voltages as great as +9V/-7V outside the power supplies (i.e., +12V and -7V), making them ideal for long networks where induced voltages, and ground potential differences are realistic concerns.

The ISL3282EMRTEP includes a "full fail-safe" function that guarantees a high level receiver output if the receiver inputs are unconnected (floating), shorted together, or connected to a terminated, however, undriven bus. Fail-safe with shorted inputs is achieved by setting the Rx upper switching point to -50mV, thereby ensuring that the Rx sees 0V differential as a high input level.

The receiver can easily support a 16Mbps data rate, and its output is tri-statable using the active low  $\overline{\text{RE}}$  input.

### 4.2 Wide Supply Range

The ISL3282EMRTEP is designed to operate with a wide range of supply voltages from 3.0V to 5.5V. This device meets the RS-422 and RS-485 specifications over this full range.

### 4.3 Logic Supply ( $V_L$ Pin)

*Note:* Power-up  $V_{CC}$  before powering up the  $V_L$  supply.

The ISL3282EMRTEP includes a  $V_L$  pin that powers the logic input ( $\overline{\text{RE}}$ ) and/or the Rx output. These pins interface with "logic" devices such as UARTs, ASICs, and microcontrollers. Today, most of these devices use power supplies significantly lower than 3.3V, thus, a 3.3V output level from a 3.3V powered RS-485 IC might seriously overdrive and damage the logic device input. Similarly, the logic device's low  $V_{OH}$  might not exceed the  $V_{IH}$  of a 3.3V or 5V powered  $\overline{\text{RE}}$  input. Connecting the  $V_L$  pin to the power supply of the logic device (as shown in [Figure 19](#)) limits the ISL3282EMRTEP's Rx output  $V_{OH}$  to  $V_L$  (see [Figure 6](#) through [Figure 10](#)), and reduces the  $\overline{\text{RE}}$  input switching point to a value compatible with the logic device's output levels. Tailoring the logic pin input switching point and output levels to the supply voltage of the UART, ASIC, or microcontroller eliminates the need for a level shifter/translator between the two ICs.

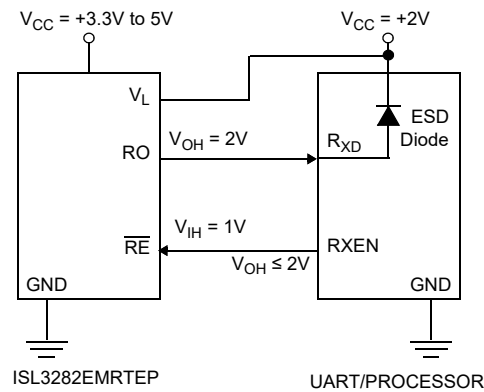


Figure 19. Using  $V_L$  Pin to Adjust Logic Levels

$V_L$  can be anywhere from  $V_{CC}$  down to 1.35V, however, the input switching points may not provide enough noise margin when  $V_L < 1.6V$ . Table 2 indicates typical  $V_{IH}$ ,  $V_{IL}$ , and data rate values for various  $V_L$  settings so the user can ascertain whether or not a particular  $V_L$  voltage meets his/her needs.

Table 2.  $V_{IH}$ ,  $V_{IL}$  and Data Rate vs  $V_L$  for  $V_{CC} = 3.3V$  or  $5V$

$V_L$ (V)	$V_{IH}$ (V)	$V_{IL}$ (V)	Data Rate (Mbps)
1.35	0.55	0.5	11
1.6	0.7	0.6	16
1.8	0.8	0.7	23
2.3	1	0.9	27
2.7	1.1	1	30
3.3	1.3	1.2	30
5.5 (i.e., $V_{CC}$ )	2	1.8	24

The quiescent, RO unloaded,  $V_L$  supply current ( $I_L$ ) is typically less than  $60\mu A$  for  $V_L \leq 3.3V$ , as shown in Figure 5.

#### 4.4 ESD Protection

All pins on the device include Class 3 (>4kV) Human Body Model (HBM) ESD protection structures, however, the RS-485 pins (receiver inputs) incorporate advanced structures allowing them to survive ESD events in excess of  $\pm 16.5kV$  HBM and  $\pm 16.5kV$  IEC61000. The RS-485 pins are particularly vulnerable to ESD damage because they typically connect to an exposed port on the exterior of the finished product. Simply touching the port pins, or connecting a cable, can cause an ESD event that might destroy unprotected ICs. These new ESD structures protect the device whether or not it is powered up, and without degrading the RS-485 common-mode range of -7V to +12V. This built-in ESD protection eliminates the need for board level protection structures (such as transient suppression diodes), and the associated, undesirable capacitive load they present.

#### 4.5 IEC61000-4-2 Testing

The IEC61000 test method applies to finished equipment, rather than to an individual IC. Therefore, the pins most likely to suffer an ESD event are those that are exposed to the outside world (the RS-485 pins in this case) and the IC is tested in its typical application configuration (power applied) rather than testing each pin-to-pin combination. The lower current limiting resistor coupled with the larger charge storage capacitor yields a test that is much more severe than the HBM test. The extra ESD protection built into this device's RS-485 pins allows the design of equipment meeting level 4 criteria without the need for additional board level protection on the RS-485 port.

### 4.5.1 Air-Gap Discharge Test Method

For this test method, a charged probe tip moves toward the IC pin until the voltage arcs to it. The current waveform delivered to the IC pin depends on approach speed, humidity, temperature, etc., so it is difficult to obtain repeatable results. The A and B RS-485 pins withstand  $\pm 16.5\text{kV}$  air-gap discharges.

### 4.5.2 Contact Discharge Test Method

During the contact discharge test, the probe contacts the tested pin before the probe tip is energized, thereby eliminating the variables associated with the air-gap discharge. The result is a more repeatable and predictable test, however, equipment limits prevent testing devices at voltages higher than  $\pm 9\text{kV}$ . The ISL3282EMRTEP can survive  $\pm 9\text{kV}$  contact discharges on the RS-485 pins.

## 4.6 Data Rate, Cables, and Terminations

RS-485, RS-422 are intended for network lengths up to 4000', however, the maximum system data rate decreases as the transmission length increases. Networks operating at 16Mbps are limited to lengths less than 100', while a 250kbps network that uses slew rate limited transmitters can operate at that data rate over lengths of several thousand feet.

Twisted pair is the cable of choice for RS-485, RS-422 networks. Twisted pair cables tend to pick up noise and other electromagnetically induced voltages as common-mode signals, which are effectively rejected by the differential receiver in these ICs.

To minimize reflections, proper termination is imperative for high data rate networks. Short networks using slew rate limited transmitters need not be terminated, however, terminations are recommended unless power dissipation is an overriding concern.

In point-to-point, or point-to-multipoint (single driver on bus) networks, the main cable should be terminated in its characteristic impedance (typically  $120\Omega$ ) at the end farthest from the driver. In multireceiver applications, stubs connecting receivers to the main cable should be kept as short as possible. Multipoint (multidriver) systems require that the main cable be terminated in its characteristic impedance at both ends. Stubs connecting a transmitter or receiver to the main cable should be kept as short as possible.

## 4.7 Low-Power Shutdown Mode

This BiCMOS receiver uses a fraction of the power required by its bipolar counterparts, and include a shutdown feature that reduces the already low quiescent  $I_{CC}$  to a  $20\mu\text{A}$  trickle. They enter shutdown whenever the receiver is disabled ( $\overline{RE} = V_{CC}$ ).

## 5. Die Characteristics

Table 3. Die and Assembly Related Information

Die Information	
Process	Si Gate BiCMOS
Assembly Information	
Substrate and TDFN Thermal Pad Potential (Powered Up)	GND
Additional Information	
Transistor Count	140

## 6. Package Outline Drawing

The package outline drawing is located at the end of this document and is accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

## 7. Ordering Information

Part Number <sup>[1]</sup>	Vendor Item Drawing	Part Marking	Package Description	PKG. DWG. #	Carrier Type <sup>[2]</sup>	Temp. Range
ISL3282EMRTEP-TK	V62/10601-01XB	282	8 Ld TDFN	L8.2x3A	Reel, 1k	-55 to +125°C
ISL3282EMRTEPZ-TK <sup>[3]</sup>	V62/10601-01XE	82Z	8 Ld TDFN <sup>[4]</sup> (RoHS Compliant)			

- For the Moisture Sensitivity Level (MSL) rating, see the product information page for [ISL3282EMRTEP](#). For more information about MSL, see [TB363](#).
- See [TB347](#) for details about reel specifications.
- These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
- For the Pb-Free Reflow Profile, see [TB493](#).

## 8. Revision History

Revision	Date	Change
2.01	Mar 4, 2026	<ul style="list-style-type: none"> <li>Placed in latest template.</li> <li>Updated Ordering Information table.</li> <li>Added Lead Finish Features bullet.</li> <li>Removed about Intersil section.</li> </ul>
2.00	Jun 17, 2016	<ul style="list-style-type: none"> <li>Updated title to fit 100 character limit.</li> <li>Removed Pb-Free bullet under Features section.</li> <li>Updated Ordering Information table by removing Pb-Free notes and obsolete parts. Added Tape and Reel Quantity and PKG DWG columns.</li> <li>Replaced Products section with About Intersil.</li> <li>Added the applicable POD.</li> </ul>
1.00	Jan 27, 2011	In Figure 4 on page 5, corrected units of y axis from mA to $\mu$ A.
0.00	Feb 26, 2010	Initial Release.



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