ISL28025

Precision Digital Power Monitor with Real Time Alerts

FN8388
Rev.6.03
Dec 1, 2022

The ISL28025 is a bidirectional high-side and low-side digital current sense and voltage monitor with a serial interface. The device monitors power supply current and voltage, which provides the digital results along with calculated power. The ISL28025 provides tight accuracy of less than 0.1% for both voltage and current monitoring.

The V_{CC} power can either be externally supplied or internally regulated, which allows the ISL28025 to handle a common-mode input voltage range from 0V to 60V. The wide range permits the device to handle telecom, automotive and industrial applications with minimal external circuitry.

An 8-bit voltage DAC enable DC/DC converter output voltage margining (20 Pin QFN) Fault indication includes Bus Voltage window and over-current fast fault logic indication. The ISL28025 includes an integrated temperature sensor for monitoring.

The ISL28025 serial interface is PMBus compatible and operates down to 1.2V. It draws an average current of just 1.3mA and is available in the space saving 16 ball WLCSP package. It is also available in a 20 lead QFN 4x4 (1.85SQmm EPAD) The parts operate across the full industrial temperature range from -40°C to +125°C.

Features

- Bus voltage sense range . . . . . 0V to 60V
- Voltage gain error. 0.05%
- Current gain error. 0.05%
- High or low (RTN) side sensing
- Bidirectional current sensing
- Auxiliary low voltage input channel
- $\Delta\sum$ADC, 16-bit native resolution
- Programmable averaging modes
- Internal 3.3V regulator
- Internal temperature sense
- Over-voltage/undervoltage and current fault monitoring with 500ns detection delay
- 8-bit voltage output DAC (20 Pin QFN)
- I^2C/SMBus/PMBus interface that handles 1.2V supply
- 55 I^2C slave addresses

Applications

- Data processing servers
- DC power distribution
- Telecom equipment
- Portable communication equipment
- DC/DC and AC/DC converters
- Automotive power
- Many I^2C ADC with alert applications

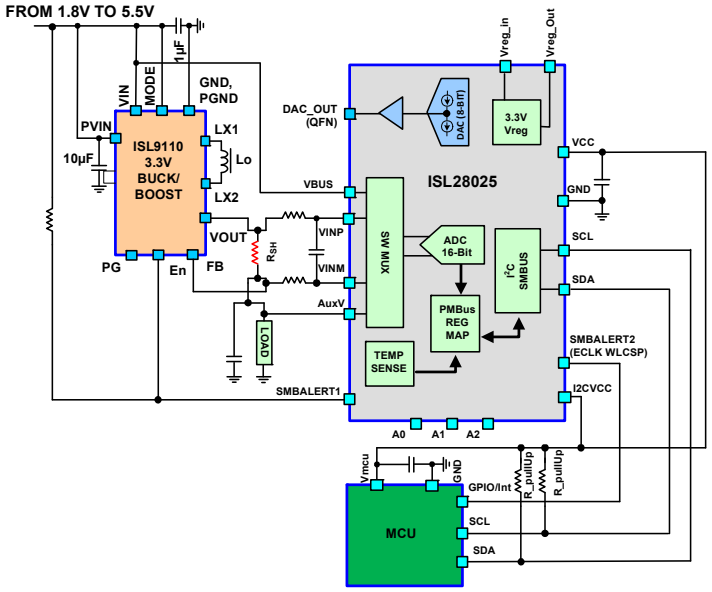

FIGURE 1. TYPICAL APPLICATION CIRCUIT

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Block Diagram

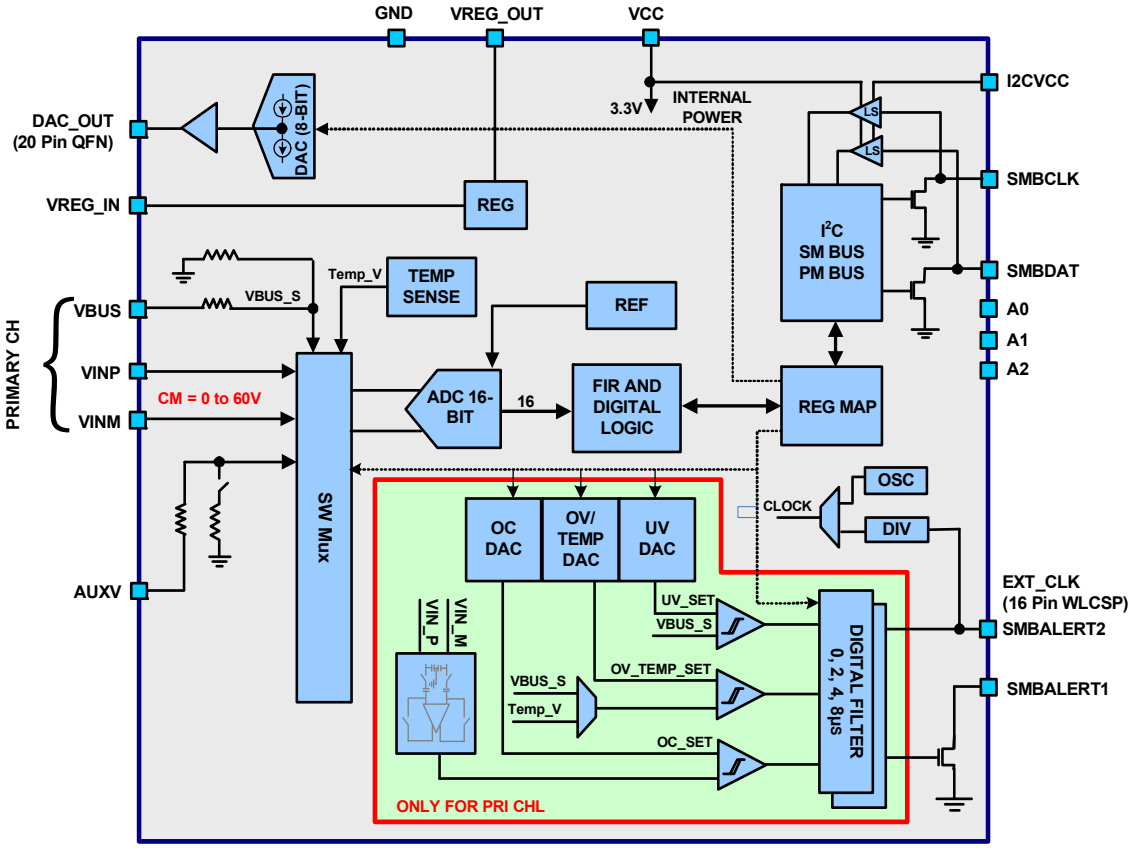


FIGURE 2. BLOCK DIAGRAM

Ordering Information

PART NUMBER	PART MARKING	V_{BUS} OPTION (V)	PACKAGE DESCRIPTION (RoHS Compliant)	PKG. DWG. #	CARRIER TYPE (Note 1)	TEMP. RANGE
ISL28025FR12Z (Notes 3, 4)	280 25R12Z	12	20 lead QFN 4x4 (1.85SQmm EPAD)	L20.4x4J	Tube	-40°C to +125°C
ISL28025FR12Z-T (Notes 3, 4)					Reel, 6k	
ISL28025FR12Z-T7A (Notes 3, 4)					Reel, 250	
ISL28025FI12Z-T (Notes 2, 3)	2512	12	16 Ball WLCSP	W4x4.16C	Reel, 3k	
ISL28025FI12Z-T7A (Notes 2, 3)					Reel, 250	
ISL28025FI60Z-T (Notes 2, 3)	2560	60	16 Ball WLCSP	W4x4.16C	Reel, 3k	
ISL28025FI60Z-T7A (Notes 2, 3)					Reel, 250	
ISL28025EVKIT1Z	Evaluation Kit					
ISL28025EVAL1Z	Evaluation Board					

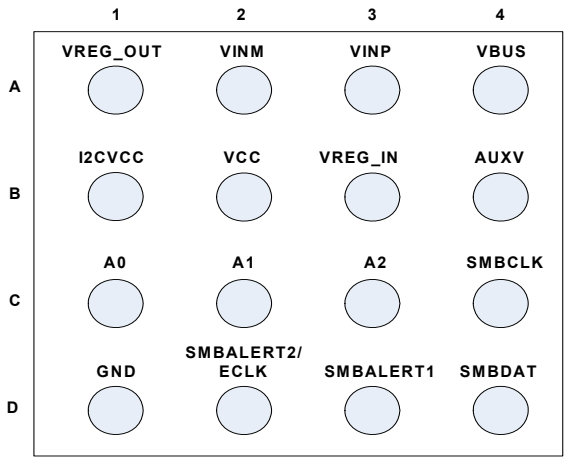
NOTES:

1. Refer to TB347 for details on reel specifications.
2. These Pb-free WLCSP packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu - e1 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free WLCSP packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the product information page for the ISL28025. For more information on MSL, see TB363.
4. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the P-free requirements of IPC/JEDEC J STD-020.

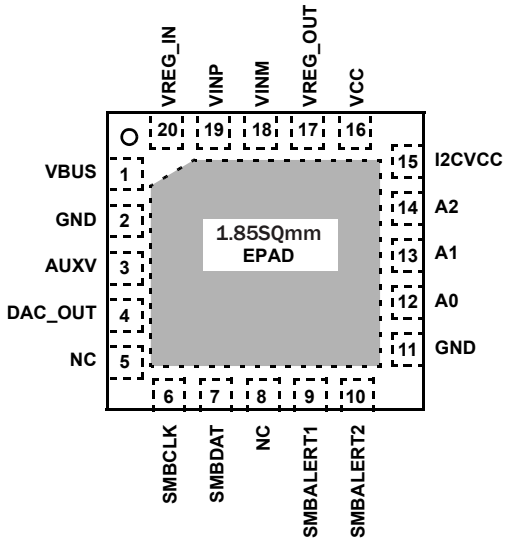
Pin Configurations

ISL28025
TOP VIEW

ISL28025FI – 16 Pin (BALL) 0.5mm PITCH WLCSP



ISL28025FR – 20 lead QFN 4x4 (1.85SQmm EPAD)



Pin Descriptions

16 Ball WLCSP

16 PIN WLCSP	PIN NAME	TYPE/DIR	PIN DEFINITION
A1	VREG_OUT	Power	Voltage regulator output. Connect a proper decoupling capacitor to this pin
A2	VINM	Analog Input	Current sense minus input
A3	VINP	Analog Input	Current sense plus input
A4	VBUS	Power	VBus voltage sense
B1	I2CVCC	Power	I^2C level shifter power supply. Connect this pin to the VCC pin if level shifters are not used
B2	VCC	Power	Chip power supply
B3	VREG_IN	Power	Voltage regulator input. Connect this pin to ground if a voltage regulator is not used
B4	AUXV	Analog Input	Auxiliary port single-ended input
C1	A0	Digital Input	I^2C address input
C2	A1	Digital Input	I^2C address input
C3	A2	Digital Input	I^2C address input
C4	SMBCLK	Digital Input	SMBus/I^2C clock input
D1	GND	Power	Ground
D2	SMBALERT2/ECLK	Digital Input/Output	External ADC clock input or CPU interrupt signal. It is used as a CPU interrupt signal only when this pin is not configured as external clock input
D3	SMBALERT1	Digital Output	SMBus Alert1, open collector output
D4	SMBDAT	Digital Input	SMBus/I^2C data

20 Lead QFN 4x4 (1.85SQmm EPAD)

PIN NUMBER	PIN NAME	TYPE/DIR	PIN DEFINITION
1	VBUS	Power	VBUS voltage sense
2	GND	Power	Ground
3	AUXV	Analog Input	Auxiliary port single-ended input
4	DAC_OUT	Analog Output	DAC voltage output
5	NC	Float	No Connection
6	SMBCLK	Digital Input	SMBus/I^2C clock input
7	SMBDAT	Digital Input/Output	SMBus/I^2C data
8	NC	Float	No Connection
9	SMBALERT1	Digital Output	SMBus Alert1, open-drain output
10	SMBALERT2	Digital Output	CPU interrupt signal
11	GND	Power	Ground
12	A0	Digital Input	SMBus/I^2C address input
13	A1	Digital Input	SMBus/I^2C address input
14	A2	Digital Input	SMBus/I^2C address input
15	I2CVCC	Power	I^2C level shifter power supply. Connect this pin to the VCC pin if a level shifter is not used
16	VCC	Power	Chip power supply
17	VREG_OUT	Power	Voltage regulator output. Connect a proper decoupling capacitor to this pin
18	VINM	Analog Input	Current sense minus input
19	VINP	Analog Input	Current sense plus input
20	VREG_IN	Power	Voltage regulator input. Connect this pin to ground if a voltage regulator is not used
EPAD	NEG	SUBSTRATE	GND or most negative voltage

TABLE 1. DPM PORTFOLIO COMPARISON - ISL28022 vs ISL28023 vs ISL28025 (Dual Package)

DESCRIPTION		BASIC DIGITAL POWER MONITOR	FULL FEATURE DIGITAL POWER MONITOR	DIGITAL POWER MONITOR DUAL PACKAGE OPTIONS
PART NUMBER		ISL28022	ISL28023	ISL28025
PACKAGE		MSOP10, QFN16	QFN24	WLCSP-16 / QFN20
Temperature Range		-40°C to +125°C	-40°C to +125°C	-40°C to +125°C
0V to 60V Input Range		0V to 60V	Opt 1: 0V to 60V Opt 2: 0V to 16V	Opt 1: 0V to 60V WLCSP-16 only Opt 2: 0V to 16V
ADC		16-bit	16-bit	16-bit
+25°C Gain Error		0.30%	0.25%	0.25%
Current Measure LSB Step		10µV	2.5µV	2.5µV
+25°C Offset		75µV	30µV	30µV
Primary	Differential Shunt Input	X	X	X
Channel	Independent Bus Voltage	X	X	X
LV Aux	Differential Shunt Input		X	
Channel	Independent Bus Voltage		X	X
VBus LSB Step	Low Voltage Bus		0.25mV	0.25mV
	High Voltage Bus	4mV	1mV/0.25mV	1mV/0.25mV
External Temperature Sensor Input			X	
HV Internal Regulator ($3.3V_{OUT}$)			X	X
Fast OC/OV/UV Alert Outputs			2 Outputs	2 Outputs
Margin DAC			X	QFN20
Internal Temperature Sensor			X	X
User Select Conversion Mode/Sample Rate		X	X	X
Peak Min/Max Current Registers			X	X
Slave Address Locations		16 Addresses	55 Addresses	55 Addresses
I^2C Level Translators			X	X
PMBus			X	X
I^2C/SMBus		X	X	X
High Speed (3.4MHz) I^2C Mode		X	X	X
External Clock Input		X	X	WLCSP-16
Power Shutdown Mode		X	X	X

Absolute Maximum Ratings

VCC 6.0V
I2C_VCC Voltage 6.0V
VBUS (ISL28025FI60), REG_IN 63V
VBUS (ISL28025FI12, ISL28025FR12) 16.684V
Common-Mode Input Voltage (VINP, VINM) 63V
Differential Input Voltage (VINP, VINM) . . . . . ±63V
AUXV . . . . . VCC - GND
Input Voltage (Digital Pins) . . . . . (GND - 0.3) to I2CVCC + 0.3V
Output Voltage (Digital Pins) . . . . . (GND - 0.3) to I2CVCC + 0.3V
Output Current (VREG_OUT, DAC_OUT (20 Pin QFN)) 10mA
Open Drain Output Current 10mA
Open Drain Voltage (SMBALERT1) 24V
ESD Ratings
- Human Body Model 6kV
- Machine Model 300V
- Charged Device Model 2kV

Latch-Up . . . . . ±100mA (at +125°C)

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ball WLCSP (Notes 5, 6)	80	1
20 lead QFN 4x4 (1.85SQmm EPAD) (Notes 5, 6)	40	2.5

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature (T_{JMAX}) . . . . . +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Ambient Temperature Range (T_A) . . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
6. For θ_{JC}, the case temperature location is taken at the package top center. or bottom thermal pad/PCB though hole array.

Electrical Specifications

T_A = +25°C, I2CVCC = V_{CC} = 3.3V, V_{INP} = V_{BUS} = 12V, V_{SENSE} = V_{INP} - V_{INM} = 80mV, Aux V = 3V, Conversion Time: Aux = Primary = 2.05ms, Internal AVG Aux = Primary = 128, unless otherwise specified. All voltages with respect to GND pin. Temperature limits established by characterization.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
PRIMARY CHANNEL						
V_{SHUNT} Measurement Range (V_{INP} to V_{INM})	V_{SHUNT}		0		±81.91	mV
1LSB Step Shunt Voltage	Step_shunt			2.5		µV
V_{SHUNT} Offset Voltage	Vshunt_vos			±2.5	±50	µV
V_{SHUNT} Offset Voltage vs Temperature	Vshunt_TC	T = -40°C to +125°C		±0.04	±0.3	µV/°C
V_{SHUNT} Vos vs Common-Mode	Vshunt_CMRR	ISL28025FI60Z V_{BUS} = 0V to 60V		±0.2	±2	µV/V
		ISL28025FI12Z, ISL28025FR12Z V_{BUS} = 0V to 16.384V		±0.2	±2	µV/V
V_{SHUNT} Vos vs Power Supply	Vshunt_PSRR	V_{CC} = ±10% of V_{CC} nominal		±0.45		µV/V
V_{IN} Input Leakage Current	Ivin	V_{IN} = V_{SHUNT} input path selected, OC detector disabled		15	20	µA
		V_{IN} = V_{SHUNT} input path selected, OC detector enabled		30	40	µA
		V_{IN} = V_{SHUNT} input path disabled, OC detector disabled		0.05	0.1	µA
Usable Bus Voltage Measurement Range	V_{BUS}	ISL28025FI60Z	0		60	V
		ISL28025FI12Z, ISL28025FR12Z	0		16.384	V
1LSB Step Bus Voltage	Step_Vbus	ISL28025FI60Z		1		mV
		ISL28025FI12Z, ISL28025FR12Z		0.25		mV
V_{BUS} Offset Voltage	Vbus_vos	ISL28025FI60Z	-20	±1	20	mV
		ISL28025FI12Z, ISL28025FR12Z	-5	±0.25	5	mV

Electrical Specifications T_A = +25°C, I2CVCC = V_{CC} = 3.3V, V_{INP} = V_{BUS} = 12V, V_{SENSE} = V_{INP} - V_{INM} = 80mV, Aux V = 3V, Conversion Time: Aux = Primary = 2.05ms, Internal AVG Aux = Primary = 128, unless otherwise specified. All voltages with respect to GND pin. Temperature limits established by characterization. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
V_{BUS} Offset Voltage vs Temperature	Vbus_TC	ISL28025FI60Z; T = -40°C to +125°C		±4	±100	µV/°C
		ISL28025FI12Z, ISL28025FR12Z; T = -40°C to +125°C		±1	±100	µV/°C
V_{BUS} Voltage Coefficient	Vbus_Vco			50		ppm/V
V_{BUS} Vos vs Power Supply	Vbus_PSRR	ISL28025FI60Z; V_{CC} = ±10% of V_{CC} nominal		±500		µV/V
		ISL28025FI12Z, ISL28025FR12Z V_{CC} = ±10% of V_{CC} nominal		±125		µV/V
Input Impedance V_{BUS}	Zin_Vbus	ISL28025FI60Z		600		kΩ
		ISL28025FI12Z, ISL28025FR12Z		150		kΩ
AUX CHANNEL						
Usable AVXV Voltage Measurement Range	Vauxv		0		VCC	V
1LSB Step AUXV Voltage	Step_auxv			100		µV
V_{AUXV} Offset Voltage	Vauxv_vos			±0.3	±4	mV
V_{AUXV} Offset Voltage vs Temperature	Vauxv_TC	T = -40°C to +125°C		±0.2	±22	µV/°C
V_{AUXV} Vos vs Power Supply	Vauxv_PSRR	V_{CC} = ±10% of V_{CC} nominal		±1		mV/V
Auxv Input Impedance	Zin_auxv	Input path selected		200		kΩ
		Input path disabled		10		MΩ
ADC PARAMETERS						
ADC Resolution				16		Bits
Primary Shunt Voltage Gain Error				±0.05	±0.25	%
		T = -40°C to +125°C		0	±60	ppm/°C
Primary Bus Voltage Gain Error				±0.05	±0.25	%
		T = -40°C to +125°C		10	±70	ppm/°C
Aux Bus Voltage Gain Error				±0.05	±0.25	%
		T = -40°C to +125°C		10	±65	ppm/°C
Differential Nonlinearity				±1		LSB
ADC TIMING						
ADC Conversion Time Resolution	$t_{S\ Power-Up}$	ADC[2:0] = 0h		64	70.4	µs
		ADC[2:0] = 1h		128	140.8	µs
		ADC[2:0] = 2h		256	281.6	µs
		ADC[2:0] = 3h		512	563.2	µs
		ADC[2:0] = 4, 5h		1.024	1.126	ms
		ADC[2:0] = 6, 7h		2.048	2.253	ms

Electrical Specifications T_A = +25°C, I2CVCC = V_{CC} = 3.3V, V_{INP} = V_{BUS} = 12V, V_{SENSE} = V_{INP} - V_{INM} = 80mV, Aux V = 3V, Conversion Time: Aux = Primary = 2.05ms, Internal AVG Aux = Primary = 128, unless otherwise specified. All voltages with respect to GND pin. Temperature limits established by characterization. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
THRESHOLD DETECTORS						
Overvoltage (OV) V_{BUS} Threshold Voltage Range		Vbus_Thres_Rng[2:0] = ALL	25		125	% of FS
Overvoltage (OV) V_{BUS} Threshold DAC Step Size		Vbus_Thres_Rng[2:0] = ALL		1.56		% of FS
Undervoltage (UV) V_{BUS} Threshold Voltage Range		Vbus_Thres_Rng[2:0] = ALL	0		100	% of FS
Undervoltage (UV) V_{BUS} Threshold DAC Step Size		Vbus_Thres_Rng[2:0] = ALL		1.56		% of FS
V_{BUS} Threshold Detector Full-Scale Settings ISL28025FI60Z		Vbus_Thres_Rng[2:0] = 0; OT_SEL = 0		48		V
		Vbus_Thres_Rng[2:0] = 1; OT_SEL = 0		24		V
		Vbus_Thres_Rng[2:0] = 2; OT_SEL = 0		12		V
		Vbus_Thres_Rng[2:0] = 3; OT_SEL = 0		5		V
		Vbus_Thres_Rng[2:0] = 4; OT_SEL = 0		3.3		V
		Vbus_Thres_Rng[2:0] = 5; OT_SEL = 0		2.5		V
V_{BUS} Threshold Detector Full-Scale Settings ISL28025FI12Z, ISL28025FR12Z		Vbus_Thres_Rng[2:0] = 0; OT_SEL = 0		12		V
		Vbus_Thres_Rng[2:0] = 1; OT_SEL = 0		6		V
		Vbus_Thres_Rng[2:0] = 2; OT_SEL = 0		3		V
		Vbus_Thres_Rng[2:0] = 3; OT_SEL = 0		2.5		V
		Vbus_Thres_Rng[2:0] = 4; OT_SEL = 0		0.825		V
		Vbus_Thres_Rng[2:0] = 5; OT_SEL = 0		0.625		V
Over-Temperature Threshold Detector Range		OT_SEL = 1	-40		135	°C
Over-Temperature Threshold Detector Resolution Error				±5		°C
Overcurrent (OC) V_{SHUNT} Threshold Voltage Range		OCRNG = ALL	25		125	% of FS
Overcurrent (OC) V_{SHUNT} Threshold DAC Step Size		OCRNG = ALL		1.56		% of FS
V_{SHUNT} Threshold Detector Full-Scale Settings		OCRNG = 0		80		mV
		OCRNG = 1		40		mV
MARGINING DAC, ANALOG OUTPUT (20 Pin QFN)						
Resolution				8		Bits
DNL				±1		LSB
INL		MDAC[7:0] = 0 to 256		±3		LSB
Gain Error		DAC_MS[2:0] = 0		±2.5		%
Offset Error		DAC_MS[2:0] = 0		±2		mV
Output Voltage			0.055		2*Vms	V

Electrical Specifications T_A = +25°C, I2CVCC = V_{CC} = 3.3V, V_{INP} = V_{BUS} = 12V, V_{SENSE} = V_{INP} - V_{INM} = 80mV, Aux V = 3V, Conversion Time: Aux = Primary = 2.05ms, Internal AVG Aux = Primary = 128, unless otherwise specified. All voltages with respect to GND pin. Temperature limits established by characterization. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
DAC Mid-Scale	VMS	DAC_MS[2:0] = 0		0.4		V
		DAC_MS[2:0] = 1		0.5		V
		DAC_MS[2:0] = 2		0.6		V
		DAC_MS[2:0] = 3		0.7		V
		DAC_MS[2:0] = 4		0.8		V
		DAC_MS[2:0] = 5		0.9		V
		DAC_MS[2:0] = 6		1.0		V
		DAC_MS[2:0] = 7		1.2		V
Slew Rate				1		V/µs
Output Current				1		mA
Short-Circuit Current		DAC_OUT = V_{CC}			17	mA
		DAC_OUT = GND			4.2	mA
Start-Up Time				100		µs
VOLTAGE REGULATOR SPECIFICATION						
Input Voltage at REG_IN			4.5		60	V
Output Regulation Voltage			3.18	3.3	3.35	V
Line Regulation		V_{IN} 4.5V to 60V		53	150	µV/V
Load Regulation		I_{LOAD} = 3.3mA to 6mA		0.2	1.4	mV/mA
Capacitance Drive			0.01		10	µF
Output Short-Circuit		T = -40°C to +125°C		10		mA
Maximum Load Current		T = -40°C to +125°C		6		mA
Start-Up Time				1		ms
TEMPERATURE SENSOR						
Temperature Sensor Measurement Range			-40		125	°C
Temperature Accuracy		T = +25°C		+3.2		°C
Temperature Resolution				0.5		°C
Measurement Time				0.5		ms
SMBus/I^2C INTERFACE SPECIFICATIONS						
SMBDAT and SMBCLK Input Buffer Low Voltage	V_{IL}		-0.3		0.3 x I2CVCC	V
SMBDAT and SMBCLK Input Buffer High Voltage	V_{IH}		0.7 x I2CVCC		I2CVCC + 0.3	V
SMBDAT and SMBCLK Input Buffer Hysteresis	Hysteresis			0.05 x I2CVCC		V
SMBDAT Output Buffer Low Voltage, Sinking 3mA	V_{OL}	I2CVCC = 5V, I_{OL} = 3mA	0	0.02	0.4	V
SMBDAT and SMBCLK Pin Capacitance	C_{PIN}	T_A = +25°C, f = 1MHz, I2CVCC = 5V, V_{IN} = 0V, V_{OUT} = 0V			10	pF
SMBCLK Frequency	f_{SMBCLK}				400	kHz

Electrical Specifications T_A = +25°C, I2CVCC = V_{CC} = 3.3V, V_{INP} = V_{BUS} = 12V, V_{SENSE} = V_{INP} - V_{INM} = 80mV, Aux V = 3V, Conversion Time: Aux = Primary = 2.05ms, Internal AVG Aux = Primary = 128, unless otherwise specified. All voltages with respect to GND pin. Temperature limits established by characterization. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
Pulse Width Suppression Time at SMBDAT and SMBCLK Inputs	t_{IN}	Any pulse narrower than the maximum specification is suppressed			50	ns
SMBCLK Falling Edge to SMBDAT Output Data Valid	t_{AA}	SMBCLK falling edge crossing 30% of I2CVCC, until SMBDAT exits the 30% to 70% of I2CVCC window			900	ns
Time the Bus Must be Free Before the Start of a New Transmission	t_{BUF}	SMBDAT crossing 70% of I2CVCC during a STOP condition, to SMBDAT crossing 70% of I2CVCC during the following START condition	1300			ns
Clock Low Time	t_{LOW}	Measured at the 30% of I2CVCC crossing	1300			ns
Clock High Time	t_{HIGH}	Measured at the 70% of I2CVCC crossing	600			ns
START Condition Set-Up Time	$t_{SU:STA}$	SMBCLK rising edge to SMBDAT falling edge. Both crossing 70% of I2CVCC	600			ns
START Condition Hold Time	$t_{HD:STA}$	From SMBDAT falling edge crossing 30% of I2CVCC to SMBCLK falling edge crossing 70% of I2CVCC	600			ns
Input Data Set-Up Time	$t_{SU:DAT}$	From SMBDAT exiting the 30% to 70% of V_{CC} window, to SMBCLK rising edge crossing 30% of I2CVCC	100			ns
Input Data Hold Time	$t_{HD:DAT}$	From SMBCLK falling edge crossing 30% of I2CVCC to SMBDAT entering the 30% to 70% of I2CVCC window	20		900	ns
STOP Condition Set-Up Time	$t_{SU:STO}$	From SMBCLK rising edge crossing 70% of I2CVCC, to SMBDAT rising edge crossing 30% of I2CVCC	600			ns
STOP Condition Hold Time	$t_{HD:STO}$	From SMBDAT rising edge to SMBCLK falling edge. Both crossing 70% of I2CVCC	600			ns
Output Data Hold Time	t_{DH}	From SMBCLK falling edge crossing 30% of I2CVCC, until SMBDAT enters the 30% to 70% of I2CVCC window	0			ns
SMBDAT and SMBCLK Rise Time	t_R	From 30% to 70% of I2CVCC	20 + 0.1 x Cb		300	ns
SMBDAT and SMBCLK Fall Time	t_F	From 70% to 30% of I2CVCC	20 + 0.1 x Cb		300	ns
Capacitive Loading of SMBDAT or SMBCLK	Cb	Total on-chip and off-chip	10		400	pF
SMBDAT and SMBCLK Bus Pull-Up Resistor Off-Chip	R_{PU}	Maximum is determined by t_R and t_F For Cb = 400pF, max is about 2kΩ ~ 2.5kΩ. For Cb = 40pF, max is about 15kΩ ~ 20kΩ	1			kΩ
POWER SUPPLY						
Power Supply Voltage at VCC	Vvcc		3.0	3.3	5.5	V
Power Supply Voltage at I2CVCC	Vi2cvcc	f = DC to 400kHz	1.2	3.3	5.5	V
Only ADC in Conversion mode		All other blocks are disabled		690	830	µA

Electrical Specifications

T_A = +25°C, I2CVCC = V_{CC} = 3.3V, V_{INP} = V_{BUS} = 12V, V_{SENSE} = V_{INP} - V_{INM} = 80mV, Aux V = 3V, Conversion Time: Aux = Primary = 2.05ms, Internal AVG Aux = Primary = 128, unless otherwise specified. All voltages with respect to GND pin. Temperature limits established by characterization. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
Only ADC in Idle Mode		All other blocks are disabled		640	705	µA
Only Threshold Detectors		All three detectors are active		760	945	µA
Fully Enabled Chip Current		All functional blocks enabled		1000	1260	µA
Fully Disabled Chip Current		All functional blocks disabled		5	15	µA
Voltage Regulator	Ivreg_in	Vreg_in = 4.5V to 60V; R_{LOAD} = open		26	35	µA
I^2C Supply Current	Ii2cvcc	SMBCLK = 100kHz; I2CVCC = 3.3V		15		µA
I^2C Idle Supply Current	Ii2cvcc_pd	Input signals are static		100		nA

NOTE:

7. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Compliance to datasheet limits is assured by one or more of the following methods: production test, characterization and design.

Typical Performance Curves

T_A = +25°C, V_{CC} = 3.3V, V_{INP} = V_{BUS} = 12V, Auxv = 3V, conversion time; Aux = Primary = 2.05ms, Internal AVG Aux = Primary = 128, unless otherwise specified.

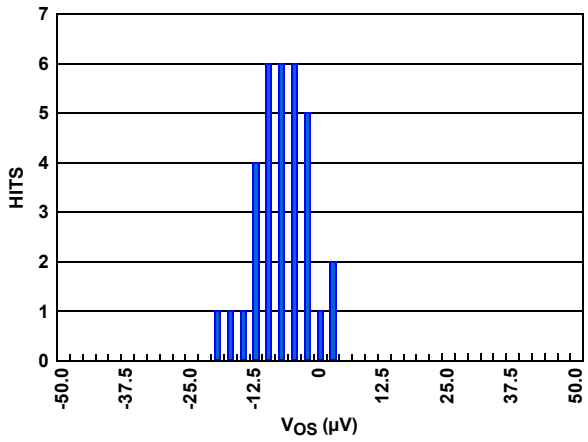


FIGURE 3. PRIMARY V_{SHUNT} V_{OS}

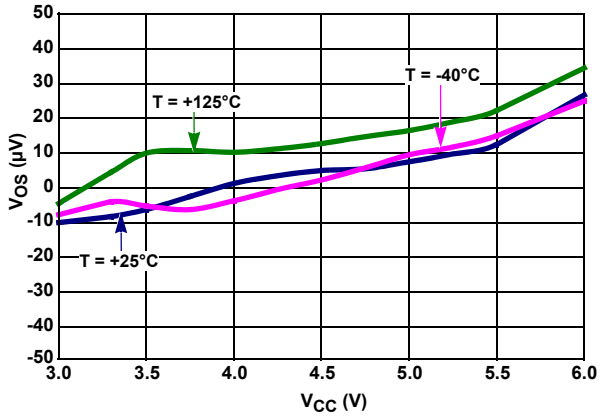


FIGURE 4. PRIMARY V_{SHUNT} V_{OS} vs VCC

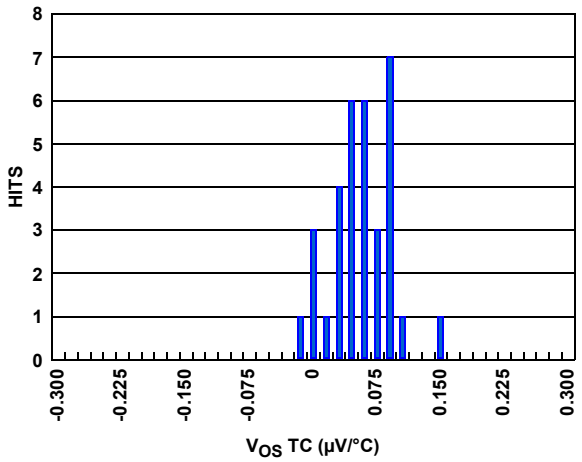


FIGURE 5. PRIMARY V_{SHUNT} V_{OS} TC (-40°C TO +125°C)

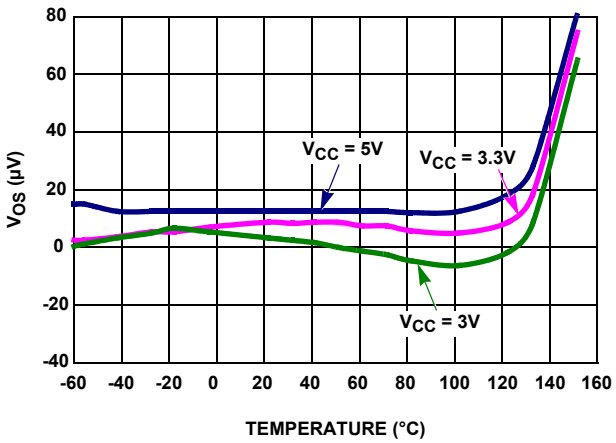


FIGURE 6. PRIMARY V_{SHUNT} V_{OS} vs TEMPERATURE

Typical Performance Curves

T_A = +25°C, V_{CC} = 3.3V, V_{INP} = V_{BUS} = 12V, Auxv = 3V, conversion time; Aux = Primary = 2.05ms, Internal AVG Aux = Primary = 128, unless otherwise specified. **(Continued)**

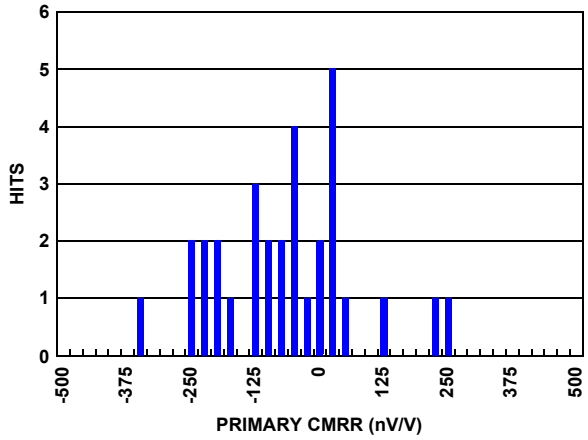


FIGURE 7. PRIMARY V_{SHUNT} CMRR, CMV = (0V TO 60V)

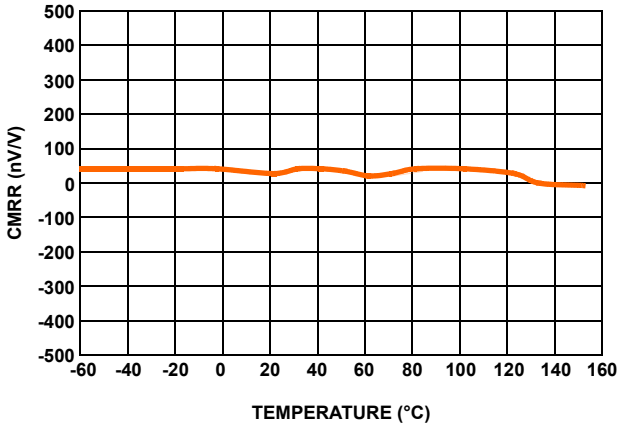


FIGURE 8. PRIMARY V_{SHUNT} CMRR vs TEMPERATURE (CMV = 0V TO 60V)

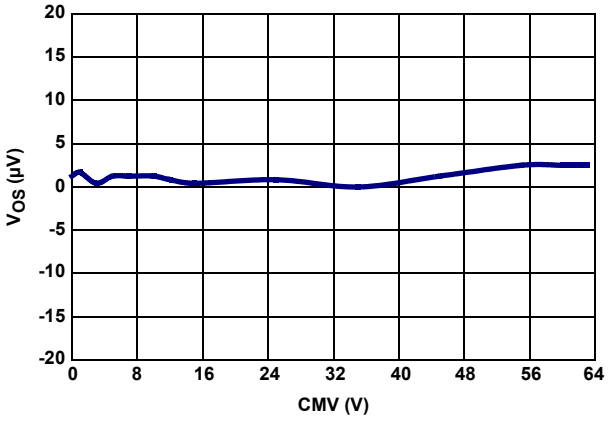


FIGURE 9. PRIMARY V_{SHUNT} V_{OS} vs CMV

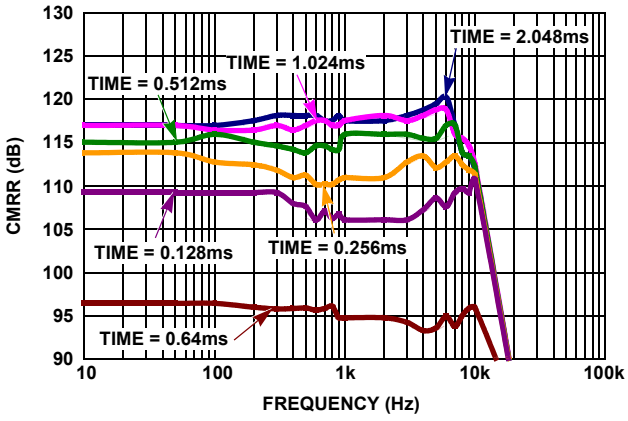


FIGURE 10. PRIMARY V_{SHUNT} AC CMRR vs FREQUENCY

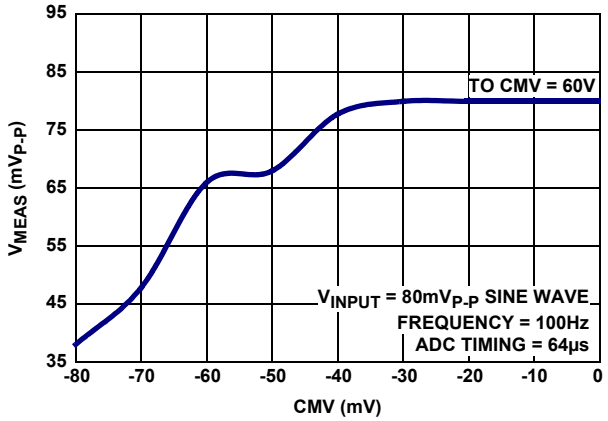


FIGURE 11. PRIMARY V_{SHUNT} COMMON-MODE RANGE

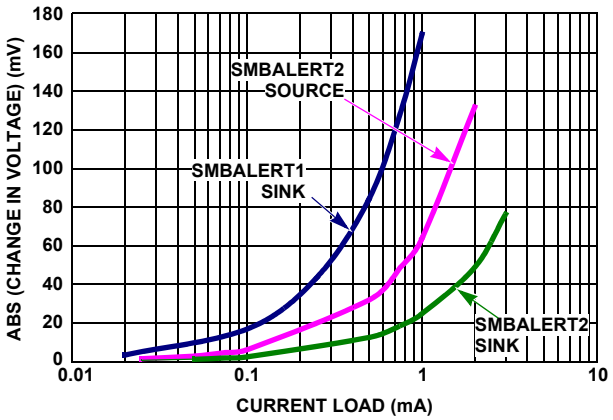


FIGURE 12. SMBALERT CURRENT DRIVES

Typical Performance Curves

T_A = +25°C, V_{CC} = 3.3V, V_{INP} = V_{BUS} = 12V, Auxv = 3V, conversion time; Aux = Primary = 2.05ms, Internal AVG Aux = Primary = 128, unless otherwise specified. **(Continued)**

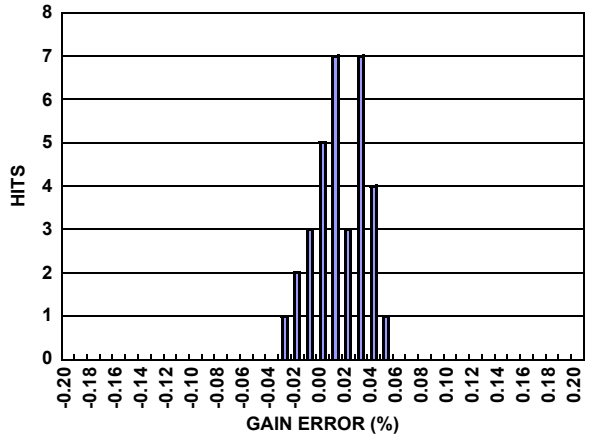


FIGURE 13. PRIMARY V_{SHUNT} ADC GAIN ERROR

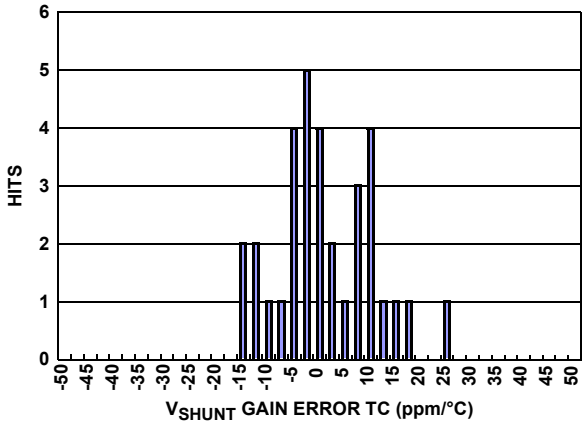


FIGURE 14. PRIMARY V_{SHUNT} ADC GAIN ERROR TC

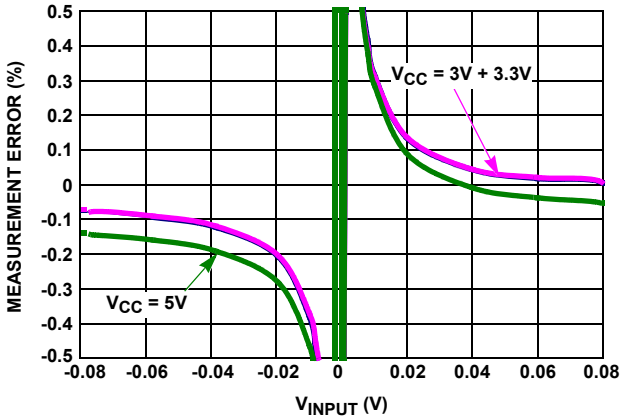


FIGURE 15. PRIMARY V_{SHUNT} MEASUREMENT ERROR vs INPUT

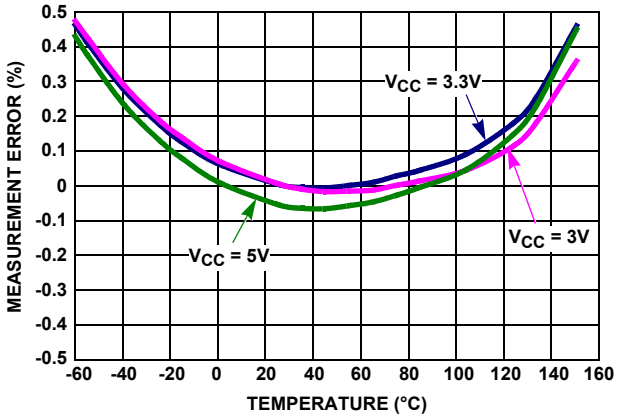


FIGURE 16. PRIMARY V_{SHUNT} MEASUREMENT ERROR vs TEMPERATURE

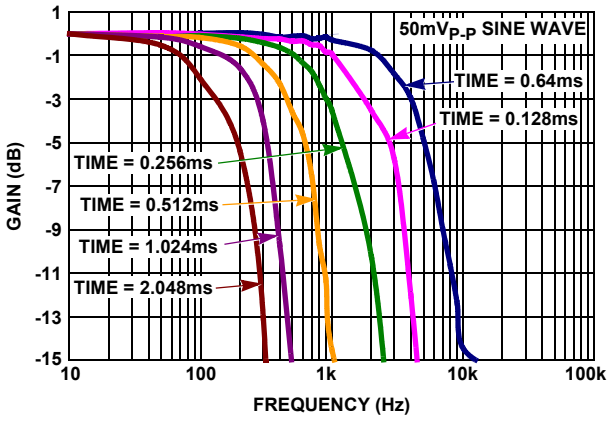


FIGURE 17. PRIMARY V_{SHUNT} BANDWIDTH vs ADC TIMING

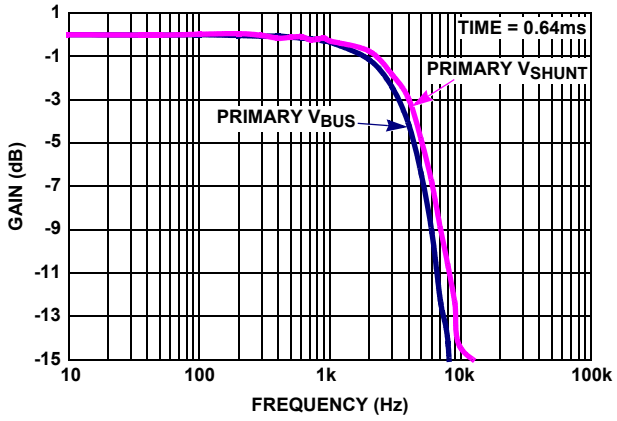


FIGURE 18. PRIMARY V_{SHUNT} AND V_{BUS} vs FREQUENCY

Typical Performance Curves

T_A = +25°C, V_{CC} = 3.3V, V_{INP} = V_{BUS} = 12V, Auxv = 3V, conversion time; Aux = Primary = 2.05ms, Internal AVG Aux = Primary = 128, unless otherwise specified. **(Continued)**

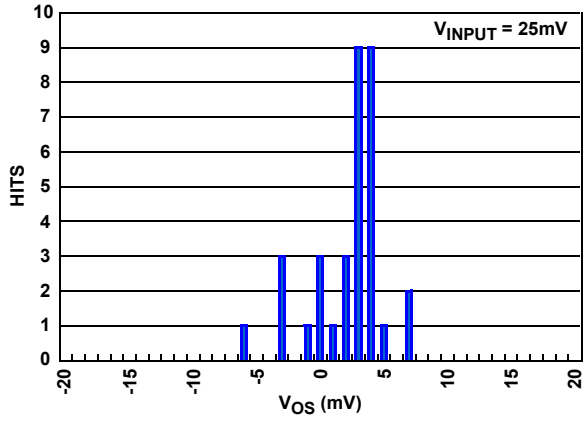


FIGURE 19. PRIMARY V_{BUS} V_{OS}

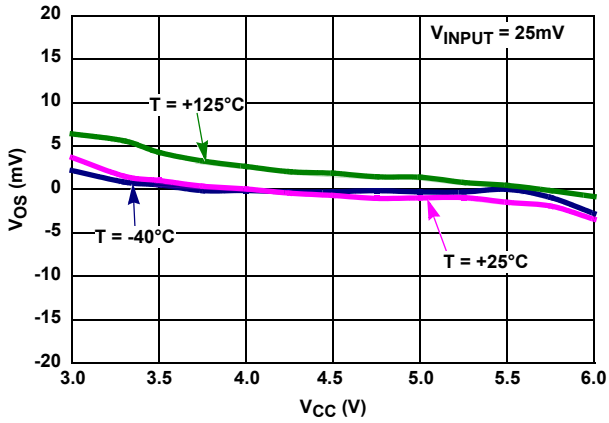


FIGURE 20. PRIMARY V_{BUS} V_{OS} vs V_{CC}

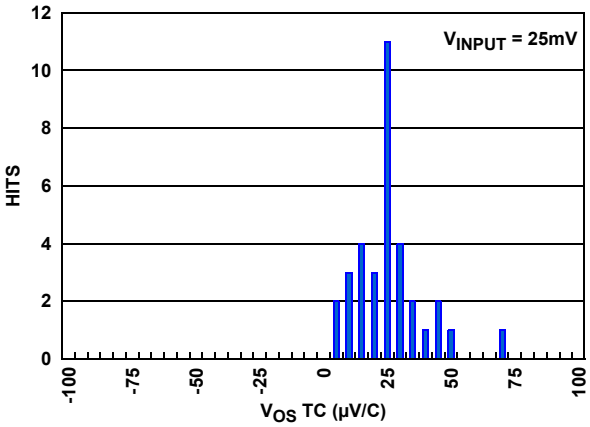


FIGURE 21. PRIMARY V_{BUS} V_{OS} TC

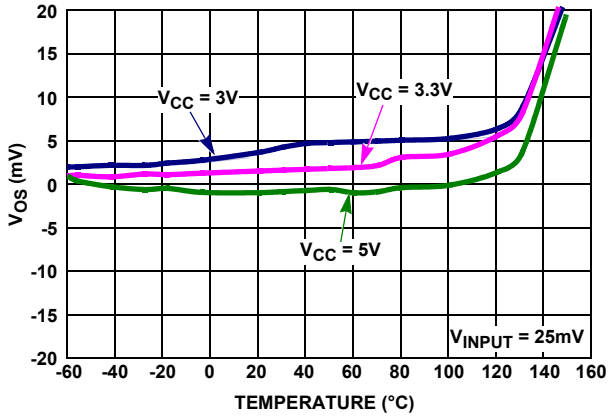


FIGURE 22. PRIMARY V_{BUS} V_{OS} vs TEMPERATURE

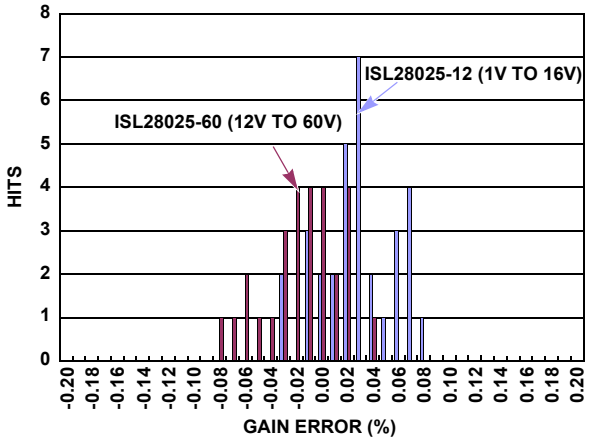


FIGURE 23. PRIMARY V_{BUS} ADC GAIN ERROR

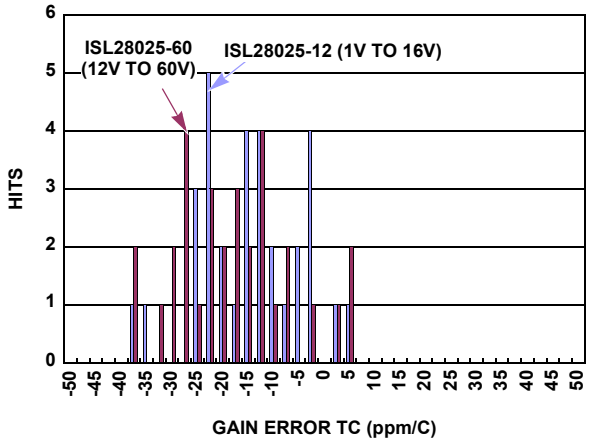


FIGURE 24. PRIMARY V_{BUS} ADC GAIN ERROR TC

Typical Performance Curves

T_A = +25°C, V_{CC} = 3.3V, V_{INP} = V_{BUS} = 12V, Auxv = 3V, conversion time; Aux = Primary = 2.05ms, Internal AVG Aux = Primary = 128, unless otherwise specified. **(Continued)**

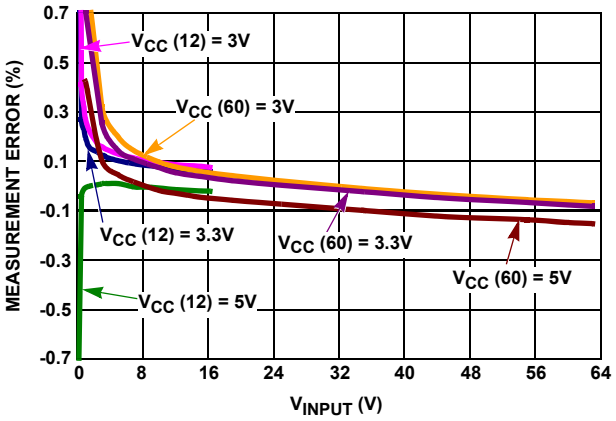


FIGURE 25. PRIMARY V_{BUS} MEASUREMENT ERROR vs INPUT

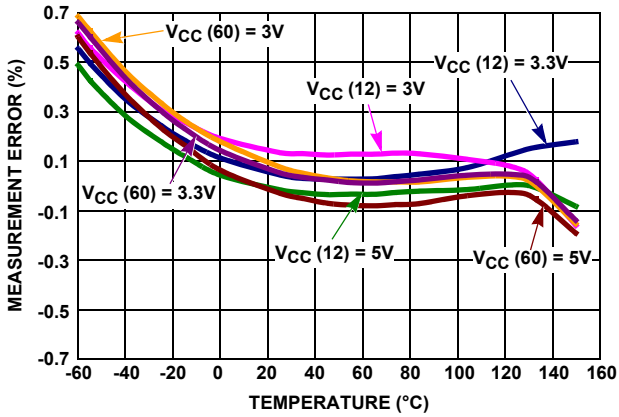


FIGURE 26. PRIMARY V_{BUS} MEASUREMENT ERROR vs TEMPERATURE

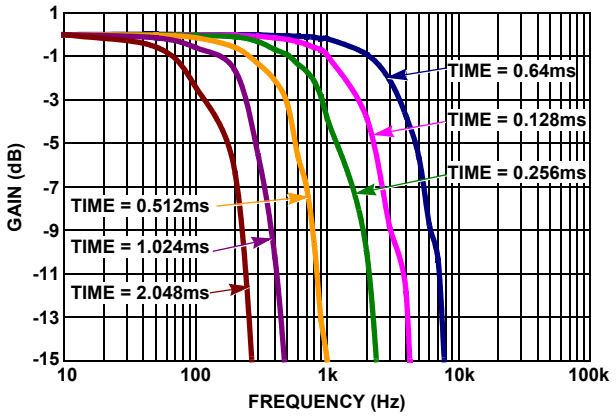


FIGURE 27. AUXILIARY V_{BUS} BANDWIDTH vs ADC TIMING

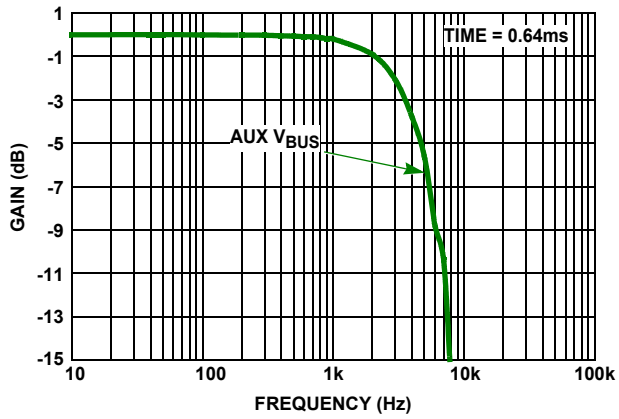


FIGURE 28. AUXILIARY V_{SHUNT} AND V_{BUS} vs FREQUENCY

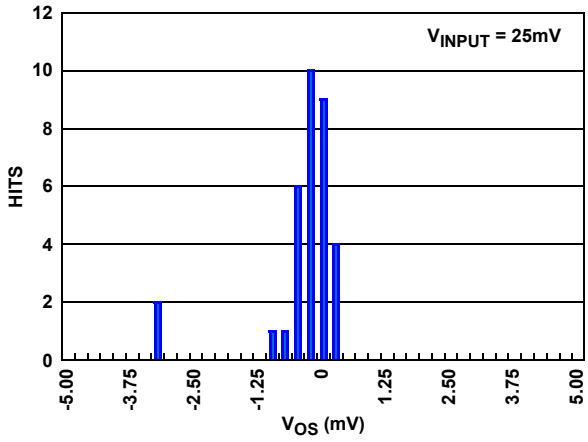


FIGURE 29. AUXILIARY V_{BUS} V_{OS}

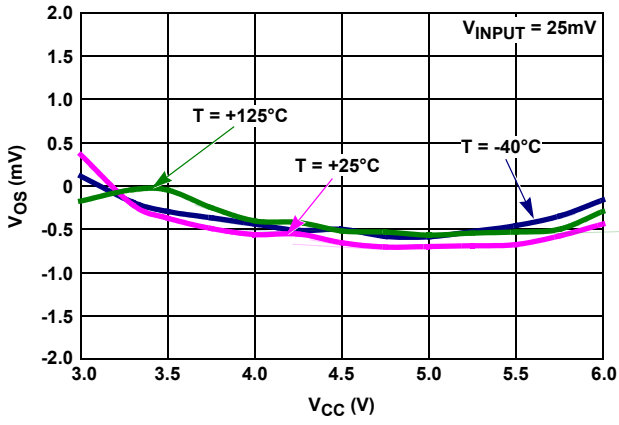


FIGURE 30. AUXILIARY V_{BUS} V_{OS} vs V_{CC}

Typical Performance Curves

T_A = +25°C, V_{CC} = 3.3V, V_{INP} = V_{BUS} = 12V, Auxv = 3V, conversion time; Aux = Primary = 2.05ms, Internal AVG Aux = Primary = 128, unless otherwise specified. **(Continued)**

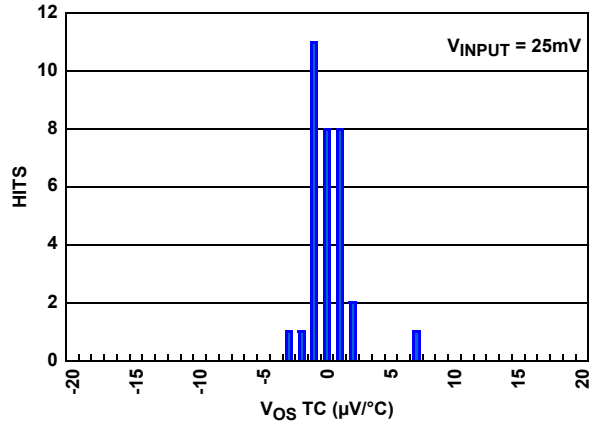


FIGURE 31. AUXILIARY V_{BUS} V_{OS} TC

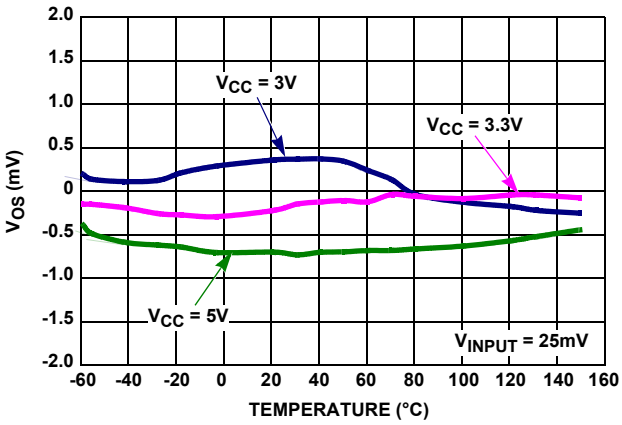


FIGURE 32. AUXILIARY V_{BUS} VOS vs TEMPERATURE

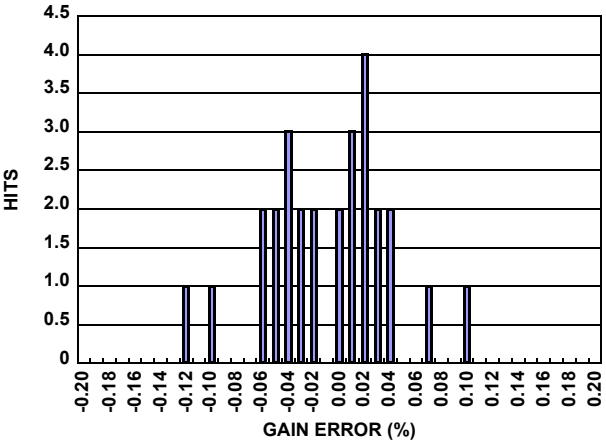


FIGURE 33. AUXILIARY V_{BUS} ADC GAIN ERROR

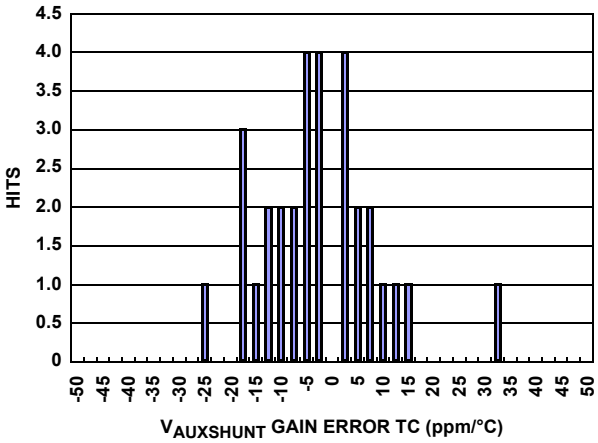


FIGURE 34. AUXILIARY V_{BUS} ADC GAIN ERROR TC

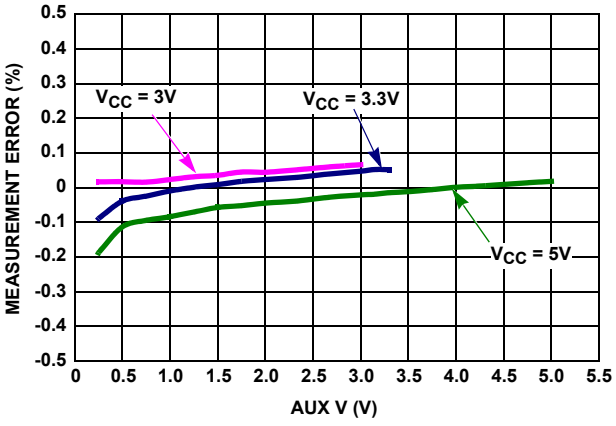


FIGURE 35. AUXILIARY V_{BUS} MEASUREMENT ERROR vs INPUT

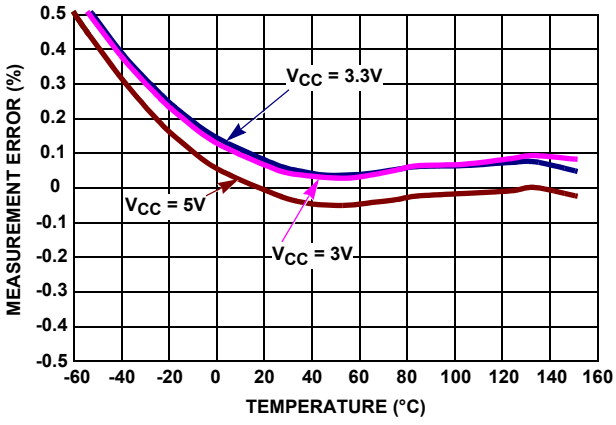


FIGURE 36. AUXILIARY V_{BUS} MEASUREMENT ERROR vs TEMPERATURE

Typical Performance Curves

T_A = +25°C, V_{CC} = 3.3V, V_{INP} = V_{BUS} = 12V, Auxv = 3V, conversion time; Aux = Primary = 2.05ms, Internal AVG Aux = Primary = 128, unless otherwise specified. **(Continued)**

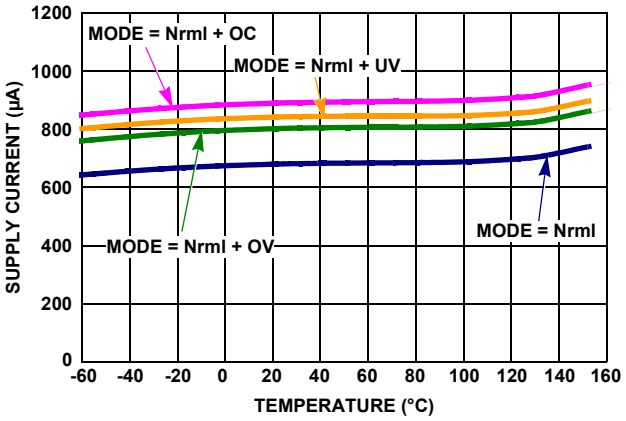


FIGURE 37. SUPPLY CURRENT vs TEMPERATURE

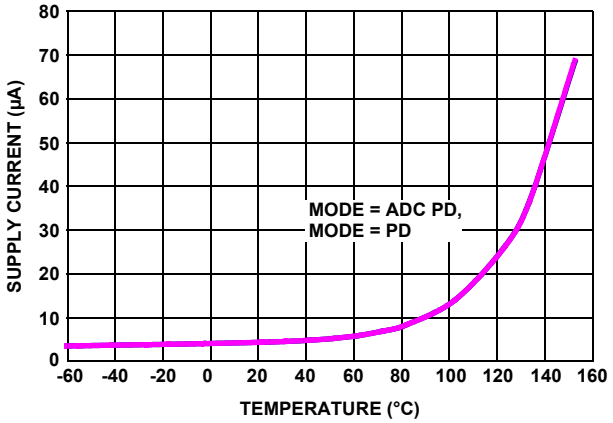


FIGURE 38. POWER-DOWN SUPPLY CURRENT vs TEMPERATURE

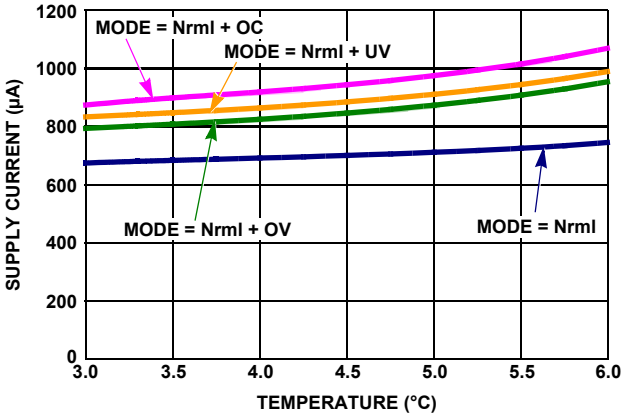


FIGURE 39. SUPPLY CURRENT vs SUPPLY VOLTAGE

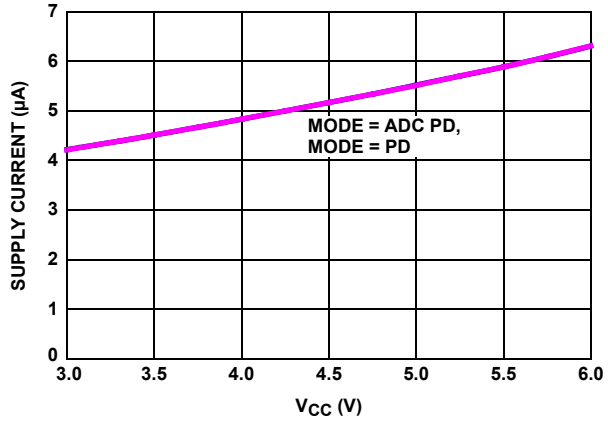


FIGURE 40. SUPPLY CURRENT vs SUPPLY VOLTAGE (POWER-DOWN MODES)

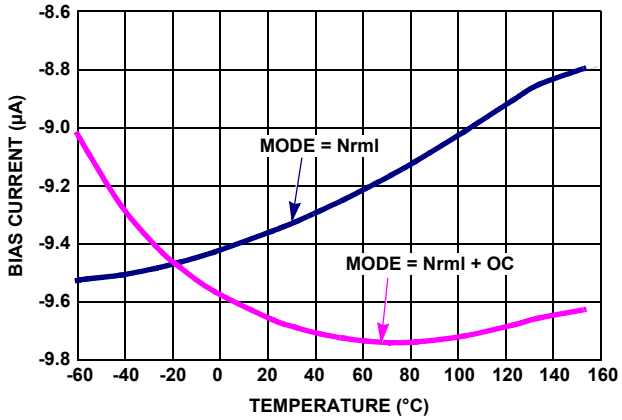


FIGURE 41. PRIMARY V_{SHUNT} BIAS CURRENT vs TEMPERATURE

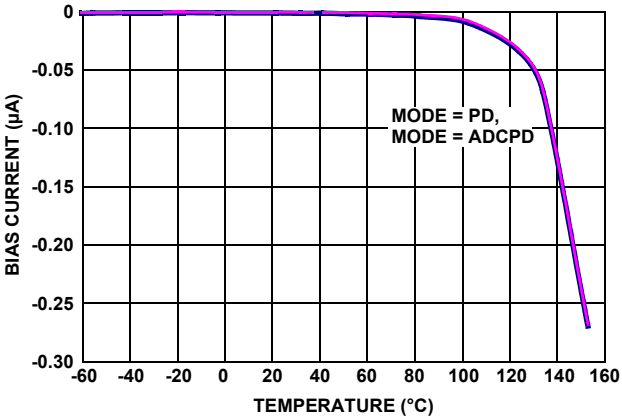


FIGURE 42. PRIMARY V_{SHUNT} BIAS CURRENT vs TEMPERATURE (POWER-DOWN MODE)

Typical Performance Curves

T_A = +25°C, V_{CC} = 3.3V, V_{INP} = V_{BUS} = 12V, Auxv = 3V, conversion time; Aux = Primary = 2.05ms, Internal AVG Aux = Primary = 128, unless otherwise specified. **(Continued)**

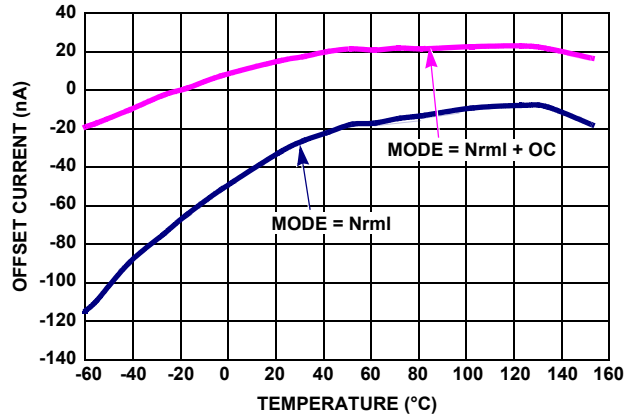


FIGURE 43. PRIMARY V_{SHUNT} BIAS CURRENT OFFSET vs TEMPERATURE

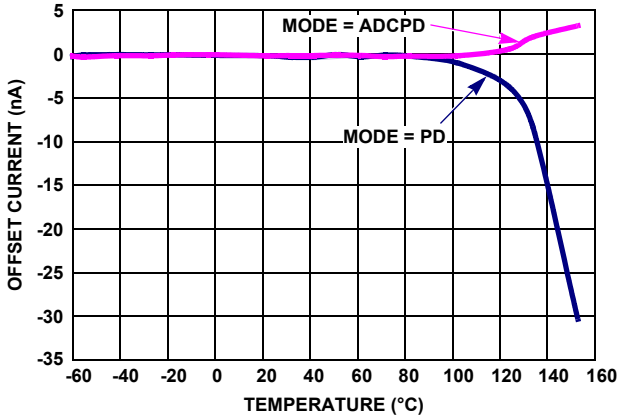


FIGURE 44. PRIMARY V_{SHUNT} BIAS CURRENT OFFSET vs TEMPERATURE (POWER-DOWN MODE)

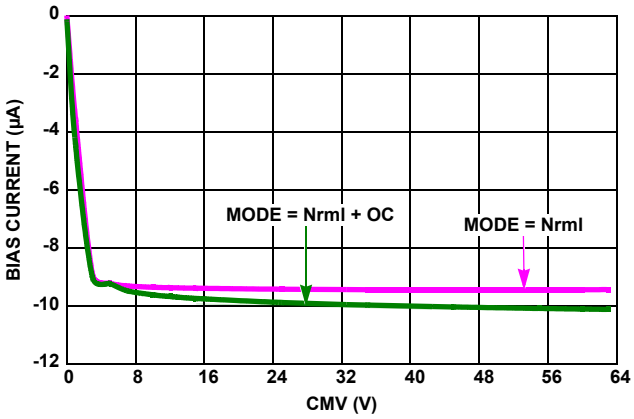


FIGURE 45. PRIMARY V_{SHUNT} BIAS CURRENT vs COMMON-MODE VOLTAGE

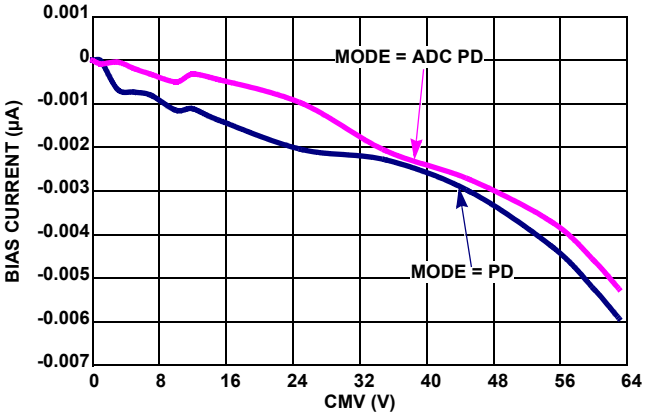


FIGURE 46. PRIMARY V_{SHUNT} BIAS CURRENT vs COMMON-MODE VOLTAGE (POWER-DOWN MODES)

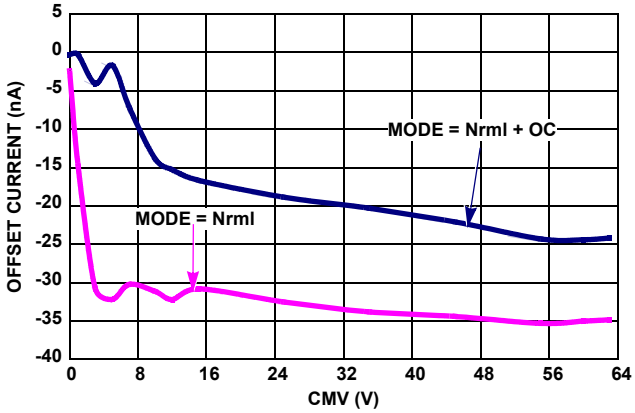


FIGURE 47. PRIMARY V_{SHUNT} OFFSET CURRENT vs COMMON-MODE VOLTAGE

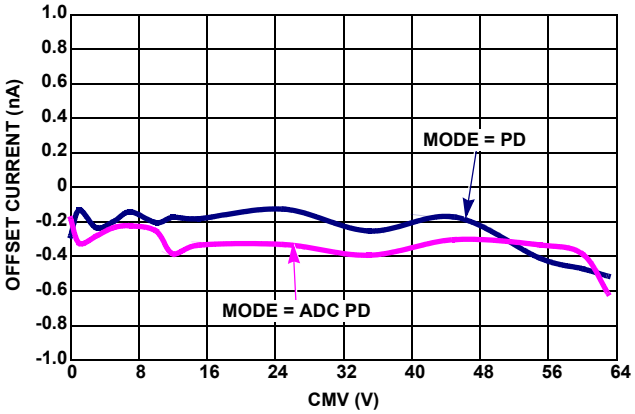


FIGURE 48. PRIMARY V_{SHUNT} OFFSET CURRENT vs COMMON-MODE VOLTAGE (POWER DOWN MODES)

Typical Performance Curves

T_A = +25°C, V_{CC} = 3.3V, V_{INP} = V_{BUS} = 12V, Auxv = 3V, conversion time; Aux = Primary = 2.05ms, Internal AVG Aux = Primary = 128, unless otherwise specified. **(Continued)**

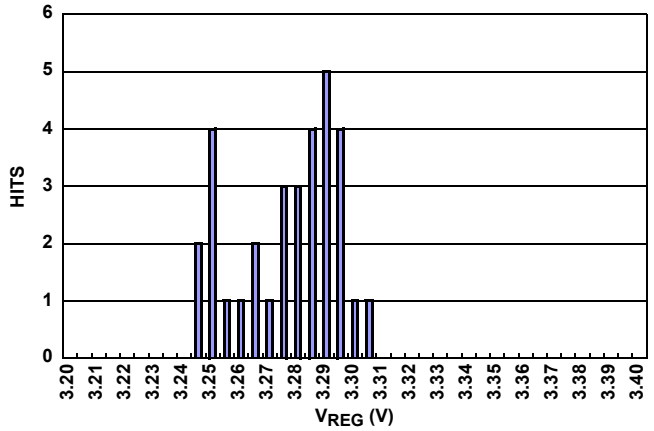


FIGURE 49. V_{REG} OUTPUT VOLTAGE DISTRIBUTION

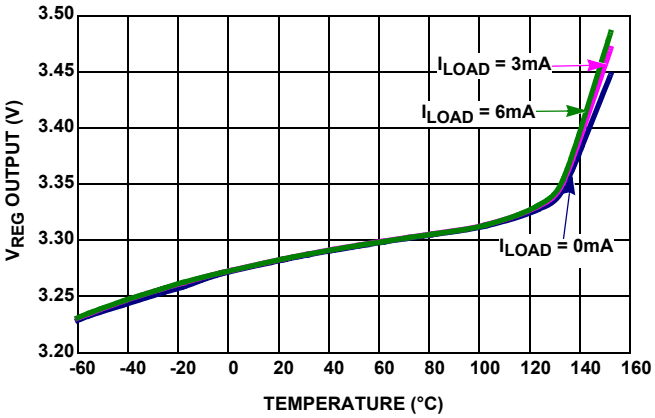


FIGURE 50. V_{REG} OUTPUT vs TEMPERATURE

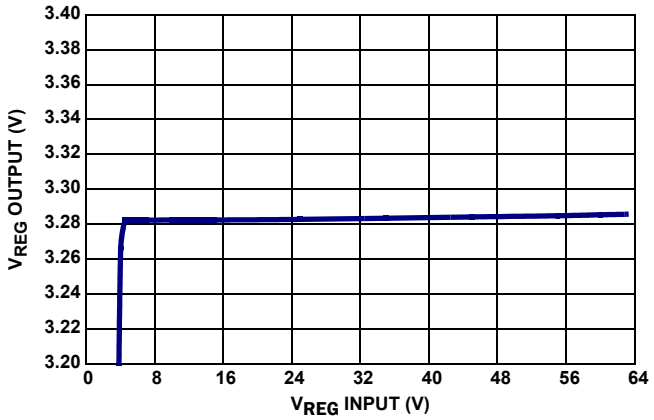


FIGURE 51. V_{REG} OUTPUT vs INPUT VOLTAGE

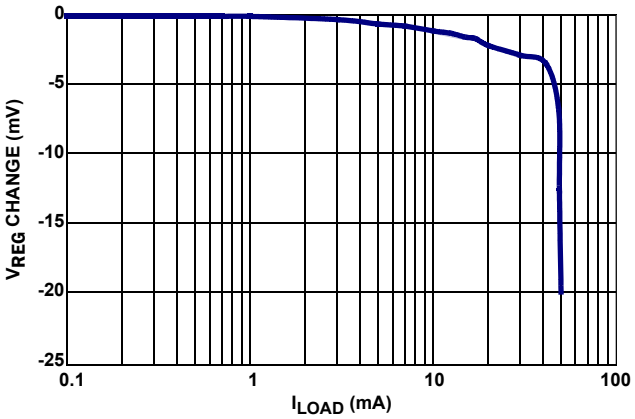


FIGURE 52. V_{REG} OUTPUT vs CURRENT LOAD

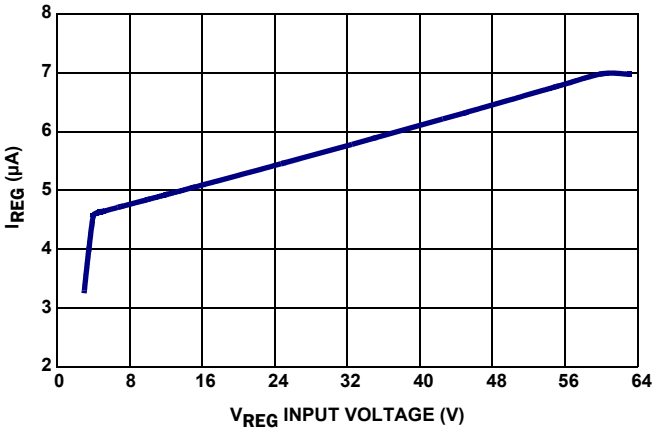


FIGURE 53. V_{REG} INPUT CURRENT vs INPUT VOLTAGE

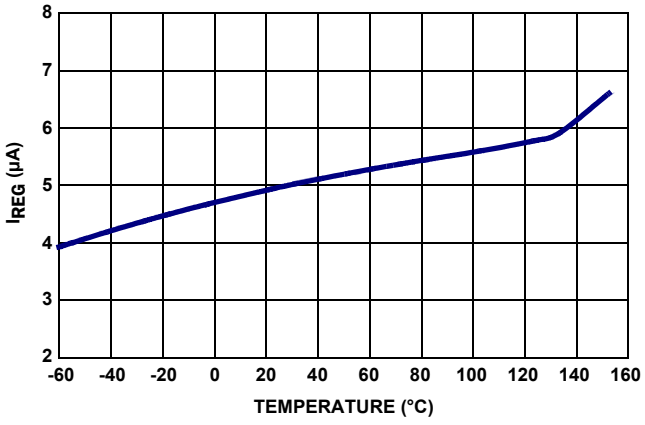


FIGURE 54. V_{REG} INPUT CURRENT vs TEMPERATURE

Typical Performance Curves

T_A = +25°C, V_{CC} = 3.3V, V_{INP} = V_{BUS} = 12V, Auxv = 3V, conversion time; Aux = Primary = 2.05ms, Internal AVG Aux = Primary = 128, unless otherwise specified. **(Continued)**

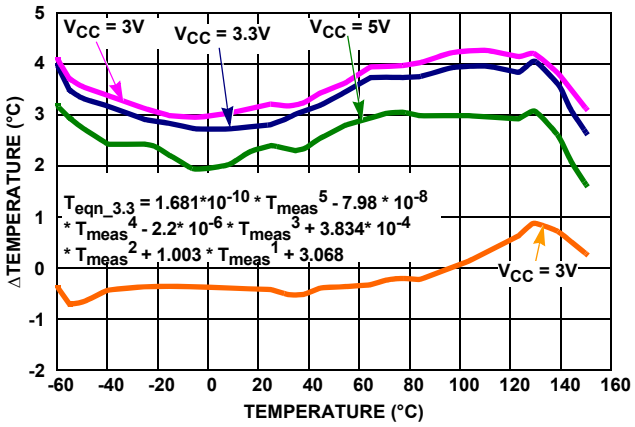


FIGURE 55. INTERNAL TEMPERATURE SENSOR ACCURACY

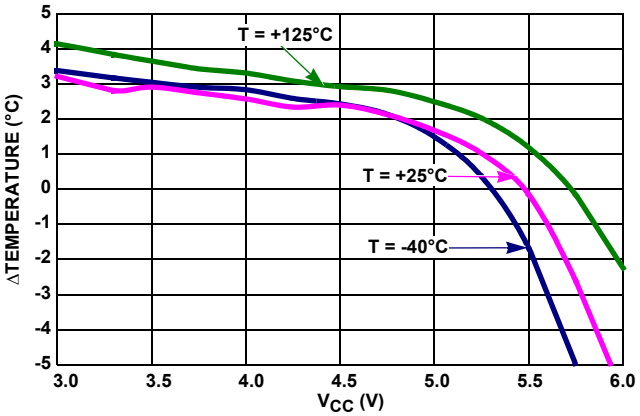


FIGURE 56. INTERNAL TEMPERATURE ACCURACY vs V_{CC}

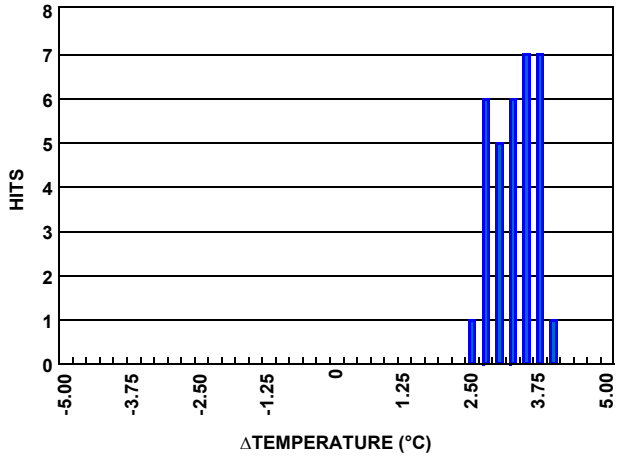


FIGURE 57. INTERNAL TEMPERATURE ACCURACY AT T = +25°C

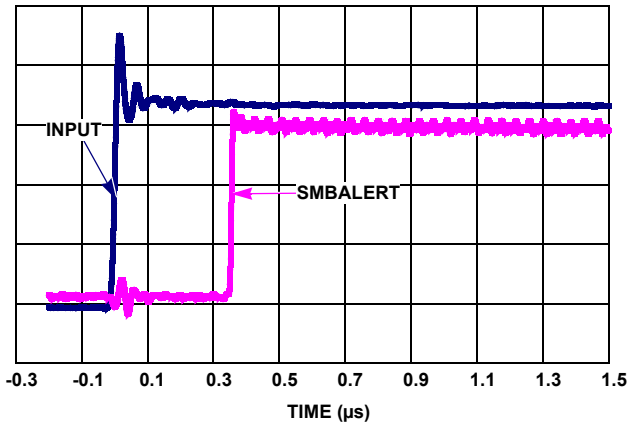


FIGURE 58. OV OR UV OR OC ALERT RESPONSE TIME

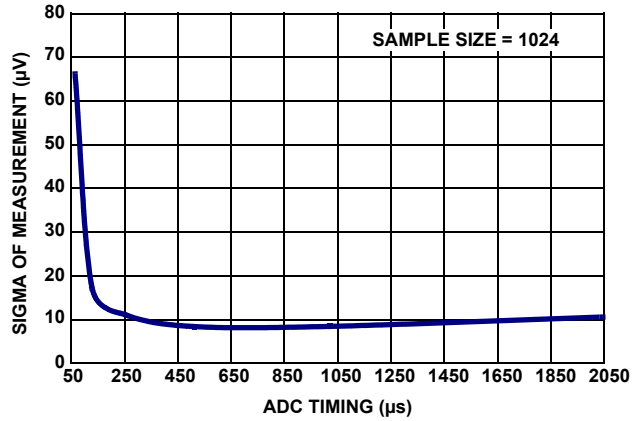


FIGURE 59. PRIMARY SHUNT STABILITY: STDEV vs ACQUISITION TIME

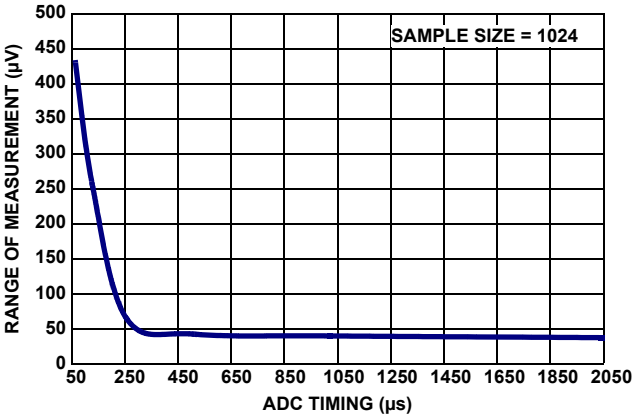


FIGURE 60. PRIMARY SHUNT STABILITY: RANGE vs ACQUISITION TIME

Typical Performance Curves

T_A = +25°C, V_{CC} = 3.3V, V_{INP} = V_{BUS} = 12V, Auxv = 3V, conversion time; Aux = Primary = 2.05ms, Internal AVG Aux = Primary = 128, unless otherwise specified. **(Continued)**

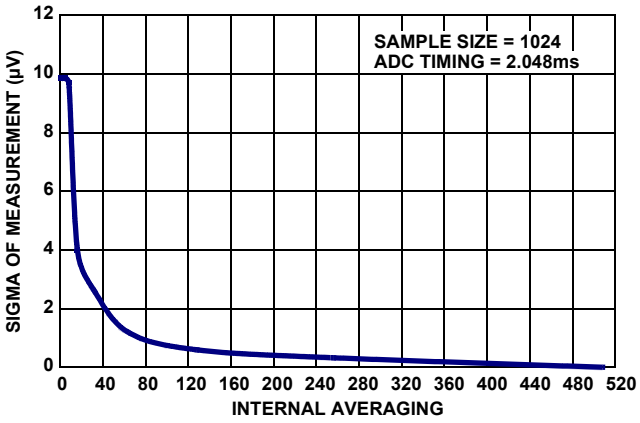


FIGURE 61. PRIMARY SHUNT STABILITY: STDEV vs INTERNAL AVERAGING

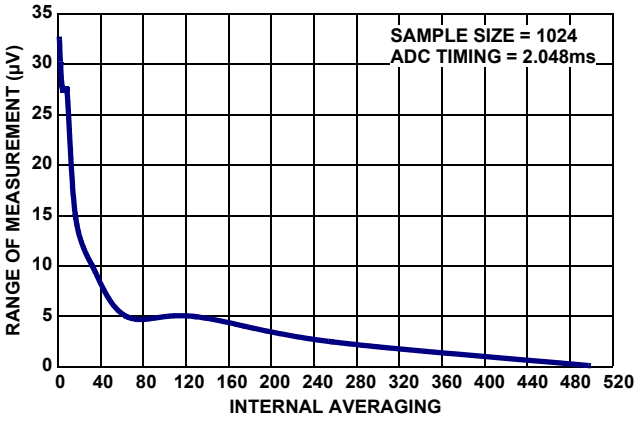


FIGURE 62. PRIMARY SHUNT STABILITY: RANGE vs INTERNAL AVERAGING

Functional Description

Overview

The ISL28025 is a digital current, voltage and power monitoring device for high and low-side power monitoring in positive and negative voltage applications.

The Digital Power Monitor (DPM) requires an external shunt resistor to enable current measurements. The shunt resistor translates the bus current to a voltage. The DPM measures the voltage across the shunt resistors and reports the measured value out digitally using an I^2C interface. A register within the DPM is reserved to store the value of the shunt resistor. The stored current sense resistor value allows the DPM to output a current value to an external digital device.

The ISL28025 can monitor the voltage, current and power of a power supply rail. The ISL28025 has an additional low voltage read to measure a voltage after the rail has been regulated. The primary channel will allow and measure voltages from 0V to 60V or from 0V to 16.384V, depending on the option of the ISL28025. The auxiliary channel can tolerate and measure voltage from 0V to VCC.

The ISL28025 has continuous fault detection for the primary channel. The DPM can be configured to set an alert in the instance of an overvoltage, undervoltage and/or overcurrent event. The response time of the alert is 500ns from the event. The ISL28025 has a temperature sensor with fault detection.

An 8-bit margin DAC, controllable through I^2C communication, is incorporated into the DPM. The voltage margining feature allows for the adjustment of the regulated voltage to the load. The margin DAC can help in proving the load robustness versus the applied supply voltage.

The ISL28025 offers a 3.3V voltage regulator that can be used to power the chip in addition to low power peripheral circuitry. The DPM has an I^2C power pin that allows the I^2C master to set the digital communication supply voltage to the chip. The operating supply voltage for the DPM ranges from 3V to 5.5V. The device will accept I^2C supply voltages between 1.2V and 5.5V.

The ISL28025 accepts SMBus protocols up to 3.4MHz. The device is PMBus compliant up to 400MHz. The device has Packet Error Code (PEC) functionality. The PEC protocol uses an 8-bit Cyclic Redundance Check (CRC-8) represented by the polynomial $x^8+x^2+x^1+1$. The ISL28025 can be configured for up to 55 unique slave addresses using three address select bits. The large amount of addressing allows 55 parts to communicate on a single I^2C bus. It also gives the designer the flexibility to select a unique address when another slave address conflicts with the DPM on the same I^2C bus.

Functional Pin Descriptions

VBUS

VBUS is the power bus voltage input pin. The pin should be connected to the desired power supply bus to be monitored. The voltage range for the pin is from 0V to 60V or 0V to 16V depending on the ISL28025 version.

VINP

VINP is the shunt voltage monitor positive input pin. The pin connects to the most positive voltage of the current shunt resistor. The voltage range for the pin is from 0V to 60V or 0V to 16V depending on the ISL28025 version. The maximum measurable voltage differential between VINP and VINM is 80mV.

VINM

VINM is the shunt voltage monitor negative input pin. The pin connects to the most negative voltage of the current shunt resistor. The voltage range for the pin is from 0V to 60V or 0V to 16V depending on the ISL28025 version. The maximum measurable voltage differential between VINP and VINM is 80mV.

AUXV

AUXV is the power bus voltage input pin. The pin should be connected to the desired power supply bus to be monitored. The voltage range for the pin is from 0V to VCC.

VCC

VCC is the positive supply voltage pin. VCC is an analog power pin. VCC supplies power to the device. The allowable voltage range is from 3V to 5.5V.

I2CVCC

I2CVCC is the positive supply voltage pin. I2CVCC is an analog power pin. I2CVCC supplies power to the digital communication circuitry, I^2C, of the device. The allowable voltage range is from 1.2V to 5.5V.

GND

GND is the device ground pin. For single supply systems, the pin connects to system ground. For dual supply systems, the pin connects to the negative voltage supply in the system.

VREG_IN

VREG_IN is the voltage regulator input pin. The operable input voltage range to the regulator is 4.5V to 60V.

VREG_OUT

VREG_OUT is the voltage regulator output pin. The regulated output voltage of 3.3V is sourced from the VREG_OUT pin.

DAC_OUT (20PIN QFN)

DAC_OUT is the margin DAC output pin. The output of the DAC voltage ranges from 0V to 2.4V. The voltage DAC is controlled through internal registers.

ADDRESS PINS (A0, A1, A2)

A0, A1 and A2 are address selectable pins. The address pins are I^2C/SMBus slave address select pins that are multilogic programmable for a total of 55 different address combinations. There are four selectable levels for the address pins, I2CVCC, GND, SCL/SMBCLK and SDA/SMBDAT. See Table 48 on page 40 for more details in setting the slave address of the device.

SMBDAT

SDA/SMBDAT is the serial data input/output pin. SDA/SMBDAT is a bidirectional pin used to transfer data to and from the device. The pin is an open-drain output and may be wired with other open-drain/collector outputs. The input buffer is always active (not gated). The open-drain output requires a pull-up resistor for proper functionality. The pull-up resistor should be connected to I2CVCC of the device.

SMBCLK

SCL/SMBCLK is the serial clock input pin. The SCL/SMBCLK input is responsible for clocking in all data to and from the device. The input buffer on the pin is always active (not gated). The input pin requires a pull-up resistor to I2CVCC of the device.

SMBALERT PINS (SMBALERT1, SMBALERT2)

The SMBALERT pins are output pins. The SMBALERT1 is an open-drain output and requires a pull-up resistor to a power supply up to 24V. The SMBALERT2 has a push/pull output stage. The SMBALERT pins are fault acknowledgment pins. The pin can be connected to peripheral circuitry to halt operations when a fault event occurs.

ECLK (16 PIN WLCSP)

ECLK is the External clock pin. ECLK is an input pin. The pin provides a connection to the system clock. The system clock is connected to the ADC. The acquisitions rate of the ADC can be varied through the ECLK pin. The pin functionality is set through a control register bit.

TABLE 2. ISL28025 REGISTER DESCRIPTIONS

REGISTER ADDRESS (HEX)	REGISTER NAME	FUNCTION	POWER ON RESET VALUE (HEX)	NUMBER OF BYTES	ACCESS TYPE	PAGE
IC DEVICE DETAILS						
19	CAPABILITY	PMBus Supportability	B0	1	R	26
20	VOUT_MODE	Describes the ADC Read Back Format	40	1	R	26
99	PMBUS_REV	PMBus Revision	22	1	R	26
AD	IC_DEVICE_ID	Device ID	0849534C3238303235	8	R	26
AE	IC_DEVICE_REV	Device Revision and Silicon Version	000002	3	R	26
GLOBAL IC CONTROLS						
12	RESTORE_DEFAULT_ALL	Soft Reset	N/A	0	W	27
01	OPERATION	Turns the Device On and Off	80	1	R/W	27
PRIMARY AND AUXILIARY CHANNEL CONTROLS						
D2	SET_DPM_MODE	Configures the ISL28025	0A	1	R/W	27
D3	DPM_CONV_STATUS	Indicates the Status of a Conversion	N/A	1	R	28
D4	CONFIG_ICHANNEL	Shunt Inputs (Primary and Auxiliary) Configuration	0387	2	R/W	28

TABLE 2. ISL28025 REGISTER DESCRIPTIONS (Continued)

REGISTER ADDRESS (HEX)	REGISTER NAME	FUNCTION	POWER ON RESET VALUE (HEX)	NUMBER OF BYTES	ACCESS TYPE	PAGE
38	IOUT_CAL_GAIN	Calibration that Enables Primary Current Measurements	0000	2	R/W	29
D5	CONFIG_VCHANNEL	Bus Inputs (Primary and Auxiliary) Configuration	0387	2	R/W	29
D7	CONFIG_PEAK_DET	Enables Primary Channel Current Peak Detector	00	1	R/W	29
MEASUREMENT REGISTERS						
D6	READ_VSHUNT_OUT	Primary Shunt Measurement Value	0000	2	R	30
8B	READ_VOUT	Primary Bus Measurement Value	0000	2	R	30
8C	READ_IOUT	Primary Current Measurement Value	0000	2	R	30
D8	READ_PEAK_MIN_IOUT	Primary Current Minimum Measurement Value	7FFF	2	R	30
D9	READ_PEAK_MAX_IOUT	Primary Current Maximum Measurement Value	8001	2	R	30
96	READ_POUT	Primary Power Measurement Value	0000	2	R	30
E1	READ_VOUT_AUX	Auxiliary Bus Measurement Value	0000	2	R	30
8D	READ_TEMPERATURE_1	Internal Temperature Measurement Value	0000	2	R	30
THRESHOLD DETECTORS						
DA	VOUT_OV_THRESHOLD_SET	Overvoltage/Over-Temperature Threshold Configuration	003F	2	R/W	31
DB	VOUT_UV_THRESHOLD_SET	Undervoltage Threshold Configuration	00	1	R/W	31
DC	IOUT_OC_THRESHOLD_SET	Overcurrent Threshold Configuration	003F	2	R/W	32
SMB ALERT						
DD	CONFIG_INTR	Configure the Behavior of the Interrupts	0000	2	R/W	34
DE	FORCE_FEEDTHR_ALERT	Configure the Path of the Interrupt Signal	00	1	R/W	35
1B	SMBALERT_MASK	Alert Mask for the SMBALERT1 Pin	N/A	2	R/W	37
DF	SMBALERT2_MASK	Alert Mask for the SMBALERT2 Pin	N/A	1	R/W	37
03	CLEAR_FAULTS	Clears All Faults	N/A	0	W	35
7A	STATUS_VOUT	Alert Bits Related to the Primary Bus	00	1	R/W	35
7B	STATUS_IOUT	Alert Bit Related to the Primary Shunt	00	1	R/W	35
7D	STATUS_TEMPERATURE	Alert Bit Related to Temperature	00	1	R/W	35
7E	STATUS_CML	Alert Bits Related to Communication Errors	00	1	R/W	36
78	STATUS_BYTE	Alert Bits Related to Temperature and Device Status	00	1	R/W	36
79	STATUS_WORD	Alert Bits Related to all Primary Inputs	0000	2	R/W	36
VOLTAGE MARGIN – DAC OUT (20 Pin QFN)						
E4	CONFIG VOL MARGIN	Configures the Margin DAC	00	1	R/W	37
E3	SET VOL MARGIN	Value to Load the Margin DAC	80	1	R/W	37
EXTERNAL CLOCK CONTROL (16 Pin WLCSP)						
E5	CONFIG_EXT_CLK	Configures External Clock; Enable/Disable SMBALERT2	00	1	R/W	37

Communication Protocol

The DPM chip communicates with the host using PMBus commands. PMBus command structure is an industry SMBus standard for communicating with power supplies and converters. All communications to and from the chip use the SMBCLK and SMBDAT to communicate to the DPM master. The SMB pins require a pull-up resistor to enable proper operation. The default logic state of the communication pins are high when the bus is in an idle state.

The SMBus standard is a variant of the I^2C communication standard with minor differences with timing and DC parameters. SMBus supports Packet Error Corrections (PEC) for data integrity certainty. The PMBus is the standardization of the SMBus register designation. The standardization is specific to power and converter devices.

The DPM employs the following command structures from the I^2C communication standard.

1. Send Byte
2. Write Byte/Word
3. Read Byte/Word
4. Read Block
5. Write Block

Packet Error Correction (PEC)

PEC is often used in environments where data being transferred to and from the device can be compromised. Applications where the device is connected by way of a cable is common use of PEC. The cable's integrity may be compromised resulting in error transactions between the master and the device. The ISL28025 uses an 8-bit cyclic redundancy check (CRC-8). Figure 63 shows an example of a flow algorithm for CRC-8 protocol.

```
Public Function crc8Decode(binStr As String) As Byte

Dim crc8(0 To 7) As Byte, index As Byte, doInvert As Byte
The input to the subroutine is a binary string consisting of
the slave address, the register address and data inputted to or received from the part.
Anything inputted into or received from the device is part of the binary string (binStr)
to be calculated by this routine.
Clear the crc8 variable. This variable is used to return the PEC value.
For index = 0 To UBound(crc8)
   crc8(index) = 0
Next index
index = 0
While index <> (Len(binStr))
  index = index + 1
The If statement below reads the binary value of each bit in the binary string (binStr).
  If Mid(binStr, index, 1) = "1" Then
    doInvert = 1 Xor crc8(7)
  Else
    doInvert = 0 Xor crc8(7)
  End If

  crc8(7) = crc8(6)
  crc8(6) = crc8(5)
  crc8(5) = crc8(4)
  crc8(4) = crc8(3)
  crc8(3) = crc8(2)
  crc8(2) = crc8(1) Xor doInvert
  crc8(1) = crc8(0) Xor doInvert
  crc8(0) = doInvert
Wend
crc8Decode = 0
For index = 0 To 7 'This assembles the crc8 value in byte form.
   crc8Decode = crc8(index) * 2 ^ index + crc8Decode
Next index 'crc8Decode is returned from this routine.
End Function
```

FIGURE 63. ALGORITHM TO CALCULATE A CRC8 (PEC) BYTE VALUE

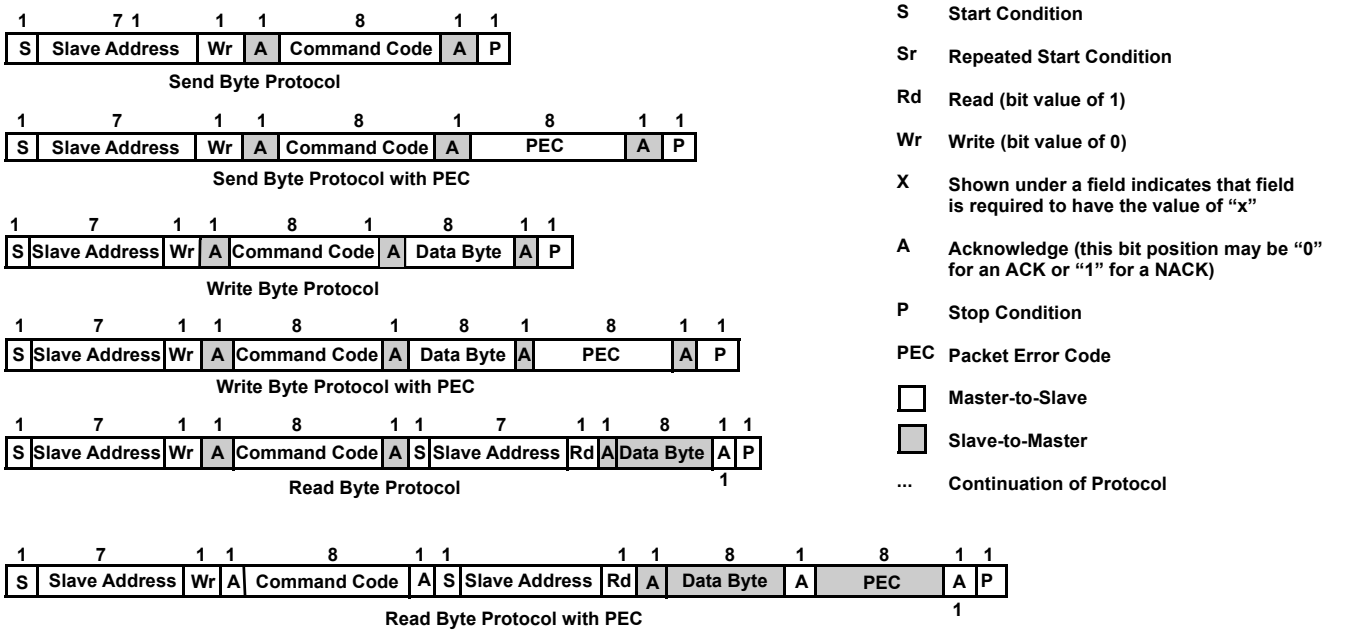


FIGURE 64. READ/WRITE SMBus PROTOCOLS WITH AND WITHOUT PEC

NOTE: Diagrams copied from a SMBus specification document. The document can be found at http://smbus.org/specs/

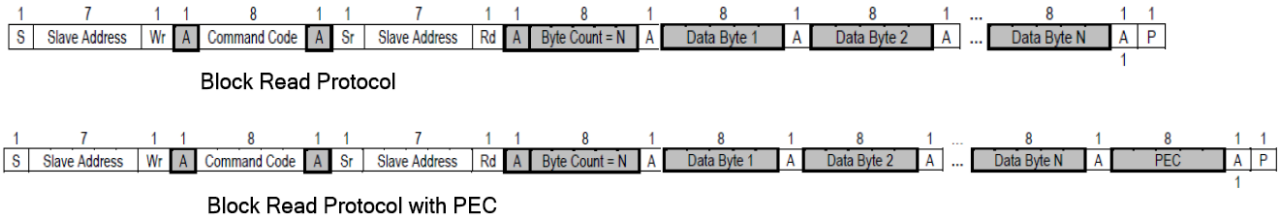


FIGURE 65. BLOCK READ SMBUS PROTOCOLS WITH AND WITHOUT PEC.

NOTE: Diagrams copied from SMBus specification document. The document can be found at http://smbus.org/specs/

IC Device Details

0X19 CAPABILITY (R)

The capability register is a read only byte register that describes the supporting communication standard by the DPM chip.

TABLE 3. 0x19 CAPABILITY REGISTER DEFINITION

BIT NUMBER	D7	D[6:5]	D4	D[3:0]
Bit Name	PEC	Max Bus Speed	SMB Alert Support	N/A
Default Value	1	01	1	0000

The DPM chip supports Packet Error Correction (PEC) protocol. The maximum PMBus bus speed that the DPM supports is 400kHz. The DPM supports a higher speed option that is not compliant to the PMBus standard. The higher speed option is discussed later in the datasheet. The DPM chip has SMB alert pins, which supports SMB alert commands.

0X20 V_{OUT} MODE (R)

The V_{OUT} Mode register is a readable byte register that describes the method to calculate read back values from the DPM such as voltage, current, power and temperature. The value for the register is 0x40. The register value represents a direct data read back format. For unsigned registers such as V_{BUS}, the register value is calculated using Equation 1.

$$\text{Register}_{\text{Value}} = \left[\sum_{n=0}^{15} \left(\text{Bit\_Val}_n \cdot 2^n \right) \right] \quad \text{(EQ. 1)}$$

Otherwise, Equation 2 is used for signed readings.

$$\text{Register}_{\text{Value}} = \left[\sum_{n=0}^{14} \left(\text{Bit\_Val}_n \cdot 2^n \right) \right] - \left(\text{Bit\_Val}_{15} \cdot 2^{15} \right) \quad \text{(EQ. 2)}$$

where n is the bit position within the register value. Bit_Val is the value of the bit either 1 or 0.

0X99 PMBUS REV (R)

The PMBUS Rev register is a readable byte register that describes the PMBUS revision that the DPM is compliant to.

TABLE 4. 0x99 PMBUS REV REGISTER DEFINITION

BIT NUMBER	D[7:4]	D[3:0]
Bit Name	PMBUS Rev Part I	PMBUS Rev Part II
Default Value	0010	0010

PMBUS Rev part 1 is a PMBus specification pertaining to electrical transactions and hardware interface. PMBUS Rev part 2 specification pertains to the command calls used to address the DPM.

A nibble of 0000 translates to revision 1.0 of either PMBUS revision. A nibble of 0001 equals 1.1 of either PMBus revision.

0XAD IC DEVICE ID (BR)

The IC Device ID is a block readable register that reports the device product name being addressed. The product ID that is stored in the register is “ISL28025”. Each character is stored as an ASCII number. A 0x30 equals ASCII “0”. A 0x49 translates to an ASCII “I”. Figure 65 illustrates the convention for performing a block read.

0XAE IC_DEVICE_REV (BR)

The IC Device Revision is a block readable register that reports back the revision number of the silicon and the version of the silicon. The register is three bytes in length.

TABLE 5. 0xAE IC DEVICE REV REGISTER DEFINITION

BIT NUMBER	D[23:12]	D[11]	D[10:0]
Bit Name	N/A	Silicon Version	Silicon Revision
Default Value	0000 0011 0000	0	0000 0000 0010

SILICON VERSION D[11]

Data Bit 11 of the IC Revision register reports the version of the silicon.

TABLE 6. D[11] SILICON VERSION BIT DEFINED

D11	STATUS
0	60V
1	12V

Global IC Controls

0X12 RESET DEFAULT ALL (S)

The Restore Default All register is a send byte command that restores all registers to the default state defined in Table 2 on page 23.

0X01 OPERATION (R/W)

The Operation register is a read/write byte register that controls the overall power-up state of the chip. Data Bit 7 of the register configures the power status of chip. The power status is defined in Table 7. Yellow shading in the table is the default setting of the bit at power-up.

TABLE 7. 0x01 OPERATION REGISTER BIT 7 DEFINED

D7	STATUS
0	Power-Down
1	Normal Operation

Primary and Auxiliary Channel Controls

0XD2 SET DPM MODE (R/W)

The Set DPM Mode is a read/write byte register that controls the data acquisition behavior of the chip.

TABLE 8. 0xD2 SET DPM MODE REGISTER DEFINITION

BIT NUMBER	D[7]	D6	D[5]	D[4]	D[3]	D[2:0]
Bit Name	N/A	ADC Enable	ADC State	Post Trigger State	ADC Mode Type	Operating Mode
Default Value	0	0	0	0	1	010

ADC ENABLE D[6]

Data Bit 6 of the Set DPM Mode register controls the ADC power state within the DPM chip. At power-up, the ADC is powered up and is available to take data.

TABLE 9. 0xD2 SET DPM MODE REGISTER BIT 6 DEFINED

D6	ADC PD
0	Normal Mode
1	ADC Powered Down

ADC STATE D[5]

Data Bit 5 of the Set DPM Mode register controls the ADC state. The idle state of the ADC does not acquire data from any input of the DPM. Normal operating mode has the ADC acquiring data in a systematic way.

TABLE 10. 0xD2 SET DPM MODE REGISTER BIT 5 DEFINED

D5	ADC STATE
0	Normal State
1	ADC in Idle State

POST TRIGGER STATE D[4]

Data Bit 4 of the Set DPM Mode register controls the post ADC state once an acquisition has been made in the trigger mode.

TABLE 11. 0xD2 SET DPM MODE REGISTER BIT 4 DEFINED

D4	ADC TRIGGER STATE
0	Idle Mode after a Trigger Measurement
1	PD Mode after a Trigger Measurement

ADC MODE TYPE D[3]

Data Bit 3 of the Set DPM Mode register controls the behavior of the ADC to either triggered or continuous. The continuous mode has the ADC continuously acquiring data in a systematic manner described by data bits [2:0] in the SET DPM MODE register. The triggered mode instructs the ADC to make an acquisition described by data bits [2:0]. The beginning of a triggered cycle starts once writing to the Set DPM Mode register commences. The trigger mode is useful for reading a single measurement per acquisition cycle.

TABLE 12. 0xD2 SET DPM MODE REGISTER BIT 3 DEFINED

D3	ADC MODE TYPE
0	Trigger
1	Continuous

OPERATING MODE D[2:0]

The Operating Mode bits of the Set DPM Mode register control the state machine within the chip. The state machine globally controls the overall functionality of the chip. Table 13 shows the various measurement states the chip can be configured to, as well as the mode bit definitions to achieve a desired measurement state. The shaded row is the default setting upon power-up.

TABLE 13. 0xD2 SET DPM MODE REGISTER BITS 2 TO 0 DEFINED

D[2:0]	MEASUREMENT INPUT
0	Primary Channel Shunt Voltage
1	Primary Channel V_{BUS} Voltage
2	Primary Shunt and V_{BUS} Voltages
3	Do Not Select
4	Auxiliary Channel V_{BUS} Voltage
5	Do Not Select
6	Internal Temperature
7	All

0XD3 DPM CONVERSION STATUS (R)

The DPM conversion status register is a readable byte register that reports the status of a conversion when the DPM is programmed in the trigger mode.

TABLE 14. 0xD3 DPM CONVERSION STATUS REGISTER DEFINITION

BIT NUMBER	D[7:2]	D[1]	D[0]
Bit Name	N/A	CNVR	OVF
Default Value	0	0	0

CNVR: CONVERSION READY D[1]

The Conversion Ready bit indicates when the ADC has finished a conversion and has transferred the reading(s) to the appropriate register(s). The CNVR is operable only when the ADC state is set to trigger. The CNVR is in a low state when the conversion is in progress. When the CNVR bit transitions from a low state to a high state and remains at a high state, the conversion is complete. The CNVR initializes or reinitializes when writing to the Set DPM Mode register.

OVF: MATH OVERFLOW FLAG D[0]

The Math Overflow Flag (OVF) bit is set to indicate the current and power data being read from the DPM is overranged and meaningless.

0XD4 CONFIGURE $I_{CHANNEL}$ (R/W)

The Configure $I_{CHANNEL}$ register is a read/write word register that configures the ADC measurement acquisition settings for the primary and auxiliary voltage shunt inputs.

TABLE 15. 0xD4 CONFIGURE $I_{CHANNEL}$ REGISTER DEFINITION

BIT NUMBER	D[15:7]	D[13:10]	D[9:7]	D[6:3]	D[2:0]
Bit Name	N/A	N/A	N/A	Primary Shunt Sample AVG	Primary Shunt Conversion Time
Default Value	00	00 00	11 1	000 0	111

SHUNT VOLTAGE CONVERSION TIME D[2:0]

The Shunt Voltage Conversion Time bits set the acquisition speed of the ADC when measuring the primary voltage shunt channel of the DPM. The primary voltage shunt channel has independent timing control bits allowing for the primary voltage shunt channel to have a unique acquisition time with the respect to other channels within the DPM. Table 16 is a list of the selectable voltage shunt ADC time settings. The shaded row indicates the default setting.

TABLE 16. PRIMARY V_{SHUNT} CONVERSION TIMES DEFINED

Config_Ichannel: D[2:0]			CONVERSION TIME
0	0	0	64µs
0	0	1	128µs
0	1	0	256µs
0	1	1	512µs
1	0	X	1.024ms
1	1	X	2.048ms

SHUNT VOLTAGE SAMPLE AVERAGE D[6:3]

The Shunt Voltage Sample Average bits set the number of averaging samples for a unique sampling time. The DPM records all samples and outputs the average resultant to the voltage shunt register. Table 17 defines the list of selectable averages the DPM can be set to. The shaded row indicates the default setting.

TABLE 17. PRIMARY V_{SHUNT} NUMBER OF SAMPLES TO AVERAGE DEFINED

AVG[3:0]				CONVERTER AVERAGES
0	0	0	0	1
0	0	0	1	2
0	0	1	0	4
0	0	1	1	8
0	1	0	0	16
0	1	0	1	32
0	1	1	0	64
0	1	1	1	128
1	0	0	0	256
1	0	0	1	512
1	0	1	0	1024
1	0	1	1	2048
1	1	X	X	4096

0X38 IOUT CALIBRATION GAIN (R/W)

The IOUT Calibration Gain register is a read/write word register that is used to calculate current and power measurements for the primary channel of the DPM. When the register is programmed, the DPM calculates the current and power based on the primary channels V_{BUS} and V_{SHUNT} measurements. The calculation resultant is stored in the READ_IOUT and READ_POUT registers.

The calibration register value can be calculated as follows:

1. Calculate the full-scale current range that is desired. This can be calculated using Equation 3.

$$\text{Current}_{FS} = \frac{\text{Vshunt}_{FS}}{R_{shunt}} \quad \text{(EQ. 3)}$$

R_{shunt} is the value of the shunt resistor. Vshunt_{FS} is the full scale range of the primary channel, which equals 80mV.

2. From the current full-scale range, the current LSB can be calculated using Equation 4. Current full-scale is the outcome from Equation 3.

$$\text{Current}_{LSB} = \frac{\text{Current}_{FS}}{\text{ADC}_{res}} \quad \text{(EQ. 4)}$$

ADC_{res} is the resolution of shunt voltage reading. The output of the ADC is a signed 15 bit binary number. Therefore, the ADC_{res} value equals 2^{15} or 32768.

From Equation 4, the calibration resistor value can be calculated using Equation 5. The resolution of the math that is processed internally in the DPM is 2048 or 11 bits of resolution. The V_{SHUNT} LSB is set to 2.5µV. Equation 5 yields a 15-bit binary number that can be written to the calibration register. The calibration register format is represented in Table 18.

$$\text{CalReg}_{val} = \text{integer}\left[\frac{\text{Math}_{res}\cdot\text{Vshunt}_{LSB}}{(\text{Current}_{LSB}\cdot R_{shunt})}\right]$$

$$\text{CalReg}_{val} = \text{integer}\left[\frac{0.00512}{(\text{Current}_{LSB}\cdot R_{shunt})}\right] \quad \text{(EQ. 5)}$$

TABLE 18. 0x38 IOUT_CAL_GAIN DEFINITION

BIT NUMBER	D[15]	D[14:0]
Bit Name	N/A	IOUT_CAL_GAIN
Default Value	0	000 0000 0000 0000

0XD5 CONFIGURE $V_{CHANNEL}$ (R/W)

The Configure $V_{CHANNEL}$ register is a read/write word register that configures the ADC measurement acquisition settings for the primary and auxiliary voltage bus inputs.

TABLE 19. 0xD5 CONFIGURE $V_{CHANNEL}$ REGISTER DEFINITION

BIT NUMBER	D[15:14]	D[13:10]	D[9:7]	D[6:3]	D[2:0]
Bit Name	N/A	AuxV Sample AVG	AuxV Conversion Time	V_{BUS} Sample AVG	V_{BUS} Conversion Time
Default Value	00	00 00	11 1	000 0	111

The ADC configuration of the sampling average and conversion time settings for V_{BUS} and AuxV channels have the same setting choices as the V_{SHUNT} primary and auxiliary channels.

0XD7 CONFIGURE PEAK DETECTOR (R/W)

The Configure Peak Detector register is a read/write byte register that toggles the minimum and maximum current tracking feature. A Peak Detect Enable bit setting of 1 enables the current peak detect feature of the DPM. The feature is discussed in more detail in the "0xD8 Read Peak Min I_{OUT} (R) 0xD9 Read Peak Max I_{out} (R)" section.

TABLE 20. 0xD7 CONFIGURE PEAK DETECTOR REGISTER DEFINITION

BIT NUMBER	D[7:1]	D[0]
Bit Name	N/A	Peak Detect Enable
Default Value	0000 000	0

Measurement Registers

0XD6 READ V_{SHUNT} OUT (R)

The Read V_{SHUNT} Out register is a readable word register that stores the signed measured digital value of the primary V_{SHUNT} input of the DPM. Using Equation 2 to calculate the integer value of the register, Equation 6 calculates the floating point measured value for the primary V_{SHUNT} channel.

$$V_{SHUNT} = Register_{value} \cdot V_{SHUNT(LSB)} \quad \text{(EQ. 6)}$$

$V_{SHUNT(LSB)}$ is the numerical weight of each level for the V_{SHUNT} channel, which equals 2.5µV.

0X8B READ V_{OUT} (R)

The Read V_{OUT} register is a readable word register that stores the unsigned measured digital value of the primary V_{BUS} input of the DPM. Using Equation 1 to calculate the integer value of the register, Equation 7 calculates the floating point measured value for the primary V_{BUS} channel.

$$V_{BUS} = Register_{value} \cdot V_{BUS(LSB)} \quad \text{(EQ. 7)}$$

$V_{BUS(LSB)}$ is the numerical weight of each level for the V_{BUS} channel. The $V_{BUS(LSB)}$ equals 1mV for the 60V version of the DPM and 250µV for the 12V version of the DPM.

0X8C READ I_{OUT} (R)

The Read I_{OUT} register is a readable word register that stores the signed measured digital value of the current passing through the primary channel's shunt. The register uses the measured value from V_{SHUNT} and the IOUT_CAL_GAIN register. Equation 8 yields the current for the primary channel.

$$Current = Register_{value} \cdot Current_{LSB} \quad \text{(EQ. 8)}$$

The $Register_{value}$ is calculated using Equation 2. The $Current_{LSB}$ is calculated using Equation 4.

0XD8 READ PEAK MIN I_{OUT} (R)
0XD9 READ PEAK MAX I_{OUT} (R)

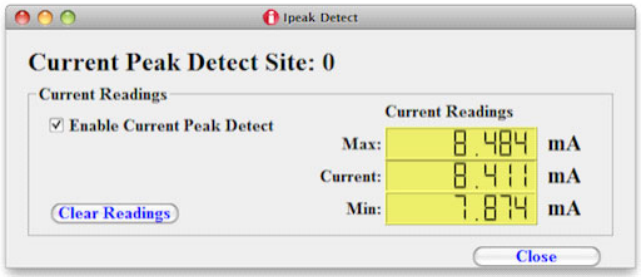


FIGURE 66. THE ISL28025 TRACKS MINIMUM AND MAXIMUM AVERAGE CURRENT READINGS

The Read Peak Min/Max I_{OUT} registers are readable word registers that store the minimum and maximum current value of an averaging cycle for the current passing through the primary shunt.

The min/max current tracking is enabled by setting the Peak Detect Enable bit in the CONFIG_PEAK_DET (0xD7) register. The current peak detect feature only works for the current register.

At the conclusion of each primary channel current, the DPM will record and store the minimum and maximum values of the current measured. The feature operates for both the trigger and continuous modes. Disabling the Peak Detector Enable bit will turn off the feature as well as clear the Read Peak Min/Max I_{OUT} registers.

0X96 READ P_{OUT} (R)

The Read P_{OUT} register is a signed readable word register that reports the digital value of the power from the primary channel. The register uses the values from READ_IOUT and READ_VSHUNT_OUT registers to calculate the power.

The units for the power register are in watts. The power can be calculated using Equation 9.

$$Power = Register_{value} \cdot Power_{LSB} \cdot 40000 \quad \text{(EQ. 9)}$$

The $Register_{value}$ is calculated using Equation 2 on page 26. The $Power_{LSB}$ can be calculated from Equation 10.

$$Power_{LSB} = Current_{LSB} \cdot V_{BUS(LSB)} \quad \text{(EQ. 10)}$$

The $V_{BUS(LSB)}$ equals 1mV for the 60V version of the DPM and 250µV for the 12V version of the DPM. The $Current_{LSB}$ is the value yielded from Equation 4.

0XE1 READ VOUT AUX (R)

The Read V_{OUT} Aux register is a readable word register that stores the unsigned measured digital value of the auxiliary V_{BUS} input of the DPM. Using Equation 1 on page 26 to calculate the integer value of the register, Equation 11 calculates the floating point measured value for the auxiliary V_{BUS} channel.

$$V_{BUS} = Register_{value} \cdot V_{BUS(LSB)} \quad \text{(EQ. 11)}$$

$V_{BUS(LSB)}$ is the numerical weight of each level for the auxiliary V_{BUS} channel. The auxiliary $V_{BUS(LSB)}$ equals 100µV. The voltage range for the auxiliary V_{BUS} is 0 to VCC.

0X8D READ TEMPERATURE (R)

The Read Temperature register is a readable word register that reports out the internal temperature of the chip. The register is a 16-bit signed register. Bit 15 of the register is the signed bit. The register value can be calculated using Equation 12.

$$Register\ Value = \left[\sum_{n=0}^{14}\left(Bit\_Val_n \cdot 2^n\right)\right] - \left(Bit\_Val_{15} \cdot 2^{15}\right) \quad \text{(EQ. 12)}$$

n is the bit position within the register value. Bit_Val is the value of the bit either 1 or 0. The register value multiplied by 0.016 yields the internal temperature reading in degrees Celsius (°C).

Threshold Detectors

The DPM has three integrated comparators that allow for real time fault detection of overvoltage, undervoltage for the primary V_{BUS} input, and overcurrent detection for the primary V_{SHUNT} input. An over-temperature detection is available by multiplexing the input to the overvoltage comparator.

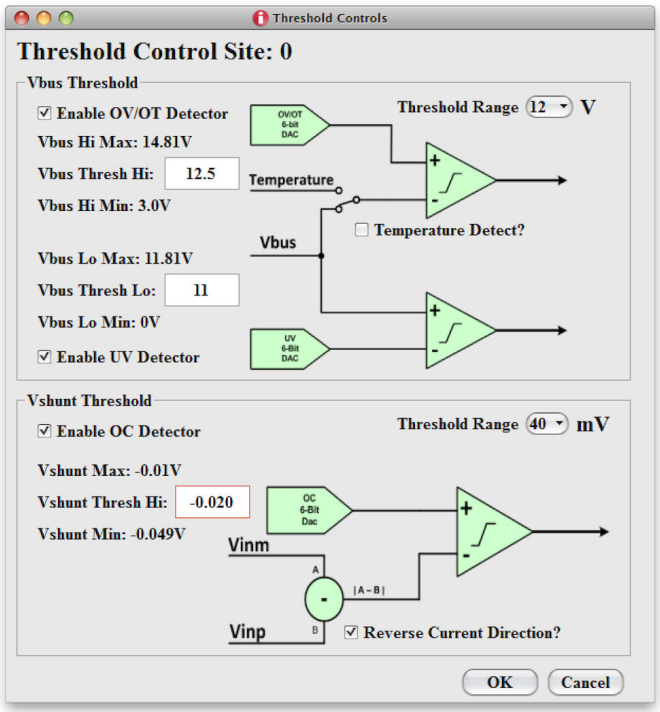


FIGURE 67. SIMPLIFIED BLOCK DIAGRAM OF THE THRESHOLD FUNCTIONS WITHIN THE DPM

0XDA V_{OUT} OV THRESHOLD SET (R/W)

The V_{OUT} OV Threshold Set register is a read/write word register that controls the threshold voltage level to the overvoltage comparator. The description of the functionality within this register is found in Table 21.

The compared reference voltage level to the OV comparator is generated from a 6-bit DAC. The 6-bit DAC has four or six voltage ranges to improve detection voltage resolution for a specific voltage range.

TABLE 21. 0xDA VOUT OV THRESHOLD SET REGISTER DEFINITION

BIT NUMBER	D[15:10]	D[9]	D[8:6]	D[5:0]
Bit Name	N/A	OV_OT SEL	Vbus_Thres_Rng	Vbus_OV_OT_Set
Default Value	0000 00	0	0 00	11 1111

OV_OT_SEL D[9]

The OV_OT_SEL bit configures the multiplexer to the input of the OV comparator to compare for over-temperature or overvoltage. Setting the OV_OT_SEL to a 1 configures the OV comparator to detect an over-temperature condition.

VBUS_THRES_RNG D[8:6]

The Vbus_Thres_Rng bits set the threshold voltage range for the overvoltage and undervoltage DACs. There are six selectable ranges for the 60V version of the DPM. Only four selectable ranges for the 12V version of the DPM. Table 22 defines the range settings for the V_{BUS} threshold detector. The yellow shaded row denotes the default setting.

The temperature threshold reference level has one range setting, which equals +125°C at full scale.

TABLE 22. Vbus_Thres_Rng BITS DEFINED

Vbus_Thres_Rng: D[8:6]			Vbus_12V (RANGE)	Vbus_60V (RANGE)
0	0	0	12	48
0	0	1	6	24
0	1	0	3	12
0	1	1	1.25	5
1	0	0	X	3.3
1	0	1	X	2.5

VBUS_OV_OT_SET D[5:0]

The Vbus_OV_OT_Set bits control the voltage/temperature level to the input of the OV comparator. The LSB of the DAC is 1.56% of the full-scale range chosen using the Vbus_Thres_Rng bits. For the temperature feature, the LSB for the temperature level is 5.71°C. The mathematical range is -144°C to +221.4°C.

The overvoltage range starts at 25% of the full-scale range chosen using the Vbus_Thres_Rng bits and ends at 125% of the chosen full-scale range. The same range applies to the temperature measurements.

TABLE 23. Vbus_OV_OT_Set BITS DEFINED

Vbus_OV_OT_Set: D[5:0]	OV THRESHOLD VALUE	OT THRESHOLD VALUE
00 0000	25% of FS	-144
00 0001	(25 + 1.56)% of FS	-138.3
00 0010	(25 + 3.12)% of FS	-132.6
.....	.....	.....
11 1101	(125 to 4.68)% of FS	210
11 1110	(125 to 3.12)% of FS	215.7
11 1111	(125 to 1.56)% of FS	221.4

Table 23 defines an abbreviated breakdown to set the OV/OT comparator level. The shaded row is the default condition.

0XDB V_{OUT} UV THRESHOLD SET (R/W)

The V_{OUT} UV Threshold Set register is a read/write byte register that controls the threshold voltage level to the undervoltage comparator. The description of the functionality within this register is found in Table 24.

The compared reference voltage level to the UV comparator is generated from a 6-bit DAC. The 6-bit DAC has 4 to 6 voltage

ranges that are determined by the Vbus_Thres_Rng bits in the V_{OUT} OV Threshold Set register.

TABLE 24. 0xDB VOUT UV THRESHOLD SET REGISTER DEFINITION

BIT NUMBER	D[7:6]	D[5:0]
Bit Name	N/A	Vbus_UV_Set
Default Value	00	00 0000

VBUS_UV_SET D[4:0]

The Vbus_UV_Set bits control the undervoltage level to the input of the UV comparator. The LSB of the DAC is 1.56% of the full-scale range chosen using the Vbus_Thres_Rng bits.

The undervoltage ranges from 0% to 100% of the full-scale range set by the Vbus_Thres_Rng bits.

TABLE 25. Vbus_UV_Set BITS DEFINED

Vbus_UV_Set: D[5:0]	UV THRESHOLD VALUE
00 0000	0%
00 0001	1.56% of FS
00 0010	3.12% of FS
.....	.....
11 1101	(100 to 4.68)% of FS
11 1110	(100 to 3.12)% of FS
11 1111	(100 to 1.56)% of FS

Table 25 defines an abbreviated breakdown to set the undervoltage comparator levels. The shaded row is the default condition.

0XDC I_{OUT} OC THRESHOLD SET (R/W)

The I_{OUT} OC Threshold Set register is a read/write word register that controls the threshold current level to the overcurrent comparator. The description of the functionality within this register is found in Table 26.

TABLE 26. 0xDC I_{OUT} OC THRESHOLD SET REGISTER DEFINITION

BIT NUMBER	D[15:10]	D[9]	D[8:7]	D[6]	D[5:0]
Bit Name	N/A	Iout_Dir	N/A	Vshunt Thres Rng	Vshunt_OC_Set
Default Value	0000 00	0	0 0	0	11 1111

The overcurrent threshold is defined through the V_{SHUNT} reading. The product of the current through the shunt resistor defines the V_{SHUNT} voltage to the DPM. The current through the shunt resistor is directly proportional the V_{SHUNT} voltage measured by the DPM. An overvoltage threshold for V_{SHUNT} is the same as an overcurrent threshold.

IOUT_ DIR D[9]

The Iout_Dir bit controls the polarity of the V_{SHUNT} voltage threshold. The bit functionality allows an overcurrent threshold to be set for currents flowing from VINP to VINM and the reverse direction. Table 27 defines the range settings for the V_{BUS} threshold detector. The yellow shaded row denotes the default setting.

TABLE 27. Vbus_Thres_Rng BITS DEFINED

Iout_Dir: D[9]	CURRENT DIRECTION
0	VINP to VINM
1	VINM to VINP

VSHUNT_THRES_RNG D[6]

The Vshunt_Thres_Rng bit sets the overvoltage threshold range for the overcurrent DAC. The selectable V_{SHUNT} range improves the overvoltage threshold resolution for lower full-scale current applications. Table 28 defines the range settings for the V_{BUS} threshold detector. The yellow shaded row denotes the default setting.

TABLE 28. Vshunt_Thres_Rng BIT DEFINED

Vshunt_Thres_Rng: D[6]	V_{SHUNT} (RANGE)
0	80mV
1	40mV

VSHUNT_OC_SET D[5:0]

The Vshunt_OC_Set bits control the V_{SHUNT} voltage level to the input of the OC comparator. The LSB of the DAC is 1.56% of the full-scale range chosen using the Vshunt_Thres_Rng bits.

The overvoltage range starts at 25% of the full-scale range chosen using Vbus_Thres_Rng bits and ends at 125% of the chosen full-scale range.

TABLE 29. Vshunt_OC_Set BITS DEFINED

Vshunt_OC_Set: D[5:0]	OC THRESHOLD VALUE
00 0000	25% of FS
00 0001	(25 + 1.56)% of FS
00 0010	(25 + 3.12)% of FS
.....	.....
11 1101	(125 to 4.68)% of FS
11 1110	(125 to 3.12)% of FS
11 1111	(125 to 1.56)% of FS

SMB Alert

The DPM has two alert pins (SMBALERT1, SMBALERT2) to alert the peripheral circuitry that a failed event has occurred. SMBALERT1 output is an open drain allowing the user the flexibility to connect the alert pin to other components requiring different logic voltage levels than the DPM. The SMBALERT2 has a push/pull output stage for driving pins with logic voltage levels

equal to the voltage applied to the I2CVCC pin. The push/pull output is useful for driving peripheral components that require the DPM to source and sink a current. The alert pins are commonly connected to an interrupt pin of a microcontroller or an enable pin of a device.

The SMBALERT registers control the functionality of the SMBALERT pins. The threshold comparators are the inputs to the SMBALERT registers. The output are the SMBALERT pins. Figure 68 is a simple functional block diagram of the SMB Alert features.

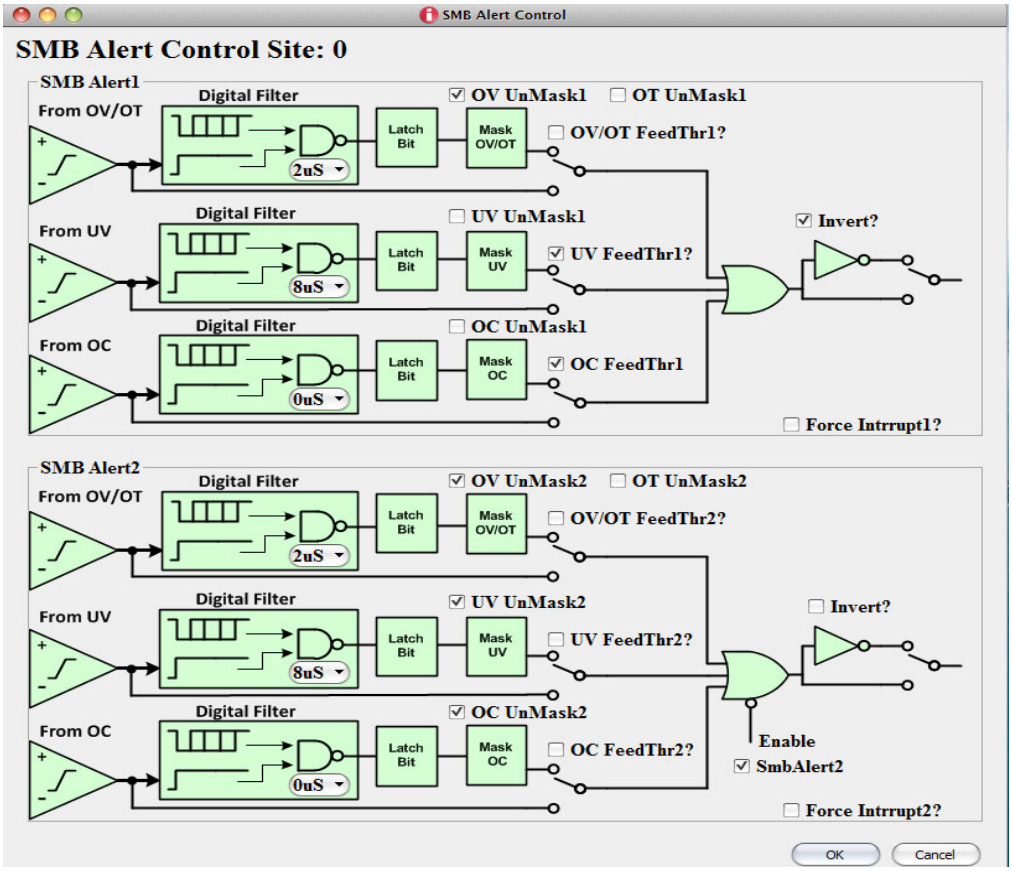


FIGURE 68. SIMPLIFIED BLOCK DIAGRAM OF THE SMBALERT FUNCTIONS WITHIN THE DPM

0XDD CONFIGURE INTERRUPTS (R/W)

The Configure Interrupt register is a read/write word register that controls the behavior of the two SMBALERT pins. The definition of the control bits within the Configure Interrupt register is defined in Table 30.

TABLE 30. 0xDD CONFIGURE INTERRUPT REGISTER DEFINITION

BIT NUMBER	D [15]	D [14:12]	D [11:9]	D [8:7]	D [6:5]	D [4:3]	D [2]	D [1]	D [0]
Bit Name	N/A	ALERT2 FeedTh	ALERT1 FeedTh	OC FIL	OV FIL	UV FIL	OC EN	OV EN	UV EN
Default Value	0	000	000	0 0	00	0 0	0	0	0

ALERT2_FEEDTHR D[14:12]

The Alert2_FeedThr bits determine whether the bit from each alert comparator is digitally conditioned or not. The alert comparators, digital filters and latching bits are the same for both SMBALERT channels. Table 31 defines the functionality of the Alert2_FeedThr bits.

TABLE 31. Alert2_FeedThr BITS DEFINED

Alert2_FeedThr Bits D[14:12]		BIT VALUE	FUNCTIONALITY
D[14]	0	0	OV/OT Digitally Conditioned
		1	OV/OT Pass Through
D[13]	1	0	UV Digitally Conditioned
		1	UV Pass Through
D[13]	2	0	OC Digitally Conditioned
		1	OC Pass Through

ALERT1_FEEDTHR D[11:9]

The Alert1_FeedThr bits determine whether the bit from each alert comparator is digitally conditioned or not. The alert comparators, digital filters and latching bits are the same for both SMB alert channels. Table 32 defines the functionality of the Alert1_FeedThr bits.

TABLE 32. Alert1_FeedThr BITS DEFINED

Alert1_FeedThr Bits D[11:9]		BIT VALUE	FUNCTIONALITY
D[11]	0	0	OV/OT Digitally Conditioned
		1	OV/OT Pass Through
D[10]	1	0	UV Digitally Conditioned
		1	UV Pass Through
D[9]	2	0	OC Digitally Conditioned
		1	OC Pass Through

OC_FIL D[8:7]

The OC_FIL bits control the digital filter for the overcurrent circuitry. The digital filter will prevent short duration events from passing to the output pins. The filter is useful in preventing high frequency power glitches from triggering a shutdown event. The filter time delay ranges from 0µs to 8µs. An 8µs filter setting requires an error event to be at least 8µs in duration before passing the result to the SMBALERT pins. There is one OC digital filter for both SMBALERT pins. Configuring OC_FIL bits will change the OC digital filter setting for both SMBALERT pins. See Table 33 for the filter selections.

UV_FIL D[6:5]

The UV_FIL bits control the digital filter for the undervoltage circuitry. The digital filter will prevent short duration events from passing to the output pins. The filter is useful in preventing high frequency power glitches from triggering a shutdown event. The filter time delay ranges from 0µs to 8µs. An 8µs filter setting requires an error event to be at least 8µs in duration before passing the result to the SMBALERT pins. There is one UV digital filter for both SMBALERT pins. Configuring UV_FIL bits will change the UV digital filter setting for both SMBALERT pins. See Table 33 for the filter selections.

OV_FIL D[4:3]:

The OV_FIL bits control the digital filter for the overvoltage circuitry. The digital filter will prevent short duration events from passing to the output pins. The filter is useful in preventing high frequency power glitches from triggering a shutdown event. The filter time delay ranges from 0µs to 8µs. An 8µs filter setting requires an error event to be at least 8µs in duration before passing the result to the SMBAlert pins. There is one OV digital filter for both SMB alert pins. Configuring OV_FIL bits will change the OV digital filter setting for both SMB alert pins. See Table 33 for the filter selections.

TABLE 33. DIGITAL GLITCH FILTER SETTINGS DEFINED

OC_FIL D[8:7] UV_FIL D[6:5] OV_FIL D[4:3]		FILTER TIME (µs)
0	0	0
0	1	2
1	0	4
1	1	8

OC_EN D[2]

The OC_EN enable bit controls the power to the overcurrent DAC and comparator. Setting the bit to 1 enables the overcurrent circuitry.

OV_EN D[1]

The OV_EN enable bit controls the power to the overvoltage DAC and comparator. Setting the bit to 1 enables the overvoltage circuitry.

UV_EN D[0]

The UV_EN enable bit controls the power to the undervoltage DAC and comparator. Setting the bit to 1 enables the undervoltage circuitry.

0XDE FORCE FEED-THROUGH ALERT REGISTER (R/W)

The Force Feed-through Alert Register is a read/write byte register that controls the polarity of the interrupt. The definition of the control bits within the Force Feed-through Alert register is defined in Table 34.

TABLE 34. 0xDE FORCE FEED-THROUGH ALERT REGISTER DEFINITION

BIT NUMBER	D[7:4]	D[3]	D[2]	D[1]	D[0]
Bit Name	N/A	A2POL	A1POL	FORCE A2	FORCE A1
Default Value	0000	0	0	0	0

A2POL D[3], A2POL D[2]

The AxPOL bits control the polarity of an interrupt. A2POL bit defines the SMBALERT2 pin active interrupt state. A1POL bit defines the SMBALERT1 pin active interrupt state. Table 35 defines the functionality of the bit.

TABLE 35. AxPol BIT DEFINED

A2POL D[3], A1POL D[2]	INTERRUPT ACTIVE STATE
0	low
1	high

FORCEA2 D[1], FORCEA1 D[0]

The FORCEAx bits allow the user to force an interrupt by setting the bit. FORCEA2 bit controls the SMBALERT2 pin state. FORCEA1 bit controls the SMBALERT1 pin state. Table 36 defines the functionality of the bit.

TABLE 36. FORCEAx BIT DEFINED

FORCEA2 D[1], FORCEA1 D[0]	INTERRUPT STATUS
0	Normal
1	Interrupt Forced

0X03 CLEAR FAULTS (S)

The Clear Faults register is a send byte command that clears all faults pertaining to the status registers. Upon execution of the command, the status registers returns to the default state defined in Table 2 on page 23.

0X7A STATUS V_{OUT} (R/W)

The Status V_{OUT} register is a read/write byte register that reports over and undervoltage warnings for the V_{BUS} input.

TABLE 37. 0x7A STATUS V_{OUT} REGISTER DEFINITION

BIT NUMBER	D[7]	D[6]	D[5]	D[4:0]
Bit Name	N/A	V_{OUT} OV Warning	V_{OUT} UV Warning	N/A
Default Value	0	0	0	0 0000

V_{OUT} OV WARNING D[6]

The V_{OUT} OV Warning bit is set to 1 when an overvoltage fault occurs on the V_{BUS} input. The V_{BUS} overvoltage threshold is set from the V_{OUT} OV Threshold Set register. In the event of a V_{BUS} overvoltage condition, the V_{OUT} OV Warning is latched to 1. Writing a 1 to the V_{OUT} OV Warning bit will clear the warning resulting in a bit value equal to 0.

VOUT UV WARNING D[5]

The V_{OUT} UV Warning bit is set to 1 when an undervoltage fault occurs on the V_{BUS} input. The V_{BUS} undervoltage threshold is set from the V_{OUT} UV Threshold Set register. In the event of a V_{BUS} undervoltage condition, the V_{OUT} UV Warning is latched to 1. Writing a 1 to the V_{OUT} UV Warning bit will clear the warning resulting in a bit value equal to 0.

0X7B STATUS I_{OUT} (R/W)

The Status I_{OUT} register is a read/write byte register that reports an overcurrent warning for the V_{SHUNT} input.

TABLE 38. 0x7B STATUS I_{OUT} REGISTER DEFINITION

BIT NUMBER	D[7]	D[6]	D[5]	D[4:0]
Bit Name	N/A	N/A	I_{OUT} OC Warning	N/A
Default Value	0	0	0	0 0000

I_{OUT} OC WARNING D[5]

The I_{OUT} OC Warning bit is set to 1 when an overcurrent fault occurs on the V_{SHUNT} input. The V_{SHUNT} overcurrent threshold is set from the I_{OUT} OC Threshold Set register. In the event of a V_{SHUNT} overcurrent condition, the I_{OUT} OC Warning is latched to 1. Writing a 1 to the I_{OUT} OC Warning bit will clear the warning resulting in a bit value equal to 0.

0X7D STATUS TEMPERATURE (R/W)

The Status Temperature register is a read/write byte register that reports an over-temperature warning initiated from the internal temperature sensor.

TABLE 39. 0x7D STATUS TEMPERATURE REGISTER DEFINITION

BIT NUMBER	D[7]	D[6]	D[5]	D[4:0]
Bit Name	N/A	OT Warning	N/A	N/A
Default Value	0	0	0	0 0000

OT WARNING D[6]

The OT Warning bit is set to 1 when an over-temperature fault occurs from the internal temperature sensor. The over-temperature threshold is set from the V_{OUT} OV Threshold Set register. In the event of an over-temperature condition, the OT Warning bit is latched to 1. Writing a 1 to the OT Warning bit will clear the warning resulting in a bit value equal to 0.

0X7E STATUS CML (R/W)

The Status CML register is a read/write byte register that reports warnings and errors associated with communications, logic, and memory.

TABLE 40. 0x7E STATUS CML REGISTER DEFINITION

BIT NUMBER	D[7]	D[6]	D[5]	D[4:2]	D[1]	D[0]
Bit Name	USCMD	USDATA	PECERR	N/A	COMERR	N/A
Default Value	0	0	0	0 00	0	0

USCMD D[7]

The USCMD bit is set to 1 when an unsupported command is received from the I^2C master. Reading from an undefined register is an example of an action that would set the USCMD bit. The USCMD bit is a latched bit. Writing a 1 to the USCMD bit clears the warning resulting in a bit value equal to 0.

USDATA D[6]

The USDATA bit is set to 1 when an unsupported data is received from the I^2C master. Writing a word to a byte register is an example of an action that would set the USDATA bit. The USDATA bit is a latched bit. Writing a 1 to the USDATA bit clears the warning resulting in a bit value equal to 0.

PECERR D[5]

The PECERR bit is set to 1 when a Packet Error Check (PEC) event has occurred. Writing the wrong PEC to the DPM is an example of an action that would set the PECERR bit. The PECERR bit is a latched bit. Writing a 1 to the PECERR bit clears the warning resulting in a bit value equal to 0.

COMERR D[1]

The COMERR bit is set to 1 for communication errors that are not handled by the USCMD, USDATA and PECERR errors. Reading from a write only register is an example of an action that would set the COMERR bit. The COMERR bit is a latched bit. Writing a 1 to the COMERR bit clears the warning resulting in a bit value equal to 0.

0X78 STATUS BYTE (R/W)

The Status Byte register is a read/write byte register that is a hierarchical register to the Status Temperature and Status CML registers. The Status Byte registers bits are set if an over-temperature or a CML error has occurred.

TABLE 41. 0x78 STATUS BYTE REGISTER DEFINITION

BIT NUMBER	D[7]	D[6:3]	D[2]	D[1]	D[0]
Bit Name	BUSY	N/A	Temperature	CML	N/A
Default Value	0	000 0	0	0	0

BUSY D[7]

The BUSY bit is set to 1 when the DPM is busy and unable to respond. The BUSY bit is a latched bit. Writing a 1 to the BUSY bit clears the warning resulting in a bit value equal to 0.

TEMPERATURE D[2]

The Temperature bit is set to 1 when an over-temperature fault occurs from the internal temperature sensor. This bit is the same action bit as the OT Warning bit in the Status Temperature register. The over-temperature threshold is set from the V_{OUT} OV Threshold Set register. In the event of an over-temperature condition, the Temperature bit is latched to 1. Writing a 1 to the Temperature bit will clear the warning resulting in a bit value equal to 0.

CML D[1]

The CML bit is set to 1 when any errors occur within the Status CML register. There are four Status CML error bits that can set the CML bit. The CML bit is a latched bit. Writing a 1 to the CML bit clears the warning resulting in a bit value equal to 0.

0X79 STATUS WORD (R/W)

The Status Word register is a read/write word register that is a hierarchical register to the Status V_{OUT}, Status I_{OUT} and Status Byte registers. The Status Word registers bits are set when any errors previously described occur. The register generically reports all errors.

TABLE 42. 0x79 STATUS WORD REGISTER DEFINITION

BIT NUMBER	D[15]	D[14]	D[13:8]	D[7:0]
Bit Name	V_{OUT}	I_{OUT}	N/A	See Status Byte
Default Value	0	0	00 0000	0000 0000

V_{OUT} D[15]

The V_{OUT} bit is set to 1 when any errors occur within the Status V_{OUT} register. Whether either or both an undervoltage or overvoltage fault occurs, the V_{OUT} bit will be set. The V_{OUT} bit is a latched bit. Writing a 1 to the V_{OUT} bit clears the warning resulting in a bit value equal to 0.

I_{OUT} D[14]:

The I_{OUT} bit is set to 1 when an overcurrent fault occurs. This bit is the same action bit as the I_{OUT} OC Warning bit in the Status I_{OUT} register. In the event of an overcurrent condition, the I_{OUT} bit is latched to 1. Writing a 1 to the I_{OUT} bit will clear the warning resulting in a bit value equal to 0.

0X1B SMBALERT MASK (BR/BW)
0XDF SMBALERT2 MASK (BR/BW)

The SMBALERT registers are block read/write registers that mask error conditions from electrically triggering the respective SMBALERT pin.

The SMBALERT can mask bits of any of the status registers. Masking lower level bits prevents the hierarchical bit from being set. For example, a COMERR bit being masked will not set the CML bit of the Status Byte register.

To mask a bit, the first data byte is the register address of the bit(s) to be masked. The second and third data bytes are the masking bits of the register. A masking bit of 1 prevents the signal from triggering an interrupt.

All alert bits are masked as the default state for both the SMB alert pins. The master needs to send instructions to unmask the alert bits.

As an example, a user would like to allow the COMERR bit to trigger a SMBALERT2 interrupt while masking the rest of the alerts within the Status CML register. The command that is sent from the master to the DPM is the slave address, SMBALERT2 register address, Status CML register address and the mask bit value. In a hexadecimal format, the data sent to the DPM is as follows; 0x80 DF 7E FD.

To read the mask status of any alert register, write a four byte command, without PEC, consisting of the slave address of the device, the SMB mask register address, the number of bytes to be read back and the register address of the mask to be read. Once the write command has commenced, a read command consisting of the device slave address and the register address of the SMB mask will return the mask of the desired alert register.

As an example, a user would like to read the status of the Status Byte register. The first command sent to the DPM is in hexadecimal bytes is 0x82 1B 01 78. The second command is a standard read. The slave address is 0x83 (0x82 + read bit set) and the register address is 0x1B.

SMBALERT1 RESPONSE ADDRESS

The SMBALERT1 pin of each ISL28025 device is commonly shared to a single GPIO pin of the microcontroller. The SMBALERT1 pin is an open drain allowing for multiple devices to be OR'ed to a single GPIO pin.

The SMBALERT1 Response Address command reports the slave address of the device that has triggered alert. The SMB Respond Address command is shown in Figure 69.

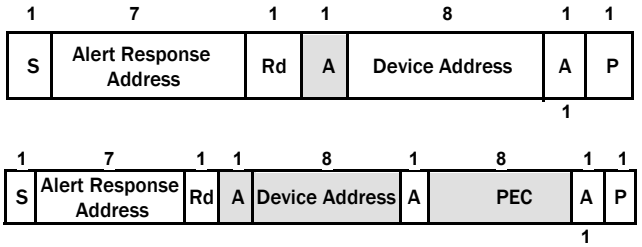


FIGURE 69. THE COMMAND STRUCTURE OF THE SMBALERT RESPONSE ADDRESS

The alert response address is 0x18. In the event of multiple alerts pulling down the GPIO line, the alert respond command will return the lowest slave address that is connected to the I^2C bus. Upon clearing the lowest slave address alert, the alert command will return the lowest slave address of the remaining alerts that are activated.

The alert response is operable when the interrupt active state is forced low by the device at the SMBALERT1 pin. Changing SMBALERT1 interrupt polarity or forcing an interrupt will enable the alert response. By design the open drain of the SMBALERT1 pin allows for ANDing of the interrupt via a pull-up resistor. The alert response command is valid for only the SMBALERT1 pin. The alert response command will return a 0x19 when there are no errors detected.

External Clock Control (16 Pin WLCSP)

The DPM has an external clock feature that allows the chip to be synchronized to an external clock. The feature is useful in limiting the number of clocks running asynchronously within a system.

0XE5 CONFIGURE EXTERNAL CLOCK (R/W)

The Configure External Clock register is a read/write byte register that controls the functionality of the external clock feature.

TABLE 43. 0xE5 CONFIGURE EXTERNAL CLOCK REGISTER DEFINITION

BIT NUMBER	D[7]	D[6]	D[5:4]	D[3:0]
Bit Name	ExtCLK_EN	SMBLALERT2OEN	N/A	EXTClkDIV
Default Value	0	0	00	0000

EXTCLK_EN D[7]

The ExtClk_EN bit enables the external clock feature. The ExtClk_En default bit setting is 0 or disabled. A bit setting of 1 disables the internal oscillator of the DPM and connects circuitry such that the system clock is routed from the external clock pin.

SMBALERT2_OEN D[6]

The SMBALERT2_OEN bit within the Configure External Clock register either enables or disables the buffer that drives the SMBALERT2 pin.

TABLE 44. SMBALERT2_OEN BIT DEFINED

SMBALERT_OEN	SMBALERT2 STATUS
0	Disabled
1	Enabled

EXTCLKDIV D[3:0]

The EXTCLKDIV bits control an internal clock divider that is useful for fast system clocks. The internal clock frequency from pin to chip is represented in Equation 13.

$$\text{freq}_{\text{internal}} = \frac{f_{EXTCLK}}{(\text{ClkDiv} \cdot 8) + 8} \quad \text{(EQ. 13)}$$

f_{EXTCLK} is the frequency of the signal driven to the External Clock pin. ClkDiv is the decimal value of the clock divide bits.

Voltage Margin / DAC_OUT (20 Pin QFN)

The voltage margining feature within the DPM is commonly used as a means to test the robustness of a system. The voltage DAC from the DPM is connected to a summation circuit allowing the voltage sourced from the DAC to raise or lower the overall voltage supply to system. A simplified block diagram is illustrated in Figure 70.

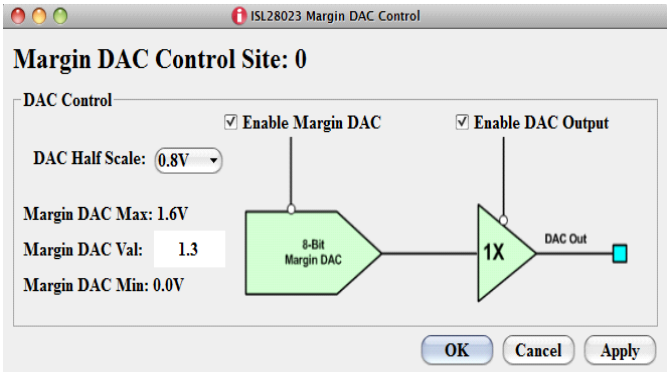


FIGURE 70. SIMPLIFIED BLOCK DIAGRAM OF THE MARGIN DAC FUNCTIONS WITHIN THE DPM

The voltage margining feature can be used to improve accuracy of the voltage applied to the load of a system. For nonfeedback driving applications, the sense resistor used to measure current to the load reduces the voltage to the load. The voltage drop from the sense resistor can be a large percentage with respect to the supply voltage for point of load applications.

0XE4 CONFIGURE VOL MARGIN (R/W)

The Configure VOL Margin register is a read/write byte register that controls the functionality of the voltage margin DAC.

TABLE 45. 0xE4 CONFIGURE VOL MARGIN REGISTER DEFINITION

BIT NUMBER	D[7:6]	D[5:3]	D[2]	D[1]	D[0]
Bit Name	N/A	MDAC_HS	Load	DAC_OEN	DAC_EN
Default Value	00	00 0	0	0	0

MDAC_HS D[5:3]

The MDAC_HS bits control the half-scale output voltage from the margin DAC. There are 8 half-scale voltages the margin DAC can be programmed to. Table 46 lists the selections.

TABLE 46. MDAC_HS BITS DEFINED

MDAC_HS[2:0]			HALF-SCALE VOLTAGE (V)
0	0	0	0.4
0	0	1	0.5
0	1	0	0.6
0	1	1	0.7
1	0	0	0.8
1	0	1	0.9
1	1	0	1.0

TABLE 46. MDAC_HS BITS DEFINED

MDAC_HS[2:0]			HALF-SCALE VOLTAGE (V)
1	1	1	1.2

The voltage at the DAC_OUT is the value of the MDAC_HS setting when the Set VOL Margin register equals 0x80.

LOAD D[2]

The Load bit programs the Set VOL Margin register to the DAC. The DAC is programmed when the Load bit is programmed from a 0 to a 1.

DAC_OEN D[1]

The DAC_OEN bit either enables or disables the output of the margin DAC. Setting the bit to a 1 connects the output of the margin DAC to the DAC_OUT pin.

DAC_EN D[0]

The DAC_EN bit either enables or disables the margin DAC circuitry. Setting the bit to a 1 powers up the margin DAC, making it operational to use.

0XE3 SET VOL MARGIN (R/W)

The Set VOL Margin register is an unsigned read/write byte register that controls the output voltage of the margin DAC referenced to the half-scale setting.

TABLE 47. 0xE3 SET VOL MARGIN REGISTER DEFINITION

BIT NUMBER	D[7:0]
Bit Name	MDAC[7:0]
Default Value	0000 0000

The full-scale voltage is twice the half-scale range minus the DAC LSB for the margin DAC half-scale range. A half-scale setting of 1.0V has a full-scale setting of 1.992V. The LSB for the margin DAC is a function of the half-scale setting. Using Equation 14, the LSB for the margin DAC is calculated as;

$$MDAC_{LSB} = \frac{(2 \cdot MDAC_{HS})}{2^8} = \frac{2 \cdot MDAC_{HS}}{256} \quad \text{(EQ. 14)}$$

$MDAC_{HS}$ is the half-scale setting for the voltage DAC.

The VOL margin register value for programming the DAC to a specific voltage is calculated using Equation 15.

$$MDAC_{value} = \text{integer}\left(\frac{Vout_{desired}}{MDAC_{LSB}}\right) \quad \text{(EQ. 15)}$$

The value for $VOUT_{desired}$ ranges from 0V to two times the $MDAC_{HS}$ value minus one $MDAC_{LSB}$.

SMBus/I^{2}C Serial Interface

The ISL28025 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL28025 operates as a slave device in all applications.

The ISL28025 uses two byte data transfer. All reads and writes are required to use two data bytes. All communication over the I^{2}C interface is conducted by sending the MSB of each byte of data first, followed by the LSB.

Protocol Conventions

For normal operation, data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 71). On power-up, the SDA pin is in the input mode.

All I^{2}C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The device continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 71). A START condition is ignored during the power-up sequence.

All I^{2}C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 71). A STOP condition at the end of a read operation or at the end of a write operation places the device in its standby mode.

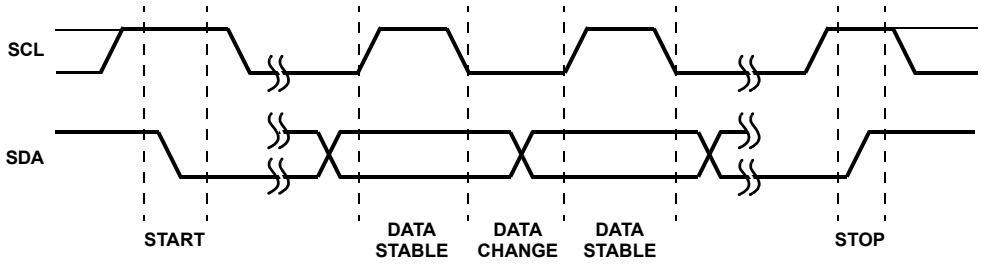


FIGURE 71. VALID DATA CHANGES, START AND STOP CONDITIONS

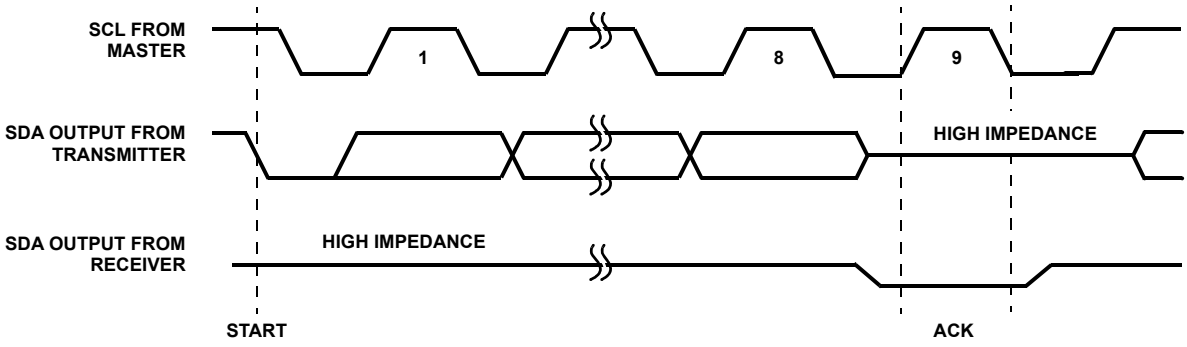


FIGURE 72. ACKNOWLEDGE RESPONSE FROM RECEIVER

SMBus and PMBus Support

The ISL28025 supports SMBus and PMBus protocol, which is a subset of the global I^2C protocol. SMBCLK and SMBDAT have the same pin functionality as the SCL and SDA pins, respectively. The SMBus operates at 100kHz. The PMBus protocol standardizes the functionality of each register by address.

Device Addressing

Following a start condition, the master must output a slave address byte. The 7 MSBs are the device identifiers. The A0, A1 and A2 pins control the bus address (these bits are shown in Table 48). There are 55 possible combinations depending on the A0, A1 and A2 connections.

TABLE 48. I^2C SLAVE ADDRESSES

A2	A1	A0	SLAVE ADDRESS
GND	GND	GND	1000 000
GND	GND	I2CVCC	1000 001
GND	GND	SDA	1000 010
GND	GND	SCL	1000 011
GND	I2CVCC	GND	1000 100
GND	I2CVCC	I2CVCC	1000 101
GND	I2CVCC	SDA	1000 110
GND	I2CVCC	SCL	1000 111
GND	SDA	GND	1001 000
GND	SDA	I2CVCC	1001 001
GND	SDA	SDA	1001 010
GND	SDA	SCL	1001 011
GND	SCL	GND	1001 100
GND	SCL	I2CVCC	1001 101
GND	SCL	SDA	1001 110
GND	SCL	SCL	1001 111
I2CVCC	GND	GND	1010 000
.....	.....	.....	.....
I2CVCC	SCL	SCL	1011 111
SDA	GND	GND	1100 000
SDA	GND	VCC	Do Not Use. Reserved
.....	.....	.....	.....
SDA	SCL	SCL	1101 111
SCL	GND	GND	1110 000
.....	.....	.....	.....
SCL	SDA	X	Do Not Use. Reserved
SCL	SCL	X	Do Not Use. Reserved

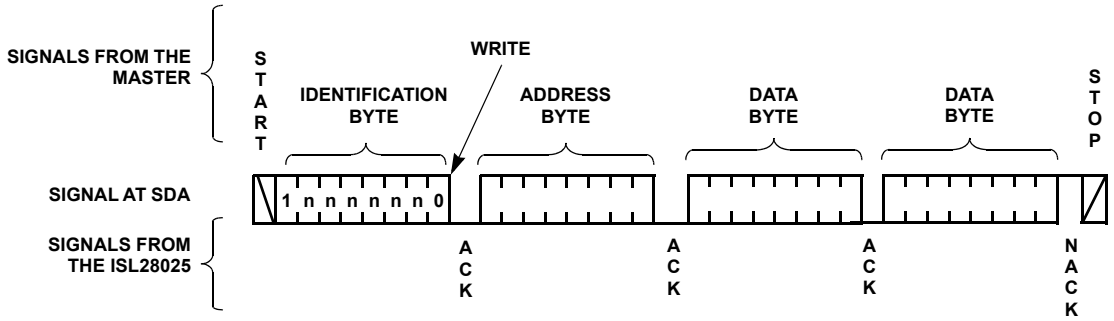


FIGURE 73. BYTE WRITE SEQUENCE (SLAVE ADDRESS INDICATED BY nnnn)

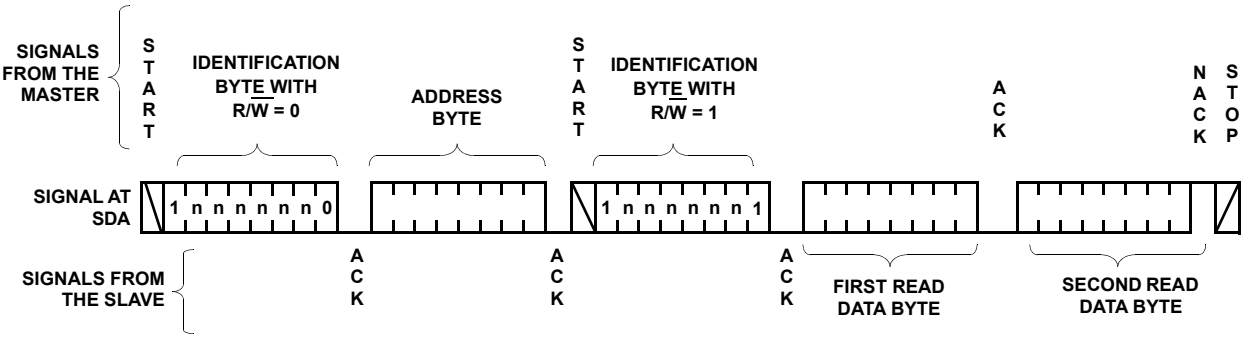


FIGURE 74. READ SEQUENCE (SLAVE ADDRESS SHOWN AS nnnn)

The last bit of the slave address byte defines a read or write operation to be performed. When this R/$\overline{W}$ bit is a "1", a read operation is selected. A "0" selects a write operation (refer to Figure 73).

After loading the entire slave address byte from the SDA bus, the device compares with the internal slave address. Upon a correct compare, the device outputs an acknowledge on the SDA line.

Following the slave byte is a one byte word address. The word address is either supplied by the master device or obtained from an internal counter. On power-up, the internal address counter is set to address 00h, so a current address read starts at address 00h. When required, as part of a random read, the master must supply the one word address bytes, as shown in Figure 74.

In a random read operation, the slave byte in the "dummy write" portion must match the slave byte in the "read" section. For a random read of the registers, the slave byte must be "1nnnnnnx" in both places.

Write Operation

A write operation requires a START condition, followed by a valid identification byte, a valid Address byte, two data bytes, and a STOP condition. The first data byte contains the MSB of the data, the second contains the LSB. After each of the four bytes, the device responds with an ACK. At this time, the I^2C interface enters a standby state.

Read Operation

A read operation consists of a three byte instruction, followed by two data bytes (see Figure 74). The master initiates the operation issuing the following sequence: A START, the identification byte with the R/$\overline{W}$ bit set to "0", an address byte, a second START and a second identification byte with the R/$\overline{W}$ bit set to "1". After each of the three bytes, the ISL28025 responds with an ACK. Then the ISL28025 transmits two data bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of the first byte. The master terminates the read operation (issuing no ACK then a STOP condition) following the last bit of the second data byte (see Figure 74).

The data bytes are from the memory location indicated by an internal pointer. This pointer's initial value is determined by the address byte in the read operation instruction and increments by one during transmission of each pair of data bytes.

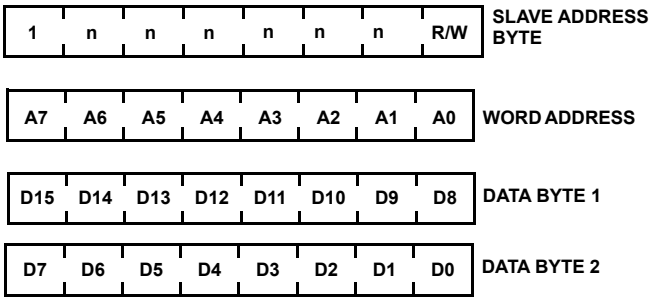


FIGURE 75. SLAVE ADDRESS, WORD ADDRESS AND DATA BYTES

Group Command

The DPM has a feature that allows the master to configure the settings of all DPM chips at once. The configuration command for each device does not have to be same. Device 1 on an I^2C bus can be configured to set the voltage threshold of the OV comparator while device 2 is configured for the acquisition time of the VBUS input. To achieve the scenario described without group command, the master sends two write commands, one to each slave device. Each command sent from the master has a start bit and a stop bit. The group command protocol concatenates the two commands but replaces the stop bit of the first command and the start bit of the second command with a repeat start bit. The actions sent in a Group Command format will execute once the stop bit has been sent. The stop bit signifies the end of a packet.

The broadcast feature saves time in configuring the DPM as well as measuring signal parameters in time synchronization. The broadcast should not be used for DPM read backs. This will cause all devices connected to the I^2C bus to talk to the master simultaneously.

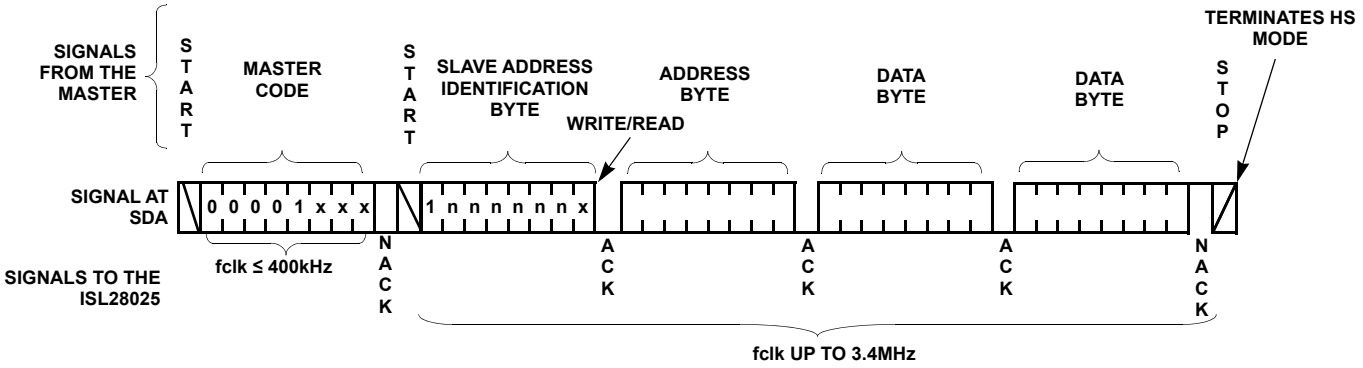


FIGURE 76. BYTE TRANSACTION SEQUENCE FOR INITIATING DATA RATES ABOVE 400kbps

Clock Speed

The device supports high-speed digital transactions up to 3.4Mbs. To access the high speed I^2C feature, a master byte code of 0000 1xxx is attached to the beginning of a standard frequency read/write I^2C protocol. The x in the master byte signifies a do not care state. X can either equal a 0 or a 1. The master byte code should be clocked into the chip at frequencies equal or less than 400kHz. The master code command configures the internal filters of the ISL28025 to permit data bit frequencies greater than 400kHz. Once the master code has been clocked into the device, the protocol for a standard read/write transaction is followed. The frequency at which the standard protocol is clocked in at can be as great as 3.4MHz. A stop bit at the end of a standard protocol will terminate the high speed transaction mode. Appending another standard protocol serial transaction to the data string without a stop bit, will resume the high speed digital transaction mode. Figure 76 illustrates the data sequence for the high speed mode. The minimum I^2C supply voltage when operating at clock speeds 400kHz is 1.8V.

Signal Integrity

A filter stage should be considered to limit the effects of common-mode signals from bleeding into the measurement made by the ADC. The filter attenuates the amplitude of the unwanted signal to the noise level of the ISL28025. Figure 77 is a simple filter example to attenuate unwanted signals.

Measuring large currents require low value sense resistors. A large valued capacitor is required to filter low frequencies if the shunt capacitor, C_{SH} is connected directly in parallel to the sense resistor, R_{SH}. For more manageable capacitor values, it may be better to directly connect the shunt resistor across the shunt inputs of the ISL28025. The connection is illustrated in Figure 77. A single pole filter constructed of 2 resistors, R_1, and R_{SH} will improve capacitor value selections for low frequency filtering.

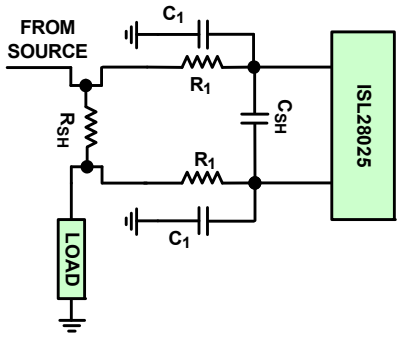


FIGURE 77. SIMPLIFIED FILTER DESIGN TO IMPROVE NOISE PERFORMANCE TO THE ISL28025

R_1 and C_1 at both shunt inputs are single-ended low pass filters. The value of the series resistor to the ISL28025 can be a larger value than the shunt resistor, R_{SH}. A larger series resistor to the input allows for a lower cutoff frequency filter design to the ISL28025. The ISL28025 inputs can source up to 20µA of transient current in the measurement mode. The transient or switching offset current can be as large as 10µA. The switching offset current combined with the series resistance, R_1, creates an error offset voltage. A balance of the value of R_1 and the shunt measurement error should be achieved for this filter design.

The common-mode voltage of the shunt input stage ranges from 0V to 60V. The capacitor voltage rating for C_1 and C_{SH} should comply with the nominal voltage being applied to the input.

Fast Transients

An small isolation resistor placed between ISL28025 inputs and the source is recommended. In hot swap or other fast transient events, the amplitude of a signal can exceed the recommended operating voltage of the part due to the line inductance. The isolation resistor creates a low pass filter between the device and the source. The value of the isolation resistor should not be too large. A large value isolation resistor can effect the measurement accuracy. The value of the isolation resistor combined with the offset current creates an offset voltage error at the shunt input. The input of the Bus channel is connected to the top of a precision resistor divider. The accuracy of the resistor divider determines the gain error of the Bus channel. The input resistance of the Bus channel is 600kΩ. Placing an isolation resistor of 10Ω will change the gain error of the Bus channel by 0.0016%.

External Clock

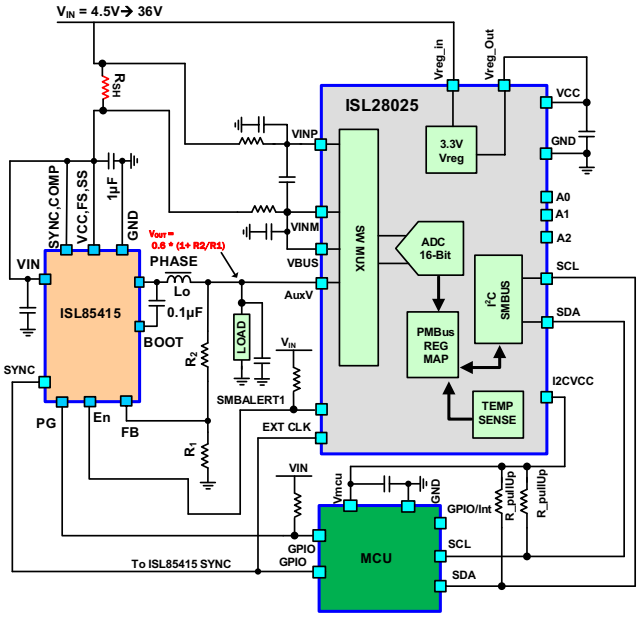


FIGURE 78. SIMPLIFIED SCHEMATIC OF THE ISL28025 SYNCHRONIZED TO A MCU SYSTEM CLOCK

An externally controlled clock allows measurements to be synchronized to an event that is time dependent. The event could be application generated, such as timing a current measurement to a charging capacitor in a switch regulator application or the event could be environmental. A voltage or current measurement may be susceptible to crosstalk from a controlled source. Instead of filtering the environmental noise from the measurement, another approach would be to synchronize the measurement to the source. The variability and accuracy of the measurement will improve.

The ISL28025 has the functionality to allow for synchronization to an external clock. The speed of the external clock combined with the choice of the internal chip frequency division value determines the acquisition times of the ADC. The internal system clock frequency is 500kHz. The internal system clock is also the ADC sampling clock. The acquisition times scale linearly from 500kHz. For example, an external clock frequency of 4.0MHz with a frequency divide setting of 0 (internal divide by 8) results in acquisition times that equals the internal oscillator frequency when enabled. The ADC modulator is optimized for frequencies of 500kHz. Operating internal clock frequencies beyond 500kHz may result in measurement accuracy errors due to the modulator not having enough time to settle.

Suppose an external clock frequency of 5.5MHz is applied with a divide by 88 internal frequency setting, the system clock speed is 62.5kHz or 8x slower than internal system clock. The acquisition times for this example will increase by 8. For a channel's conversion time setting of 2.048ms, the ISL28025 will have an acquisition time of 256µs.

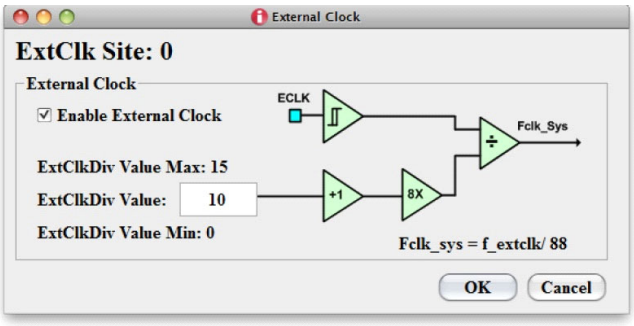


FIGURE 79. EXTERNAL CLOCK MODE

Figure 79 illustrates a simple mathematical diagram of the ECLK pin internal connection. The external clock divide is controlled by way of the EXTCLKDIV bit in register 0xE5.

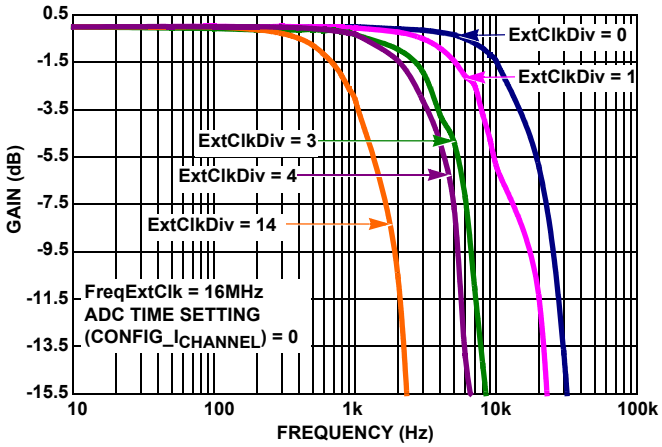


FIGURE 80. MEASUREMENT BANDWIDTH vs EXTERNAL CLK FREQUENCY

Figure 80 illustrates how changing the system clock frequency effects the measurement bandwidth (the ADC acquisition time).

The bandwidth of the external clock circuitry is 25MHz. Figure 81 shows the bandwidth of the external clock circuitry when the external clock division bits equals to 0.

The external clock pin can accept signal frequencies above 25MHz by programming the system clock frequency, so that the internal clock frequency is below 25MHz.

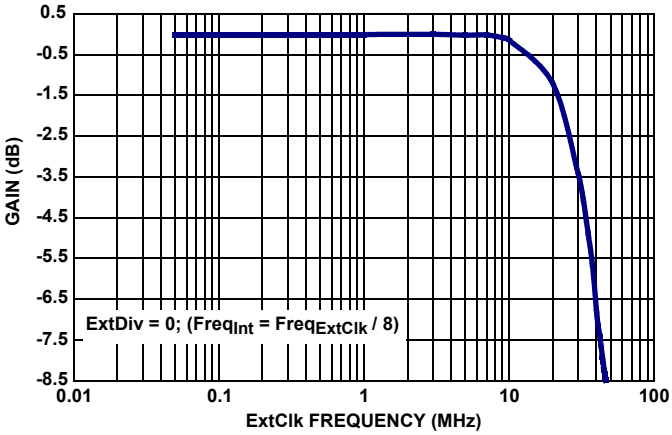


FIGURE 81. EXTERNAL CLOCK BANDWIDTH vs MEASUREMENT ACCURACY

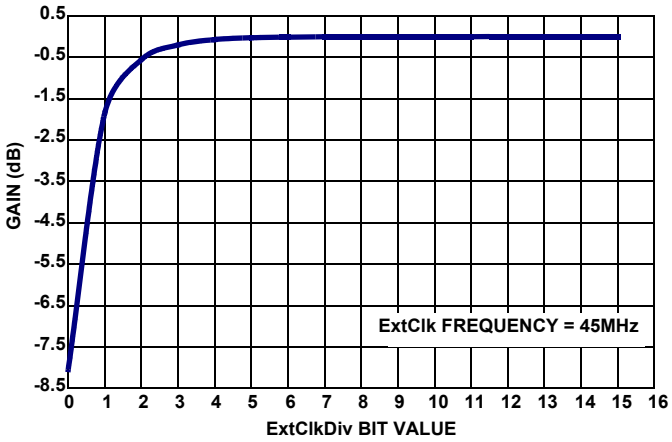


FIGURE 82. EXTERNAL CLOCK vs EXTERNAL BIT VALUE

Figure 82 illustrates the effects of dividing the external clock frequency on the V_{SHUNT} measurement accuracy.

Figures 81 and 82 were generated by applying a DC voltage to the V_{SHUNT} input and measuring the signal by way of an ADC conversion.

Overranging

Do not operate the ISL28025 outside the set voltage range. In the event of measuring a shunt voltage beyond the maximum set range (80mV) and lower than the clamp voltage of the protection diode (1V), the measured output reading may be within the accepted range but will be incorrect.

Shunt Resistor Selection

In choosing a sense resistor, the following resistor parameters need to be considered; the resistor value, resistor temperature coefficient and resistor power rating.

The sense resistor value is a function of the full-scale voltage drop across the shunt resistor and the maximum current measured for the application. The maximum measurable range for the V_{SHUNT} input (V_{INP} - V_{INM}) of the ISL28025 is 80mV. The ISL28025 allows the user to define a unique range other than ±80mV.

Once the voltage range for the input is chosen and the maximum measurable current is known, the sense resistor value is calculated using Equation 16.

$$R_{sense} = \frac{V_{shunt\_range}}{Imeas_{Max}} \quad \text{(EQ. 16)}$$

In choosing a sense resistor, the sense resistor power rating should be taken into consideration. The physical size of a sense resistor is proportional to the power rating of the resistor. The maximum power rating for the measurement system is calculated as the V_{shunt_range} multiplied by the maximum measurable current expected. The power rating equation is represented in Equation 17.

$$P_{res\_rating} = V_{shunt\_range} \cdot Imeas_{Max} \quad \text{(EQ. 17)}$$

A general rule of thumb is to multiply the power rating calculated in Equation 17 by 2. This allows the sense resistor to survive an event when the current passing through the shunt resistor is greater than the measurable maximum current. The higher the ratio between the power rating of the chosen sense resistor and the calculated power rating of the system (Equation 17), the less the resistor will heat up in high current applications.

The Temperature Coefficient (TC) of the sense resistor directly degrades the current measurement accuracy. The surrounding temperature of the sense resistor and the power dissipated by the resistor will cause the sense resistor value to change. The change in resistor temperature with respect to the amount of current that flows through the resistor is directly proportional to the ratio of the power rating of the resistor versus the power being dissipated. A change in sense resistor temperature results in a change in sense resistor value. Overall, the change in sense resistor value contributes to the measurement accuracy for the system. The change in a resistor value due to a temperature rise can be calculated using Equation 18.

$$\Delta R_{sense} = R_{sense} \cdot Rsense_{TC} \cdot \Delta Temperature \quad \text{(EQ. 18)}$$

ΔTemperature is the change in temperature in Celsius. $Rsense_{TC}$ is the temperature coefficient rating for a sense resistor. R_{sense} is the resistance value of the sense resistor at the initial temperature.

Table 49 is a shunt resistor look-up table for select full-scale current measurement ranges ($Imeas_{Max}$). The table also provides the minimum rating for each shunt resistor.

TABLE 49. SHUNT RESISTOR VALUES AND POWER RATINGS FOR SELECT MEASURABLE CURRENT RANGES

R_{SENSE}/P_{RATING}	V_{SHUNT} RANGE (PGA SETTING)
$Imeas_{Max}$	80mV
100µA	800Ω/8µW
1mA	80Ω/80µW
10mA	8Ω/800µW
100mA	800mΩ/8mW
500mA	160mΩ/40mW
1A	80mΩ/80mW
5A	16mΩ/400mW
10A	8mΩ/800mW
50A	1.6mΩ/4W
100A	0.8mΩ/8W
500A	0.16mΩ/40W

It can be difficult to readily purchase shunt resistor values for a desired measurable current range. Either the value of the shunt resistor does not exist or the power rating of the shunt resistor is too low. To avoid this problem, use two or more shunt resistors in parallel to set the desired current measurement range. For example, an application requires a full-scale current of 100A with a maximum voltage drop across the shunt resistor of 80mV. From Table 49, this requires a sense resistor of 0.8mΩ, 8W resistor. Assume the power ratings and the shunt resistor values to chose from are 1mΩ/4W, 2mΩ/4W and 4mΩ/4W.

Let's use a 1mΩ and a 4mΩ resistor in parallel to create the shunt resistor value of 0.8mΩ. Figure 83 shows an illustration of the shunt resistors in parallel.

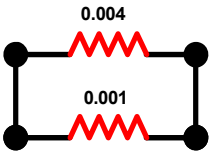


FIGURE 83. SIMPLIFIED SCHEMATIC ILLUSTRATING THE USE OF TWO SHUNT RESISTORS TO CREATE A DESIRED SHUNT VALUE

The power to each shunt resistor should be calculated before calling a solution complete. The power to each shunt resistor is calculated using Equation 19.

$$P_{shuntRes} = \frac{V_{shunt\_range}^{2}}{R_{sense}} \quad \text{(EQ. 19)}$$

The power dissipated by the 1mΩ resistor is 6.4W. 1.6W is dissipated by the 4mΩ resistor. 1.6W exceeds the rating limit of 1W for the 1mΩ sense resistor. Another approach would be to use three shunt resistors in parallel as illustrated in Figure 84.

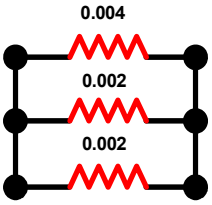


FIGURE 84. INCREASING THE NUMBER OF SHUNT RESISTORS IN PARALLEL TO CREATE A SHUNT RESISTOR VALUE REDUCES THE POWER DISSIPATED BY EACH SHUNT RESISTOR

Using Equation 19, the power dissipated to each shunt resistor yields 3.2W for the 2mΩ shunt resistors and 1.6W for the 4mΩ shunt resistor. All shunt resistor are within the specified power ratings.

Layout

The layout of a current measuring system is equally important as choosing the correct sense resistor and the correct analog converter. Poor layout techniques can result in severed traces, signal path oscillations, and magnetic contamination, which all contribute to poor system performance.

TRACE WIDTH

Matching the current carrying density of a copper trace with the maximum current that will pass through is critical in the performance of the system. Neglecting the current carrying capability of a trace will result in a large temperature rise in the trace, and the loss in system efficiency due to the increase in resistance of the copper trace. In extreme cases, the copper trace could be severed because the trace could not pass the current. The current carrying capability of a trace is calculated using Equation 20.

$$Trace_{width} = \frac{\left(\frac{Imax}{k \cdot \Delta T^{0.44}}\right)^{\frac{1}{0.725}}}{Trace_{Thickness}} \quad \text{(EQ. 20)}$$

I_{max} is the largest current expected to pass through the trace. ΔT is the allowable temperature rise in Celsius when the maximum current passes through the trace. $Trace_{Thickness}$ is the thickness of the trace specified to the PCB fabricator in mils. A typical thickness for general current carrying applications (<100mA) is 0.5oz. copper or 0.7mils. For larger currents, the trace thickness should be greater than 1.0oz. or 1.4mils. A balance between thickness, width and cost needs to be achieved for each design. The coefficient k in Equation 20 changes depending on the trace location. For external traces, the value of k equals 0.048 while for internal traces the value of k reduces to 0.024. The k values and Equation 20 are stated per the ANSI IPC-2221(A) standards.

TRACE ROUTING

It is always advised to make the distance between the voltage source, sense resistor, and load as close as possible. The longer the trace length between components will result in voltage drops between components. The additional resistance will reduce the efficiency of a system.

The bulk resistance, ρ, of copper is 0.67µΩ/in or 1.7µΩ/cm at +25°C. The resistance of trace can be calculated from Equation 21.

$$R_{trace} = \rho \cdot \frac{Trace_{length}}{Trace_{width} \cdot Trace_{thickness}} \quad \text{(EQ. 21)}$$

Figure 85 illustrates each dimension of a trace.

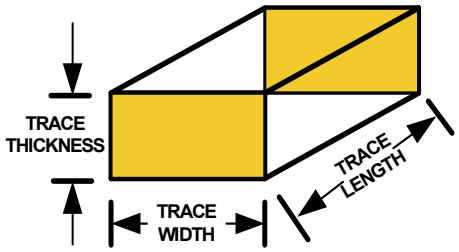


FIGURE 85. ILLUSTRATION OF THE TRACE DIMENSIONS OF A STRIP LINE TRACE

For example, assume a trace has 2oz. of copper or 2.8mil thickness, a width of 100mil and a length of 0.5in. Using Equation 21, the resistance of the trace is approximately 2mΩ. Assume 1A of current is passing through the trace. A 2mV voltage drop would result from trace routing.

Current flowing through a conductor will take the path of least resistance. When routing a trace, avoid orthogonal connections for current bearing traces.

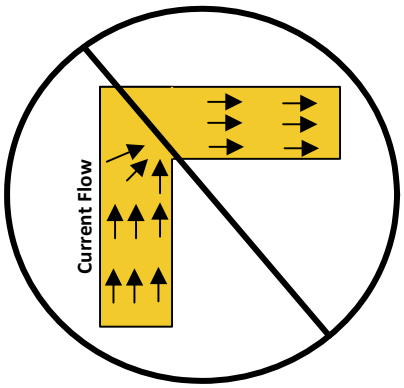


FIGURE 86. AVOID ROUTING ORTHOGONAL CONNECTIONS FOR TRACES THAT HAVE HIGH CURRENT FLOWS.

Orthogonal routing for high current flow traces will result in current crowding, localized heating of the trace and a change in trace resistance.

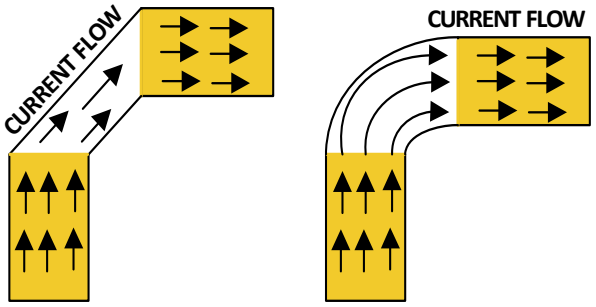


FIGURE 87. USE ARCS AND 45° TRACES TO SAFELY ROUTE TRACES WITH LARGE CURRENT FLOWS

The utilization of arcs and 45° traces in routing large current flow traces will maintain uniform current flow throughout the trace. Figure 87 illustrates the routing technique.

CONNECTING SENSE TRACES TO THE CURRENT SENSE RESISTOR

Ideally, a four terminal current sense resistor would be used as the sensing element. Four terminal sensor resistors can be hard to find in specific values and in sizes. Often a two terminal sense resistor is designed into the application.

Sense lines are high impedance by definition. The connection point of a high impedance line reflects the voltage at the intersection of a current bearing trace and a high impedance trace.

The high impedance trace should connect at the intersection where the sense resistor meets the landing pad on the PCB. The best place to make current sense line connection is on the inner side of the sense resistor footprint. The illustration of the connection is shown in Figure 88. Most of the current flow is at the outer edge of the footprint. The current ceases at the point the sense resistor connects to the landing pad. Assume the sense resistor connects at the middle of the each landing pad, this leaves the inner half of the each landing pad with little current flow. With little current flow, the inner half of each landing pad is classified as high impedance and perfect for a sense connection.

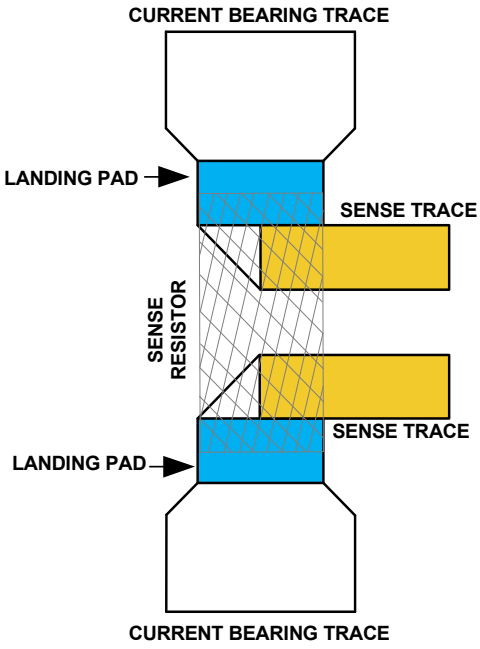
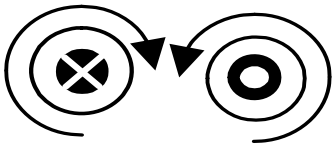


FIGURE 88. CONNECTING THE SENSE LINES TO A CURRENT SENSE RESISTOR

Current sense resistors are often smaller than the width of the traces that connect to the footprint. The trace connecting to the footprint is tapered at a 45° angle to control the uniformity of the current flow.

MAGNETIC INTERFERENCE

The magnetic field generated from a trace is directly proportional to the current passing through the trace and the distance from the trace the field is being measured at. Figure 89 illustrates the direction the magnetic field flows versus current flow.



$$B = \frac{\mu_o \cdot I}{2 \cdot \pi \cdot r}$$

FIGURE 89. THE CONDUCTOR ON THE LEFT SHOWS THE MAGNETIC FIELD FLOWING IN A CLOCKWISE DIRECTION FOR CURRENTS FLOWING INTO THE PAGE. CURRENT FLOW OUT OF THE PAGE HAS A COUNTER CLOCKWISE MAGNETIC FLOW

The equation in Figure 89 determines the magnetic field, B, the trace generates in relation to the current passing through the trace, I, and the distance the magnetic field is being measured from the conductor, r. The permeability of air, μ_o, is $4\pi * 10^{-7}$ H/m.

When routing high current traces, avoid routing high impedance traces in parallel with high current bearing traces. One way of limiting the magnetic interference from high current traces is to closely route the paths connected to and from the sense resistor. The magnetic fields will cancel outside the two traces and add between the two traces. Figure 90 illustrates a magnetic field insensitive layout.

If possible, do not cross traces with high current. If a trace crossing cannot be avoided, cross the trace in an orthogonal manner and the furthest layer from the current bearing trace. The inference from the current bearing trace will be limited.

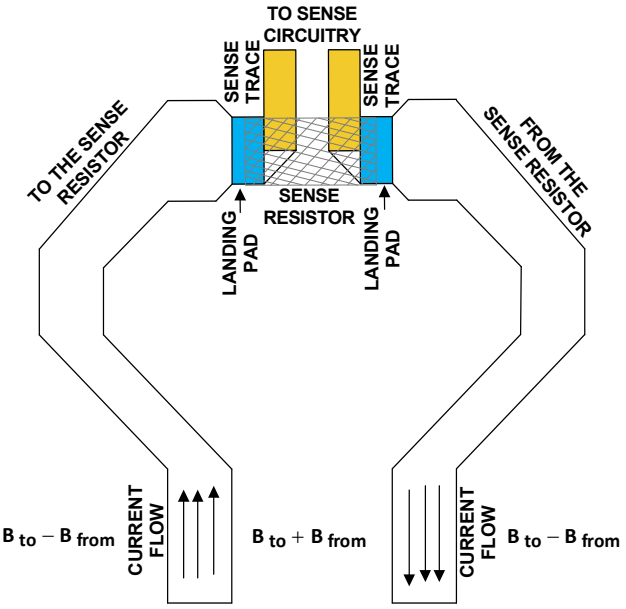


FIGURE 90. CLOSELY ROUTED TRACES THAT CONNECT TO THE SENSE RESISTOR REDUCES THE MAGNETIC INTERFERENCE SOURCED FROM THE CURRENT FLOWING THROUGH THE TRACES

A Trace as a Sense Resistor

In previous sections, the resistance and the current carrying capabilities of a trace were discussed. In high current sense applications, a design may utilize the resistivity of a current sense trace as the sense resistor. This section will discuss how to design a sense resistor from a copper trace.

Suppose an application needs to measure current up to 200A. The design requires the least amount of voltage drop for maximum efficiency. The full-scale voltage range of 40mV is chosen. From Ohm's law, the sense resistor is calculated to be 200µΩ. The power rating of the resistor is calculated to be 8W. Assume the PCB trace thickness of the board equals 2oz./2.8mils and the maximum temperature rise of the trace is +20°C. Using Equation 20 on page 45, the calculated trace width is 2.192in. The trace width, thickness and the desired sense resistor value is known. Utilizing Equation 21 on page 46, the trace length is calculated to be 1.832in.

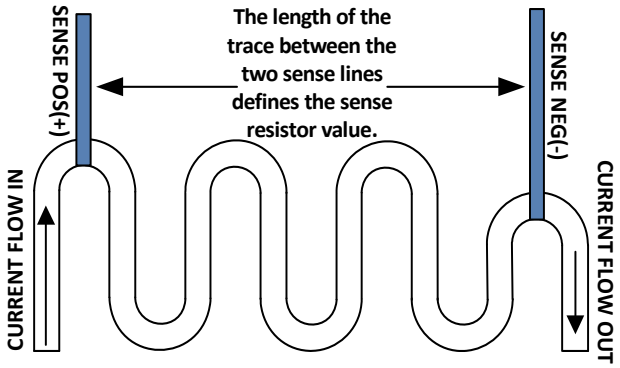


FIGURE 91. ILLUSTRATES A LAYOUT EXAMPLE OF A CURRENT SENSE RESISTOR MADE FROM A PCB TRACE

Figure 91 illustrates a layout example of a current sense resistor defined by a PCB trace. The serpentine pattern of the resistor reduces current crowding as well as limiting the magnetic interference caused by the current flowing through the trace.

For the example discussed, the width of the trace in Figure 91 illustration would equal 2.192in and the length between the sense lines equals 1.832in.

The width of the resistor is long for some applications. A means of shortening the trace width is to connect two traces in parallel. For calculation ease, assume the resistive traces are routed on the outside layers of a PCB. Using Equations 20 and 21, the width of the trace is reduced from 2.192in to 1.096in.

When using multiple layers to create a trace resistor, use multiple vias to keep the trace potentials between the two conductors the same. Vias are highly resistive compared to a copper trace. Multiple vias should be employed to lower the voltage drop due to current flowing through resistive vias. Figure 92 illustrates a layout technique for a multiple layered trace sense resistor.

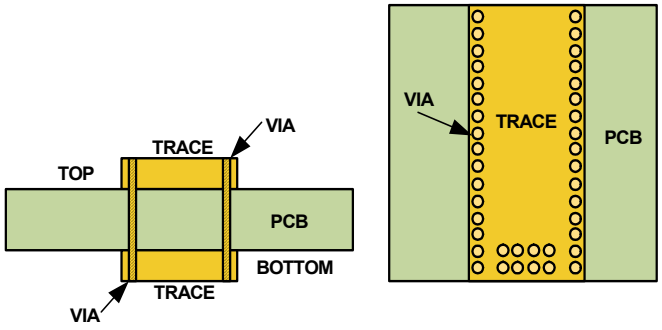


FIGURE 92. ILLUSTRATES A LAYOUT EXAMPLE OF A MULTIPLE LAYER TRACE RESISTOR

Lossless Current Sensing (DCR)

A DCR sense circuit is an alternative to a sense resistor. The DCR circuit utilizes the parasitic resistance of an inductor to measure the current to the load. A DCR circuit remotely measures the current through an inductor. The lack of components in series with the regulator to the load makes the circuit lossless.

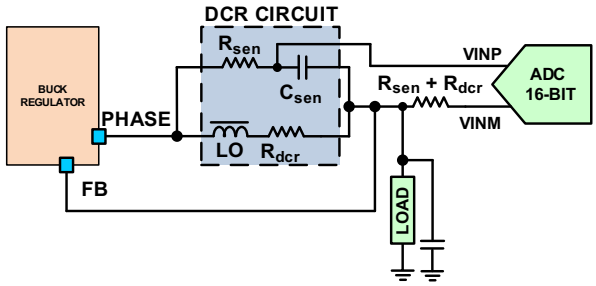


FIGURE 93. SIMPLIFIED CIRCUIT EXAMPLE OF A DCR

A properly matched DCR circuit has an equivalent circuit seen by the ADC equals to R_{dcr} in Figure 93. Before deriving the transfer function between the inductor current and voltage seen by the ISL28025, let's review the definition of an inductor and capacitor in the Laplacian domain.

$$X_c(f) = \frac{1}{j\cdot\omega(f)\cdot C} \qquad X_L(f) = j\cdot\omega(f)\cdot L \qquad \text{(EQ. 22)}$$

X_C is the impedance of a capacitor related to the frequency and X_L is the impedance of an inductor related to frequency. ω equals to 2πf. f is the chop frequency dictated by the regulator. Using Ohm's law, the voltage across the DCR circuit in terms of the current flowing through the inductor is define in Equation 23.

$$V_{dcr}(f) = \left(R_{dcr} + j\cdot\omega(f)\cdot L\right)\cdot i_L \qquad \text{(EQ. 23)}$$

[1] In Equation 23, R_{dcr} is the parasitic resistance of the inductor. The voltage drop across the inductor (Lo) and the resistor (R_{dcr}) circuit is the same as the voltage drop across the resistor (R_{sen}) and the capacitor (C_{sen}) circuit. Equation 24 defines the voltage across the capacitor (V_{csen}) in terms of the inductor current (I_L).

$$V_c(f) = \frac{\left(j\cdot\omega(f)\cdot L + R_{dcr}\right)}{1 + j\cdot\omega(f)\cdot C_{sen}\cdot R_{sen}} = R_{dcr}\left[\frac{\left[1 + \frac{\left(j\cdot\omega(f)\cdot L\right)}{R_{dcr}}\right]}{1 + j\cdot\omega(f)\cdot C_{sen}\cdot R_{sen}}\right]\cdot i_L \qquad \text{(EQ. 24)}$$

The relationship between the inductor load current (I_L) and the voltage across capacitor simplifies if the following component selection holds true;

$$\frac{L}{R_{dcr}} = C_{sen}\cdot R_{sen} \qquad \text{(EQ. 25)}$$

If Equation 25 holds true, the numerator and denominator of the fraction in Equation 24 cancels out, reducing the voltage across the capacitor to the equation represented in Equation 26.

$$V_c = R_{dcr} \cdot i_L \quad \text{(EQ. 26)}$$

Most inductor datasheets will specify the average value of the R_{dcr} for the inductor. R_{dcr} values are usually below 1mΩ with a tolerance averaging 8%. Common chip capacitor tolerances average to 10%.

Inductors are constructed out of metal, which has a high temperature coefficient. The temperature drift of the inductor value could cause the DCR circuit to be untuned. An untuned circuit results in inaccurate current measurements along with a chop signal bleeding into the measurement. To counter the temperature variance, a temperature sensor may be incorporated into the design to track the change in component values.

A DCR circuit is good for gross current measurements. As discussed, inductors and capacitors have high tolerances and are temperature dependent, which will result in less than accurate current measurements.

In Figure 93, there is a resistor in series with the ISL28025 negative shunt terminal, VINM, with the value of R_{sen} + R_{dcr}. The resistor's purpose is to counter the effects of the bias current from creating a voltage offset at the input of the ADC.

Revision History

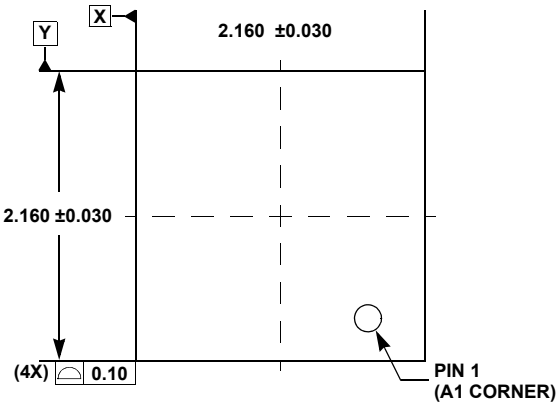
The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Pease visit the website to ensure you have the latest version.

DATE	REVISION	CHANGE
Dec 1, 2022	6.03	Updated Table 6 by fixing the bit name from D4 to D11.
Oct 27, 2022	6.02	Updated Table 2 by fixing the descriptions for READ_PEAK_MIN_IOUT and READ_PEAK_MAX_IOUT.
Feb 22, 2022	6.01	Removed Related Literature section. Updated links throughout. Updated Ordering Information Table formatting. Updated the DEVICE ID value to 0849534C3238303235 in Table 2.
Feb 27, 2018	6.00	Ordering Information table, corrected note references for ISL28025FR12Z-T and ISL28025FR12Z-T7A. Removed About Intersil section. Updated disclaimer.
Nov 9, 2017	5.00	Added ISL28025FR12Z, 20 lead QFN Quad Flat No-Lead Plastic Package 12V version. Updated the Related Literature section on page 1. Added Note 4 to the Ordering Information table. Added ISL28025FR12 to the VBUS entry in the Absolute Maximum Ratings table.
Feb 19, 2016	4.00	Changed the Polarity of the CNVR bit from HIGH to LOW when the ADC is making a conversion. See "CNVR: Conversion Ready D[1]" on page 28. Updated "Ordering Information" table on page 3 by adding Tape and Reel option column. Figure 73 on page 40, removed 0s from Address Byte and changed last "ACK" to "NACK". Figure 74 on page 41 added "NACK" before "STOP" Figure 76 on page 42, changed "signals from the ISL28025" to "signals to the ISL28025" added "NACK" to the diagram before the repeat start and changed last "ACK" to "NACK".
Jun 17, 2015	3.00	Added Related Literature section on page 1. Added DPM Portfolio Comparison table on page 5. Removed Typical Applications section (which included Figure 102) and made into an appnote (AN1955).
Feb 17, 2015	2.00	Changed Reference of ZL9050 in Figure 102 on page 51 to ISL8272M.
Oct 24,2014	1.00	"Vbus_OV_OT_Set D[5:0]" on page 31, changed step size from "1.95°" to "5.71°C" and added "The mathematical range is -144°C to +221.4.°C". Updated Table 23 on page 31 by adding column OT THRESHOLD VALUE. Changed title of Table 29 on page 32 from "Vbus_OV_OT_Set BITS DEFINED" to "Vshunt_OC_Set BITS DEFINED".
Jun 30, 2014	0.00	Initial release

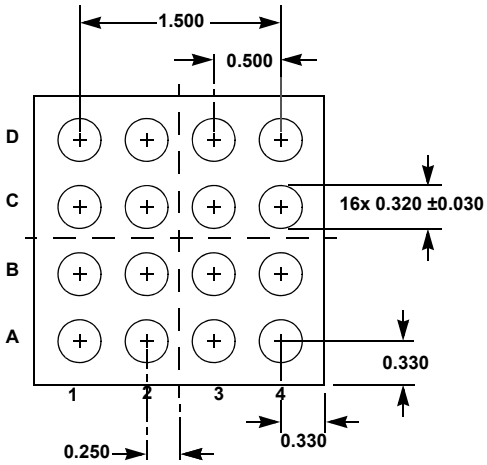
Package Outline Drawings

For the most recent package outline drawing, see W4x4.16C

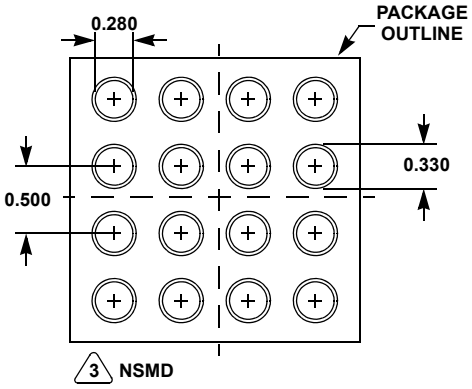
W4x4.16C
(WLCSP 0.5mm PITCH) WAFER LEVEL CHIP SCALE PACKAGE
Rev 1, 05/14



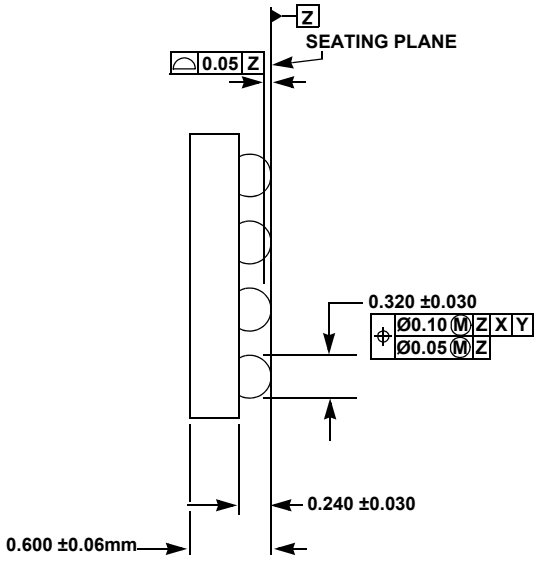
TOP VIEW



BOTTOM VIEW



RECOMMENDED LAND PATTERN



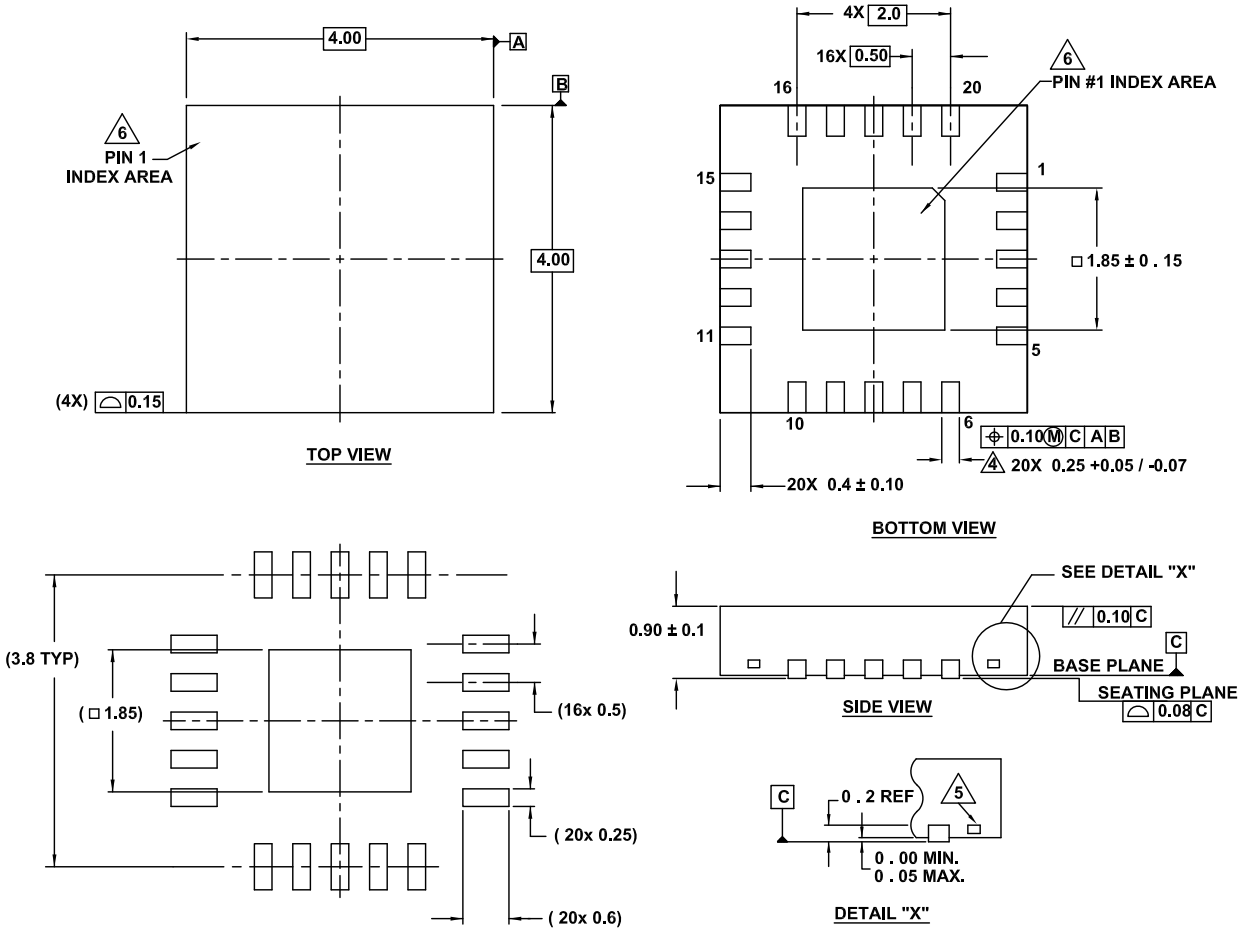
SIDE VIEW

NOTES:

1. All dimensions are in millimeters.
2. Dimension and tolerance per ASMEY 14.5M-1994, and JESD 95-1 SPP-010.
3. NSMD refers to non-solder mask defined pad design per Intersil Techbrief TB451.

For the most recent package outline drawing, see L20.4x4J

L20.4x4J
20 Lead Quad Flat No-Lead Plastic Package
Rev 0, 9/16



NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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