ISL22512

Single Push Button Controlled Potentiometer (XDCP™) Low Noise, Low Power, 16 Taps, Push Button Controlled Potentiometer

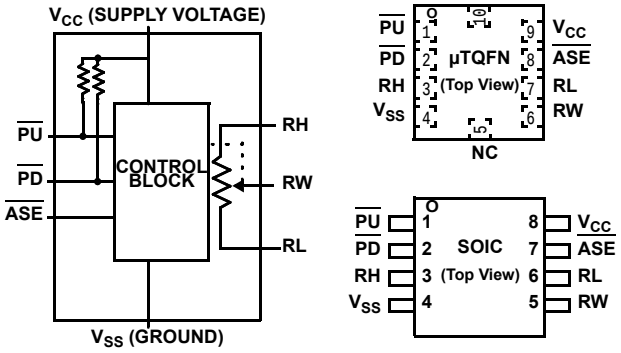
FN6679
Rev 3.00
October 12, 2015

The Intersil ISL22512 is a three-terminal digitally-controlled potentiometer (XDCP) implemented by a resistor array composed of 15 resistive elements and a wiper switching network. The ISL22512 features a push button control, a shutdown mode, as well as an industry-leading µTQFN package.

The push button control has individual $\overline{PU}$ and $\overline{PD}$ inputs for adjusting the wiper. To eliminate redundancy, the wiper position will automatically increment or decrement if one of these inputs is held longer than one second.

Forcing both $\overline{PU}$ and $\overline{PD}$ low for more than two seconds activates shutdown mode. Shutdown mode disconnects the top of the resistor chain and moves the wiper to the lowest position, minimizing power consumption.

The three terminals accessing the resistor chain naturally configure the ISL22512 as a voltage divider. A rheostat is easily formed by floating an end terminal or connecting it to the wiper.



Features

- Solid-State Non-Volatile Potentiometer
- Push Button Controlled
- Single or Auto Increment/Decrement
  - Fast Mode after 1s Button Press
- AUTOSTORE of Last Wiper Position or Manual Store of Wiper Position
- Shutdown Mode
- 16 Wiper Tap Points
  - Middle Scale Wiper Position on Power-Up
- Low Power CMOS
  - V_{CC} = 2.7V to 5.5V
  - Terminal Voltage, 0 to V_{CC}
  - Standby Current, 3µA max
- R_{TOTAL} Value = 10kΩ
- High Reliability
  - Endurance: 1,000,000 data changes per bit per register
  - Register data retention: 50 years @ T ≤ +55°C
- Packages
  - 8 Ld SOIC
  - 10 Ld µTQFN (2.1mmx1.6mm)
- Pb-Free (RoHS Compliant)

Applications

- Volume Control
- LED/LCD Brightness Control
- Contrast Control
- Programming Bias Voltages
- Ladder Networks

Ordering Information

PART NUMBER	PART MARKING	R_{TOTAL} (kΩ)	TEMP. RANGE(°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL22512WFB8Z* (Note 1)	22512 WFBZ	10	-40 to +125	8 Ld SOIC	M8.15
ISL22512WFRU10Z-TK (Note 2) **(No longer available, recommended replacement: ISL22512WFB8Z-TK)**	GE	10	-40 to +125	10 Ld µTQFN Tape and Reel	L10.2.1x1.6A

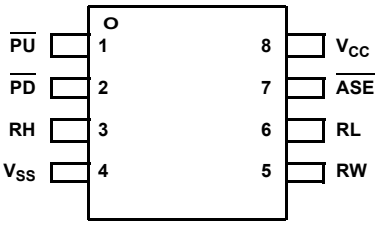
*Add "-TK" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE:

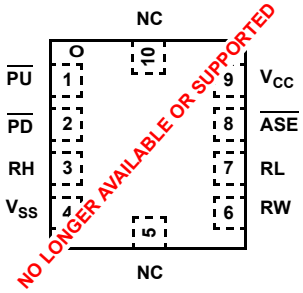
1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinouts

ISL22512
(8 LD SOIC)
TOP VIEW



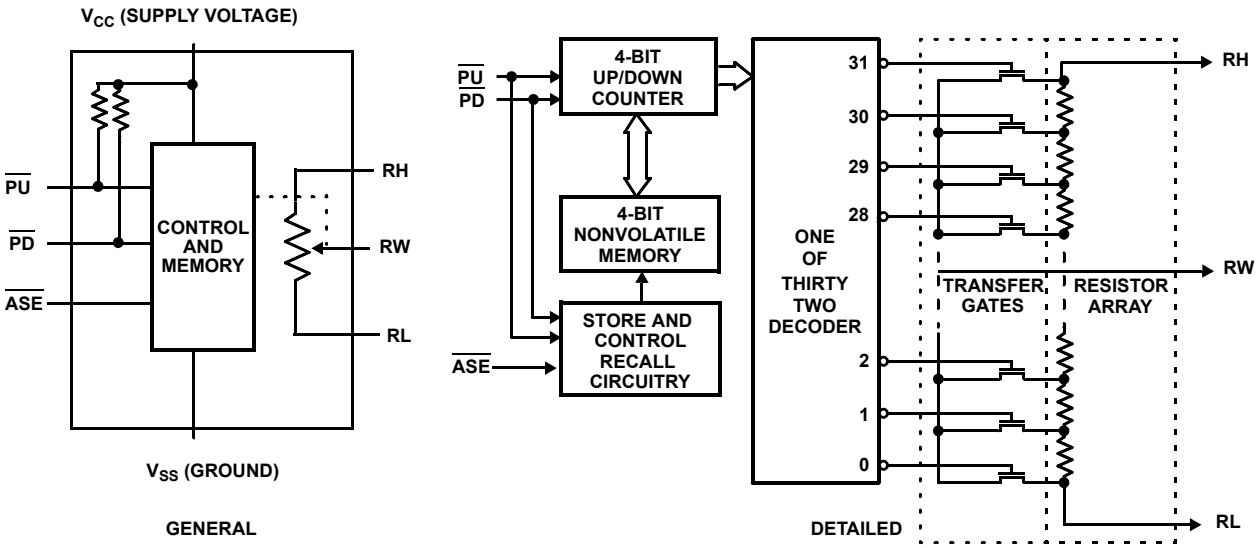
ISL22512
(10 LD MTQFN)
TOP VIEW



Pin Descriptions

SOIC PIN	µTQFN PIN	SYMBOL	BRIEF DESCRIPTION
1	1	$\overline{PU}$	The $\overline{PU}$ is a falling-edge triggered input with internal pull-up. Toggling $\overline{PU}$ will move the wiper close to RH terminal.
2	2	$\overline{PD}$	The $\overline{PD}$ is a falling-edge triggered input with internal pull-up. Toggling $\overline{PD}$ will move the wiper close to RL terminal.
3	3	RH	The RH and RL pins of the ISL22512 are equivalent to the fixed terminals of a mechanical potentiometer. The minimum voltage is V_{SS} and the maximum is V_{CC}. The terminology of RH and RL references the relative position of the terminal in relation to wiper movement direction selected by the $\overline{PU}$/$\overline{PD}$ input.
4	4	V_{SS}	Ground
5	6	RW	The RW pin is the wiper terminal of the potentiometer which is equivalent to the movable terminal of a mechanical potentiometer.
6	7	RL	The RH and RL pins of the ISL22512 are equivalent to the fixed terminals of a mechanical potentiometer. The minimum voltage is V_{SS} and the maximum is V_{CC}. The terminology of RH and RL references the relative position of the terminal in relation to wiper movement direction selected by the $\overline{PU}$/$\overline{PD}$ input.
7	8	$\overline{ASE}$	Active low AUTOSTORE enable input or Manual Store active low input
8	9	V_{CC}	Supply Voltage
	5, 10	NC	No connection

Block Diagrams



Absolute Maximum Ratings

Storage temperature . . . . . -65°C to +150°C
Voltage at $\overline{PU}$ and $\overline{PD}$ Pin with Respect to GND . -0.3V to V_{CC} + 0.3
V_{CC} . . . . . -0.3V to +6V
Voltage at any DCP Pin with Respect to GND. . . . . -0.3V to V_{CC}
I_W (10s) . . . . . ±6mA
Latchup . . . . . Class II, Level A @ +125°C
ESD Rating
Human Body Model 4kV
Machine Model. 300V

Thermal Information

Thermal Resistance (Typical, Notes 3, 4)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Lead µTQFN (Notes 3, 4)	150	48.3
8 Lead SOIC (Note 3)	125	N/A

Maximum Junction Temperature (Plastic Package). . . . . +150°C
Pb-free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Temperature Range (Extended Industrial). . . . . -40°C to +125°C
V_{CC} . . . . . 2.7V to 5.5V
Power Rating 15mW
Wiper Current . . . . . ±3.0mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
4. θ_{JC} is for the location in the center of the exposed metal pad on the package underside.

Potentiometer Specifications

Over recommended operating conditions, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 18)	TYP (Note 5)	MAX (Note 18)	UNIT
R_{TOTAL}	RH to RL Resistance			10		kΩ
	RH to RL Resistance Tolerance		-20		+20	%
	End-to-End Temperature Coefficient			±80		ppm/°C (Note 16)
R_W	Wiper Resistance	V_{CC} = 3.3V, wiper current $I_{RW} = V_{CC}/R_{TOTAL}$		130	400	Ω
V_{RH}, V_{RL}	V_{RH} and V_{RL} Terminal Voltages	V_{RH} and V_{RL} to GND	0		V_{CC}	V
	Noise on Wiper Terminal	From 0Hz to 10MHz		-80		dBV
$C_H/C_L/C_W$ (Note 17)	Potentiometer Capacitance			10/10/25		pF
I_{LkgDCP}	Leakage on DCP Pins	Voltage at pin from GND to V_{CC}		0.05	0.4	µA
VOLTAGE DIVIDER MODE (0V @ R_L; V_{CC} @ RH; measured at RW unloaded)						
INL (Note 10)	Integral Non-Linearity		-1		1	LSB (Note 6)
DNL (Note 9)	Differential Non-Linearity	Monotonic over all tap positions	-0.5		0.5	LSB (Note 6)
ZSerror (Note 7)	Zero-scale Error		0	0.1	2	LSB (Note 6)
FSerror (Note 8)	Full-scale Error		-2	-0.1	0	LSB (Note 6)
TC_V (Note 11)	Ratiometric Temperature Coefficient	Wiper from 5 hex to 1F hex		±25		ppm/°C
f_{CUTOFF}	3dB Cut-Off Frequency	Wiper at the middle scale		500		kHz
RESISTOR MODE (Measurements between RW and RL with RH not connected, or between RW and RH with RL not connected)						
RINL (Note 15)	Integral Non-Linearity	DCP register set between 1 hex and 1F hex; monotonic over all tap positions	-1.5		1.5	MI (Note 12)
RDNL (Note 14)	Differential Non-Linearity		-0.5		0.5	MI (Note 12)
Roffset (Note 13)	Offset		0	1	2	MI (Note 12)

DC Electrical Specifications Over recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 18)	TYP (Note 5)	MAX (Note 18)	UNIT
I_{CC}	V_{CC} Active Current	V_{CC} = 5.5V, perform wiper move operation			150	µA
I_{CC}	V_{CC} Current During Store Operation	V_{CC} = 5.5V, perform non-volatile store operation			2	mA
I_{SB}	Standby Current			0.6	3	µA
I_{Lkg}	$\overline{PU}$, $\overline{PD}$ Input Leakage Current	V_{IN} = V_{SS} to V_{CC}	-2		+2	µA
V_{IH}	$\overline{PU}$, $\overline{PD}$ Input HIGH Voltage		V_{CC} x 0.7			V
V_{IL}	$\overline{PU}$, $\overline{PD}$ input LOW Voltage				V_{CC} x 0.1	V
C_{IN} (Note 17)	$\overline{PU}$, $\overline{PD}$ Input Capacitance	V_{CC} = 3.3V, T_A = +25°C, f = 1MHz		10		pF
Rpull_up (Note 17)	Pull-Up Resistor for $\overline{PU}$ and $\overline{PD}$			1		MΩ
EEPROM SPECIFICATIONS						
	EEPROM Endurance		1,000,000			Cycles
	EEPROM Retention	Temperature ≤ +55°C	50			Years

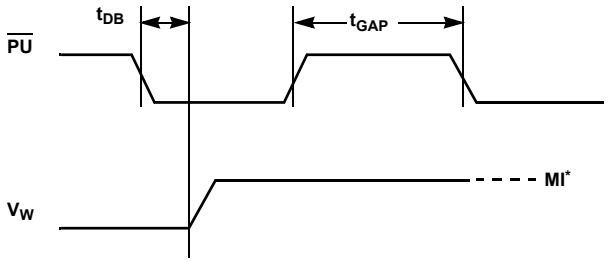
AC Electrical Specifications Over recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	MIN (Note 18)	TYP (Note 5)	MAX (Note 18)	UNIT
t_{GAP}	Time Between Two Separate Push Button Events	2			ms
t_{DB}	Debounce Time		15	28	ms
$t_{S\ SLOW}$	Wiper Change on a Slow Mode	100	250	390	ms
$t_{S\ FAST}$	Wiper Change on a Fast Mode	25	50	78	ms
t_{stdn} (Note 17)	Time to Enter Shutdown Mode (keep $\overline{PU}$ and $\overline{PD}$ LOW)		2		s
t_{PU}	Power-Up to Wiper Stable			500	µs
t_R VCC	V_{CC} Power-Up Rate	0.2		50	V/ms

NOTES:

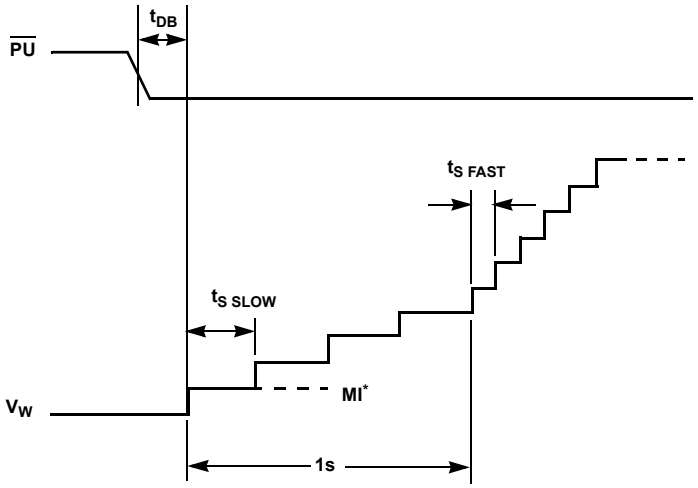
5. Typical values are for T_A = +25°C and 3.3V supply voltage.
6. LSB: $[V(RW)_{15} – V(RW)_0]/15$. $V(RW)_{31}$ and $V(RW)_0$ are voltage on RW pin for the DCP register set to 0F hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
7. ZS error = $V(RW)_0$/LSB.
8. FS error = $[V(RW)_{31} – V_{CC}]$/LSB.
9. DNL = $[V(RW)_i – V(RW)_{i-1}]$/LSB -1, for i = 1 to 15; i is the DCP register setting.
10. INL = $[V(RW)_i – i • LSB – V(RW)]$/LSB for i = 1 to 15
11. $TC_V = \frac{Max(V(RW)_i) - Min(V(RW)_i)}{[Max(V(RW)_i) + Min(V(RW)_i)]/2} \times \frac{10^6}{+165°C}$ for i = 5 to 15 decimal, T = -40°C to +125°C. Max( ) is the maximum value of the wiper voltage and Min ( ) is the minimum value of the wiper voltage over the temperature range.
12. MI = $|RW_{15} – RW_0|$/15. MI is a minimum increment. RW_{15} and RW_0 are the measured resistances for the DCP register set to 1F hex and 00 hex respectively.
13. Roffset = RW_0/MI, when measuring between RW and RL.
    Roffset = RW_{15}/MI, when measuring between RW and RH.
14. RDNL = $(RW_i – RW_{i-1})$/MI, for i = 1 to 15.
15. RINL = $[RW_i – (MI • i) – RW_0]$/MI, for i = 1 to 15.
16. $TC_R = \frac{[Max(Ri) - Min(Ri)]}{[Max(Ri) + Min(Ri)]/2} \times \frac{10^6}{+165°C}$ for i = 5 to 15, T = -40°C to +125°C. Max( ) is the maximum value of the resistance and Min ( ) is the minimum value of the resistance over the temperature range.
17. Limits should be considered typical and are not production tested.
18. Parts are 100% tested at +25°C. Temperature limits established by characterization and are not production tested.

Slow Mode Timing



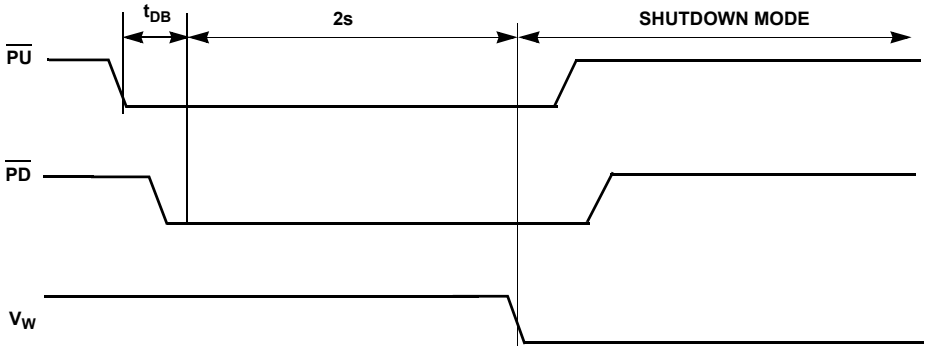
*MI in the AC timing diagram refers to the minimum incremental change in the wiper voltage.

Fast Mode Timing

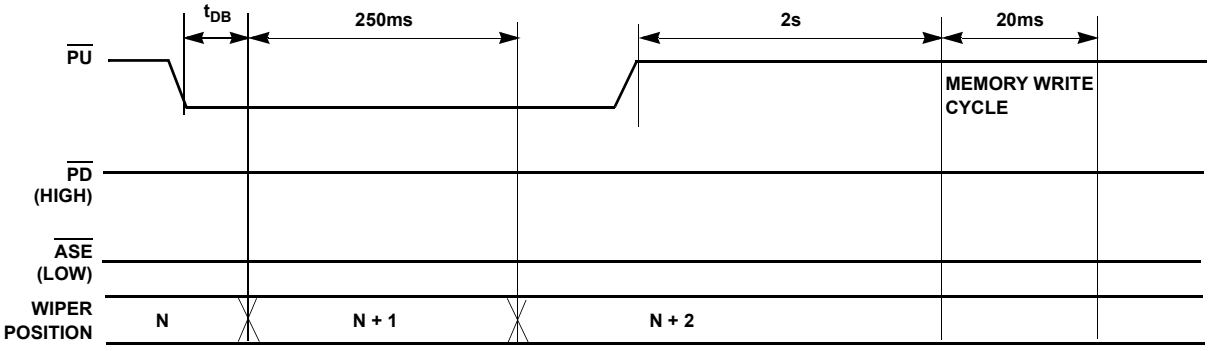


*MI in the AC timing diagram refers to the minimum incremental change in the wiper voltage.

Shutdown Mode Timing



AUTOSTORE Mode Timing



Typical Performance Curves

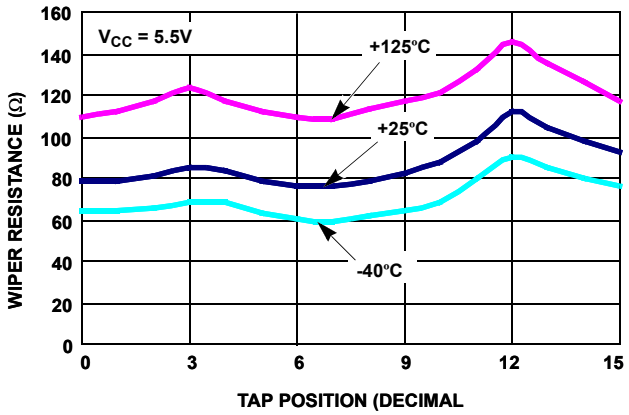


FIGURE 1. WIPER RESISTANCE vs TAP POSITION [I(RW) = V_{CC}/R_{TOTAL}] FOR 10kΩ (W)

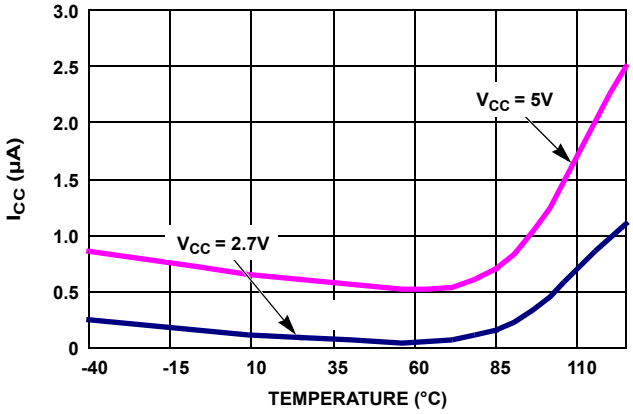


FIGURE 2. STANDBY I_{CC} vs TEMPERATURE

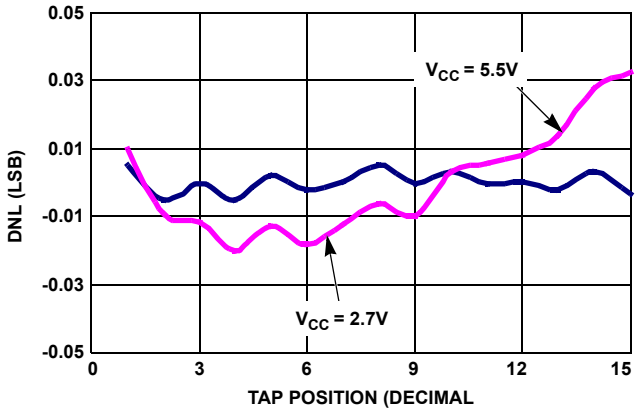


FIGURE 3. DNL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

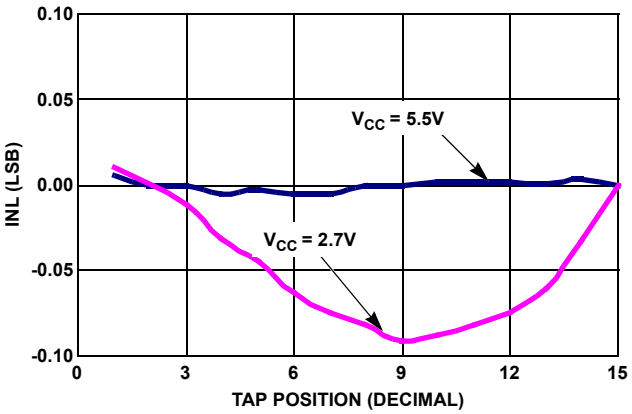


FIGURE 4. INL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

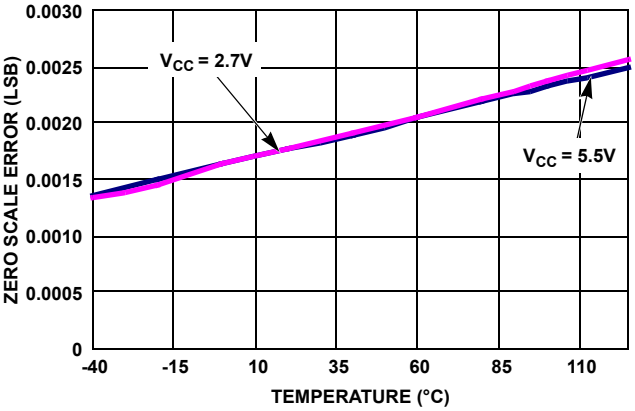


FIGURE 5. ZS ERROR vs TEMPERATURE

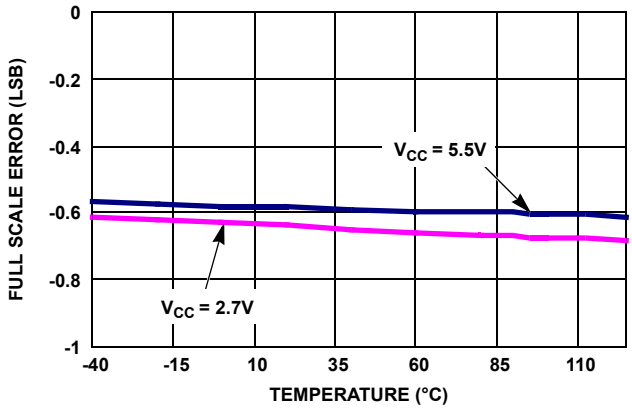


FIGURE 6. FS ERROR vs TEMPERATURE

Typical Performance Curves (Continued)

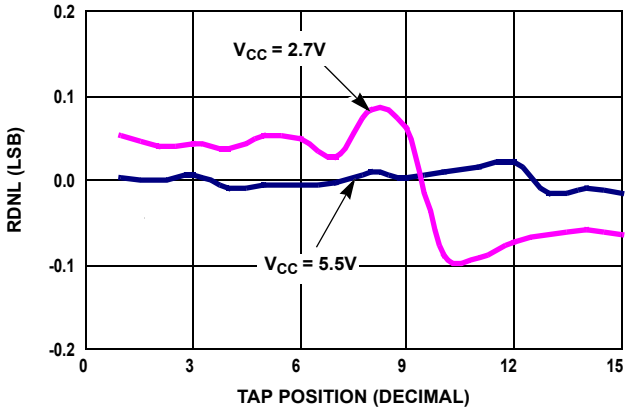


FIGURE 7. DNL vs TAP POSITION IN RHEOSTAT MODE FOR 10kΩ (W)

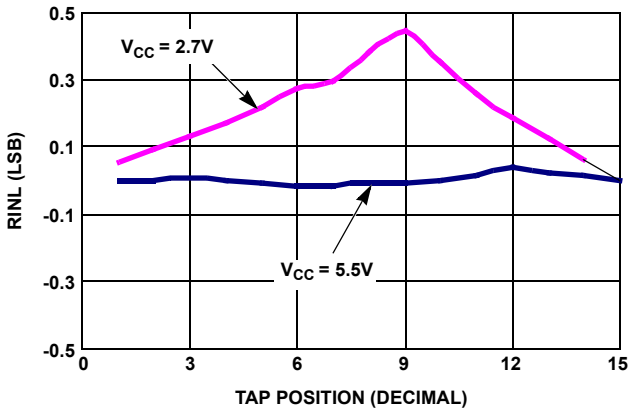


FIGURE 8. INL vs TAP POSITION IN RHEOSTAT MODE FOR 10kΩ (W)

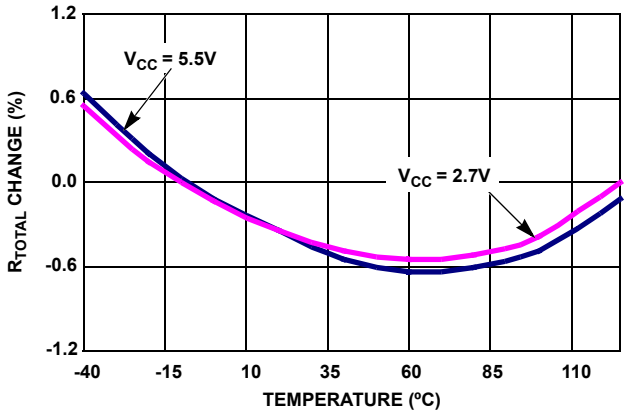


FIGURE 9. END TO END R_{TOTAL} % CHANGE vs TEMPERATURE

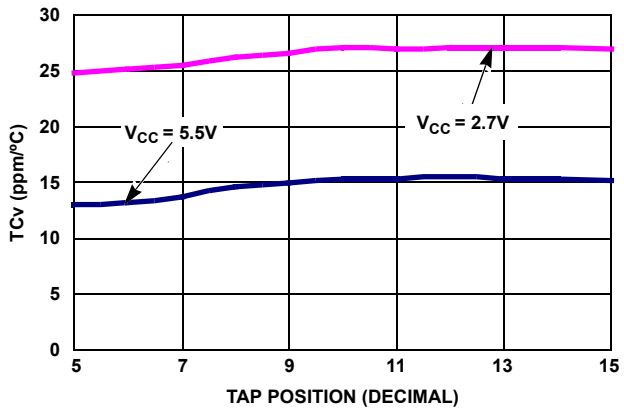


FIGURE 10. TC FOR VOLTAGE DIVIDER MODE IN ppm

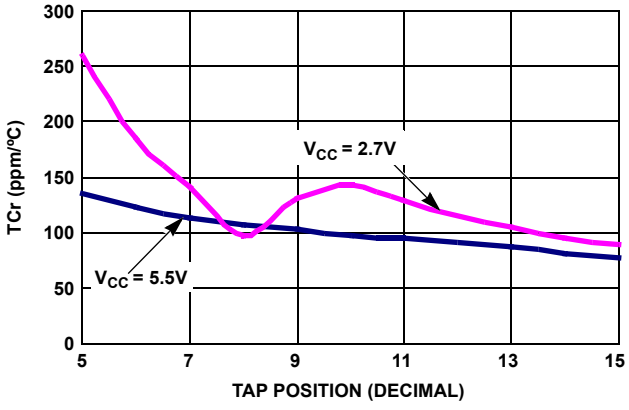


FIGURE 11. TC FOR RHEOSTAT MODE IN ppm

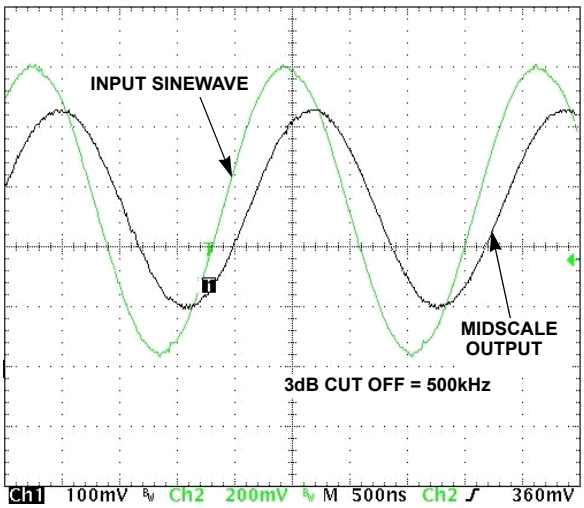


FIGURE 12. FREQUENCY RESPONSE (500kHz)

Power-Up and Down Requirements

There are no restrictions on the power-up or power-down conditions of V_{CC} and the voltages applied to the potentiometer pins provided that V_{CC} is always more positive than or equal to V_{RH} and V_{RL}, i.e., $V_{CC} \geq V_{RH}, V_{RL}$. The V_{CC} ramp rate specification is always in effect.

Pin Descriptions

RH and RL

The RH and RL pins of the ISL22512 are equivalent to the fixed terminals of a mechanical potentiometer. The minimum voltage is V_{SS} and the maximum is V_{CC}. The terminology of RH and RL references the relative position of the terminal in relation to wiper movement direction.

RW

The RW pin is the wiper terminal of the potentiometer which is equivalent to the movable terminal of a mechanical potentiometer.

$\overline{PU}$

The debounced $\overline{PU}$ input is used to increment the wiper position. An on-chip pull-up holds the $\overline{PU}$ input HIGH. A switch closure to ground or a LOW logic level will, after a debounce time, move the wiper to the next adjacent higher tap position.

$\overline{PD}$

The debounced $\overline{PD}$ input is used to decrement the wiper position. An on-chip pull-up holds the $\overline{PD}$ input HIGH. A switch closure to ground or a LOW logic level will, after a debounce time, move the wiper to the next adjacent lower tap position.

$\overline{ASE}$

The debounced $\overline{ASE}$ (AUTOSTORE enable) pin can be in one of two states:

1. AUTOSTORE is enabled if $\overline{ASE}$ is held LOW during power-up.
2. AUTOSTORE is disabled if $\overline{ASE}$ is held HIGH during power-up. A LOW to HIGH transition will initiate a manual store operation. This is for the user who wishes to connect a push button switch to this pin. For every valid push, the ISL22512 will store the current wiper position to the EEPROM.

Device Operation

There are three sections of the ISL22512: the input control, counter and decode section; the EEPROM memory; and the resistor array. The input control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch, connecting a point on the resistor array to the wiper output. Under the proper conditions, the contents of the counter can be stored in EEPROM memory and retained for future use. The resistor array is comprised of 15 individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The ISL22512 is designed to interface directly to two push button switches for effectively moving the wiper up or down. The $\overline{PU}$ and $\overline{PD}$ inputs increment or decrement a 4-bit counter respectively. The output of this counter is decoded to select one of the thirty-two wiper positions along the resistive array. The wiper increment input, $\overline{PU}$ and the wiper decrement input, $\overline{PD}$ are both connected to an internal pull-up so that they normally remain HIGH. When pulled LOW by an external push button switch or a logic LOW level input, the wiper will be switched to the next adjacent tap position.

Internal debounce circuitry prevents inadvertent switching of the wiper position if $\overline{PU}$ or $\overline{PD}$ remain LOW for less than 15ms, typical. Each of the buttons can be pushed either once for a single increment/decrement or continuously for a multiple increments/decrements. The number of increments/decrements of the wiper position depends on how long the button is being pushed. When making a continuous push, after the first second, the increment/decrement speed increases. For the first second, the device will be in the slow scan mode. Then, if the button is held for longer than 1 second, the device will go into the fast scan mode. As soon as the button is released, the ISL22512 will return to a standby condition.

If two or more buttons are pressed simultaneously, all commands are ignored upon release of ALL buttons, except Shutdown Mode condition.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

AUTOSTORE

The value of the counter is stored in EEPROM memory after 2 seconds of no activity on $\overline{PU}$ or $\overline{PD}$ inputs while $\overline{ASE}$ is enabled (held LOW). When power is restored, the content of the memory is recalled and the counter resets to the last value stored.

If AUTOSTORE is to be implemented, $\overline{ASE}$ is typically hard wired to V_{SS}. If $\overline{ASE}$ is held HIGH during power-up and then taken LOW, the wiper will not respond to the $\overline{PU}$ or $\overline{PD}$ inputs until $\overline{ASE}$ is brought HIGH and held HIGH.

Manual (Push Button) Store

When $\overline{ASE}$ is not enabled (held HIGH), a push button switch may be used to pull $\overline{ASE}$ LOW for more than 15ms and released to perform a manual store of the wiper position.

During memory write cycle all inputs will be ignored.

Shutdown Mode

The ISL22512 enters into Shutdown Mode if both $\overline{PU}$ and $\overline{PD}$ inputs are kept LOW for 2 seconds. In this mode, the resistors array is totally disconnected from its RH pin and the wiper is moved to position closest to RL pin, as shown in Figure 13. Note, that $\overline{PU}$ and $\overline{PD}$ inputs must be pulled LOW within t_{DB} time window of 15ms, see “Shutdown Mode Timing” on page 6. Otherwise all command will be ignored till both inputs will be released.

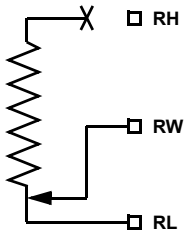


FIGURE 13. DCP CONNECTION IN SHUTDOWN MODE

Holding either $\overline{PU}$, $\overline{PD}$ or $\overline{ASE}$ input LOW for more than 15ms will exit shutdown mode and return wiper to prior shutdown position. If $\overline{PU}$ or $\overline{PD}$ will be held LOW for more than 250ms, the ISL22512 will start auto-increment or auto-decrement of wiper position.

R_{TOTAL} with V_{CC} Removed

The end- to-end resistance of the array will fluctuate once V_{CC} is removed.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
10/12/15	FN6679.3	Updated the Ordering Information Table on page 2. Added About Intersil section. Updated the Package Outline Drawing M8.15 to the latest revision. Changes are as follows: -Updated to new POD format by removing table and moving dimensions onto drawing and adding land pattern. -Changed in Typical Recommended Land Pattern the following: 2.41(0.095) to 2.20(0.087) 0.76 (0.030) to 0.60(0.023) 0.200 to 5.20(0.205) -Changed Note 1 “1982” to “1994”
07/06/09	FN6679.2	Added reliability information on page 1 under Features and EEPROM Specifications in DC Electrical Spec Table. Changed Tja for 8 LD SOIC from “120” to “125” Added Revision History
07/17/08	FN6679.1	1. Removed U option specs from table as there is no U option for this device. 2. Updated Pb-free note to new verbiage.
03/24/08	FN6679.0	Initial Release to web

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

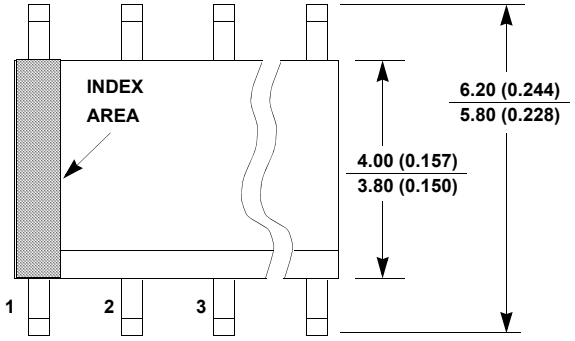
Reliability reports are also available from our website at www.intersil.com/support.

Package Outline Drawing

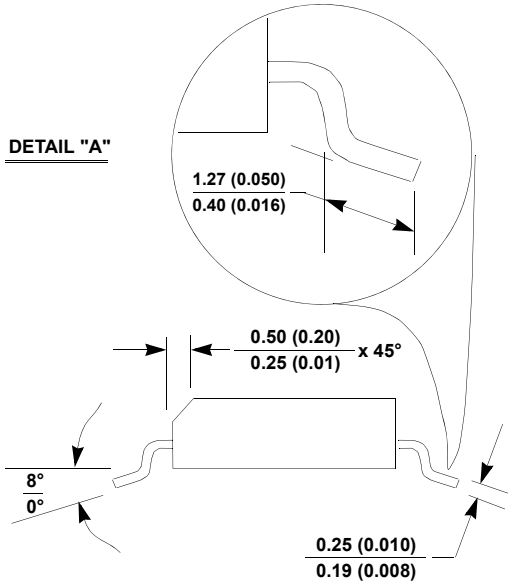
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

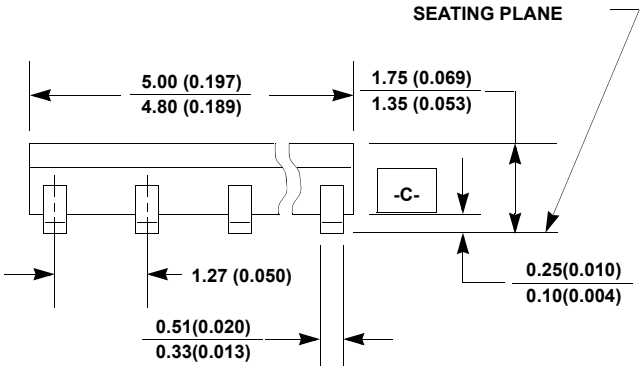
Rev 4, 1/12



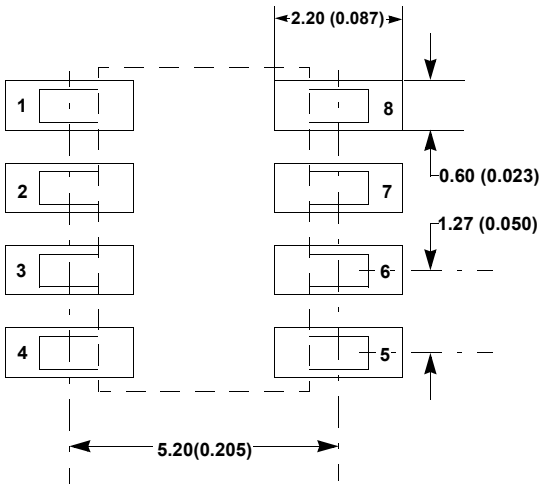
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"

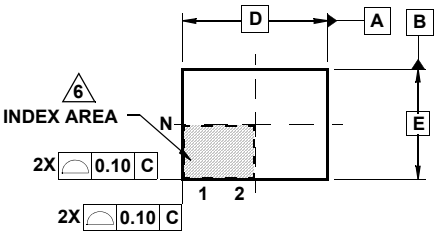


TYPICAL RECOMMENDED LAND PATTERN

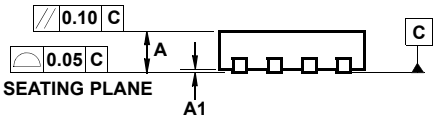
NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

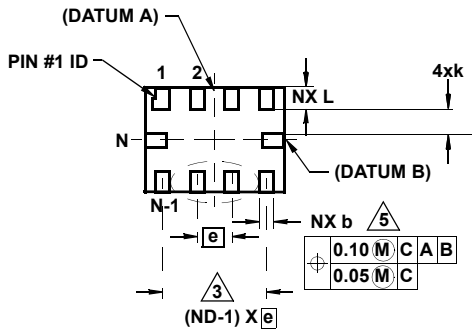
Ultra Thin Quad Flat No-Lead Plastic Package (UTQFN)



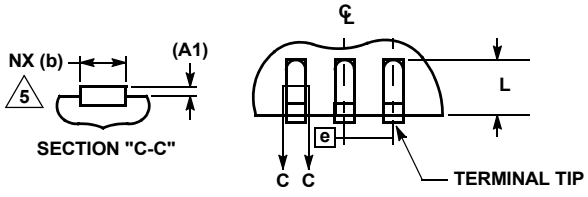
TOP VIEW



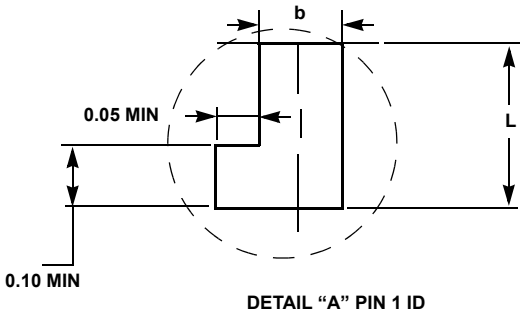
SIDE VIEW



BOTTOM VIEW



FOR ODD TERMINAL/SIDE



DETAIL “A” PIN 1 ID

L10.2.1x1.6A

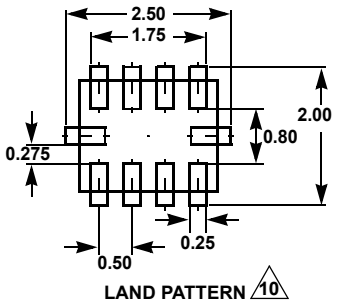
10 LEAD ULTRA THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.45	0.50	0.55	-
A1	-	-	0.05	-
A3		0.127 REF		-
b	0.15	0.20	0.25	5
D	2.05	2.10	2.15	-
E	1.55	1.60	1.65	-
e		0.50 BSC		-
k	0.20	-	-	-
L	0.35	0.40	0.45	-
N		10		2
Nd		4		3
Ne		1		3
θ	0	-	12	4

Rev. 3 6/06

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on D and E side, respectively.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Maximum package warpage is 0.05mm.
8. Maximum allowable burrs is 0.076mm in all directions.
9. Same as JEDEC MO-255UABD except:
   No lead-pull-back, "A" MIN dimension = 0.45 not 0.50mm
   "L" MAX dimension = 0.45 not 0.42mm.
10. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.



LAND PATTERN 10