ISL22326WM

Dual Digitally Controlled Potentiometers (XDCP™) Low Noise, Low Power, I^2C Bus, 128 Taps

FN6623
Rev 1.00
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The ISL22326WMVEP integrates two digitally controlled potentiometers (XDCP) and non-volatile memory on a monolithic CMOS integrated circuit.

The digitally controlled potentiometers are implemented with a combination of resistor elements and CMOS switches. The position of the wipers are controlled by the user through the I^2C bus interface. Each potentiometer has an associated volatile Wiper Register (WR) and a non-volatile Initial Value Register (IVR) that can be directly written to and read by the user. The contents of the WR controls the position of the wiper. At power-up, the device recalls the contents of the two DCP's IVR to the corresponding WRs.

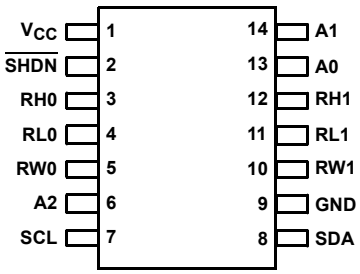
The DCPs can be used as three-terminal potentiometers or as two-terminal variable resistors in a wide variety of applications including control, parameter adjustments and signal processing.

Device Information

The specifications for an Enhanced Product (EP) device are defined in a Vendor Item Drawing (VID), which is controlled by the Defense Logistics Agency (DLA). "Hot-links" to the applicable VID and other supporting application information are provided on our website.

Pinout

ISL22326WMVEP
(14 LD TSSOP)
TOP VIEW



Features

- Specifications per DLA VID V62/08604-01XE
- Full Mil-Temp Electrical Performance from -55°C to +125°C
- Controlled Baseline with One Wafer Fabrication Site and One Assembly/Test Site
- Full Homogeneous Lot Processing in Wafer Fab
- No Combination of Wafer Fabrication Lots in Assembly
- Full Traceability Through Assembly and Test by Date/Trace Code Assignment
- Enhanced Process Change Notification
- Enhanced Obsolescence Management
- Eliminates Need for Up-Screening a COTS Component
- Two Potentiometers in One Package
- 128 Resistor Taps
- I^2C Serial Interface
  - Three Address Pins, Up To Eight Devices/Bus
- Non-volatile Storage of Wiper Position
- Wiper Resistance: 70Ω Typical @ 3.3V
- Shutdown Mode
- Shutdown Current 5µA Max
- Power Supply: 2.7V to 5.5V
- 10kΩ Total Resistance
- High Reliability
  - Endurance: 1,000,000 Data Changes Per Bit Per Register
  - Register Data Retention:
    - 10 years @ T ≤ +125°C
    - 15 years @ T ≤ +90°C
    - 50 years @ T ≤ +55°C
- 14 Ld TSSOP

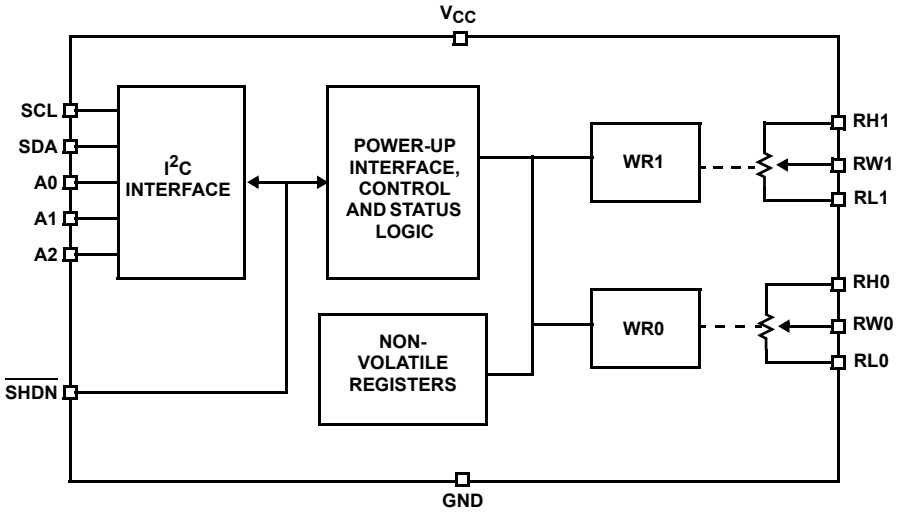
Ordering Information

VENDOR PART NUMBER (Notes 1, 2)	VENDOR ITEM DRAWING	PART MARKING	RESISTANCE OPTION (kΩ)	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL22326WMVEP	V62/08604-01XE	22326 WMVEP	10	-55 to +125	14 Ld TSSOP	M14.173

NOTES:

1. Add "-TK" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. Devices must be procured to the VENDOR PART NUMBER.

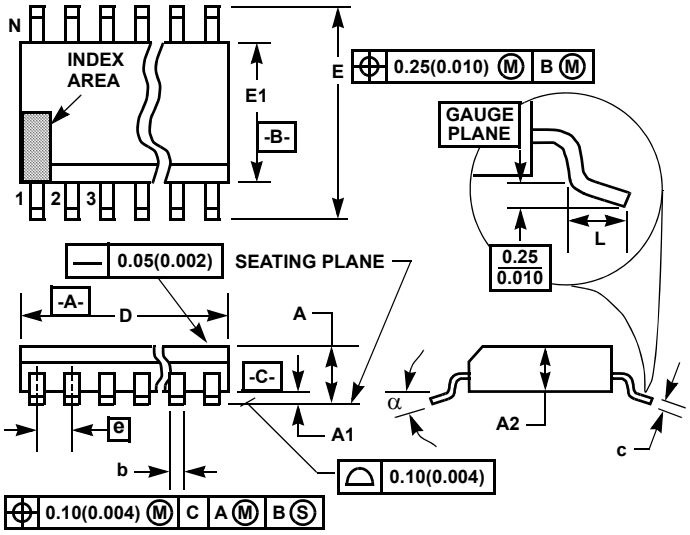
Block Diagram



Pin Descriptions

TSSOP PIN	SYMBOL	DESCRIPTION
1	V_{CC}	Power supply pin
2	$\overline{SHDN}$	Shutdown active low input
3	RH0	“High” terminal of DCP0
4	RL0	“Low” terminal of DCP0
5	RW0	“Wiper” terminal of DCP0
6	A2	Device address input for the I^2C interface
7	SCL	Open drain I^2C interface clock input
8	SDA	Open drain Serial data I/O for the I^2C interface
9	GND	Device ground pin
10	RW1	“Wiper” terminal of DCP1
11	RL1	“Low” terminal of DCP1
12	RH1	“High” terminal of DCP1
13	A0	Device address input for the I^2C interface
14	A1	Device address input for the I^2C interface

Thin Shrink Small Outline Plastic Packages (TSSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AC, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

M14.173

14 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.041	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.195	0.199	4.95	5.05	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	14		14		7
α	0°	8°	0°	8°	-

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