ISL21009MEP

High Voltage Input Precision, Low Noise FGA™ Voltage References

FN6744
Rev 0.00
December 15, 2008

The ISL21009MEP FGA™ voltage references are extremely low power, high precision, and low noise voltage references fabricated on Intersil's proprietary Floating Gate Analog technology. The ISL21009MEP features very low noise ($4.5\mu V_{P-P}$ for 0.1Hz to 10Hz), low operating current (180µA, Max), and 3ppm/°C of temperature drift. In addition, the ISL21009 family features guaranteed initial accuracy as low as ±0.5mV.

This combination of high initial accuracy, low power and low output noise performance of the ISL21009MEP enables versatile high performance control and data acquisition applications with low power consumption.

Device Information

The specifications for an Enhanced Product (EP) device are defined in a Vendor Item Drawing (VID), which is controlled by the Defense Supply Center in Columbus (DSCC). "Hot-links" to the applicable VID and other supporting application information are provided on our website.

Available Options

PART NUMBER	V_{OUT} OPTION (V)	INITIAL ACCURACY (mV)	TEMPCO. (ppm/°C)
ISL21009BMB825EP	2.500	±0.5	3
ISL21009CMB825EP	2.500	±1.0	5
ISL21009BMB841EP	4.096	±0.5	3
ISL21009BMB850EP	5.000	±0.5	3
ISL21009CMB850EP	5.000	±1.0	5

Features

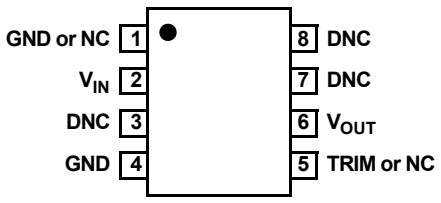
- Specifications per DSCC VID V62/08629
- Full Mil-Temp Electrical Performance from -55°C to +125°C
- Controlled Baseline with One Wafer Fabrication Site and One Assembly/Test Site
- Full Homogeneous Lot Processing in Wafer Fab
- No Combination of Wafer Fabrication Lots in Assembly
- Full Traceability Through Assembly and Test by Date/Trace Code Assignment
- Enhanced Process Change Notification
- Enhanced Obsolescence Management
- Eliminates Need for Up-Screening a COTS Component
- Output Voltages 2.500V, 4.096V, 5.000V
- Initial Accuracy . . . . . ±0.5mV, ±1.0mV
- Input Voltage Range. . . . . 3.5V to 16.5V
- Output Voltage Noise . . . . . $4.5\mu V_{P-P}$ (0.1Hz to 10Hz)
- Supply Current . . . . . 180µA (Max)
- Temperature Coefficient . . . . . 3ppm/°C, 5ppm/°C
- Output Current Capability. . . . . Up to ±7.0mA
- Operating Temperature Range. . . . . -55°C to +125°C
- Package . . . . . 8 Ld SOIC

Applications

- Defense/Commercial Avionics
- Radar/Sonar Systems
- Signal Processing Applications

Pinout

ISL21009MEP
(8 LD SOIC)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1	GND or NC	Can be either Ground or No Connect
2	V_{IN}	Power supply input connection
4	GND	Ground connection
5	TRIM	Allows user trim typically ±2.5%. Leave unconnected when unused.
6	V_{OUT}	Voltage reference output connection
3, 7, 8	DNC	Do Not Connect; Internal connection – must be left floating

Ordering Information

PART NUMBER (Note 1)	PART MARKING	V_{OUT} OPTION (V)	GRADE	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL21009BMB825EP	21009BM 25EP	2.500	±0.5mV, 3ppm/°C	-55 to +125	8 Ld SOIC	M8.15
ISL21009CMB825EP	21009CM 25EP	2.500	±1.0mV, 5ppm/°C	-55 to +125	8 Ld SOIC	M8.15
ISL21009BMB841EP	21009BM 41EP	4.096	±0.5mV, 3ppm/°C	-55 to +125	8 Ld SOIC	M8.15
ISL21009BMB850EP	21009BM 50EP	5.000	±0.5mV, 3ppm/°C	-55 to +125	8 Ld SOIC	M8.15
ISL21009CMB850EP	21009CM 50EP	5.000	±1.0mV, 5ppm/°C	-55 to +125	8 Ld SOIC	M8.15

NOTE:

1. Add “-TK” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

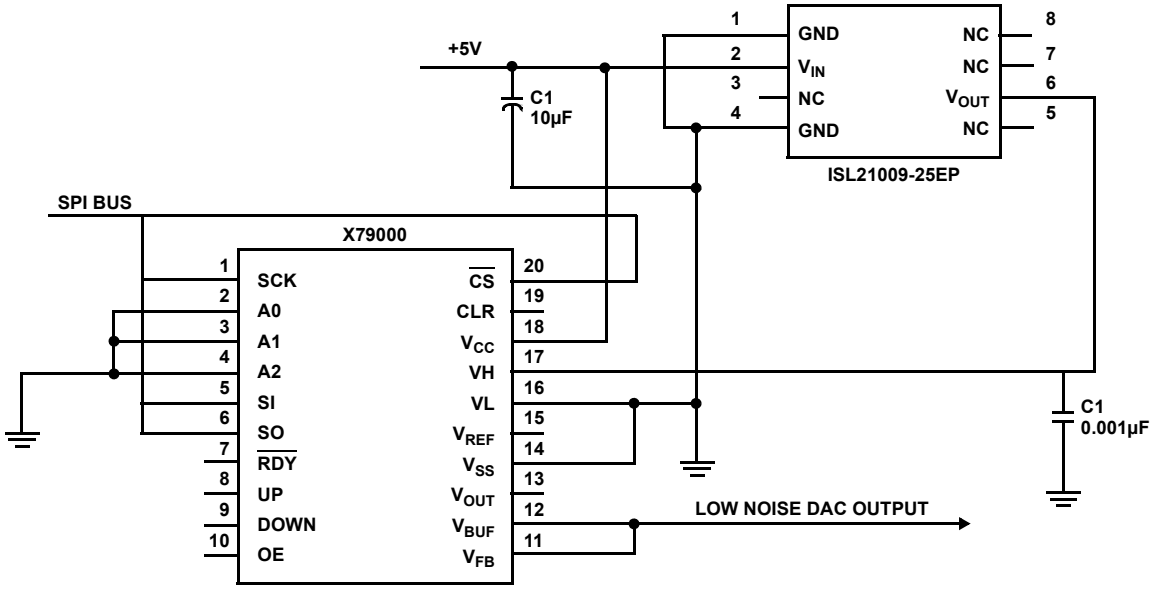


FIGURE 1. TYPICAL APPLICATION PRECISION 12-BIT SUB-RANGING DAC

Typical Performance Curves (ISL21009-25EP) (R_{EXT} = 100kΩ)

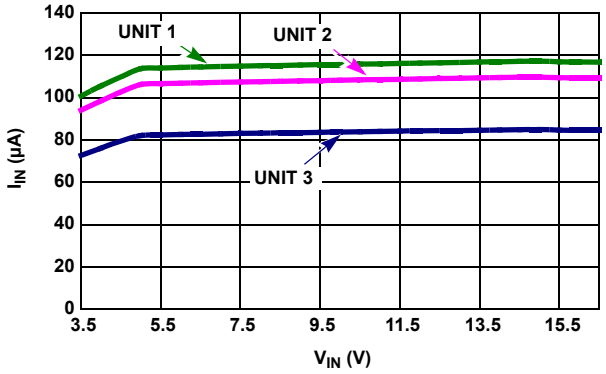


FIGURE 2. I_{IN} vs V_{IN}, 3 UNITS

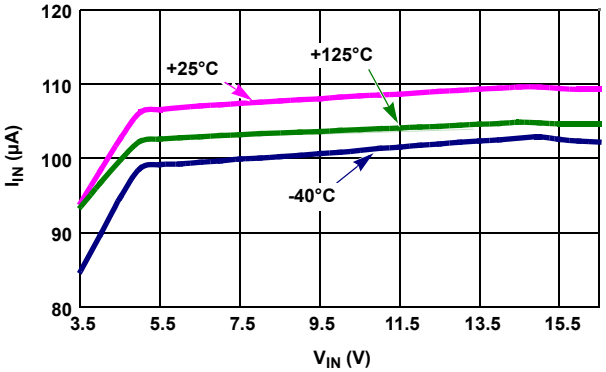


FIGURE 3. I_{IN} vs V_{IN}, 3 TEMPERATURES

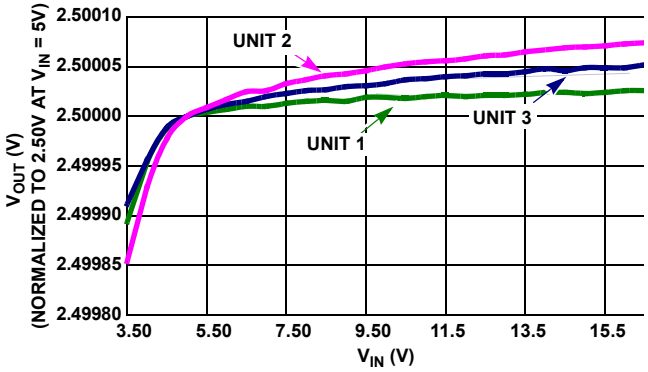


FIGURE 4. LINE REGULATION

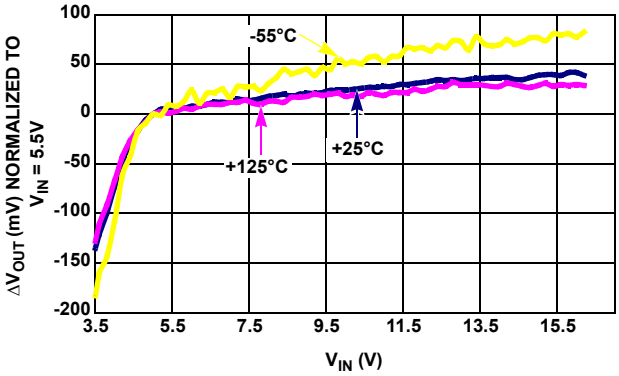


FIGURE 5. LINE REGULATION OVER-TEMPERATURE

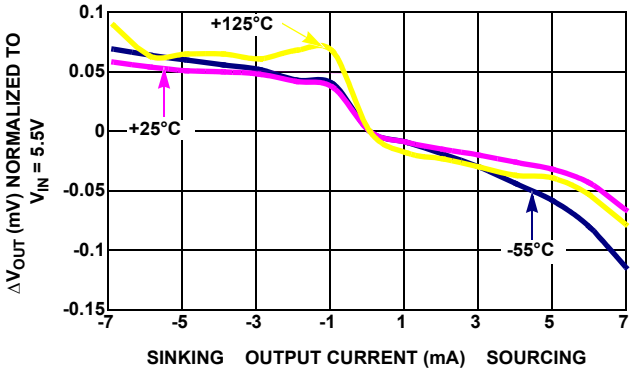


FIGURE 6. LOAD REGULATION

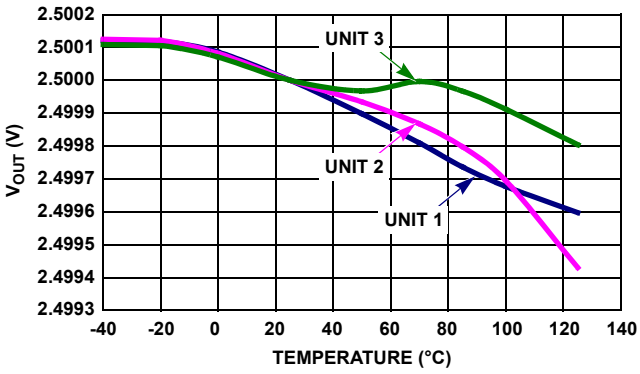


FIGURE 7. V_{OUT} vs TEMPERATURE

Typical Performance Curves (ISL21009-25EP) (R_{EXT} = 100kΩ) (Continued)

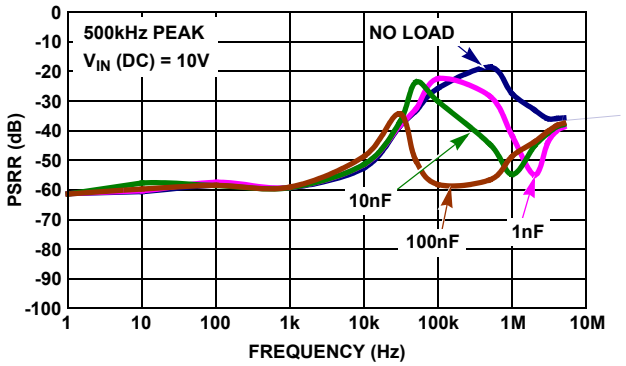


FIGURE 8. PSRR AT DIFFERENT CAPACITIVE LOADS

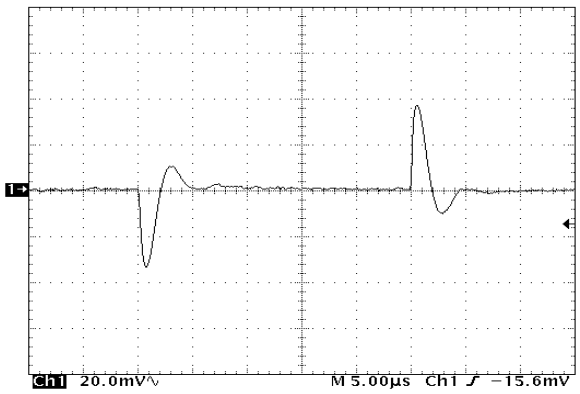


FIGURE 9. LINE TRANSIENT RESPONSE, NO CAPACITIVE LOAD

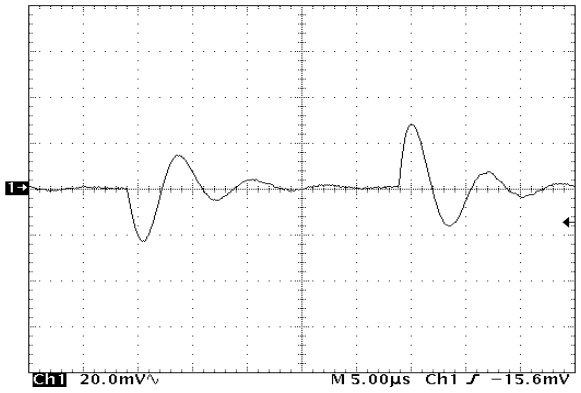


FIGURE 10. LINE TRANSIENT RESPONSE, 0.001µF LOAD CAPACITANCE

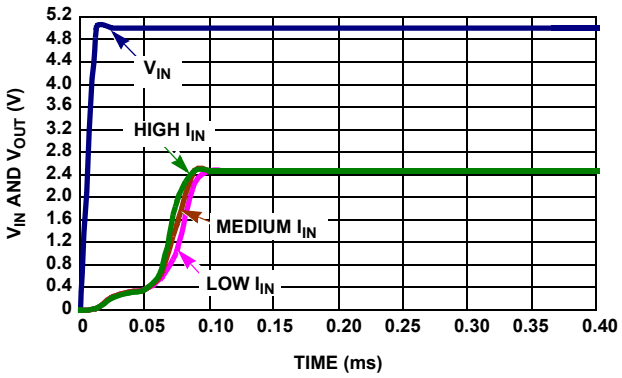


FIGURE 11. TURN-ON TIME

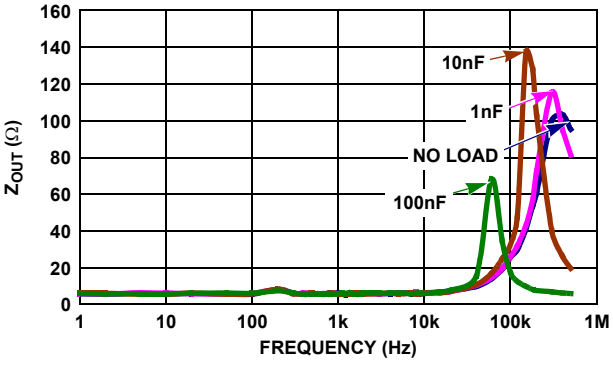


FIGURE 12. Z_{OUT} vs FREQUENCY

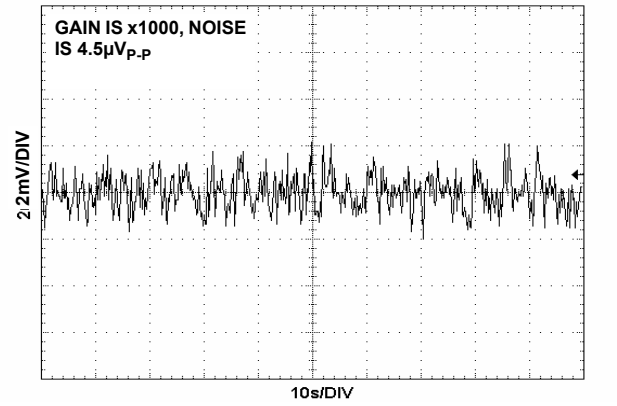


FIGURE 13. V_{OUT} NOISE, 0.1Hz TO 10Hz

Typical Performance Curves (ISL21009-25EP) *(R_{EXT} = 100kΩ)* (Continued)

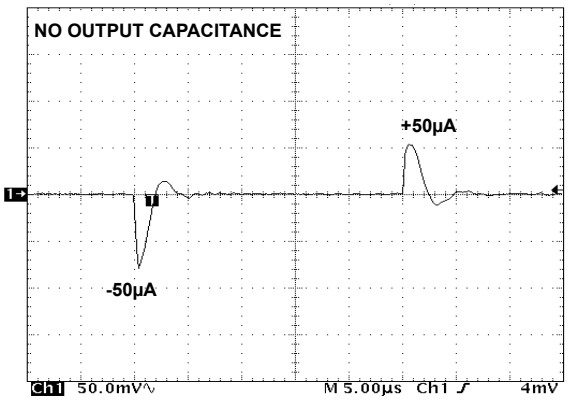


FIGURE 14. LOAD TRANSIENT RESPONSE

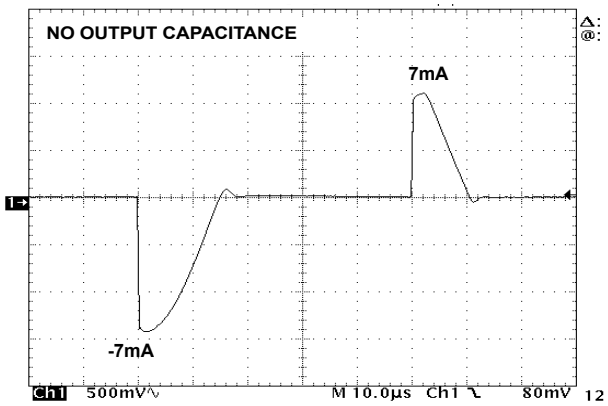


FIGURE 15. LOAD TRANSIENT RESPONSE

Typical Performance Curves (ISL21009-41EP) *(R_{EXT} = 100kΩ)*

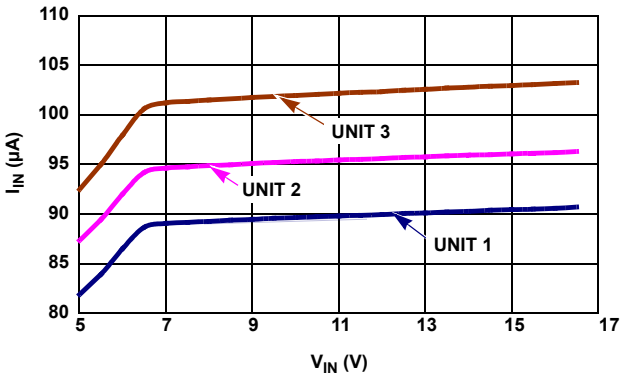


FIGURE 16. I_{IN} vs V_{IN}, 3 UNITS

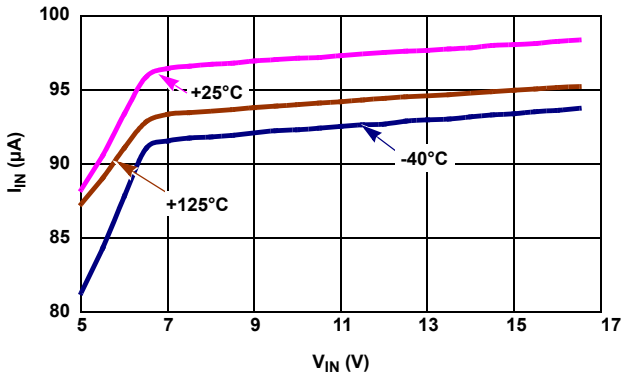


FIGURE 17. I_{IN} vs V_{IN}, 3 TEMPERATURES

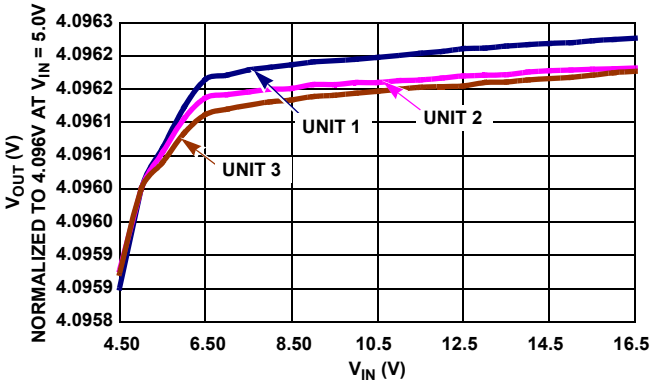


FIGURE 18. LINE REGULATION, 3 UNITS

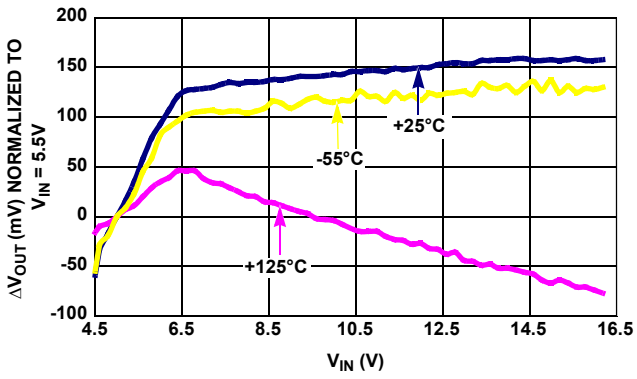


FIGURE 19. LINE REGULATION OVER-TEMPERATURE

Typical Performance Curves (ISL21009-41EP) (R_{EXT} = 100kΩ) (Continued)

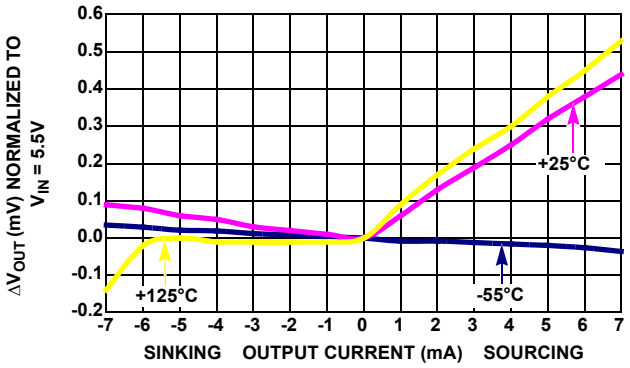


FIGURE 20. LOAD REGULATION

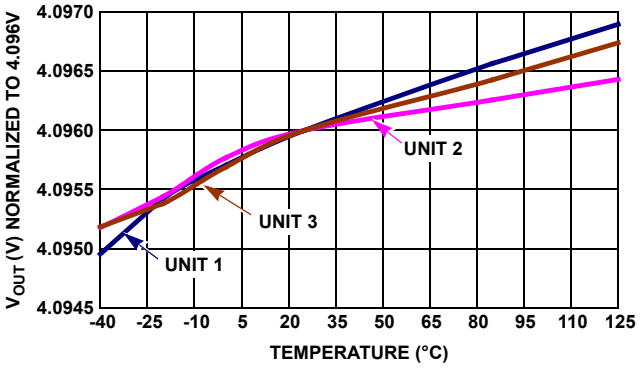


FIGURE 21. V_{OUT} vs TEMPERATURE

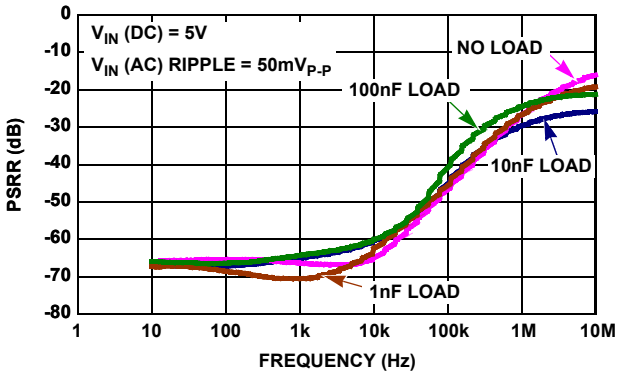


FIGURE 22. PSRR AT DIFFERENT CAPACITIVE LOADS

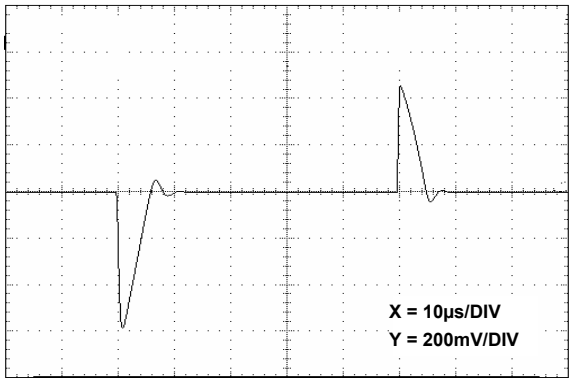


FIGURE 23. LINE TRANSIENT RESPONSE, NO CAPACITIVE LOAD

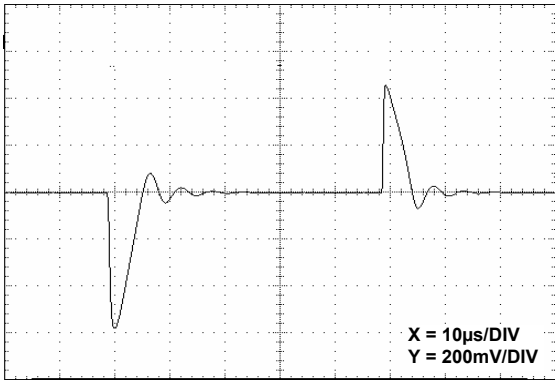


FIGURE 24. LINE TRANSIENT RESPONSE, 0.001µF LOAD CAPACITANCE

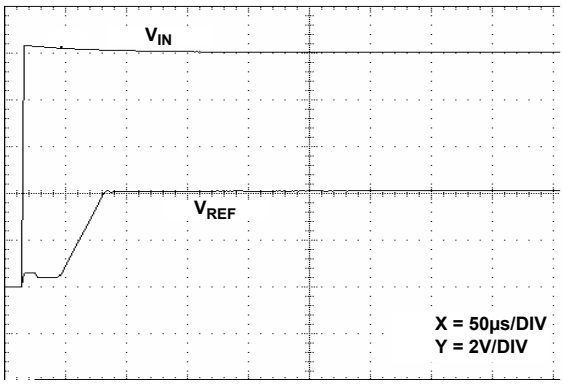


FIGURE 25. TURN-ON TIME

Typical Performance Curves (ISL21009-41EP) (R_{EXT} = 100kΩ) (Continued)

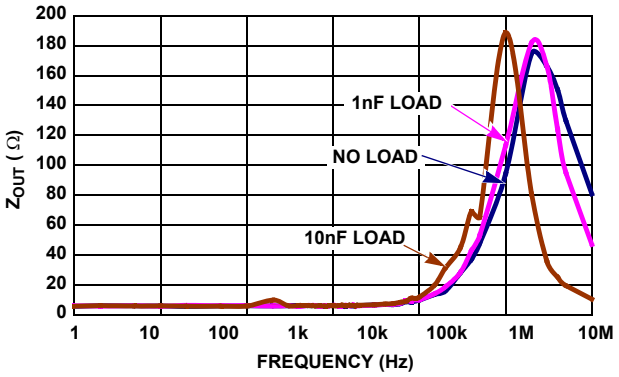


FIGURE 26. Z_{OUT} vs FREQUENCY

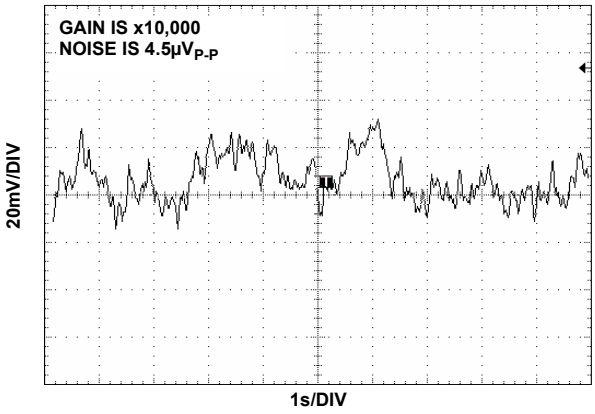


FIGURE 27. V_{OUT} NOISE, 0.1Hz TO 10Hz

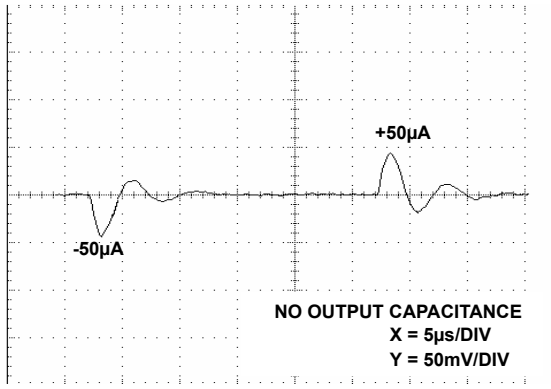


FIGURE 28. LOAD TRANSIENT RESPONSE

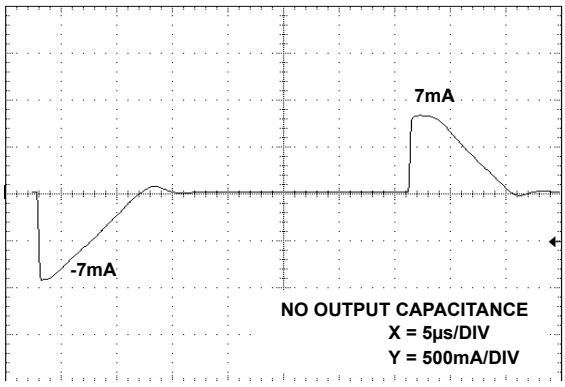


FIGURE 29. LOAD TRANSIENT RESPONSE

Typical Performance Curves (ISL21009-50EP) (R_{EXT} = 100kΩ)

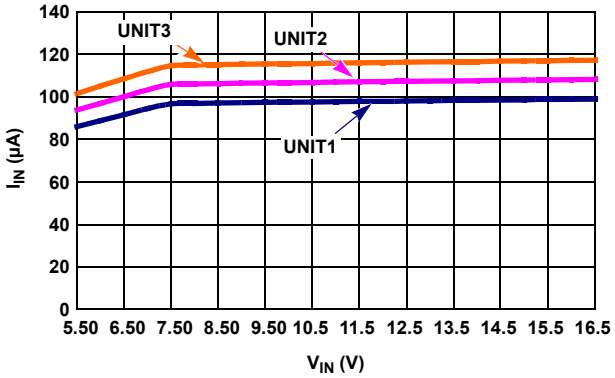


FIGURE 30. I_{IN} vs V_{IN}, 3 UNITS

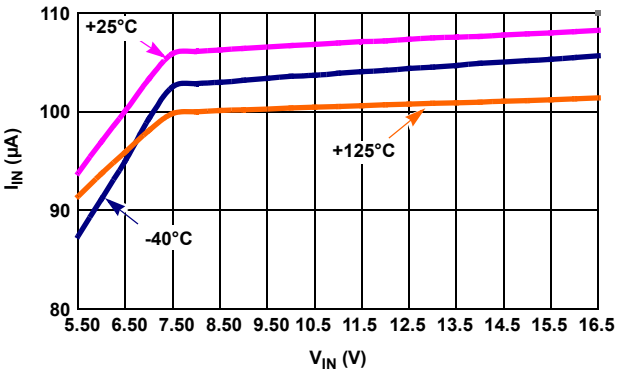


FIGURE 31. I_{IN} vs V_{IN}, 3 TEMPERATURES

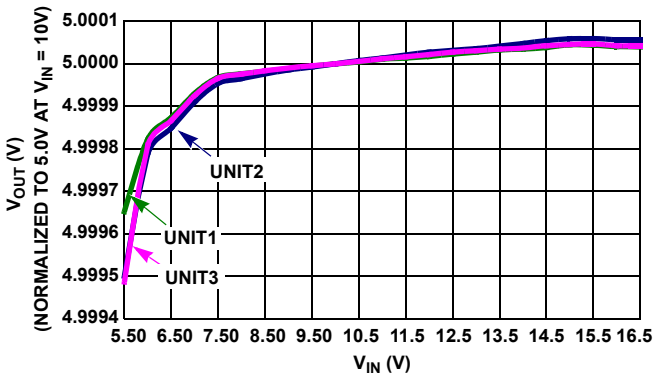


FIGURE 32. LINE REGULATION

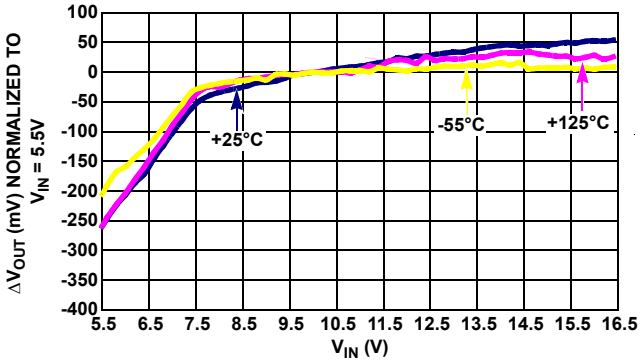


FIGURE 33. LINE REGULATION OVER-TEMPERATURE

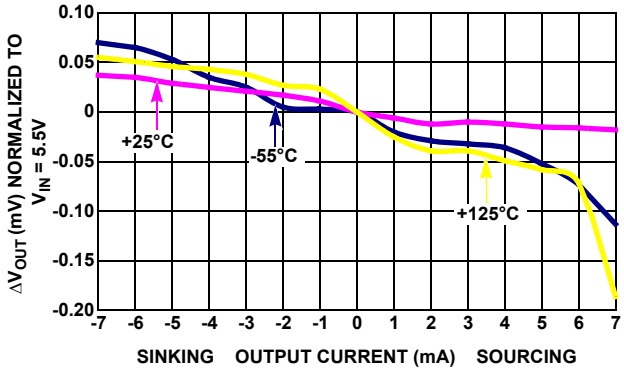


FIGURE 34. LOAD REGULATION

Typical Performance Curves (ISL21009-50EP) (R_{EXT} = 100kΩ) (Continued)

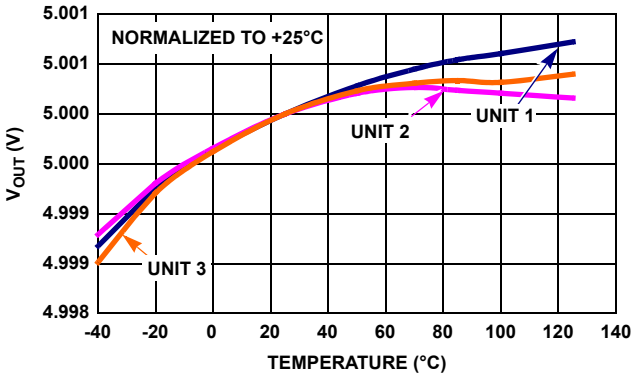


FIGURE 35. V_{OUT} vs TEMPERATURE

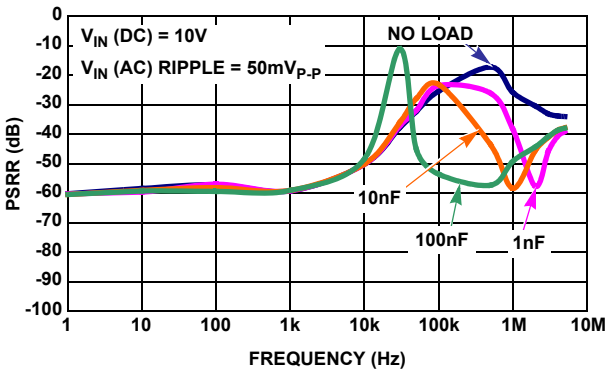


FIGURE 36. PSRR AT DIFFERENT CAPACITIVE LOADS

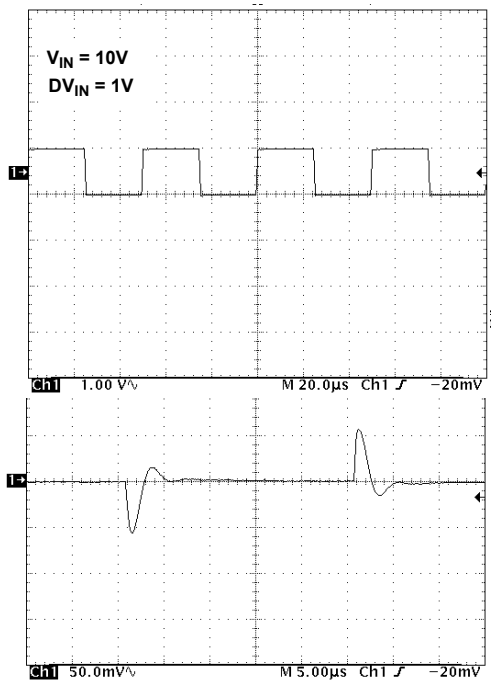


FIGURE 37. LINE TRANSIENT RESPONSE, NO CAPACITIVE LOAD

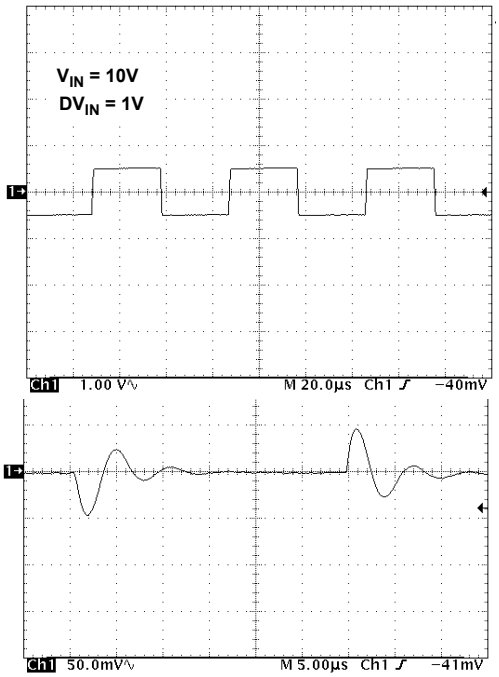


FIGURE 38. LINE TRANSIENT RESPONSE, 0.001µF LOAD CAPACITANCE

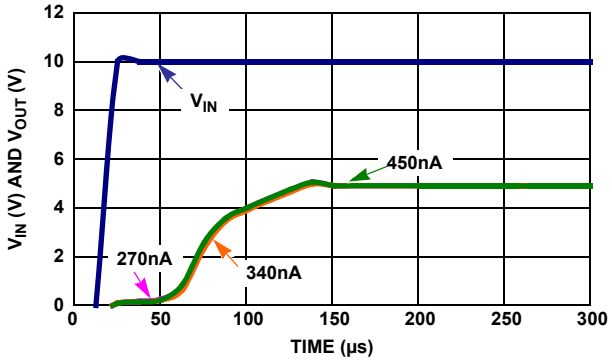


FIGURE 39. TURN-ON TIME

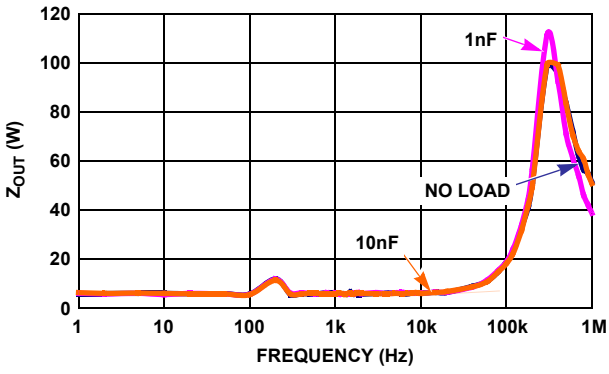


FIGURE 40. Z_{OUT} vs FREQUENCY

Typical Performance Curves (ISL21009-50EP) (R_{EXT} = 100kΩ) (Continued)

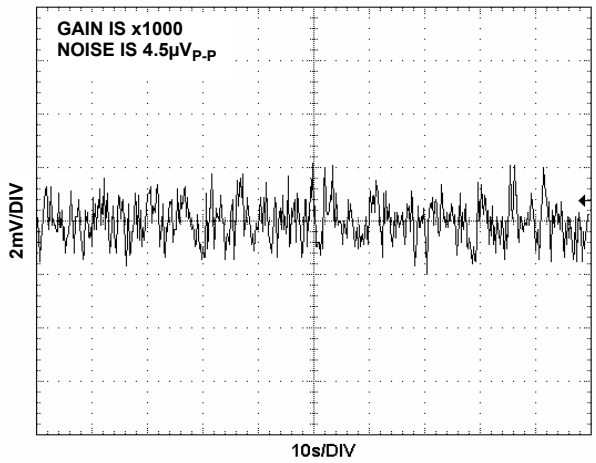


FIGURE 41. V_{OUT} NOISE, 0.1Hz TO 10Hz

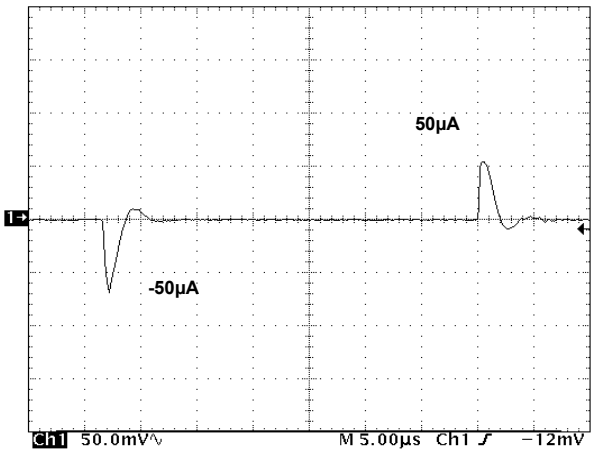


FIGURE 42. LOAD TRANSIENT RESPONSE

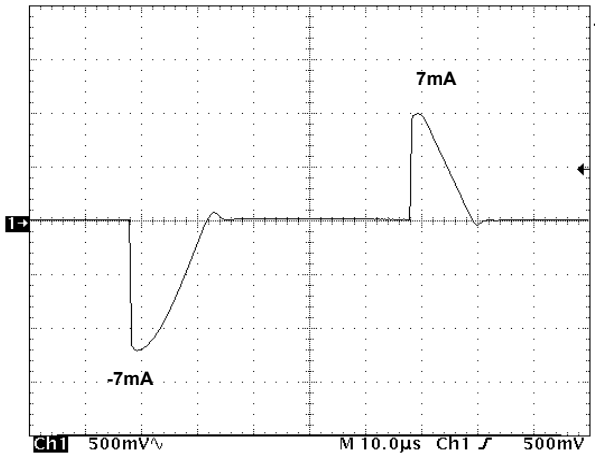


FIGURE 43. LOAD TRANSIENT RESPONSE

Applications Information

FGA Technology

The ISL21009MEP voltage reference uses floating gate technology to create references with very low drift and supply current. Essentially the charge stored on a floating gate cell is set precisely in manufacturing. The reference voltage output itself is a buffered version of the floating gate voltage. The resulting reference device has excellent characteristics, which are unique in the industry: very low temperature drift, high initial accuracy, and almost zero supply current. Also, the reference voltage itself is not limited by voltage bandgaps or zener settings, so a wide range of reference voltages can be programmed (standard voltage settings are provided, but customer-specific voltages are available).

The process used for these reference devices is a floating gate CMOS process and the amplifier circuitry uses CMOS transistors for amplifier and output transistor circuitry. While providing excellent accuracy, there are limitations in output noise level and load regulation due to the MOS device characteristics. These limitations are addressed with circuit techniques discussed in other sections.

Micropower Operation

The ISL21009MEP consumes extremely low supply current due to the proprietary FGA technology. Low noise performance is achieved using optimized biasing techniques. Supply current is typically 95µA and noise is 4.5µV_{P-P} benefitting precision, low noise portable applications such as handheld meters and instruments.

Data Converters in particular can utilize the ISL21009MEP as an external voltage reference. Low power DAC and ADC circuits will realize maximum resolution with lowest noise.

Board Mounting Considerations

For applications requiring the highest accuracy, board mounting location should be reviewed. The device uses a plastic SOIC package, which will subject the die to mild stresses when the PC board is heated and cooled, slightly changing the shape. Placing the device in areas subject to slight twisting can cause degradation of the accuracy of the reference voltage due to these die stresses. It is normally best to place the device near the edge of a board, or the shortest side, as the axis of bending is most limited at that location. Mounting the device in a cutout also minimizes flex. Obviously mounting the device on flexprint or extremely thin PC material will likewise cause loss of reference accuracy.

Noise Performance and Reduction

The output noise voltage in a 0.1Hz to 10Hz bandwidth is typically 4.5µV_{P-P}. The noise measurement is made with a bandpass filter made of a 1-pole high-pass filter with a corner frequency at 0.1Hz and a 2-pole low-pass filter with a corner frequency at 12.6Hz to create a filter with a 9.9Hz bandwidth. Noise in the 10kHz to 1MHz bandwidth is approximately 40µV_{P-P} with no capacitance on the output. This noise measurement is made with a 2 decade bandpass filter made of a 1-pole high-pass filter with a corner frequency at 1/10 of the center frequency and 1-pole low-pass filter with a corner frequency at 10x the center frequency. Load capacitance up to 1000pF can be added but will result in only marginal improvements in output noise and transient response. The output stage of the ISL21009MEP is not designed to drive heavily capactive loads, so for load capacitances above 0.001µF, the noise reduction network shown in Figure 44 is recommended. This network reduces noise significantly over the full bandwidth. Noise is reduced to less than 20µV_{P-P} from 1Hz to 1MHz using this network with a 0.01µF capacitor and a 2kΩ resistor in series with a 10µF capacitor. Also, transient response is improved with higher value output capacitor. The 0.01µF value can be increased for better load transient response with little sacrifice in output stability.

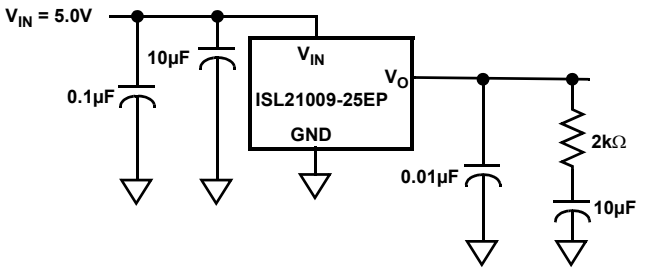


FIGURE 44. HANDLING HIGH LOAD CAPACITANCE

Turn-On Time

The ISL21009MEP devices have low supply current and thus the time to bias up internal circuitry to final values will be longer than with higher power references. Normal turn-on time is typically 100µs. This is shown in Figure 11. Circuit design must take this into account when looking at power-up delays or sequencing.

Temperature Coefficient

The limits stated for temperature coefficient (tempco) are governed by the method of measurement. The overwhelming standard for specifying the temperature drift of a reference is to measure the reference voltage at two temperatures, take the total variation, ($V_{HIGH} – V_{LOW}$), and divide by the temperature extremes of measurement ($T_{HIGH} – T_{LOW}$). The result is divided by the nominal reference voltage (at T = +25°C) and multiplied by 10^6 to yield ppm/°C. This is the “Box” method for specifying temperature coefficient.

Output Voltage Adjustment

The output voltage can be adjusted up or down by 2.5% by placing a potentiometer from V_{OUT} to GND and connecting the wiper to the TRIM pin. The TRIM input is high impedance so no series resistance is needed. The resistor in the potentiometer should be a low tempco (<50ppm/°C) and the resulting voltage divider should have very low tempco <5ppm/°C. A digital potentiometer such as the ISL95810 provides a low tempco resistance and excellent resistor and tempco matching for trim applications.

Typical Application Circuits

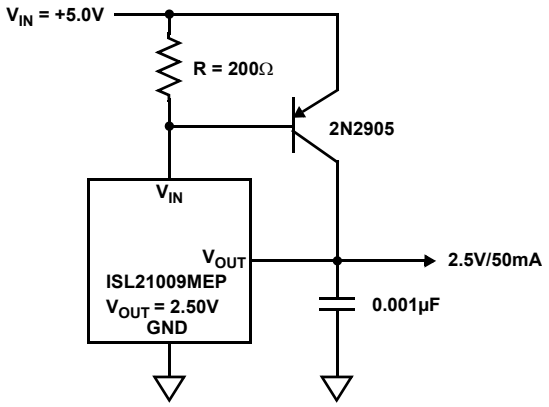


FIGURE 45. PRECISION 2.5V, 50mA REFERENCE

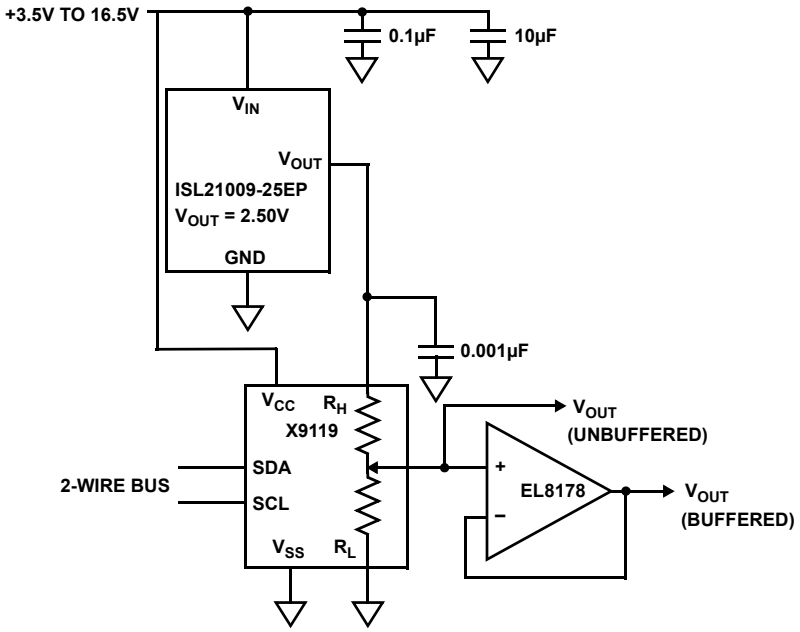


FIGURE 46. 2.5V FULL SCALE LOW-DRIFT, LOW NOISE, 10-BIT ADJUSTABLE VOLTAGE SOURCE

Typical Application Circuits (Continued)

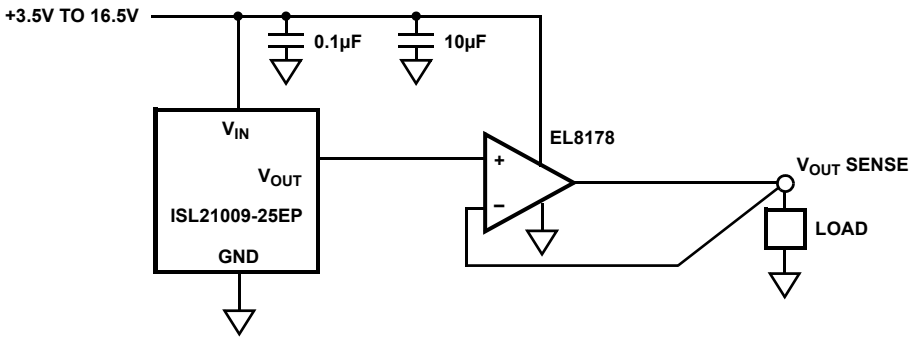


FIGURE 47. KELVIN SENSED LOAD

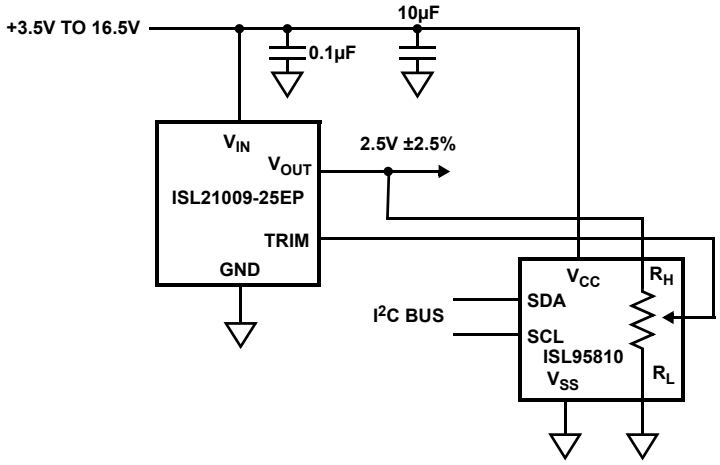
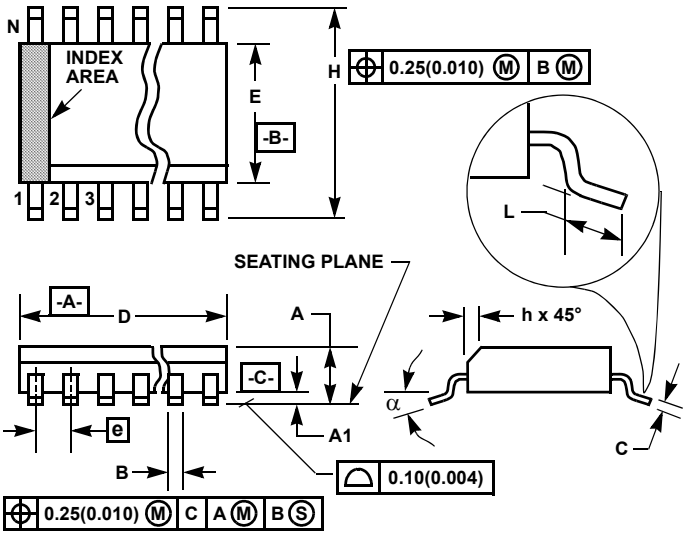


FIGURE 48. OUTPUT ADJUSTMENT USING THE TRIM PIN

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
a	0°	8°	0°	8°	-

Rev. 1 6/05

© Copyright Intersil Americas LLC 2008. All Rights Reserved.
All trademarks and registered trademarks are the property of their respective owners.

For additional products, see www.intersil.com/en/products.html

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at www.intersil.com/en/support/qualandreliability.html

Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com