

I3C IP data sheet

I3C(Improved Inter Integrated Circuit) IP

Overview

The Renesas I3C IP is compliant with the “MIPI I3C Specification v1.0”. This IP operates the I3C Main Master/Secondary Master mode and Slave mode. And the IP supports SDR, HDR-DDR, HDR-TSL, HDR-TSP to perform high data rate (up to 33.4Mbps @HDR-TSP) and In-Band Interrupt. The IP can also work as I2C master and slave.

General

- Compliant with “MIPI I3C Specification v1.0”

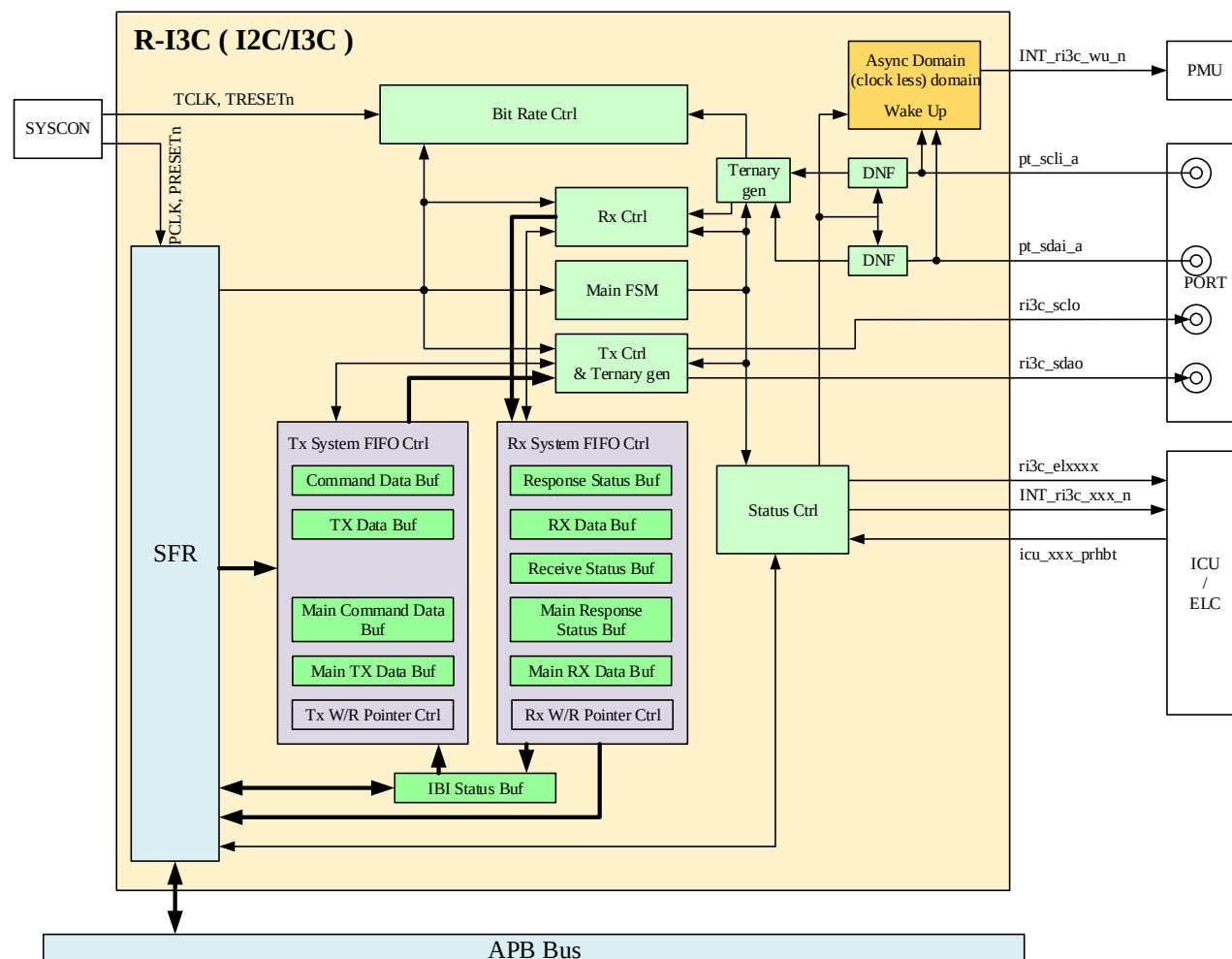
I3C features

- Master (Main Master/Secondary Master) mode and Slave mode
- SDR (I3C Single Data Rate) Mode
 - Private Message
 - Broadcast Message (Common Command Code)
 - Direct Message (Common Command Code)
- HDR (I3C High Data Rate) Mode
 - HDR-DDR (Dual Data Rate) Mode
 - HDR-TSL (Ternary Symbol Legacy) Mode
 - HDR-TSP (Ternary Symbol Pure-bus) Mode
- Legacy I2C Message
- Dynamic Address Assignment
- CCC(Common Command Code) support
- In-Band Interrupt
- Hot-Join Capability
- Synchronous/ Asynchronous Timing Control
- Error Detection
- Wake Up function support
- High Priority FIFO/Normal FIFO buffer transfer
- APB Bus interface

I2C features

- Master mode and Slave mode
- I2C Bus format
 - Standard-mode (Sm)
 - Fast-mode (Fm)
 - Fast-mode Plus (Fm+)
 - High-speed mode (Hs-mode)
- 7bit/10bit address
- Wake Up function support
- APB Bus interface

IP Block Diagram.



SYSCON : System Controller	DNF : Digital Noise Filter
PMU : Power Management Unit	SFR : Special Function Register
ICU : Interrupt Control Unit	FSM : Finite State Machine
ELC : Event Link Controller	