

32-bit RISC CPU Datasheet

SH3-DSP CPU

Overview

- The SH2 - DSP CPU interprets and executes the SH - DSP instruction that extended the SH 2 instruction. For multiply instructions and DSP arithmetic instructions, calculations are performed with a digital signal processor (DSP) module.

Key Features

- Compatible with object code level with SH - 1, SH - 2, and SH 3
- Built-in 32-bit internal data bus
- Supports abundant register groups
 - General-purpose register: 16 16-bit registers (including 8 32-bit bank registers)
 - Control register: 5 built-in 32-bit registers
 - System register: Four 32-bit registers
- The instruction execution time of the basic instruction corresponds to one instruction / cycle
- The logical address space corresponds to 4 GB
- Features of DSP
 - Mixing 16-bit instructions and 32-bit instructions
 - Supports multiplier, ALU, barrel shifter
 - Built-in 32-bit one-cycle multiplier corresponding to 16 bits x 16 bits
 - Supports large capacity DSP data register file
 - Supports extended Harvard architecture for DSP data bus
- Peripheral circuit
 - MMU, TLB, INTC, UBC, AUD, BSC, DMAC

Block diagram

