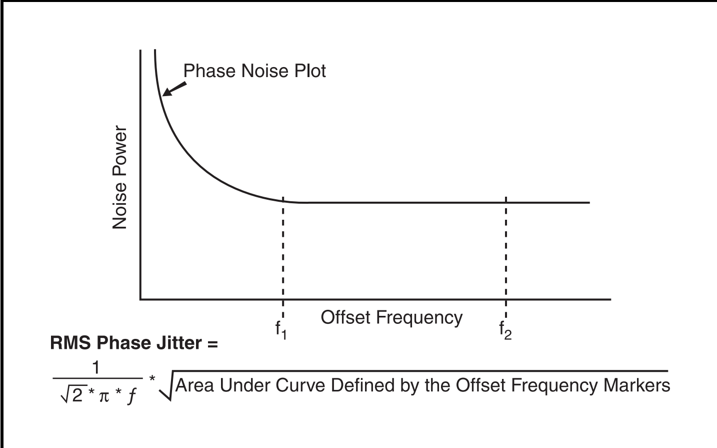
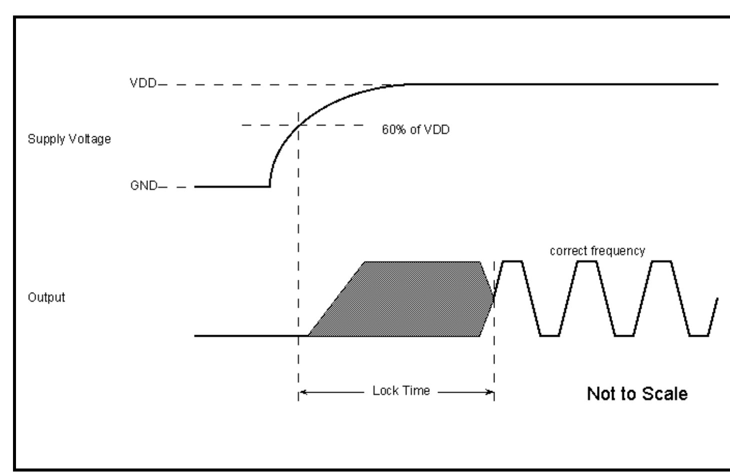
Parameter Measurement Information, continued

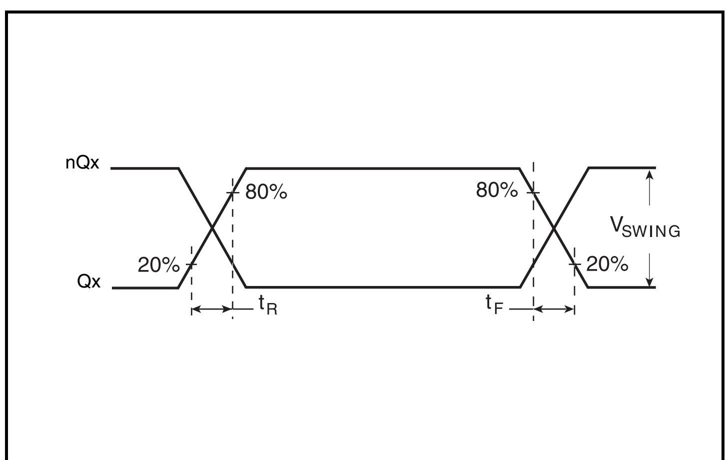


RMS Phase Jitter

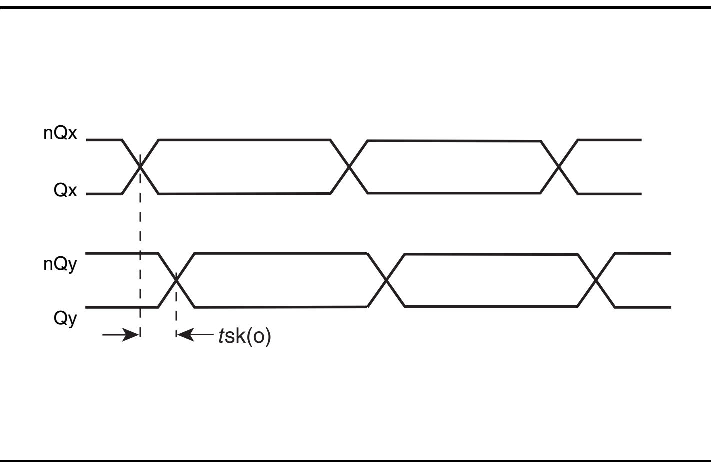


PLL Lock Time

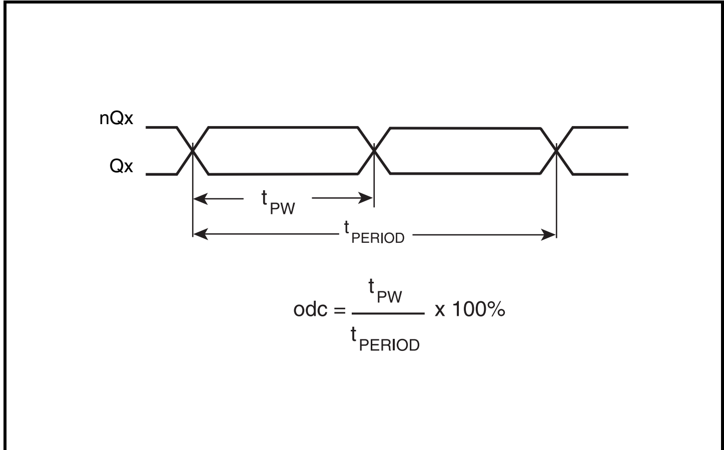
LVDS Output Rise/Fall Time



LVPECL Output Rise/Fall Time



Output Skew



Differential Output Duty Cycle/Output Pulse Width/Period

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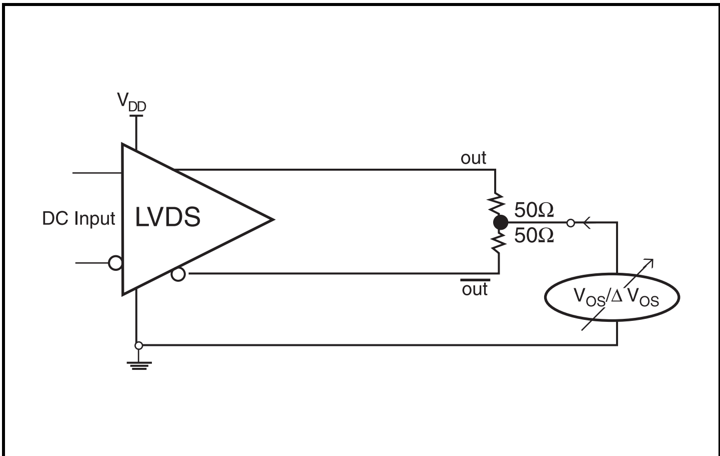
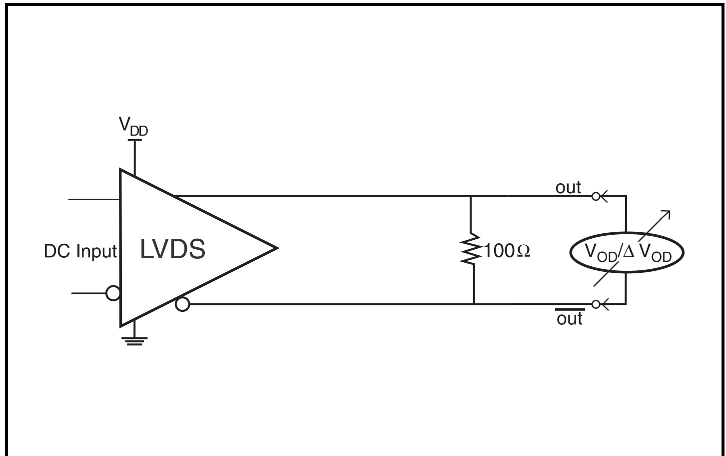
Parameter Measurement Information, continued



Offset Voltage Setup



Differential Output Voltage Setup

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Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground. It is recommended that CLK, nCLK be left unconnected in frequency synthesizer mode.

LVCMOS Control Pins

All control pins have internal pullup or pulldown resistors; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL output pairs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating there should be no trace attached.

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Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

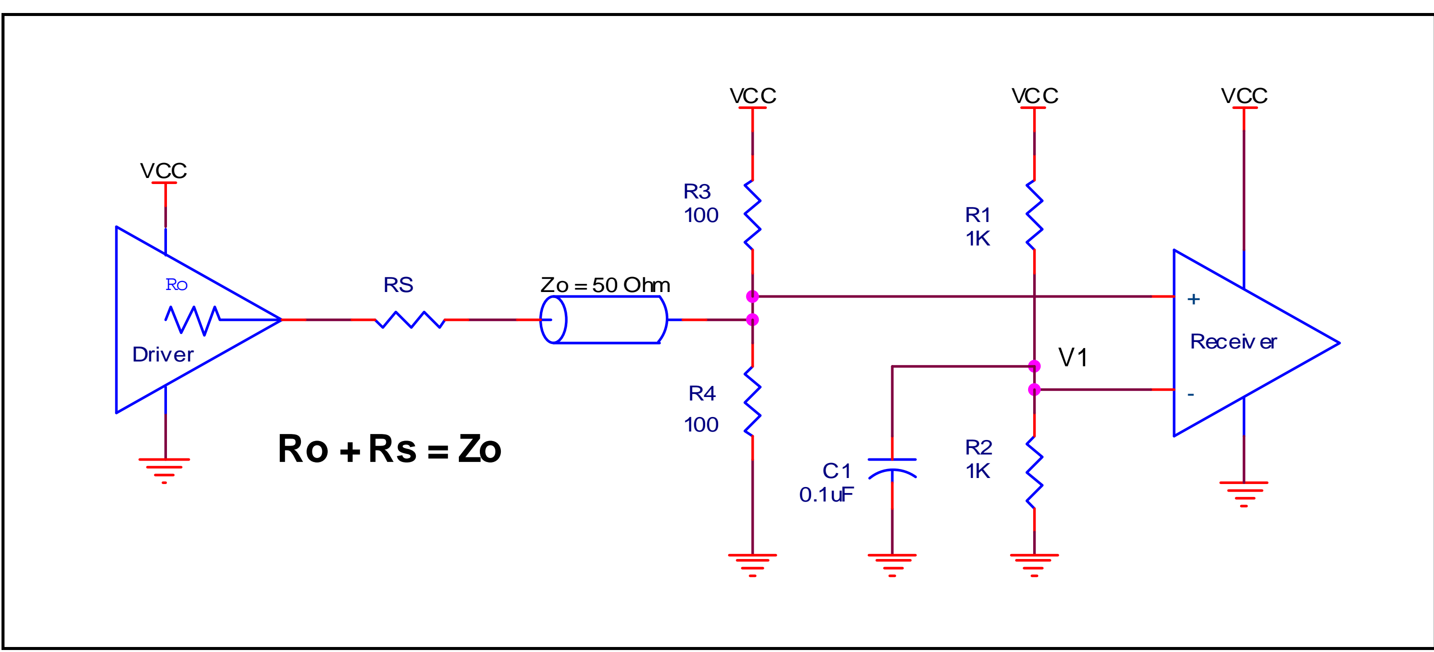

Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

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Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 2A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 2B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

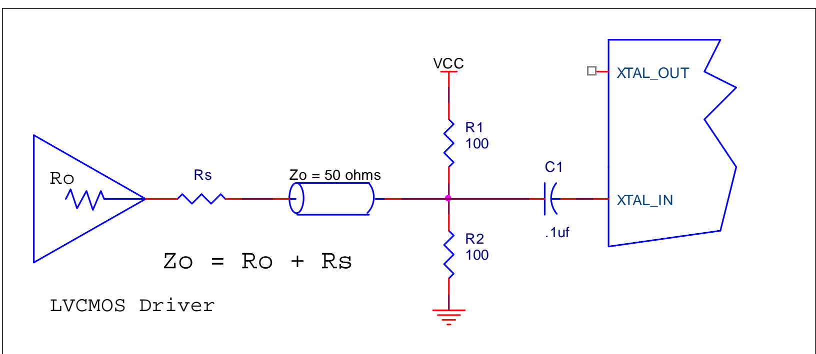

Figure 2A. General Diagram for LVCMOS Driver to XTAL Input Interface

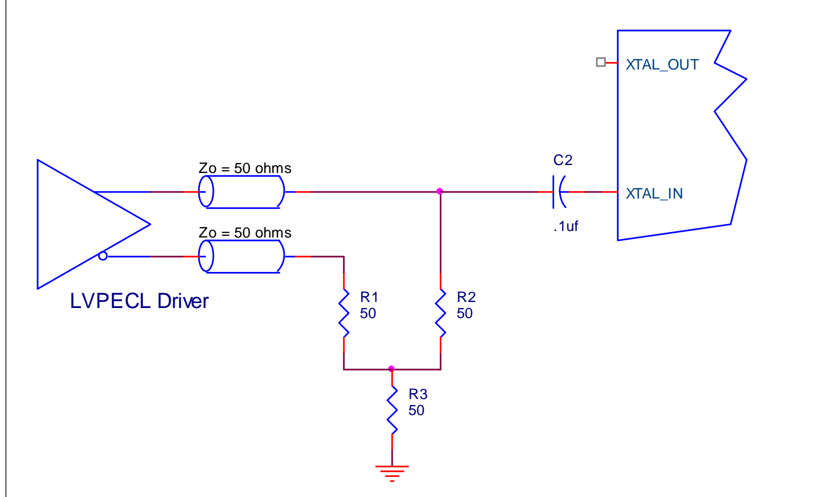

Figure 2B. General Diagram for LVPECL Driver to XTAL Input Interface

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3.3V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

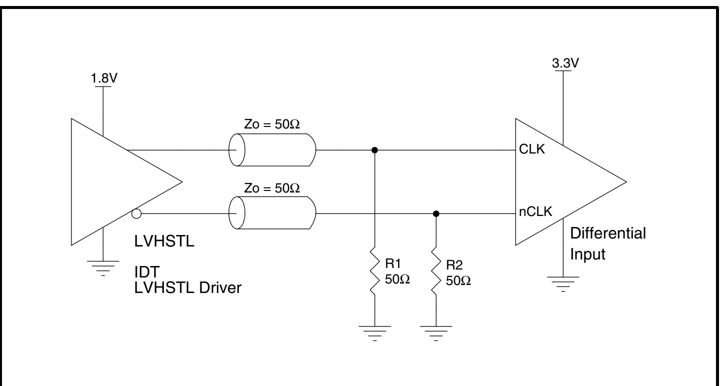

Figure 3A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

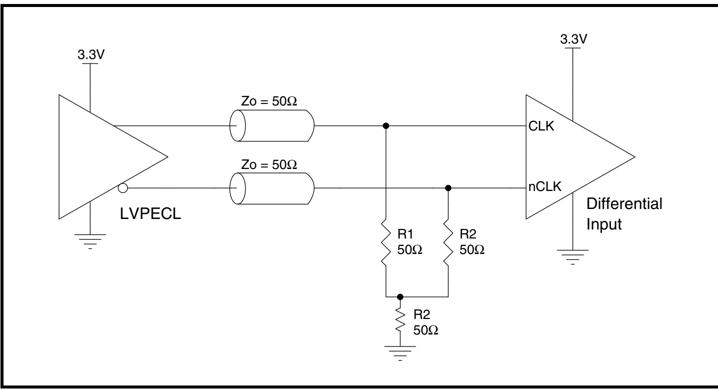

Figure 3B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

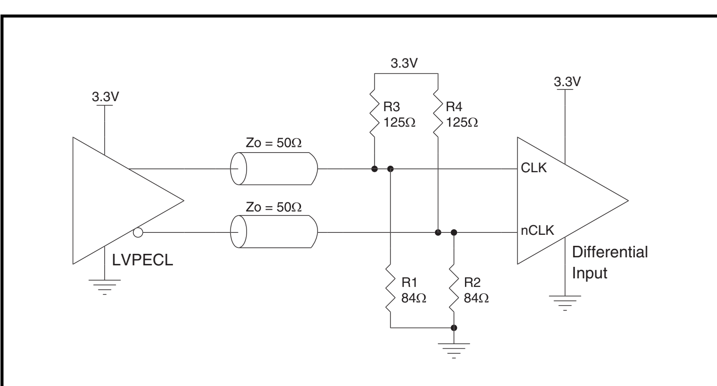

Figure 3C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

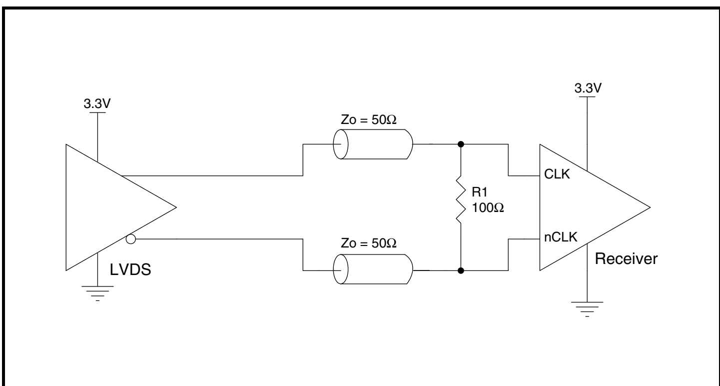

Figure 3D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

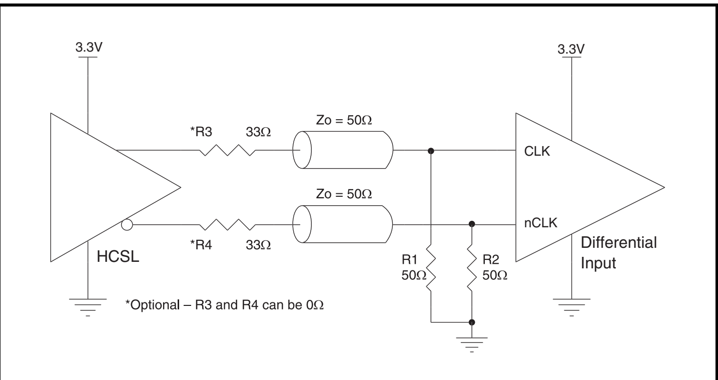

Figure 3E. CLK/nCLK Input Driven by a 3.3V HCSL Driver

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2.5V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 4A to 4E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 4A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

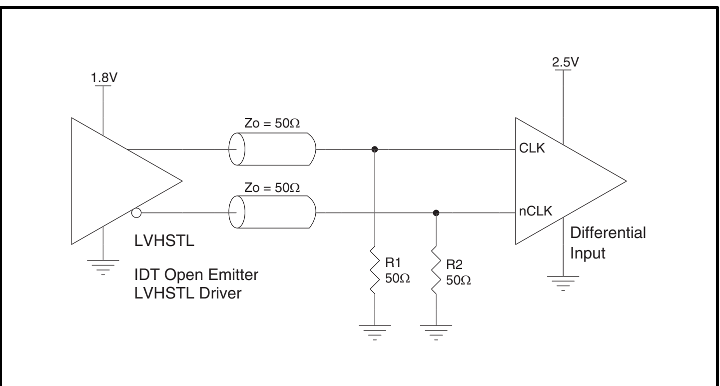

Figure 4A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

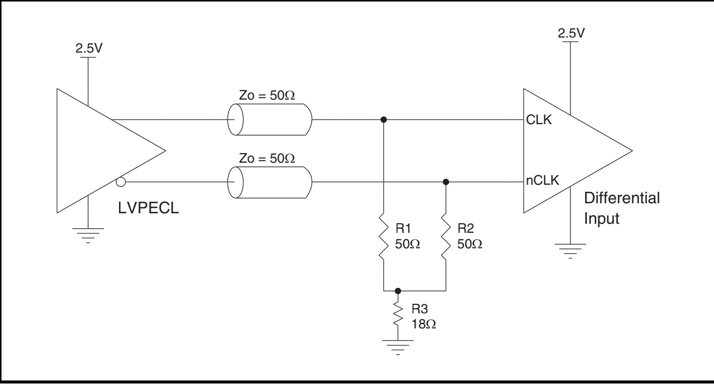

Figure 4B. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

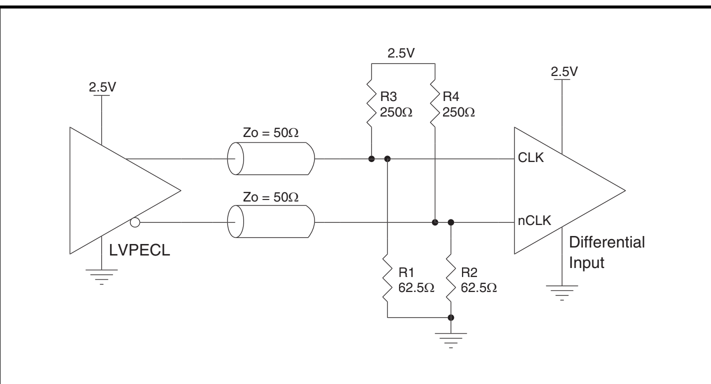

Figure 4C. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

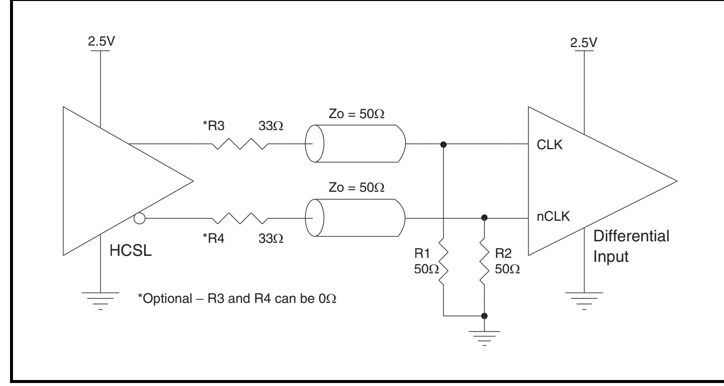

Figure 4D. CLK/nCLK Input Driven by a 2.5V HCSL Driver

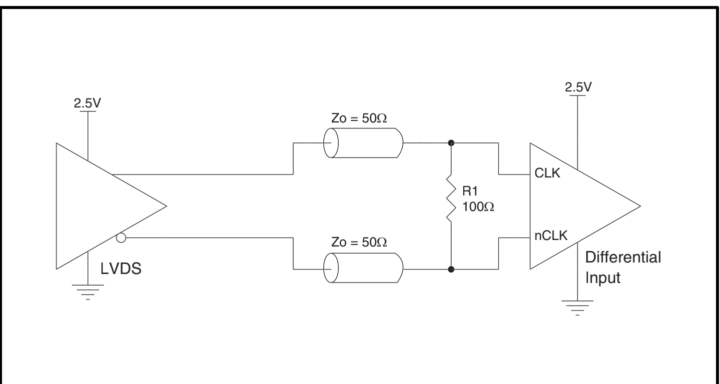

Figure 4E. CLK/nCLK Input Driven by a 2.5V LVDS Driver

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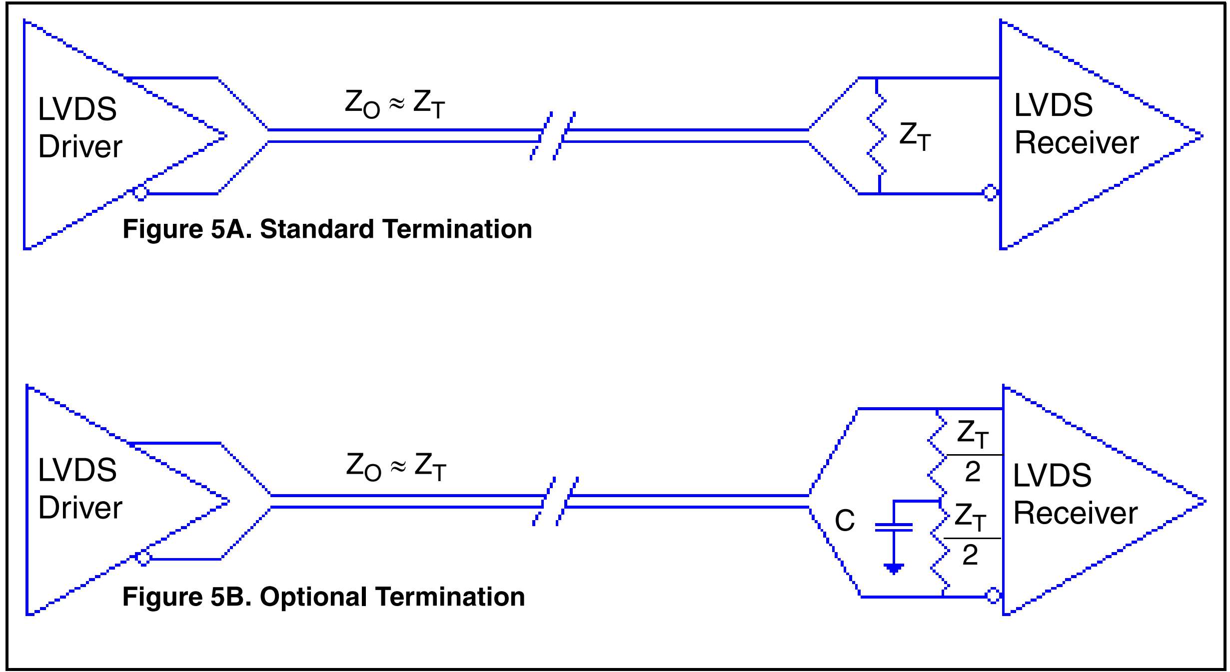
LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 5A* can be used with either type of output structure. *Figure 5B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.



LVDS Termination

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Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 6A and 6B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

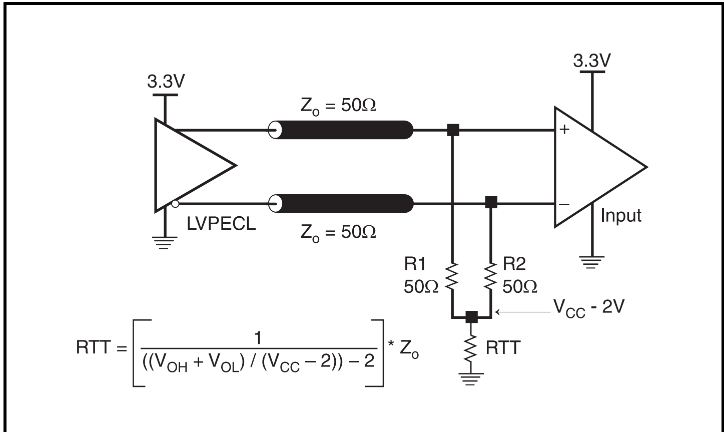

Figure 6A. 3.3V LVPECL Output Termination

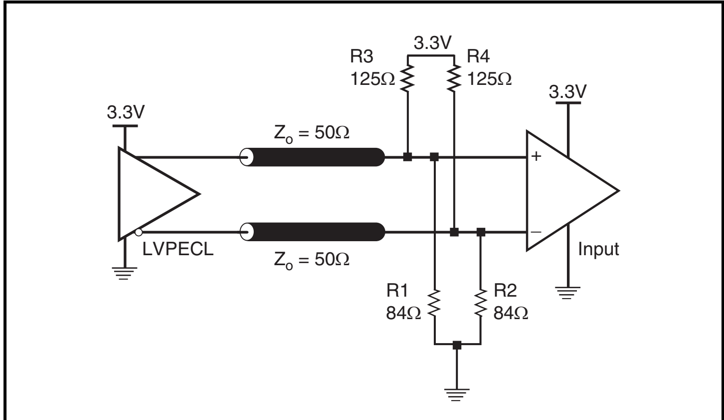

Figure 6B. 3.3V LVPECL Output Termination

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Termination for 2.5V LVPECL Outputs

Figure 7A and *Figure 7B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CCO} – 2V. For V_{CCO} = 2.5V, the V_{CCO} – 2V is very close to ground level. The R3 in Figure 7B can be eliminated and the termination is shown in *Figure 7C.*

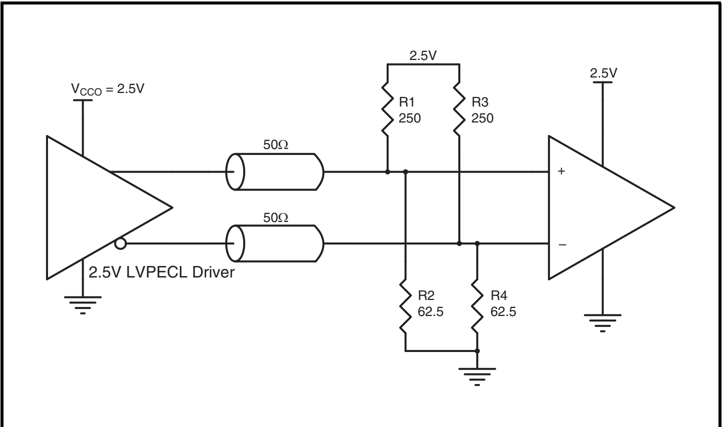

Figure 7A. 2.5V LVPECL Driver Termination Example

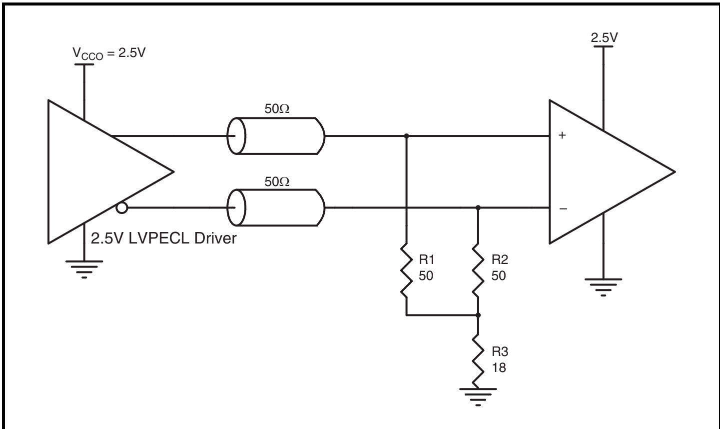

Figure 7B. 2.5V LVPECL Driver Termination Example

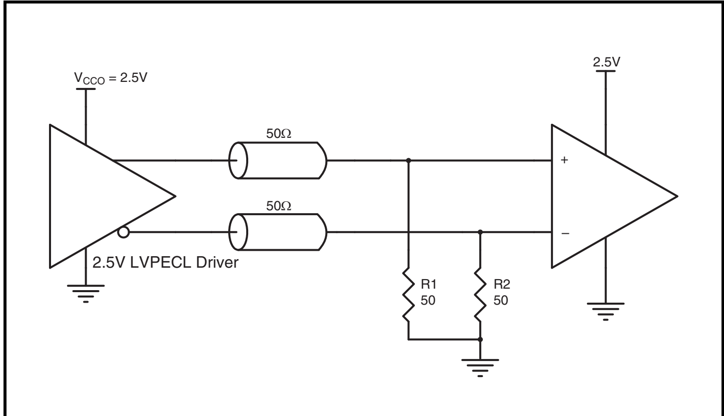

Figure 7C. 2.5V LVPECL Driver Termination Example

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VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 8.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Lead frame Base Package, Amkor Technology.

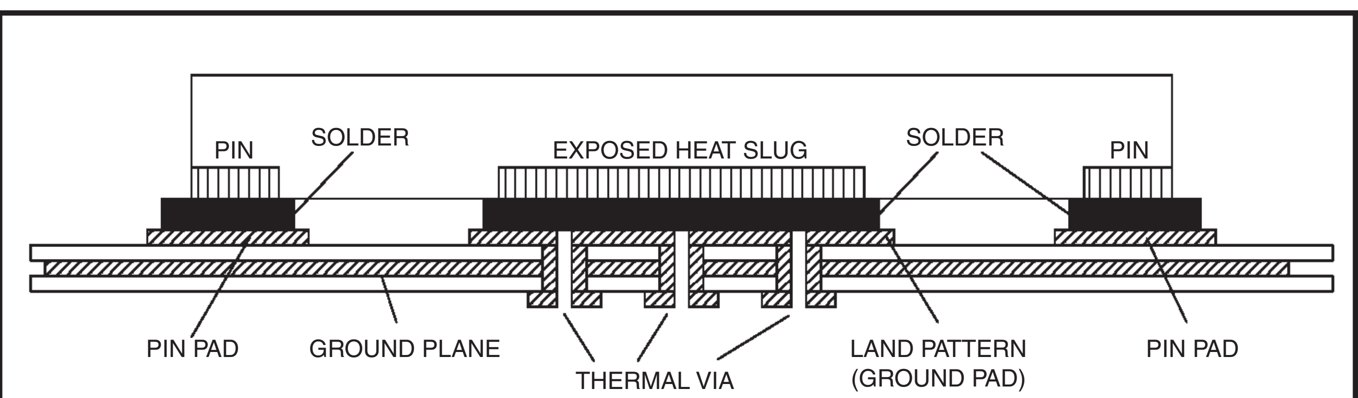

Figure 8. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

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Schematic Layout

Figure 9 (next page) shows an example IDT8T49N524I application schematic that focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set. In this example, the input reference is LVDS and the outputs have all been configured for LVPECL.

In this example a 12pF parallel resonant Fox FX325BS 25MHz crystal is used with load caps C1 = C2 = 10pF. The load caps are recommended for frequency accuracy, but these may be adjusted for different board layouts. Crystals with different load capacities may be used, but the load capacitors will have to be changed accordingly. If different crystal types are used, please consult IDT for recommendations.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The IDT8T49N524I provides separate power supplies to isolate any high switching noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1µF capacitor in each power pin filter and the resistor of the V_{DDA} power filters should be placed on the device side of the PCB and the other components can be placed on the opposite side.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for wide range of noise frequency. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component with high amplitude interference is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally general design practice for power plane voltage stability suggests adding bulk capacitances in the general area of all devices.

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3.3V
FB2
BLM18BB221SN1
C23
0.1uF
C24
10uF
VCCO

VCC
VCCA
R4 10
C6
10uF
C10
10uF
FB1
BLM18BB221SN1
C9
0.1uF
3.3V

U1
CLK_SEL
ADD_SEL
FSEL0
FSEL1
VCC
VCC
VCCA
VCCO_A
VCCO_B
LOCK
C11
0.1uF
C13
0.1uF
C14
0.1uF
C20
0.1uF
C22
0.1uF

Place each 0.1uF bypass cap directly adjacent to its corresponding VCC, VCCA, VCCO_A or VCCO_B pin.

Logic Control Input Examples

Set Logic Input to '1'
VCC
RU1
1K
To Logic Input pins
RD1
Not Install

Set Logic Input to '0'
VCC
RU2
Not Install
To Logic Input pins
RD2
1K

3.3V
R1
4.7K
R2
4.7K
SDATA
SCLK

Fox FX325BS Crystal
25 MHz
(12pf)
X1
XTAL_IN
XTAL_OUT
C1
10pF
C2
10pF

LVDS Driver
Zo = 50 Ohm
Zo = 50 Ohm
R3
100
CLK
nCLK

QA0 nQA0
QA1 nQA1
QA2 nQA2
QA3 nQA3
QB0 nQB0
QB1 nQB1
QB2 nQB2
QB3 nQB3

Zo = 50 Ohm
Zo = 50 Ohm
R5 50
R6 50
R7 50
+3.3V PECL Receiver

VEE VEE VEE VEE VEE VEE VEE VEE ePAD

2.5V
C12
0.1u
C15
0.1u
Zo = 50 Ohm
Zo = 50 Ohm
R8
180
R9
180
IN
50
50
$\overline{IN}$
CML Receiver

Optional 3.3v PECL AC Termination for PECL swing compliant 2.5V CML Receiver

Figure 9. IDT8T49N524I Application Schematic

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LVPECL Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8T49N524I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT8T49N524I is the sum of the core power plus the power dissipated due to loading.
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated due to loading.

- Power $(core)_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 300mA = **1039.5mW**
- Power $(outputs)_{MAX}$ = **31.6mW/Loaded Output pair**
  If all outputs are loaded, the total power is 8 * 31.6mW = **252.8mW**

Total Power$_{_MAX}$ (3.465V, with all outputs switching) = 1039.5mW + 252.8mW = **1292.3mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 27.9°C/W per Table 10 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 1.292W * 27.9°C/W = 121.1°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 10. Thermal Resistance θ_{JA} for 40 Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB; NOTE 1	27.9°C/W	21.6°C/W	19.1°C/W
Multi-Layer PCB, JEDEC Standard	NOTE 2	25.7°C/W	23.4°C/W

NOTE 1: θ_{JA} simulation is performed with 4-layers, 8in. x 8in. PCB.
NOTE 2: JEDEC Standard requires air flow.

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3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in *Figure 10.*

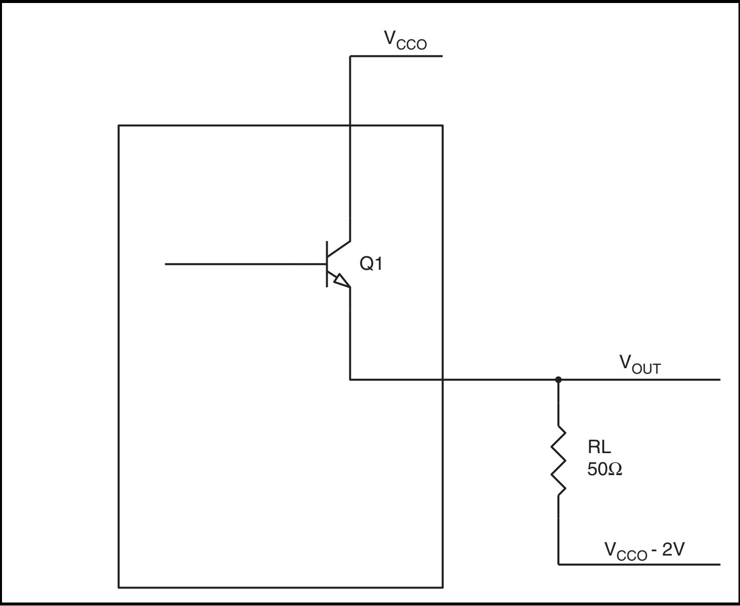

Figure 10. LVPECL Driver Circuit and Termination

To calculate power dissipation per output pair due to loading, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CCO} – 2V$.

- For logic high, $V_{OUT} = V_{OH_MAX} = \mathbf{V_{CCO_MAX} – 0.75V}$
  $(V_{CCO_MAX} – V_{OH_MAX}) = \mathbf{0.75V}$
- For logic low, $V_{OUT} = V_{OL_MAX} = \mathbf{V_{CCO_MAX} – 1.6V}$
  $(V_{CCO_MAX} – V_{OL_MAX}) = \mathbf{1.6V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd_H = [(V_{OH_MAX} – (V_{CCO_MAX} – 2V))/R_L] * (V_{CCO_MAX} – V_{OH_MAX}) = [(2V – (V_{CCO_MAX} – V_{OH_MAX}))/R_L] * (V_{CCO_MAX} – V_{OH_MAX}) = [(2V – 0.75V)/50\Omega] * 0.75V = \mathbf{18.75mW}$

$Pd_L = [(V_{OL_MAX} – (V_{CCO_MAX} – 2V))/R_L] * (V_{CCO_MAX} – V_{OL_MAX}) = [(2V – (V_{CCO_MAX} – V_{OL_MAX}))/R_L] * (V_{CCO_MAX} – V_{OL_MAX}) = [(2V – 1.6V)/50\Omega] * 1.6V = \mathbf{12.8mW}$

Total Power Dissipation per output pair = Pd_H + Pd_L = **31.6mW**

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LVDS Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8T49N524I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT8T49N524I is the sum of the core power plus the analog power plus the power dissipated due to the load. The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power (core)$_{MAX}$ = V_{CC_MAX} * (I_{CC_MAX} + I_{CCA_MAX}) = 3.465V * (212mA + 18mA) = **796.95mW**
- Power (outputs)$_{MAX}$ = V_{CCO_MAX} * I_{CCO_MAX} = 3.465V * 167mA = **578.66mW**

Total Power$_{_MAX}$ = 796.95mW + 578.66mW = **1375.61mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 27.9°C/W per Table 11 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 1.376W * 27.9°C/W = 123.40°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 11. Thermal Resistance θ_{JA} for 40 Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB; NOTE 1	27.9°C/W	21.6°C/W	19.1°C/W
Multi-Layer PCB, JEDEC Standard	NOTE 2	25.7°C/W	23.4°C/W

NOTE 1: θ_{JA} simulation is performed with 4-layers, 8in. x 8in. PCB.
NOTE 2: JEDEC Standard requires air flow.

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Reliability Information

Table 12. θ_{JA} vs. Air Flow Table for a 40 Lead VFQFN

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB; NOTE 1	27.9°C/W	21.6°C/W	19.1°C/W
Multi-Layer PCB, JEDEC Standard	NOTE 2	25.7°C/W	23.4°C/W

NOTE 1: θ_{JA} simulation is performed with 4-layers, 8in. x 8in. PCB.
NOTE 2: JEDEC Standard requires air flow.

Transistor Count

The transistor count for IDT8T49N524I is: 35,322

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40 Lead VFQFN Package Outline and Package Dimensions

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40 Lead VFQFN Package Outline and Package Dimensions, continued

DCN	REV	DESCRIPTION	DATE	APPROVED
	01	ADDED SAW VERSION	07/10/03	PKP
	02	DELETED PUNCHED VERSION	01/07/04	PKP
	03	ADD"GREEN" NLG NOMENCLTURE	10/08/04	TU VU

SYMBOL	JEDEC VARIATION VJJC-3 MIN.	NOM.	MAX.	NOTE
e		0.65 BSC		
N		28		2
Nd		7		2
Ne		7		2
b	0.25	0.30	0.35	4
D2		–		10
E2		–		10

SYMBOL	JEDEC VARIATION VJJD-5 MIN.	NOM.	MAX.	NOTE
e		0.50 BSC		
N		40		3
Nd		10		3
Ne		10		3
b	0.18	0.25	0.30	4
D2		–		10
E2		–		10

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE
A	–	0.90	1.00	
A1	0.00	0.02	0.05	7
A3		0.20 REF.		
D		6.00 BSC		
E		6.00 BSC		
k	0.20	–	–	
L	0.35	0.40	0.45	

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M. – 1994.
2. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
3. ALL DIMENSIONS ARE IN MILLIMETERS.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.30mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST EXIST ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. APPLIED TO EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
8. APPLIED ONLY FOR TERMINALS.
9. THIS OUTLINES CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO–220, VARIATION VJJC–3 & VJJD–5 WITH THE EXCEPTION OF D2 & E2.
10. DIMENSIONS D2 & E2 VARY DEPENDING ON DEVICE, SUPPLIER, ETC.
    40 Lead VFQFN, D2/E2 EPAD Dimensions: 4.65mm x 4.65mm

TOLERANCES UNLESS SPECIFIED
DECIMAL XX± XXX± XXXX± ANGULAR ±

APPROVALS	DATE
DRAWN PKP	06/26/02
CHECKED	

IDT™ www.IDT.com
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FAX: (408) 492-8674

TITLE NL/NLG PACKAGE OUTLINE 6.0 X 6.0 mm BODY VFQFP-N

SIZE C | DRAWING No. PSC–4115 | REV 03

DO NOT SCALE DRAWING | SHEET 2 OF 2

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Ordering Information

Table 13. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8T49N524-dddNLGI	IDT8T49N524-dddNLGI	"Lead-Free" 40 Lead VFQFN	Tray	-40°C to 85°C
8T49N524-dddNLGI8	IDT8T49N524-dddNLGI	"Lead-Free" 40 Lead VFQFN	Tape & Reel	-40°C to 85°C

NOTE: For the specific -ddd order codes, refer to *Programmable FemtoClock® NG Product Ordering Guide* document.

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Revision History Sheet

Rev	Table	Page	Description of Change	Date
A			In footer, corrected year of date from 2012 to 2013.	4/2/2013
A	 T5D T9	1 12 18 32 33	Features: Changed 'Output frequencies from 15.5MHz - 650MHz, and 975MHz - 1300MHz' to 'Output frequencies from 15.234MHz - 645MHz, and 975MHz - 1290MHz, (See Table 5D for details)' Changed f_{MAX} column: 1300 to 1290; 650 to 645; 433.33333 to 430; 2600 to 2580; 20.635 to 20.476; NOTE 1: 325MHz to 322.5MHz. f_{VCO}: 1910MHz Min to 1950MHz Min; 2500MHz Max to 2580MHz Max 2nd paragraph: 18pF to 12pF Updated Applications schematic to include Fox crystal	7/10/2013
A	 T13	8, 35 40	Changed name of the *IDT8T49N00xI Programmable FemtoClock® NG Product Ordering Information* document to *Programmable FemtoClock® Ordering Product Information* Deleted quantity from Tape & Reel, Deleted Lead Free note.	8/21/2013
A	 T13	1 8 35	Changed title to Programmable FemtoClock® NG LVPECL/LVDS Dual 4-Output Fractional Clock Generator. Changed text from '*Programmable FemtoClock® Ordering Product Information'* to '*Programmable FemtoClock® NG Product Ordering Guide'.* Changed Note from '*Programmable FemtoClock® Ordering Product Information'* to '*Programmable FemtoClock® NG Product Ordering Guide'.*	9/26/13
A		2	Block diagram - corrected FSELx pin names.	1/23/14

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