

## GENERAL DESCRIPTION

The 843002 is a two output LVPECL synthesizer optimized to generate Fibre Channel reference clock frequencies. Using a 26.5625MHz, 18pF parallel resonant crystal, the following frequencies can be generated based on the 2 frequency select pins (F\_SEL[1:0]): 212.5MHz, 187.5MHz, 159.375MHz, 106.25MHz, and 53.125MHz. The 843002 uses IDT's 3<sup>rd</sup> generation low phase noise VCO technology and can achieve 1ps or lower typical rms phase jitter, easily meeting Fibre Channel jitter requirements. The 843002 is packaged in a small 20-pin TSSOP package.

## FEATURES

- Two 3.3V LVPECL outputs
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- Supports the following output frequencies: 212.5MHz, 187.5MHz, 159.375MHz, 106.25MHz and 53.125MHz
- VCO range: 560MHz - 680MHz
- RMS phase jitter (637kHz - 10MHz): 0.72ps (typical)
- Typical phase noise at 212.5MHz

Phase noise:

| Offset       | Noise Power   |
|--------------|---------------|
| 100Hz .....  | -87.7 dBc/Hz  |
| 1KHz .....   | -111.6 dBc/Hz |
| 10KHz .....  | -124.3 dBc/Hz |
| 100KHz ..... | -124.3 dBc/Hz |

- Full 3.3V supply mode
- Lead-Free package RoHS compliant
- -30°C to 85°C ambient operating temperature

FREQUENCY SELECT FUNCTION TABLE

| Input Frequency (MHz) | Inputs |        |                 |                 |                   | Output Frequency (MHz) |
|-----------------------|--------|--------|-----------------|-----------------|-------------------|------------------------|
|                       | F_SEL1 | F_SEL0 | M Divider Value | N Divider Value | M/N Divider Value |                        |
| 26.5625               | 0      | 0      | 24              | 3               | 8                 | 212.5                  |
| 26.5625               | 0      | 1      | 24              | 4               | 6                 | 159.375                |
| 26.5625               | 1      | 0      | 24              | 6               | 4                 | 106.25                 |
| 26.5625               | 1      | 1      | 24              | 12              | 2                 | 53.125                 |
| 23.4375               | 0      | 0      | 24              | 3               | 8                 | 187.5                  |

## PIN ASSIGNMENT

|                  |    |    |                  |
|------------------|----|----|------------------|
| nc               | 1  | 20 | V <sub>CC0</sub> |
| V <sub>CC0</sub> | 2  | 19 | Q1               |
| Q0               | 3  | 18 | nQ1              |
| nQ0              | 4  | 17 | V <sub>EE</sub>  |
| MR               | 5  | 16 | V <sub>CC</sub>  |
| nPLL_SEL         | 6  | 15 | nXTAL_SEL        |
| nc               | 7  | 14 | TEST_CLK         |
| V <sub>CCA</sub> | 8  | 13 | XTAL_IN          |
| F_SEL0           | 9  | 12 | XTAL_OUT         |
| V <sub>CC</sub>  | 10 | 11 | F_SEL1           |

### 843002

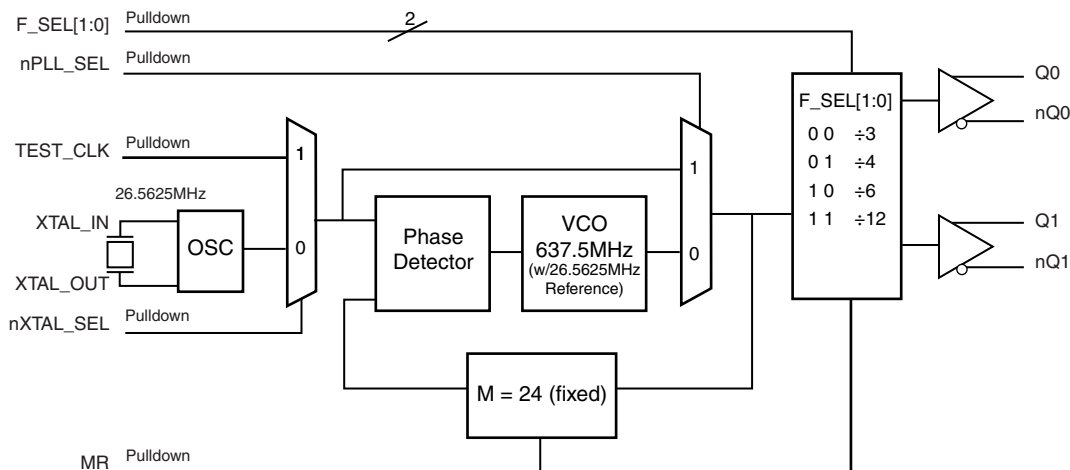
20-Lead TSSOP

6.5mm x 4.4mm x 0.92mm  
package body

**G Package**

Top View

## BLOCK DIAGRAM



**TABLE 1. PIN DESCRIPTIONS**

| Number | Name              | Type   |          | Description   |
|--------|-------------------|--------|----------|---|
| 1, 7   | nc                | Unused |          | No connect.   |
| 2, 20  | V <sub>CC0</sub>  | Power  |          | Output supply pins.   |
| 3, 4   | Q0, nQ0           | Output |          | Differential output pair. LVPECL interface levels.  |
| 5      | MR                | Input  | Pulldown | Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels. |
| 6      | nPLL_SEL          | Input  | Pulldown | Selects between the PLL and TEST_CLK as input to the dividers. When LOW, selects PLL (PLL Enable). When HIGH, deselects the reference clock (PLL Bypass). LVCMOS/LVTTL interface levels.  |
| 8      | V <sub>CCA</sub>  | Power  |          | Analog supply pin.  |
| 9, 11  | F_SEL0, F_SEL1    | Input  | Pulldown | Frequency select pins. LVCMOS/LVTTL interface levels.   |
| 10, 16 | V <sub>CC</sub>   | Power  |          | Core supply pin.  |
| 12, 13 | XTAL_OUT, XTAL_IN | Input  |          | Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.  |
| 14     | TEST_CLK          | Input  | Pulldown | LVCMOS/LVTTL clock input.   |
| 15     | nXTAL_SEL         | Input  | Pulldown | Selects between crystal or TEST_CLK inputs as the the PLL Reference source. Selects XTAL inputs when LOW. Selects TEST_CLK when HIGH. LVCMOS/LVTTL interface levels.  |
| 17     | V <sub>EE</sub>   | Power  |          | Negative supply pins.   |
| 18, 19 | nQ1, Q1           | Output |          | Differential output pair. LVPECL interface levels.  |

NOTE: *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

| Symbol                | Parameter               | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|---------|---------|---------|-------|
| C <sub>IN</sub>       | Input Capacitance       |                 |         | 4       |         | pF    |
| R <sub>PULLDOWN</sub> | Input Pulldown Resistor |                 |         | 51      |         | kΩ    |

# **ABSOLUTE MAXIMUM RATINGS**

|  |                          |
|--|--------------------------|
| Supply Voltage, $V_{CC}$                 | 4.6V                     |
| Inputs, $V_I$                            | -0.5V to $V_{CC} + 0.5V$ |
| Outputs, $I_O$                           |                          |
| Continuous Current                       | 50mA                     |
| Surge Current                            | 100mA                    |
| Package Thermal Impedance, $\theta_{JA}$ | 73.2°C/W (0 lfpm)        |
| Storage Temperature, $T_{STG}$           | -65°C to 150°C           |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 3A. POWER SUPPLY DC CHARACTERISTICS,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 10\%$ ,  $T_A = -30^\circ\text{C}$  TO  $85^\circ\text{C}$**

| Symbol    | Parameter             | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-----------------|---------|---------|---------|-------|
| $V_{CC}$  | Core Supply Voltage   |                 | 2.97    | 3.3     | 3.63    | V     |
| $V_{CCA}$ | Analog Supply Voltage |                 | 2.97    | 3.3     | 3.63    | V     |
| $V_{CCO}$ | Output Supply Voltage |                 | 2.97    | 3.3     | 3.63    | V     |
| $I_{EE}$  | Power Supply Current  |                 |         |         | 135     | mA    |
| $I_{CC}$  | Core Supply Current   |                 |         |         | 100     | mA    |
| $I_{CCA}$ | Analog Supply Current |                 |         |         | 15      | mA    |
| $I_{CCO}$ | Output Supply Current |                 |         |         | 31      | mA    |

**TABLE 3B. LVCMOS / LVTTTL DC CHARACTERISTICS,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 10\%$ ,  $T_A = -30^\circ\text{C}$  TO  $85^\circ\text{C}$**

| Symbol   | Parameter          | Test Conditions  | Minimum | Typical | Maximum        | Units         |
|----------|--------------------|--|---------|---------|----------------|---------------|
| $V_{IH}$ | Input High Voltage |  | 2       |         | $V_{CC} + 0.3$ | V             |
| $V_{IL}$ | Input Low Voltage  | nPLL_SEL, nXTAL_SEL, F_SEL0, F_SEL1, MR  | -0.3    |         | 0.8            | V             |
|          |                    | TEST_CLK   | -0.3    |         | 1.0            | V             |
| $I_{IH}$ | Input High Current | TEST_CLK, MR, F_SEL0, F_SEL1, nPLL_SEL, nXTAL_SEL, $V_{CC} = V_{IN} = 3.63V$     |         |         | 150            | $\mu\text{A}$ |
| $I_{IL}$ | Input Low Current  | TEST_CLK, MR, F_SEL0, F_SEL1, nPLL_SEL, nXTAL_SEL, $V_{CC} = 3.63V, V_{IN} = 0V$ | -150    |         |                | $\mu\text{A}$ |

**TABLE 3C. LVPECL DC CHARACTERISTICS,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 10\%$ ,  $T_A = -30^\circ\text{C}$  TO  $85^\circ\text{C}$**

| Symbol      | Parameter                         | Test Conditions | Minimum         | Typical | Maximum         | Units |
|-------------|-----------------------------------|-----------------|-----------------|---------|-----------------|-------|
| $V_{OH}$    | Output High Voltage; NOTE 1       |                 | $V_{CCO} - 1.4$ |         | $V_{CCO} - 0.9$ | V     |
| $V_{OL}$    | Output Low Voltage; NOTE 1        |                 | $V_{CCO} - 2.0$ |         | $V_{CCO} - 1.7$ | V     |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing |                 | 0.6             |         | 1.0             | V     |

NOTE 1: Outputs terminated with 50 $\Omega$  to  $V_{CCO} - 2V$ .

**TABLE 4. CRYSTAL CHARACTERISTICS**

| Parameter                          | Test Conditions | Minimum     | Typical | Maximum | Units    |
|------------------------------------|-----------------|-------------|---------|---------|----------|
| Mode of Oscillation                |                 | Fundamental |         |         |          |
| Frequency                          |                 | 23.33       | 26.5625 | 28.33   | MHz      |
| Equivalent Series Resistance (ESR) |                 |             |         | 50      | $\Omega$ |
| Shunt Capacitance                  |                 |             |         | 7       | pF       |

NOTE: Characterized using an 18pF parallel resonant crystal.

**TABLE 5. AC CHARACTERISTICS,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 10\%$ ,  $T_A = -30^\circ\text{C}$  TO  $85^\circ\text{C}$** 

| Symbol              | Parameter                            | Test Conditions              | Minimum | Typical | Maximum | Units |
|---------------------|--------------------------------------|------------------------------|---------|---------|---------|-------|
| $f_{OUT}$           | Output Frequency                     | F_SEL[1:0] = 00              | 186.67  |         | 226.67  | MHz   |
|                     |                                      | F_SEL[1:0] = 01              | 140     |         | 170     | MHz   |
|                     |                                      | F_SEL[1:0] = 10              | 93.33   |         | 113.33  | MHz   |
|                     |                                      | F_SEL[1:0] = 11              | 46.67   |         | 56.67   | MHz   |
| tsk(o)              | Output Skew; NOTE 1, 2               |                              |         |         | 20      | ps    |
| tjit( $\emptyset$ ) | RMS Phase Jitter (Random);<br>NOTE 3 | 212.5MHz, (637KHz - 10MHz)   |         | 0.72    |         | ps    |
|                     |                                      | 159.375MHz, (637KHz - 10MHz) |         | 0.76    |         | ps    |
|                     |                                      | 106.25MHz, (637KHz - 10MHz)  |         | 0.84    |         | ps    |
|                     |                                      | 53.125MHz, (637KHz - 10MHz)  |         | 0.97    |         | ps    |
| $t_R / t_F$         | Output Rise/Fall Time                | 20% to 80%                   | 300     |         | 600     | ps    |
| odc                 | Output Duty Cycle                    | F_SEL[1:0] = 00              | 46      |         | 54      | %     |
|                     |                                      | F_SEL[1:0] = 01              | 49      |         | 51      | %     |

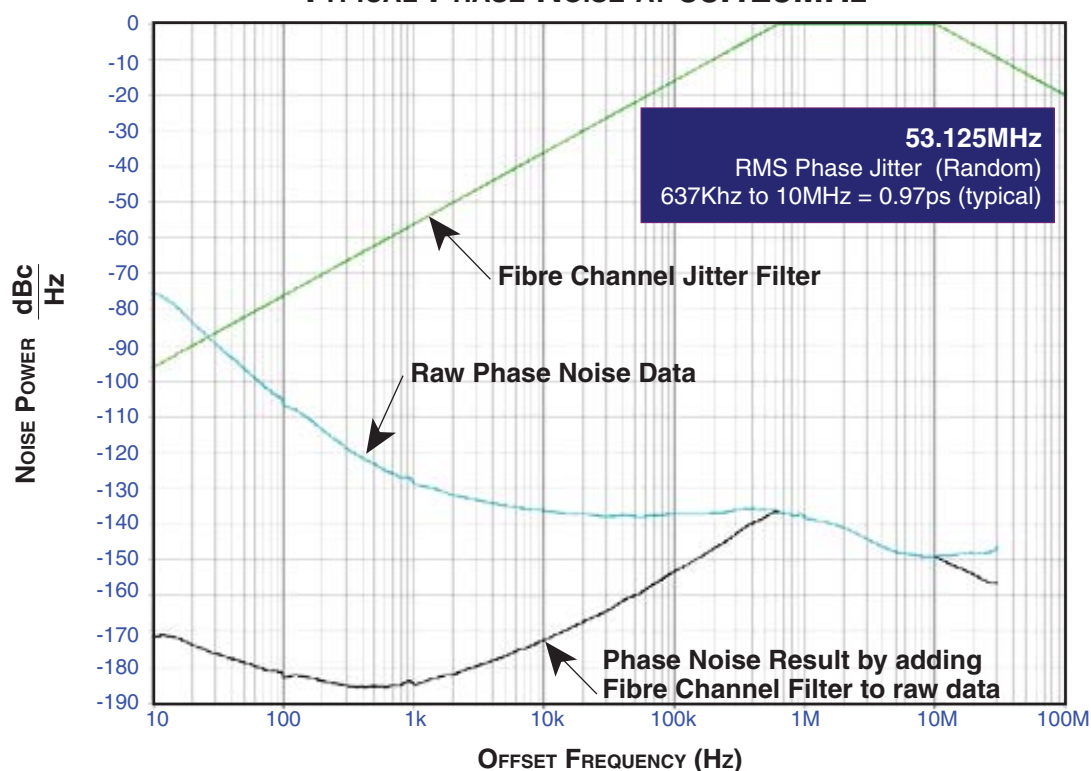
NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions.

Measured at  $V_{CCO}/2$ .

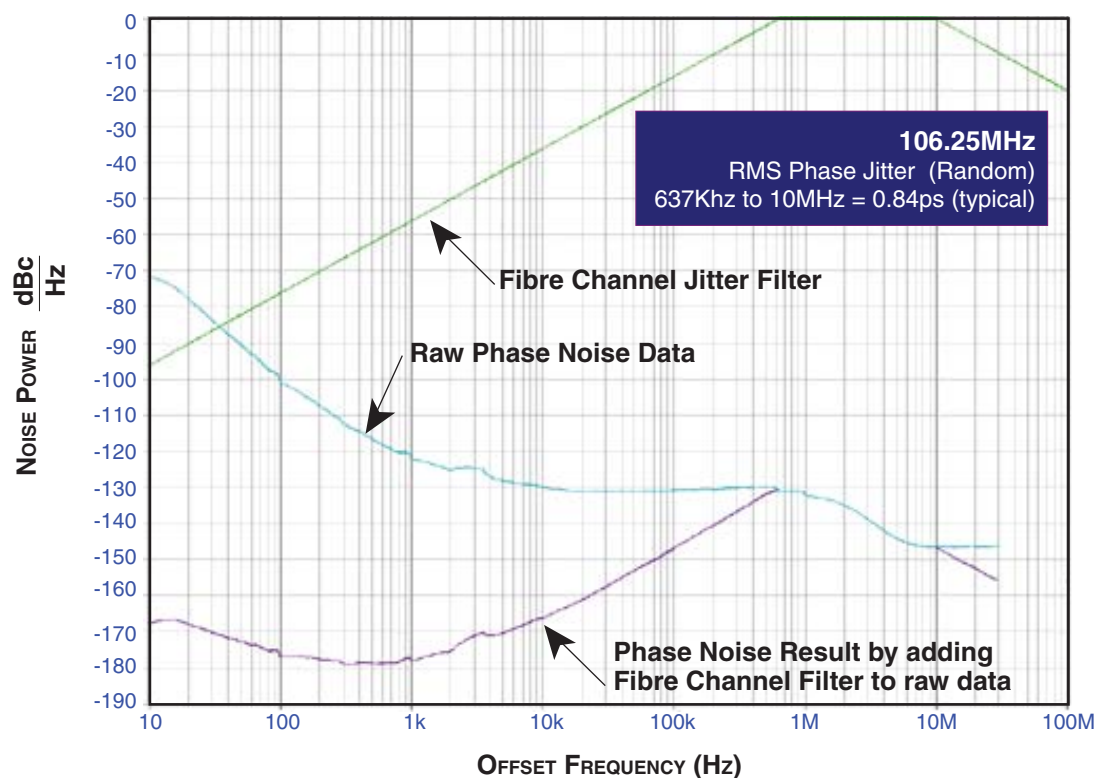
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: See Phase Noise plot.

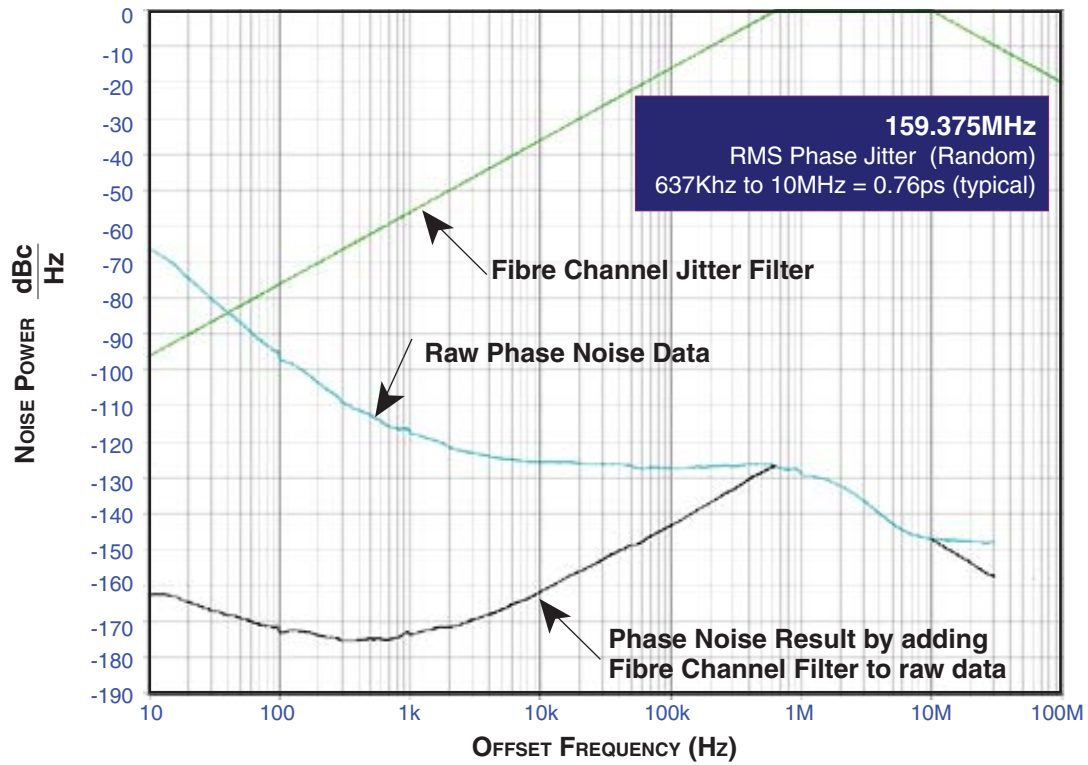
### TYPICAL PHASE NOISE AT 53.125MHz



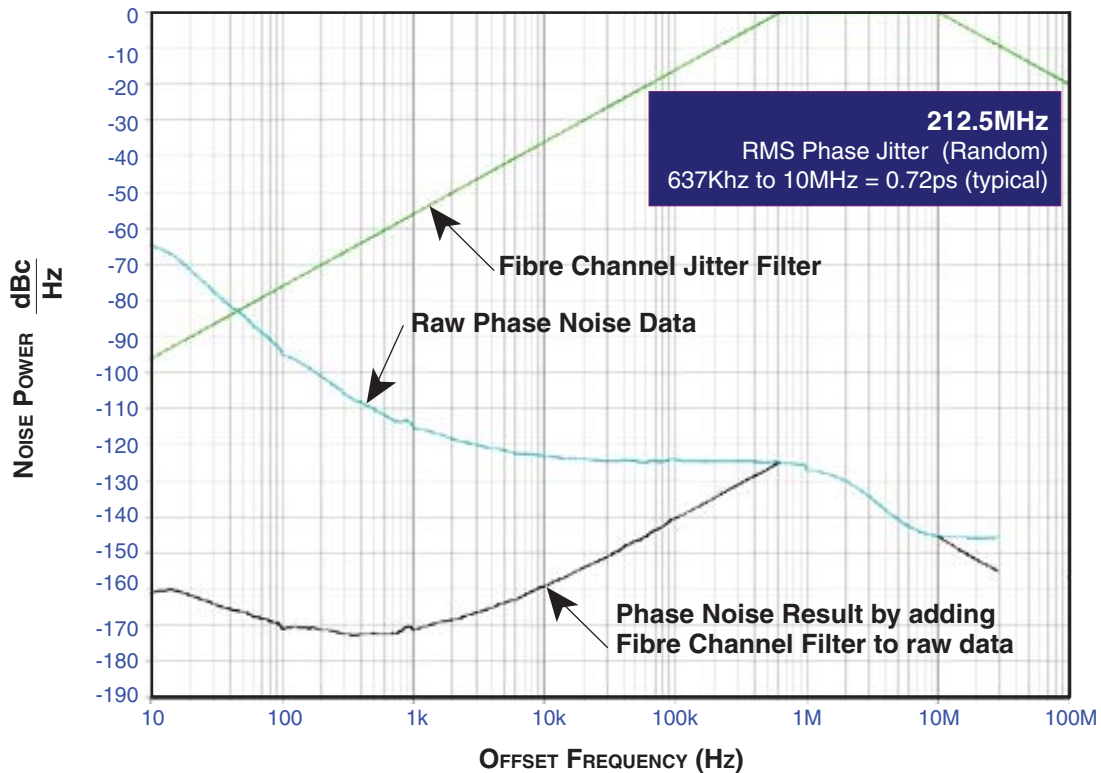
### TYPICAL PHASE NOISE AT 106.25MHz



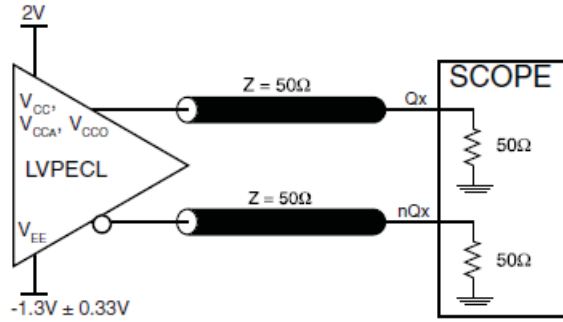
### TYPICAL PHASE NOISE AT 159.375MHz



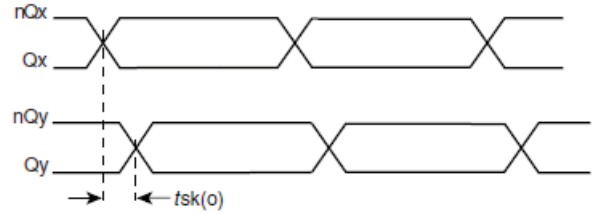
### TYPICAL PHASE NOISE AT 212.5MHz



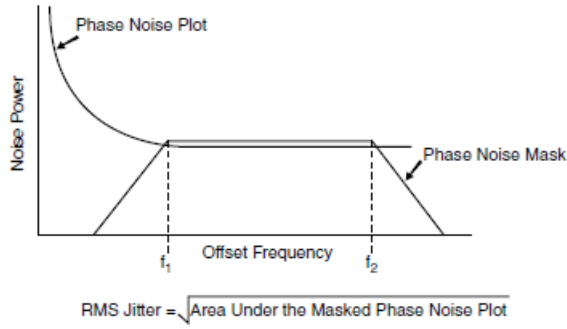
## PARAMETER MEASUREMENT INFORMATION



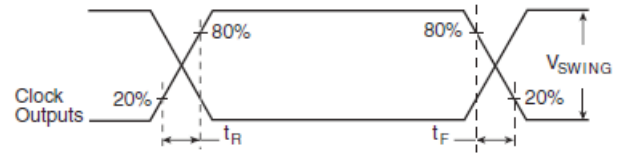
3.3V CORE/3.3V OUTPUT LOAD TEST CIRCUIT



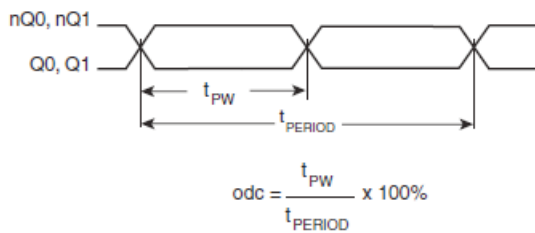
OUTPUT SKEW



RMS PHASE JITTER



OUTPUT RISE/FALL TIME



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

## APPLICATIONS INFORMATION

### POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The 843002 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{CC}$ ,  $V_{CCA}$ , and  $V_{CCO}$  should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. Figure 1 illustrates how a 10Ω resistor along with a 10μF and a .01μF bypass capacitor should be connected to each  $V_{CCA}$ .

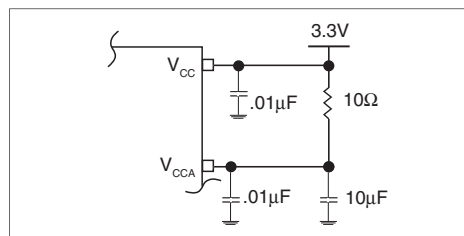


FIGURE 1. POWER SUPPLY FILTERING

### TERMINATION FOR 3.3V LVPECL OUTPUT

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

Differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to

drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. Figures 2A and 2B show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

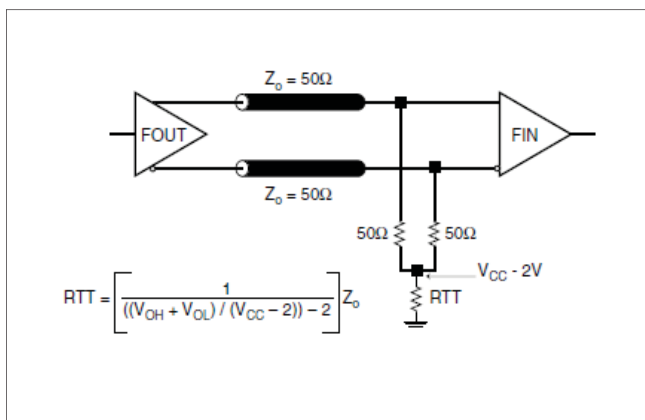


FIGURE 2A. LVPECL OUTPUT TERMINATION

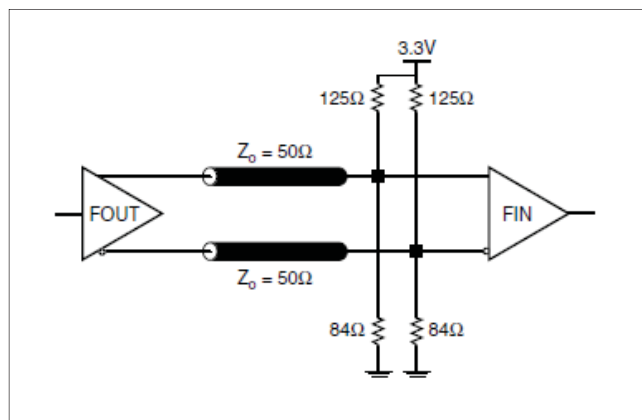
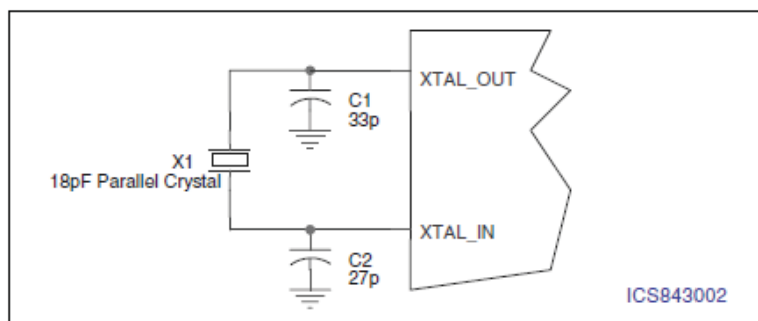


FIGURE 2B. LVPECL OUTPUT TERMINATION



## CRYSTAL INPUT INTERFACE

The 843002 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 3* below were determined using a 26.5625MHz 18pF parallel resonant crystal and were chosen to minimize the ppm error.



**Figure 3. CRYSTAL INPUT INTERFACE**

## LAYOUT GUIDELINE

Figure 4A shows a schematic example of the 843002. An example of LVEPCL termination is shown in this schematic. Additional LVPECL termination approaches are shown in the LVPECL Termination Application Note. In this example, an 18

pF parallel resonant 26.5625MHz crystal is used. The C1=27pF and C2=33pF are recommended for frequency accuracy. For different board layout, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy.

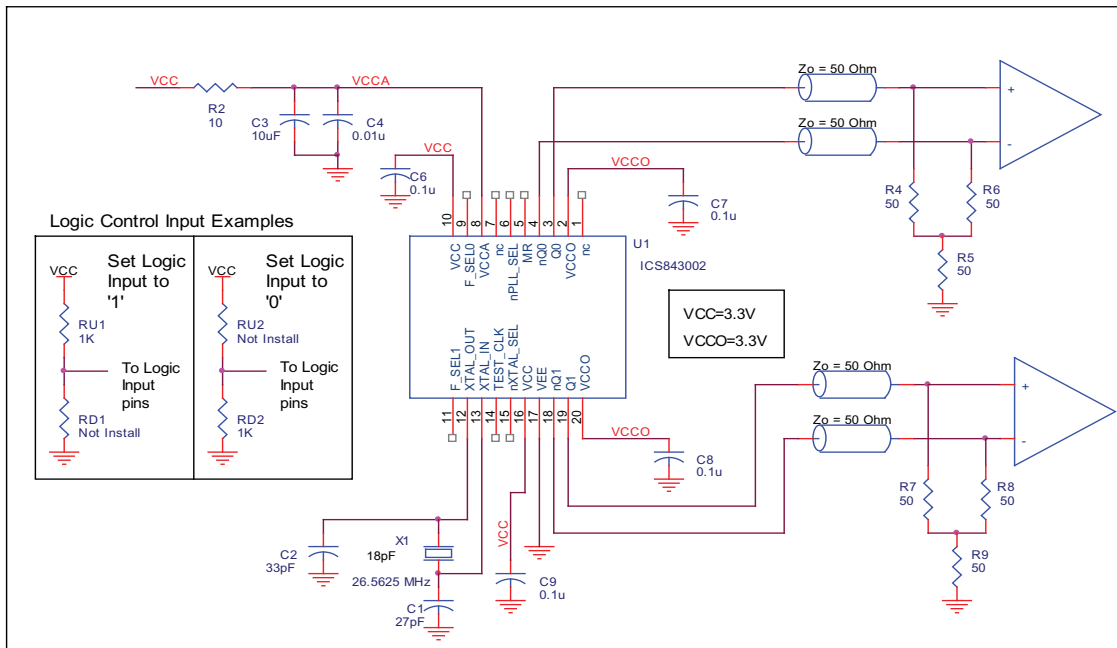


FIGURE 4A. 843002 SCHEMATIC EXAMPLE

## PC BOARD LAYOUT EXAMPLE

Figure 4B shows an example of 843002 P.C. board layout. The crystal X1 footprint shown in this example allows installation of either surface mount HC49S or through-hole HC49 package. The footprints of other components in this example are listed in

the Table 6. There should be at least one decoupling capacitor per power pin. The decoupling capacitors should be located as close as possible to the power pins. The layout assumes that the board has clean analog power ground plane.

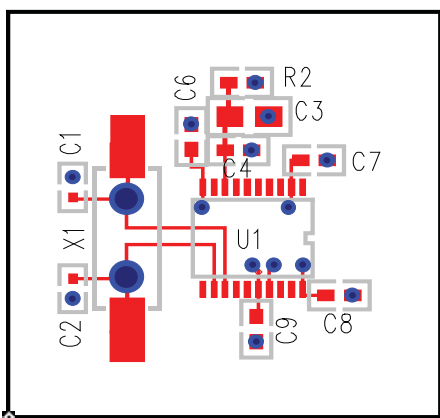


FIGURE 4B. 843002 PC BOARD LAYOUT EXAMPLE

TABLE 6. FOOTPRINT TABLE

| Reference          | Size |
|--------------------|------|
| C1, C2             | 0402 |
| C3                 |      |
| C4, C5, C6, C7, C8 |      |
| R2                 |      |

NOTE: Table 6, lists component sizes shown in this layout example.

## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 843002. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 843002 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 10\% = 3.63V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.63V * 135mA = 490mW$

- Power (outputs)<sub>MAX</sub> = **30mW/Loaded Output pair**

If all outputs are loaded, the total power is  $2 * 30mW = 60mW$

**Total Power**<sub>MAX</sub> (3.63V, with all outputs switching) =  $490mW + 60mW = 550mW$

### 2. Junction Temperature.

Junction temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 7 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.550W * 66.6^\circ C/W = 121.6^\circ C. \text{ This is below the limit of } 125^\circ C.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**TABLE 7. THERMAL RESISTANCE  $\theta_{JA}$  FOR 20-PIN TSSOP, FORCED CONVECTION**

| <b><math>\theta_{JA}</math> by Velocity (Linear Feet per Minute)</b>  |           |            |            |
|---|-----------|------------|------------|
|   | <b>0</b>  | <b>200</b> | <b>500</b> |
| Single-Layer PCB, JEDEC Standard Test Boards  | 114.5°C/W | 98.0°C/W   | 88.0°C/W   |
| Multi-Layer PCB, JEDEC Standard Test Boards   | 73.2°C/W  | 66.6°C/W   | 63.5°C/W   |
| <b>NOTE:</b> Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs. |           |            |            |

### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 5*.

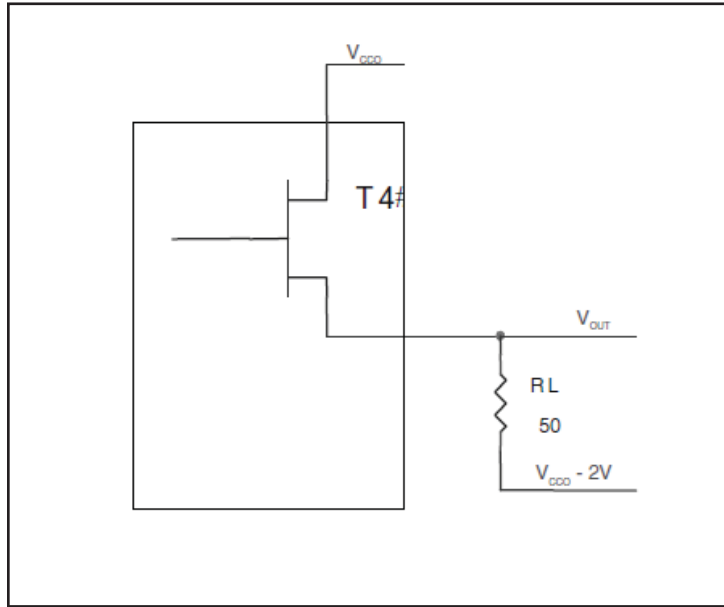


FIGURE 5. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CCO} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CCO\_MAX} - 0.9V$   
 $(V_{CCO\_MAX} - V_{OH\_MAX}) = 0.9V$
- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CCO\_MAX} - 1.7V$   
 $(V_{CCO\_MAX} - V_{OL\_MAX}) = 1.7V$

$Pd\_H$  is power dissipation when the output drives high.  
 $Pd\_L$  is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = 19.8mW$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

$$\text{Total Power Dissipation per output pair} = Pd\_H + Pd\_L = 30mW$$

RELIABILITY INFORMATION

TABLE 8.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 20 LEAD TSSOP

| $\theta_{JA}$ by Velocity (Linear Feet per Minute)  |           |          |          |
|---|-----------|----------|----------|
|   | 0         | 200      | 500      |
| Single-Layer PCB, JEDEC Standard Test Boards  | 114.5°C/W | 98.0°C/W | 88.0°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards   | 73.2°C/W  | 66.6°C/W | 63.5°C/W |
| <b>NOTE:</b> Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs. |           |          |          |

TRANSISTOR COUNT

The transistor count for 843002 is: 2578

PACKAGE OUTLINE - G SUFFIX FOR 20 LEAD TSSOP

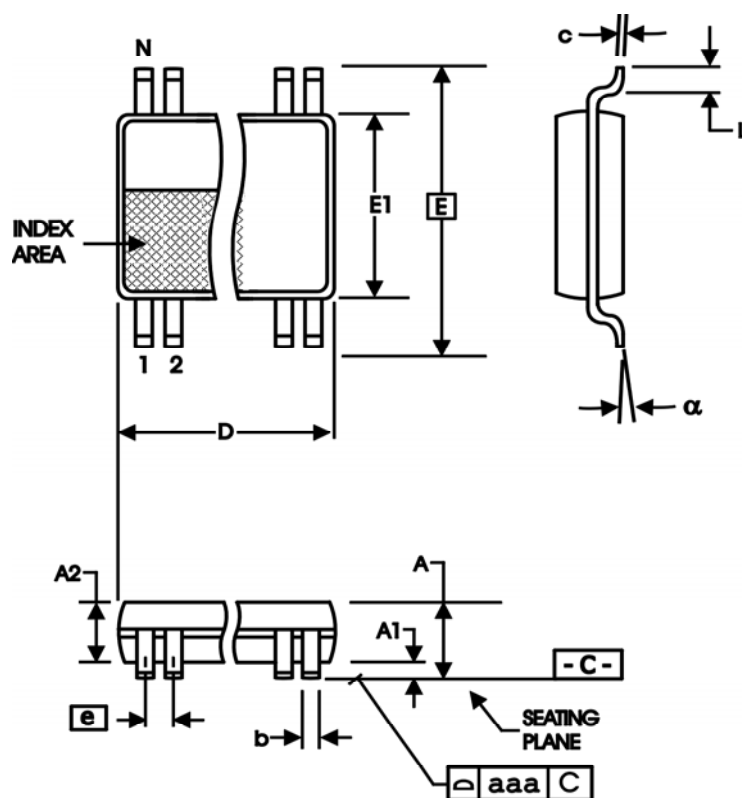


TABLE 9. PACKAGE DIMENSIONS

| SYMBOL   | Millimeters |      |
|----------|-------------|------|
|          | MIN         | MAX  |
| N        | 20          |      |
| A        | --          | 1.20 |
| A1       | 0.05        | 0.15 |
| A2       | 0.80        | 1.05 |
| b        | 0.19        | 0.30 |
| c        | 0.09        | 0.20 |
| D        | 6.40        | 6.60 |
| E        | 6.40 BASIC  |      |
| E1       | 4.30        | 4.50 |
| e        | 0.65 BASIC  |      |
| L        | 0.45        | 0.75 |
| $\alpha$ | 0°          | 8°   |
| aaa      | --          | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

**TABLE 10. ORDERING INFORMATION**

| Part/Order Number | Marking      | Package                   | Shipping Packaging | Temperature   |
|-------------------|--------------|---------------------------|--------------------|---------------|
| 843002AGLF        | ICS843002AGL | 20 Lead "Lead-Free" TSSOP | tube               | -30°C to 85°C |
| 843002AGLFT       | ICS843002AGL | 20 Lead "Lead-Free" TSSOP | tape & reel        | -30°C to 85°C |

| REVISION HISTORY SHEET |       |      |  |          |
|------------------------|-------|------|--|----------|
| Rev                    | Table | Page | Description of Change  | Date     |
| A                      |       | 1    | Added 187.5MHz to the Frequency Selection Function Table.  | 8/26/04  |
| A                      | T10   | 15   | Ordering Information Table - added Lead Free part number.  | 9/30/04  |
| A                      | T5    | 4    | AC Characteristics Table - corrected typo, $f_{OUT}$ 180.67 min. to 186.67 min.  | 12/27/04 |
| A                      | T10   | 1    | Features section - corrected frequency bullet to read "Supports...output frequencies..." from "...input frequencies..."  | 2/7/05   |
|                        |       | 15   | Ordering Information Table - updated table.  |          |
| B                      | T5    | 4    | AC Characteristics Table - deleted Propagation Delay.  | 5/6/05   |
| B                      | T10   | 14   | Ordering Information Table - corrected lead-free marking.<br>Updated Datasheet Header and Footer.  | 4/17/13  |
| B                      | T10   | 1    | Deleted ICS from part numbers where needed.  | 1/21/16  |
|                        |       | 15   | Corrected part number in the header.<br>Ordering Information - Corrected Package information from 8 Lead TSSOP to 20 Lead TSSOP. Added T to tape and reel part number.<br>Updated header and footer. |          |





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