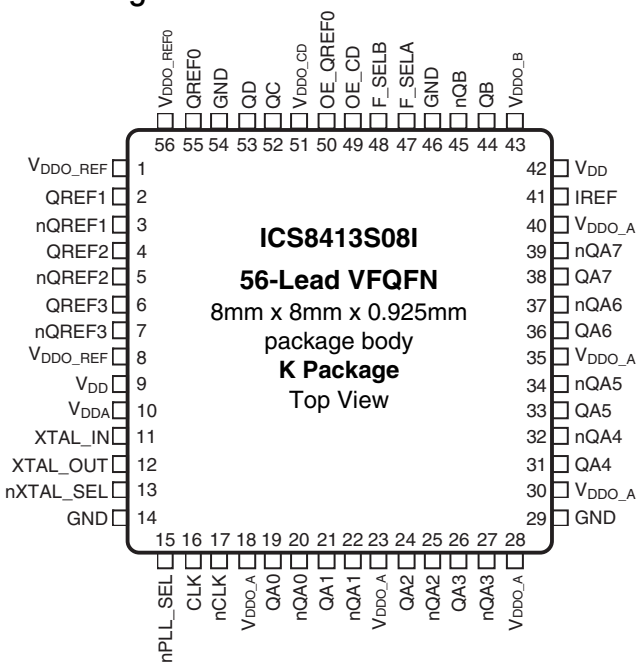
## General Description

The 8413S08 is a high performance PLL-based clock generator optimized for processor core, PCI/PCI-X/PCIe bus, SGMII and Gigabit Ethernet PHY clocks. The clock generator offers ultra-low jitter outputs that make it ideal to serve as a central clocking device for multiple clock destinations. The output frequencies are generated from a 25MHz parallel resonant crystal, or external differential input source. The industrial temperature range of the 8413S08 supports tele-communication, networking and storage requirements.

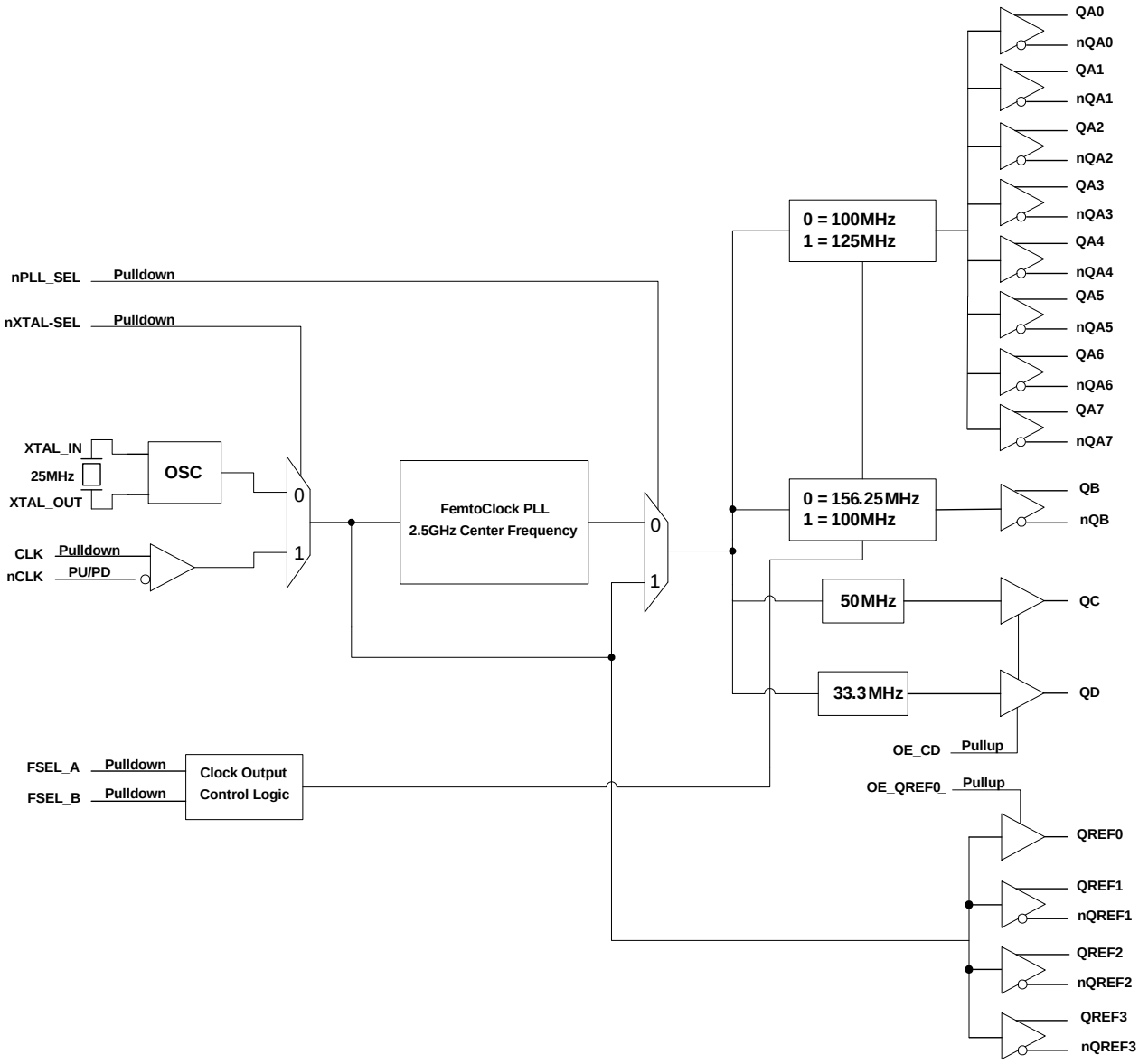
## Features

- Eight selectable 100MHz or 125MHz clocks for PCI Express™ and sRIO, HCSL interface levels
- One 156.25MHz SGMII clock, LVPECL interface levels
- Three LVCMOS/LVTTL outputs, 20Ω output impedance
- Selectable external crystal or differential (single-ended) input source
- Crystal oscillator interface designed for 25MHz, parallel resonant crystal
- Differential CLK, nCLK input pair that can accept: LVPECL, LVDS, LVHSTL, HCSL input levels
- Internal resistor bias on nCLK pin allows the user to drive CLK input with external single-ended (LVCMOS/ LVTTL) input levels
- Output supply voltage modes:
  $V_{DD}$ / $V_{DDO}$
  3.3V/3.3V
  3.3V/2.5V
- Full 3.3V output supply mode (HCSL)
- PCI Express™ (2.5 Gb/s), Gen 2 (5 Gb/s), and Gen 3 (8 Gb/s) jitter compliant
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

## Pin Assignment



## Block Diagram



## Table 1. Pin Descriptions

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1, 8 | $V_{DDO\_REF}$ | Power | | QREF[1:3], nQREF[1:3] (LVPECL) output supply pins. 3.3V or 2.5V supply. |
| 2, 3 | QREF1, nQREF1 | Output | | Differential reference output pair. 3.3V or 2.5V LVPECL interface levels. |
| 4, 5 | QREF2, nQREF2 | Output | | Differential reference output pair. 3.3V or 2.5V LVPECL interface levels. |
| 6, 7 | QREF3, nQREF3 | Output | | Differential reference output pair. 3.3V or 2.5V LVPECL interface levels. |
| 9, 42 | $V_{DD}$ | Power | | Core supply pins. |
| 10 | $V_{DDA}$ | Power | | Analog supply pin. |
| 11, 12 | XTAL_IN, XTAL_OUT | Input | | Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input. |
| 13 | nXTAL_SEL | Input | Pulldown | Input source control pin. See Table 3D. LVCMOS/LVTTL interface levels. |
| 14, 29, 46, 54 | GND | Power | | Power supply ground. |
| 15 | nPLL_SEL | Input | Pulldown | PLL bypass control pin. See Table 3C. LVCMOS/LVTTL interface levels. |
| 16 | CLK | Input | Pulldown | Non-inverting differential clock input. |
| 17 | nCLK | Input | Pullup/ Pulldown | Inverting differential clock input. Internal resistor bias to $V_{DD}/2$. |
| 18, 23, 28, 30, 35, 40 | $V_{DDO\_A}$ | Power | | Bank A (HCSL) output supply pins. 3.3V supply. |
| 19, 20 | QA0, nQA0 | Output | | Differential output pair. HCSL interface levels. |
| 21, 22 | QA1, nQA1 | Output | | Differential output pair. HCSL interface levels. |
| 24, 25 | QA2, nQA2 | Output | | Differential output pair. HCSL interface levels. |
| 26, 27 | QA3, nQA3 | Output | | Differential output pair. HCSL interface levels. |
| 31, 32 | QA4, nQA4 | Output | | Differential output pair. HCSL interface levels. |
| 33, 34 | QA5, nQA5 | Output | | Differential output pair. HCSL interface levels. |
| 36, 37 | QA6, nQA6 | Output | | Differential output pair. HCSL interface levels. |
| 38, 39 | QA7, nQA7 | Output | | Differential output pair. HCSL interface levels. |
| 41 | $I_{REF}$ | Input | | External fixed precision resistor (475Ω) from this pin to ground provides a reference current used for differential current-mode QAx, nQAx outputs. |
| 43 | $V_{DDO\_B}$ | Power | | Bank B (LVPECL) output supply pin. 3.3V or 2.5V supply. |
| 44, 45 | QB, nQB | Output | | Differential output pair. 3.3V or 2.5V LVPECL interface levels. |
| 47 | F_SELA | Input | Pulldown | Selects the QAx, nQAx output frequency. See Table 3A. LVCMOS/LVTTL interface levels. |
| 48 | F_SELB | Input | Pulldown | Selects the QB output frequency. See Table 3B. LVCMOS/LVTTL interface levels. |
| 49 | OE_CD | Input | Pullup | Active HIGH output enable for Bank C and Bank D outputs. See Table 3E. LVCMOS/LVTTL interface levels. |
| 50 | OE_QREF0 | Input | Pullup | Active HIGH output enable for QREF0 output. See Table 3F. LVCMOS/LVTTL interface levels. |

Pin Descriptions continues on next page.

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 51 | $V_{DDO\_CD}$ | Power | | Bank C and D (LVCMOS) output supply pin. 3.3V or 2.5V supply. |
| 52 | QC | Output | | Single-ended output. 3.3V or 2.5V LVCMOS/LVTTL interface levels. |
| 53 | QD | Output | | Single-ended output. 3.3V or 2.5V LVCMOS/LVTTL interface levels. |
| 55 | QREF0 | Output | | Single-ended reference output. 3.3V or 2.5V LVCMOS/LVTTL interface levels. |
| 56 | $V_{DDO\_REF0}$ | Power | | QREF0 (LVCMOS) output supply pin. 3.3V or 2.5V supply. |

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

## Table 2. Pin Characteristics

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | | 2 | | pF |
| $C_{PD}$ | Power Dissipation Capacitance (per output) | | $V_{DD}$, $V_{DDO\_A}$, $V_{DDO\_B}$, $V_{DDO\_CD}$, $V_{DDO\_QREF0}$, $V_{DDO\_QREF}$ = 3.465V | | 4 | | pF |
| | | | $V_{DD}$ = 3.465V, $V_{DDO\_B}$, $V_{DDO\_CD}$, $V_{DDO\_QREF0}$ = 2.625V | | 4 | | pF |
| $R_{PULLUP}$ | Input Pullup Resistor | | | | 51 | | kΩ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | | 51 | | kΩ |
| $R_{OUT}$ | Output Impedance | QC, QD, QREF0 | $V_{DDO\_CD}$, $V_{DDO\_QREF0}$ = 3.465V | | 20 | | Ω |
| | | QC, QD, QREF0 | $V_{DDO\_CD}$, $V_{DDO\_QREF0}$ = 2.625V | | 25 | | Ω |

## Function Tables

**Table 3A. QAx, nQAx Control Input Function Table**

| Input | Output Frequency |
|---|---|
| **FSEL_A** | **QAx, nQAx[0:7]** |
| 0 (default) | 100MHz |
| 1 | 125MHz |

**Table 3B. QB, nQB Control Input Function Table**

| Input | Output Frequency |
|---|---|
| **FSEL_B** | **QB, nQB** |
| 0 (default) | 156.25MHz |
| 1 | 100MHz |

**Table 3C. nPLL_SEL Control Input Function Table**

| Input | |
|---|---|
| **nPLL_SEL** | **Operation** |
| 0 (default) | PLL Mode |
| 1 | PLL Bypass |

**Table 3D. nXTAL_SEL Control Input Function Table**

| Input | |
|---|---|
| **nXTAL_SEL** | **Clock Source** |
| 0 (default) | XTAL_IN, XTAL_OUT |
| 1 | CLK, nCLK |

**Table 3E. OE_CD Control Input Function Table**

| Input | Outputs |
|---|---|
| **OE_CD** | **QC, QD** |
| 0 | High-Impedance |
| 1(default) | Enabled |

**able 3F. OE_QREF0 Control Input Function Table**

| Input | Output |
|---|---|
| **OE_QREF0** | **QREF0** |
| 0 | High-Impedance |
| 1(default) | Enabled |

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|---|---|
| Supply Voltage, $V_{DD}$ | 4.6V |
| Inputs, $V_I$<br>XTAL_in<br>Other Inputs | -0.5V to $V_{DD}$ + 0.5V<br>0V to $V_{DD}$<br>-0.5V to $V_{DD}$ + 0.5V |
| Outputs, $V_O$ (LVCMOS) | -0.5V to $V_{DD}$ + 0.5V |
| Outputs, $I_O$ (HCSL)<br>Continuos Current<br>Surge Current | <br>10mA<br>15mA |
| Outputs, $I_O$ (LVPECL)<br>Continuos Current<br>Surge Current | <br>50mA<br>100mA |
| Package Thermal Impedance, $\theta_{JA}$ | 31.4°C/W (0 mps) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,** $V_{DD} = V_{DDO\_X} = 3.3V \pm 5\%$, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{DDA}$ | Analog Supply Voltage | | $V_{DD}$ – 0.16 | 3.3 | $V_{DD}$ | V |
| $V_{DDO\_X}$ | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $I_{DD}$ | Power Supply Current | | | | 84 | mA |
| $I_{DDA}$ | Analog Supply Current | | | | 16 | mA |
| $I_{DDO\_X}$ | Output Supply Current | No Load, CLK selected | | | 66 | mA |

**NOTE:** $V_{DDO\_X}$ denotes $V_{DDO\_A}$, $V_{DDO\_B}$, $V_{DDO\_CD}$, $V_{DDO\_QREF0}$, $V_{DDO\_QREF}$.
**NOTE:** $I_{DDO\_X}$ denotes $I_{DDO\_A}$, $I_{DDO\_B}$, $I_{DDO\_CD}$, $I_{DDO\_QREF0}$, $I_{DDO\_QREF}$.

**Table 4B. Power Supply DC Characteristics,** $V_{DD} = 3.3V \pm 5\%$, $V_{DDO\_X} = 2.5V \pm 5\%$, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{DDA}$ | Analog Supply Voltage | | $V_{DD}$ – 0.16 | 3.3 | $V_{DD}$ | V |
| $V_{DDO\_X}$ | Output Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| $I_{DD}$ | Power Supply Current | | | | 84 | mA |
| $I_{DDA}$ | Analog Supply Current | | | | 16 | mA |
| $I_{DDO\_X}$ | Output Supply Current | No Load, CLK selected | | | 54 | mA |

**NOTE:** $V_{DDO\_X}$ denotes $V_{DDO\_B}$, $V_{DDO\_CD}$, $V_{DDO\_QREF0}$, $V_{DDO\_QREF}$.
**NOTE:** $I_{DDO\_X}$ denotes $I_{DDO\_B}$, $I_{DDO\_CD}$, $I_{DDO\_QREF0}$, $I_{DDO\_QREF}$.

**Table 4C. LVCMOS/LVTTL DC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $V_{DDO\_X}$ = 3.3V ± 5% or 2.5V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | | 2.2 | | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | | | -0.3 | | 0.8 | V |
| $I_{IH}$ | Input High Current | FSEL_A, FSEL_B, nXTAL_SEL, nPLL_SEL | $V_{DD}$ = $V_{IN}$ = 3.465V | | | 150 | µA |
| | | OE_CD, OE_QREF0 | $V_{DD}$ = $V_{IN}$ = 3.465V | | | 10 | uA |
| $I_{IL}$ | Input Low Current | FSEL_A, FSEL_B, nXTAL_SEL, nPLL_SEL | $V_{DD}$ = 3.465V, $V_{IN}$ = 0V | -10 | | | µA |
| | | OE_CD, OE_QREF0 | $V_{DD}$ = 3.465V, $V_{IN}$ = 0V | -150 | | | uA |
| $V_{OH}$ | Output High Voltage; NOTE 1 | | $V_{DDO\_X}$ = 3.465V | 2.6 | | | V |
| | | | $V_{DDO\_X}$ = 2.625V | 1.8 | | | V |
| $V_{OL}$ | Output Low Voltage: NOTE 1 | | $V_{DDO\_X}$ = 3.465V or 2.625V | | | 0.5 | V |

NOTE: $V_{DDO\_X}$ denotes $V_{DDO\_CD}$, $V_{DDO\_QREF0}$.
NOTE 1: Outputs terminated with 50Ω to $V_{DDO\_X}$/2. See Parameter Measurement Information, *Output Load Test Circuit diagrams.*

**Table 4D. Differential DC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $I_{IH}$ | Input High Current | CLK, nCLK | $V_{DD}$ = $V_{IN}$ = 3.465V | | | 150 | µA |
| $I_{IL}$ | Input Low Current | CLK | $V_{DD}$ = 3.465V, $V_{IN}$ = 0V | -10 | | | µA |
| | | nCLK | $V_{DD}$ = 3.465V, $V_{IN}$ = 0V | -150 | | | µA |
| $V_{PP}$ | Peak-to-Peak Input Voltage; NOTE 1 | | | 0.15 | | 1.3 | V |
| $V_{CMR}$ | Common Mode Input Voltage; NOTE 1, 2 | | | 0.5 | | $V_{DD}$ – 0.85 | V |

NOTE 1: $V_{IL}$ should not be less than -0.3V.
NOTE 2. Common mode voltage is defined as $V_{IH}$.

**Table 4E. LVPECL DC Characteristics,** $V_{DD}$ = $V_{DDO\_B}$ = $V_{DDO\_REF}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage; NOTE 1 | | $V_{DDO\_X}$ – 1.4 | | $V_{DDO\_X}$ – 0.9 | V |
| $V_{OL}$ | Output Low Voltage; NOTE 1 | | $V_{DDO\_X}$ – 2.0 | | $V_{DDO\_X}$ – 1.7 | V |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing | | 0.6 | | 1.0 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{DDO\_X}$ – 2V.

**Table 4F. LVPECL DC Characteristics,** $V_{DD}$ = 3.3V± 5%, $V_{DDO\_B}$ = $V_{DDO\_REF}$ = 2.5V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage; NOTE 1 | | $V_{DDO\_X}$ – 1.4 | | $V_{DDO\_X}$ – 0.9 | V |
| $V_{OL}$ | Output Low Voltage; NOTE 1 | | $V_{DDO\_X}$ – 2.0 | | $V_{DDO\_X}$ – 1.5 | V |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing | | 0.4 | | 1.0 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{DDO\_X}$ – 2V.

**Table 5. Crystal Characteristics**

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| Mode of Oscillation | | Fundamental | | | |
| Frequency | | | 25 | | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |

NOTE: Characterized using an 18pF parallel resonant crystal.

# AC Electrical Characteristics

**Table 6A. PCI Express Jitter Specifications,** $V_{DD}$ = 3.3V ± 5%, $V_{DDO\_X}$ = 3.3V ± 5% or 2.5V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | PCIe Industry Specification | Units |
|---|---|---|---|---|---|---|---|
| $t_j$ (PCIe Gen 1) | Phase Jitter Peak-to-Peak; NOTE 1, 4 | ƒ = 100MHz, 25MHz Crystal Input Evaluation Band: 0Hz - Nyquist (clock frequency/2) | | 11.51 | 17.45 | 86 | ps |
| $t_{REFCLK\_HF\_RMS}$ (PCIe Gen 2) | Phase Jitter RMS; NOTE 2, 4 | ƒ = 100MHz, 25MHz Crystal Input High Band: 1.5MHz - Nyquist (clock frequency/2) | | 1.08 | 1.67 | 3.10 | ps |
| $t_{REFCLK\_LF\_RMS}$ (PCIe Gen 2) | Phase Jitter RMS; NOTE 2, 4 | ƒ = 100MHz, 25MHz Crystal Input Low Band: 10kHz - 1.5MHz | | 0.06 | 0.11 | 3.0 | ps |
| $t_{REFCLK\_RMS}$ (PCIe Gen 3) | Phase Jitter RMS; NOTE 3, 4 | ƒ = 100MHz, 25MHz Crystal Input Evaluation Band: 0Hz - Nyquist (clock frequency/2) | | 0.26 | 0.38 | 0.8 | ps |

**NOTE:** Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions. For additional information, refer to the *PCI Express Application Note section* in the datasheet.
**NOTE 1:** Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1 is 86ps peak-to-peak for a sample size of $10^6$ clock periods.
**NOTE 2:** RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for $t_{REFCLK\_HF\_RMS}$ (High Band) and 3.0ps RMS for $t_{REFCLK\_LF\_RMS}$ (Low Band).
**NOTE 3:** RMS jitter after applying system transfer function for the common clock architecture. This specification is based on the *PCI Express Base Specification Revision 0.7, October 2009* and is subject to change pending the final release version of the specification.
**NOTE 4:** This parameter is guaranteed by characterization. Not tested in production.

**Table 6B. AC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $V_{DDO\_X}$ = 3.3V ± 5% or 2.5V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency | QB, nQB | FSEL_B = 0 | | 156.25 | | MHz |
| | | | FSEL_B = 1 | | 100 | | MHz |
| | | QC | | | 50 | | MHz |
| | | QD | | | 33.333 | | MHz |
| tjit(cc) | Cycle-to-Cycle Jitter; NOTE 2, 3 | QB, nQB | | | 47 | 80 | ps |
| | | QC | | | 155 | 200 | ps |
| | | QD | | | 105 | 185 | ps |
| tjit(Ø) | RMS Phase Jitter, (Random); NOTE 1 | QREF0 | 25MHz (10kHz to 5MHz) | | 0.61 | 0.82 | ps |
| | | QREF[1:3], nQREF[1:3] | 25MHz (10kHz to 5MHz) | | 0.51 | 0.70 | ps |
| | | QB, nQB | 156.25MHz (12kHz to 20MHz) | | 0.58 | 0.72 | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | QB, nQB | 20% to 80% | 110 | | 225 | ps |
| | | QC, QD | | 400 | | 1400 | ps |
| | | QREF0 | | 400 | | 1400 | ps |
| | | QREF[1:3] nQREF[1:3] | | 110 | | 225 | ps |
| odc | Output Duty Cycle | QB, nQB | measured at crosspoint | 48 | | 52 | % |
| | | QC, QD | measured at $V_{DDO\_CD}$/2 | 48 | | 52 | % |
| | | QREF0 | measured at $V_{DDO\_QREF0}$/2 | 45 | | 55 | % |
| | | QREF[1:3], nQREF[1:3] | measured at crosspoint | 45 | | 55 | % |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: $V_{DDO\_X}$ denotes $V_{DDO\_B}$, $V_{DDO\_CD}$, $V_{DDO\_QREF}$ and $V_{DDO\_QREF0}$.
NOTE 1: Refer to the phase noise plots.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Jitter performance using XTAL inputs.

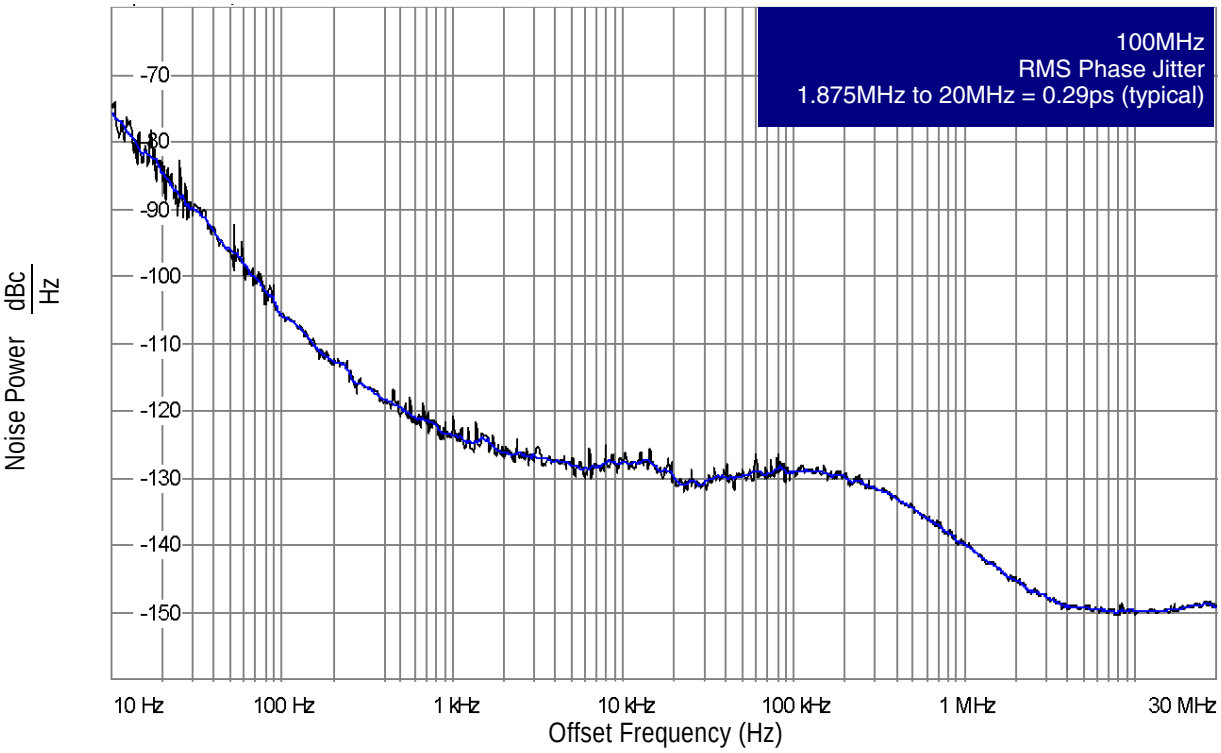
## HCSL AC Electrical Characteristics

**Table 6C. HCSL AC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $V_{DDO\_A}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C

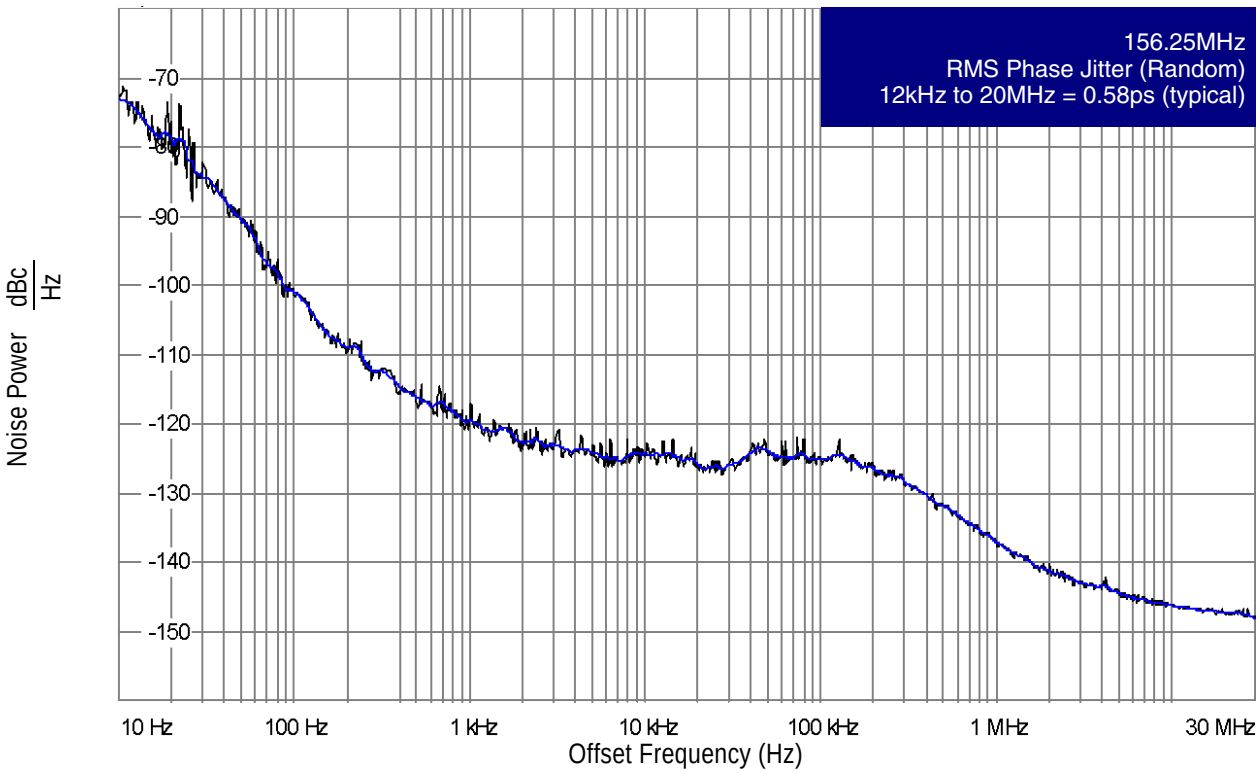
| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency | FSEL_A = 0 | | 100 | | MHz |
| | | FSEL_A = 1 | | 125 | | MHz |
| tjit(cc) | Cycle-to-Cycle Jitter; NOTE 1, 2 | | | 54 | 80 | ps |
| tsk(o) | Output Skew; NOTE 2, 3 | | | 30 | 100 | ps |
| tjit(Ø) | RMS Phase Jitter, (Random); NOTE 4 | 100MHz (1.875MHz to 20MHz) | | 0.29 | 0.37 | ps |
| | | 100MHz (12kHz to 20MHz) | | 0.63 | 0.81 | ps |
| $V_{RB}$ | Ring-Back Voltage Margin; NOTE 5, 6 | | -100 | | 100 | mV |
| $t_{STABLE}$ | Time before $V_{RB}$ is allowed; NOTE 5, 6 | | 500 | | | ps |
| $V_{MAX}$ | Absolute Max Output Voltage; NOTE 7, 8 | | | | 1150 | mV |
| $V_{MIN}$ | Absolute Min Output Voltage; NOTE 7, 9 | | -300 | | | mV |
| $V_{CROSS}$ | Absolute Crossing Voltage; NOTE 7, 10, 11 | | 250 | | 550 | mV |
| $\Delta V_{CROSS}$ | Total Variation of $V_{CROSS}$ over All Edges; NOTE 7, 10, 12 | | | | 140 | mV |
| $t_{SLEW+}$ | Rising Edge Rate; NOTE 5, 13 | | 0.6 | | 5.5 | V/ns |
| $t_{SLEW-}$ | Falling Edge Rate; NOTE 5, 13 | | 0.6 | | 5.5 | V/ns |
| odc | Output Duty Cycle; NOTE 6 | | 48 | | 52 | % |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
All parameters measured at $f_{OUT}$ unless noted otherwise.
NOTE 1: Jitter performance using XTAL inputs.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.
NOTE 4: Refer to the Phase Noise Plot.
NOTE 5: Measurement taken from differential waveform.
NOTE 6: $t_{STABLE}$ is the time the differential clock must maintain a minimum ±150mV differential voltage after rising/falling edges before it is allowed to drop back into the Vrb ±100mV range. See Parameter Measurement Information Section.
NOTE 7: Measurement taken from single-ended waveform.
NOTE 8: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.
NOTE 9: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.
NOTE 10: Measured at the crossing point where the instantaneous voltage value of the rising edge of Q[Ax:Ex] equals the falling edge of nQ[Ax:Ex].
NOTE 11: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
NOTE 12: Defined as the total variation of all crossing voltages of rising Q[Ax:Ex] and falling nQ[Ax:Ex]. This is the maximum allowed variance in $V_{cross}$ for any particular system.
NOTE 13: Measured from -150mV to +150mV on the differential waveform (derived from Q[Ax:Ex] minus nQ[Ax:Ex]). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

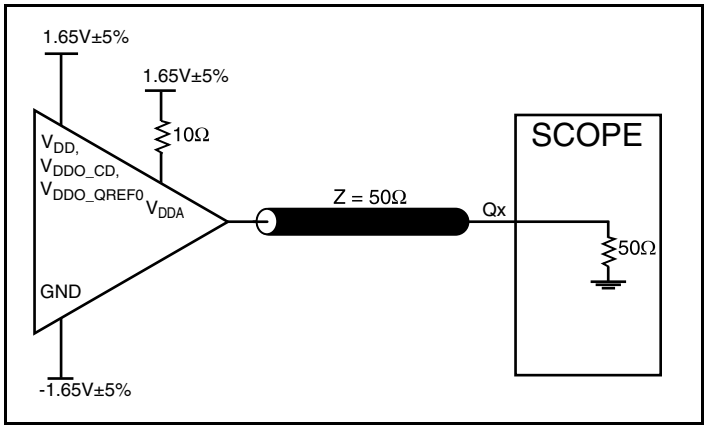
## Typical Phase Noise at 100MHz (HCSL Output)



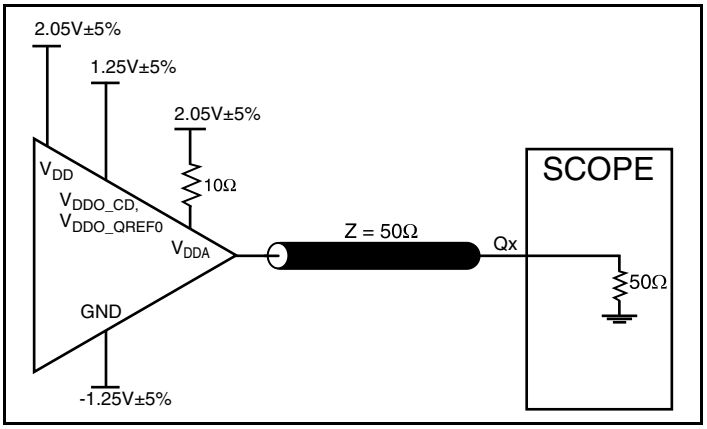
## Typical Phase Noise at 156.25MHz (LVPECL Output)



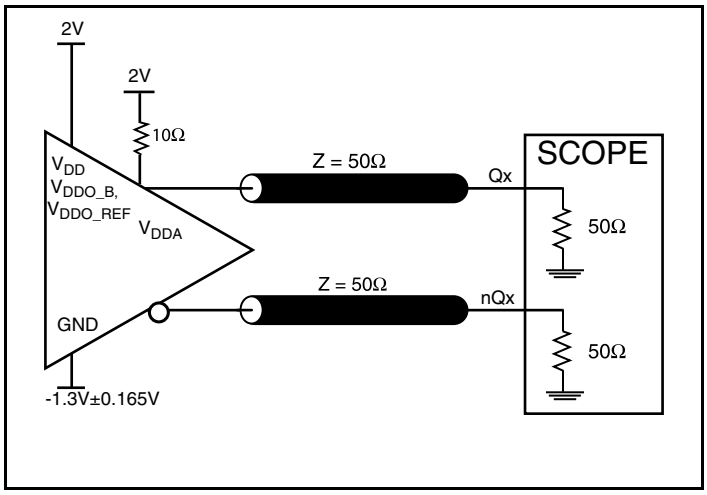
## Parameter Measurement Information



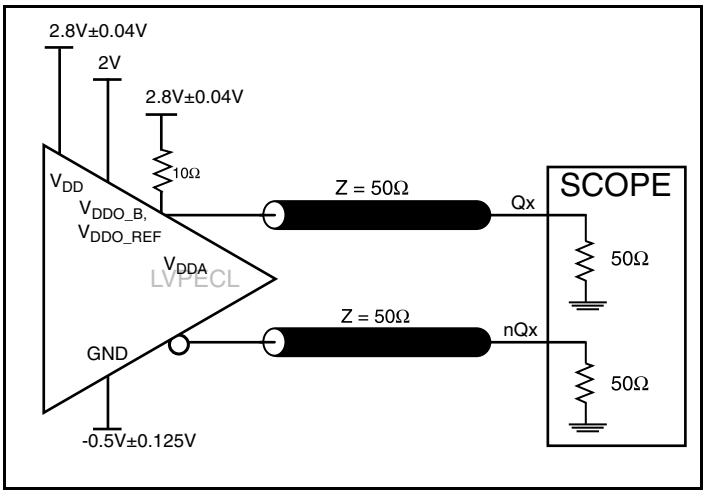

**3.3V Core/3.3V LVCMOS Output Load AC Test Circuit**



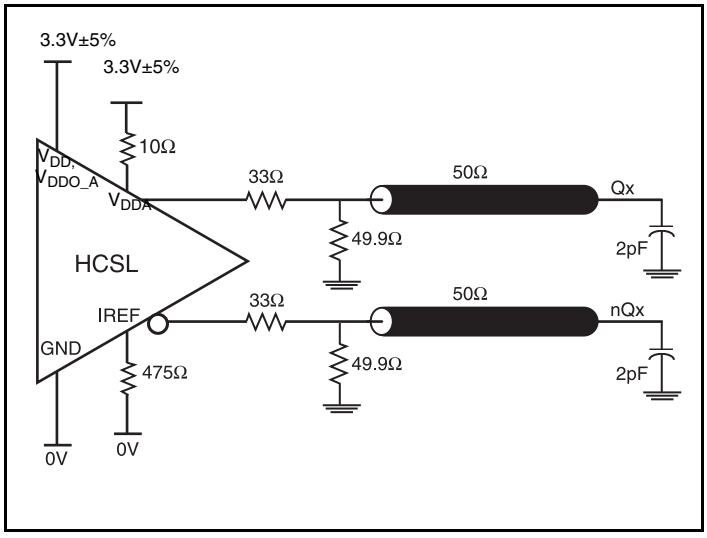

**3.3V Core/2.5V LVCMOS Output Load AC Test Circuit**



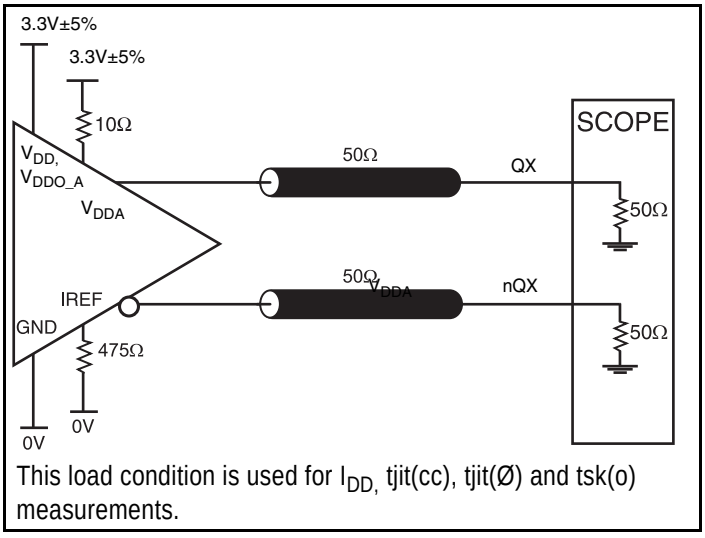

**3.3V Core/3.3V LVPECL Output Load AC Test Circuit**




**3.3V Core/2.5V LVPECL Output Load AC Test Circuit**



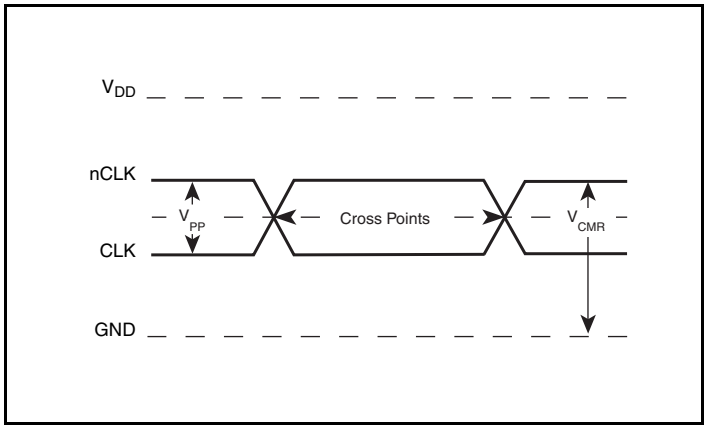

**3.3V Core/3.3V HCSL Output Load AC Test Circuit**



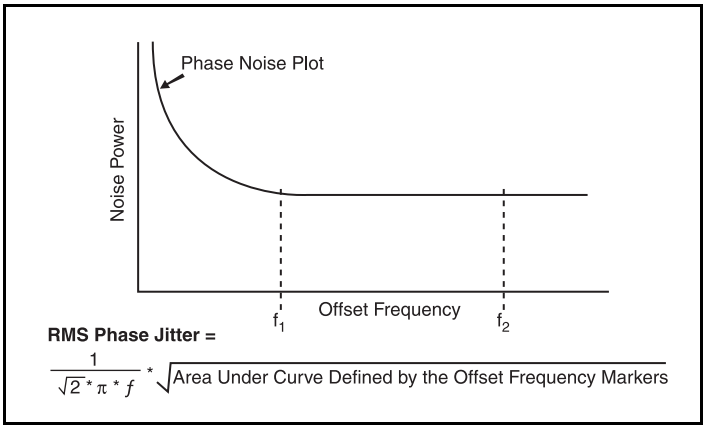

This load condition is used for $I_{DD}$, tjit(cc), tjit(Ø) and tsk(o) measurements.

**3.3V Core/3.3V HCSL Output Load AC Test Circuit**

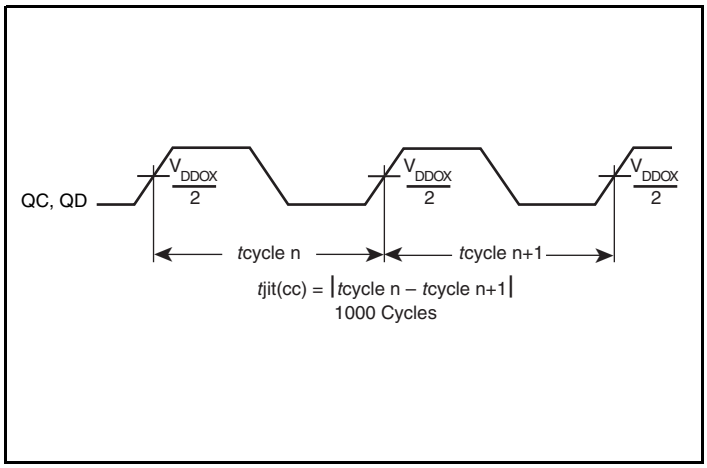
## Parameter Measurement Information, continued



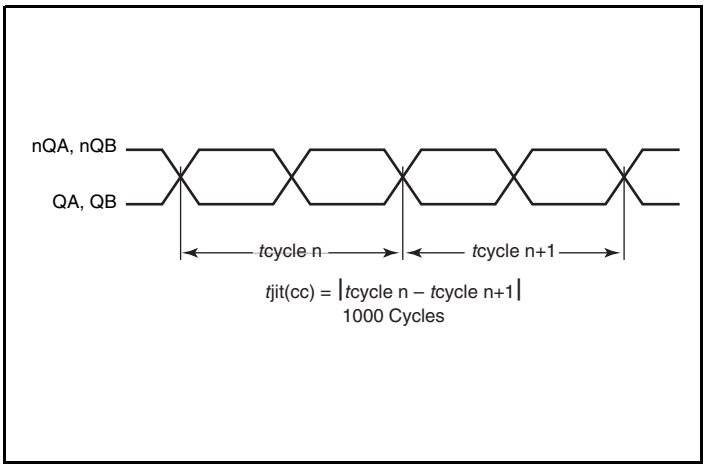

**Differential Input Level**



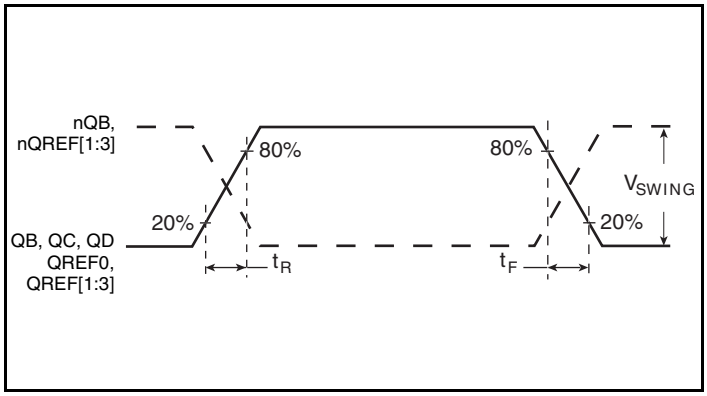

**RMS Phase Jitter**



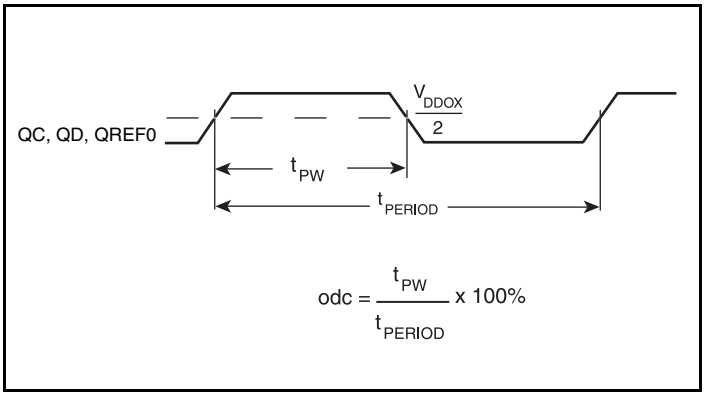

**LVCMOS Cycle-to-Cycle Jitter**




**Differential Cycle-to-Cycle Jitter**

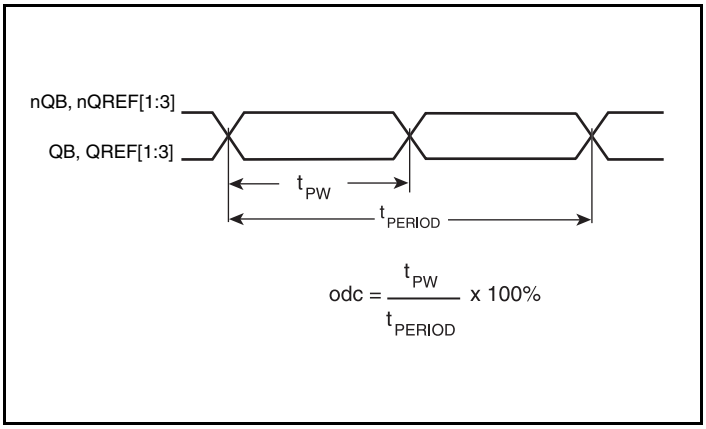



**LVCMOS/LVPECL Output Rise/Fall Time**

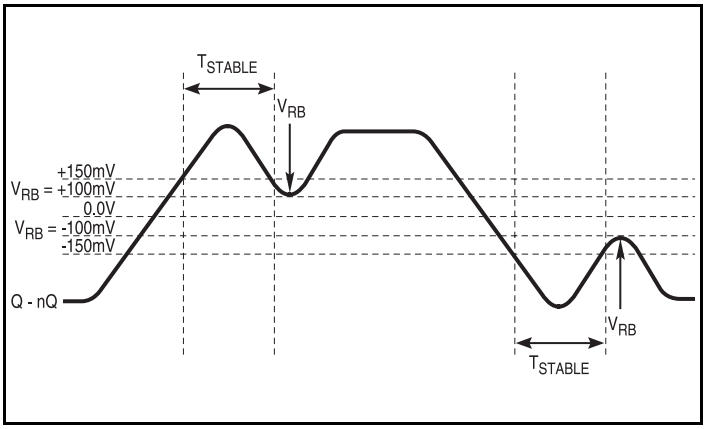



**LVCMOS Output Duty Cycle/Pulse Width**

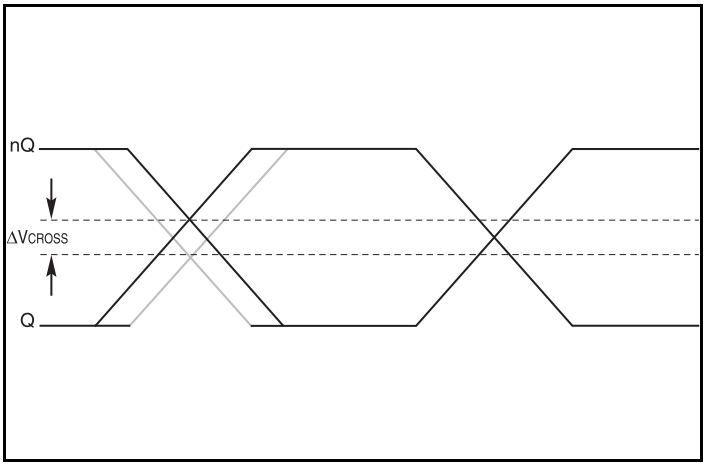
## Parameter Measurement Information, continued



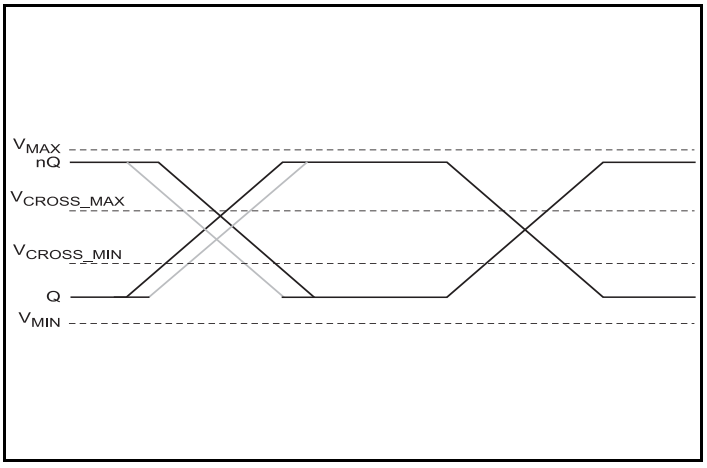

**LVPECL Output Duty Cycle/Pulse Width**



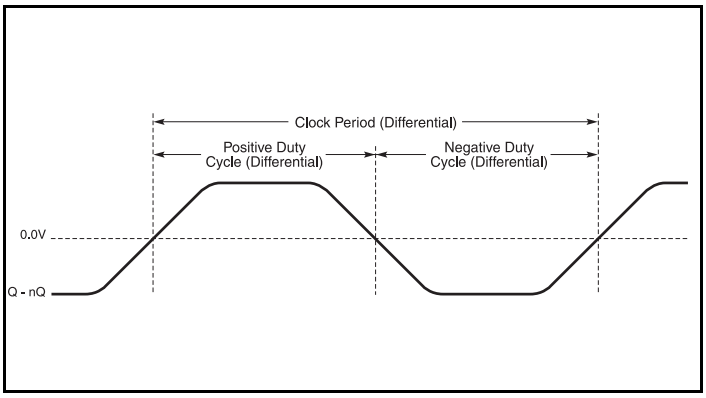

**Differential Measurement Points for Ringback**



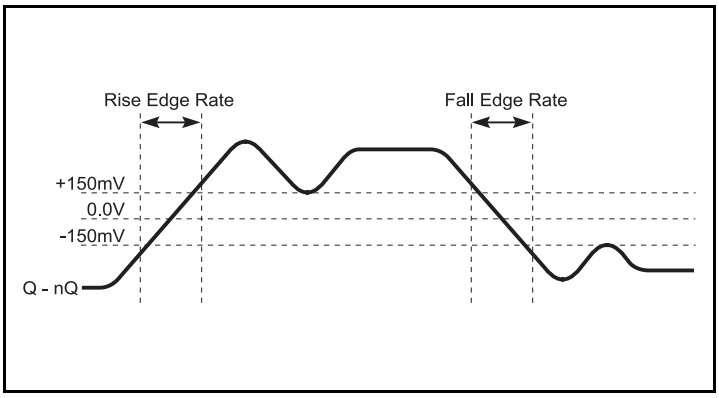

**Single-ended Measurement Points for Delta Cross Point**




**Single-ended Measurement Points for Absolute Cross Point/Swing**




**Differential Measurement Points for Duty Cycle/Period**




**Differential Measurement Points for Rise/Fall Time Edge Rate**

# Applications Information

## Recommendations for Unused Input and Output Pins

### Inputs:

#### LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

#### Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

#### CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

### Outputs:

#### LVPECL Outputs

The unused LVPECL output can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

#### LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

#### Differential Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

# PCI Express Application Note

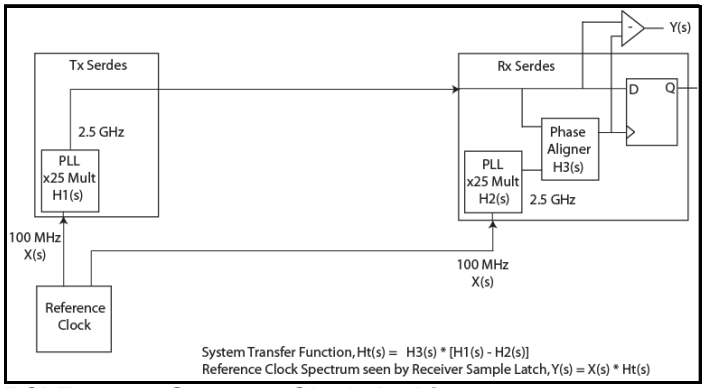
PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used *Common Clock Architecture* in which a copy of the reference clock is provided to both ends of the PCI Express Link.

In the jitter analysis, the transmit (Tx) and receive (Rx) serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is: $Ht(s) = H3(s) \times [H1(s) - H2(s)]$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

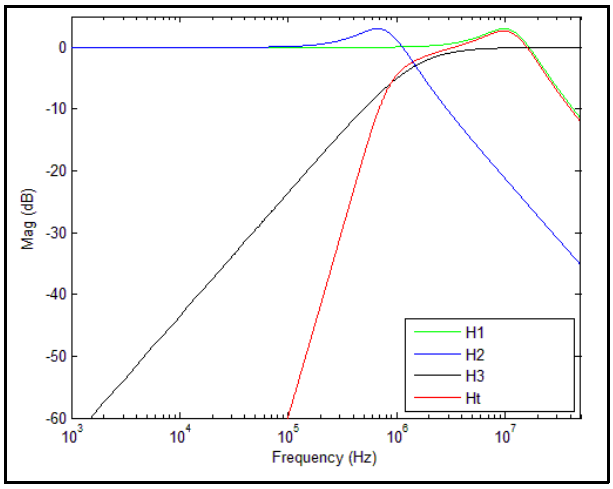
$$Y(s) = X(s) \times H3(s) \times [H1(s) - H2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on X(s)*H3(s) * [H1(s) - H2(s)].



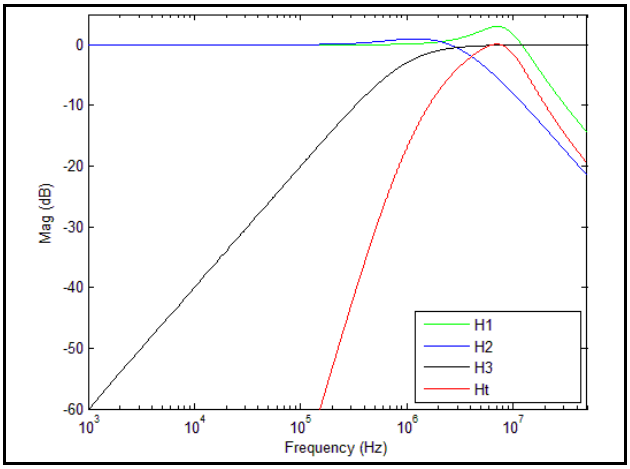

**PCI Express Common Clock Architecture**

For **PCI Express Gen 1**, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g for a 100MHz reference clock: 0Hz – 50MHz) and the jitter result is reported in peak-peak.

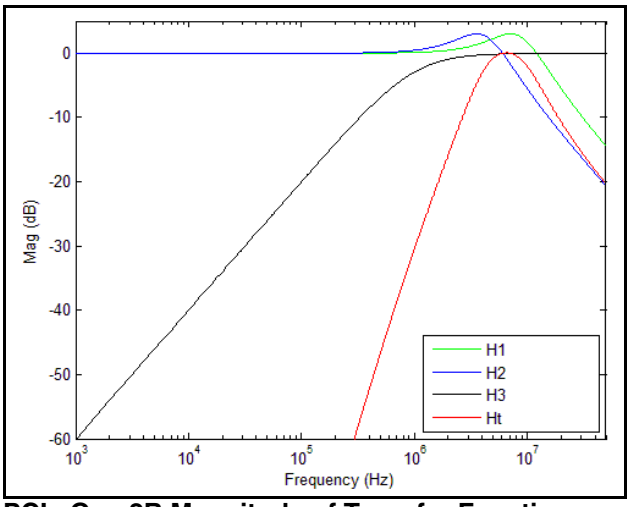



**PCIe Gen 1 Magnitude of Transfer Function**

For **PCI Express Gen 2**, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in rms. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function Ht.

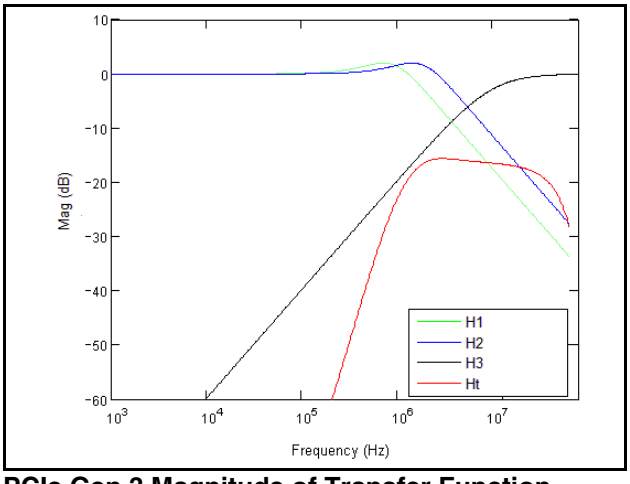



**PCIe Gen 2A Magnitude of Transfer Function**




**PCIe Gen 2B Magnitude of Transfer Function**

For PCI Express Gen 3, one transfer function is defined and the evaluation is performed over the entire spectrum. The transfer function parameters are different from Gen 1 and the jitter result is reported in RMS.




**PCIe Gen 3 Magnitude of Transfer Function**

For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note *PCI Express Reference Clock Requirements.*

## Wiring the Differential Input to Accept Single-Ended Levels

*Figure 1* shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the $V_1$ in the center of the input voltage swing. For example, if the input clock swing is 2.5V and $V_{DD}$ = 3.3V, R1 and R2 value should be adjusted to set $V_1$ at 1.25V. The values below are for when both the single ended swing and $V_{DD}$ are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however $V_{IL}$ cannot be less than -0.3V and $V_{IH}$ cannot be more than $V_{DD}$ + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

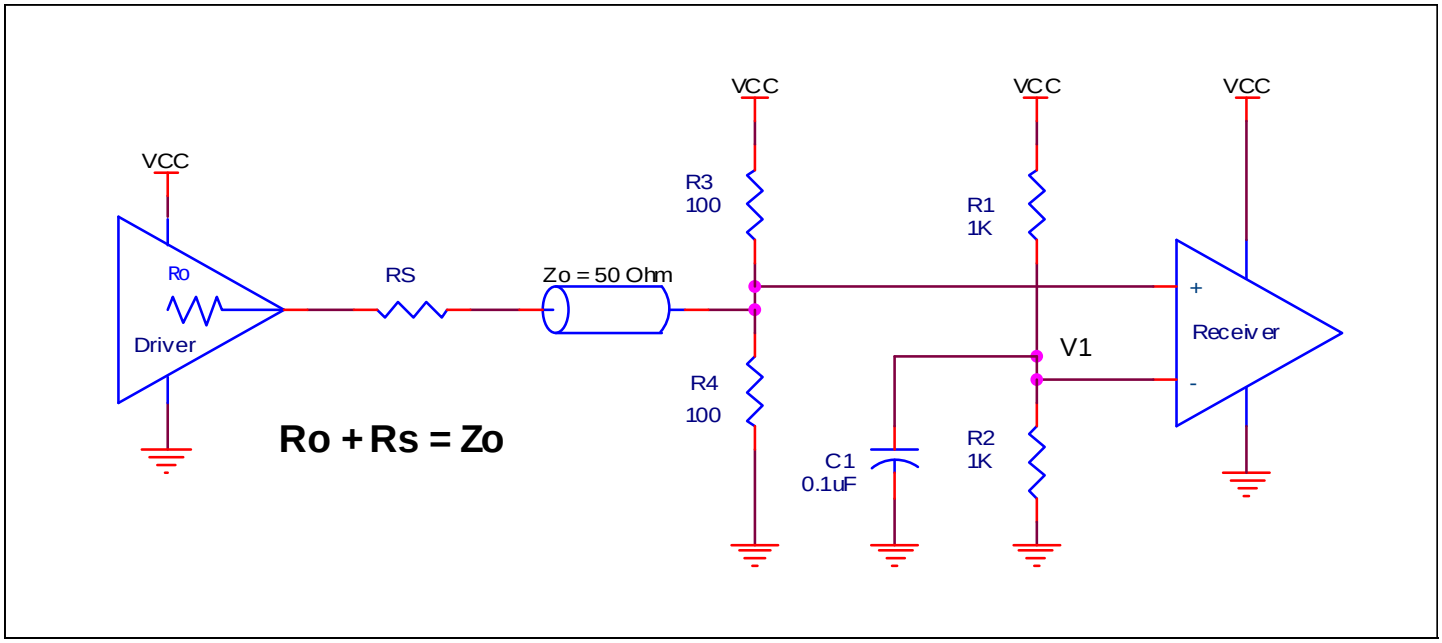



Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

## Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both signals must meet the $V_{PP}$ and $V_{CMR}$ input requirements. *Figures 2A to 2E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

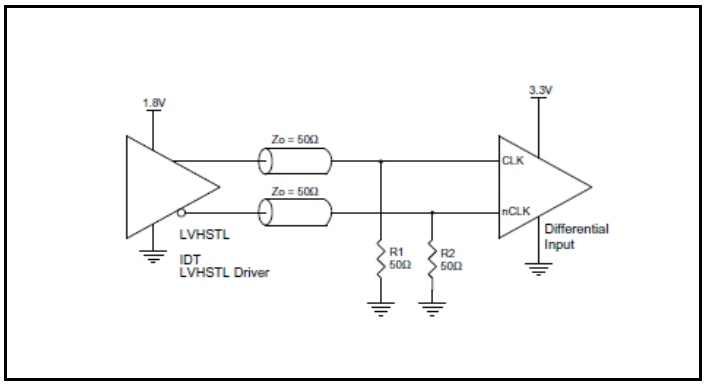



**Figure 2A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver**

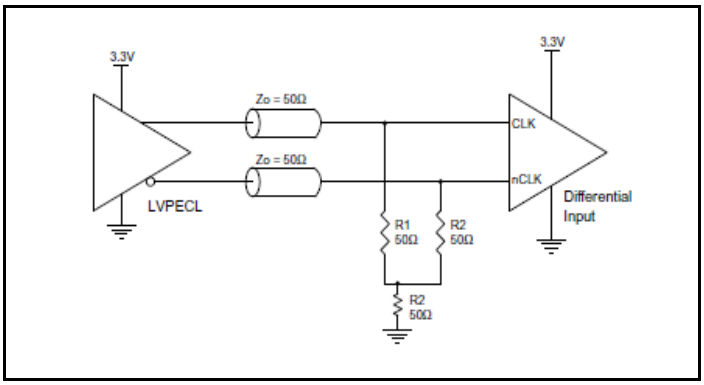



**Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**

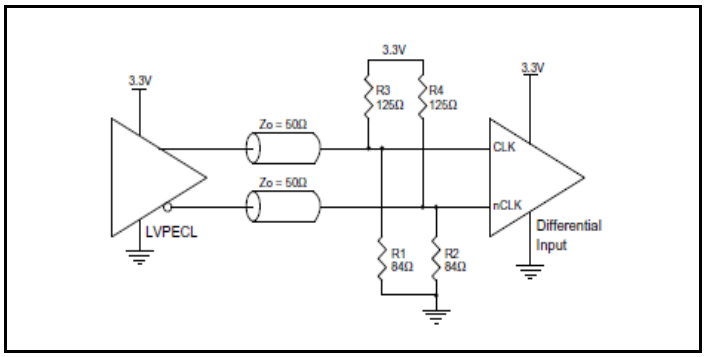



**Figure 2C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**

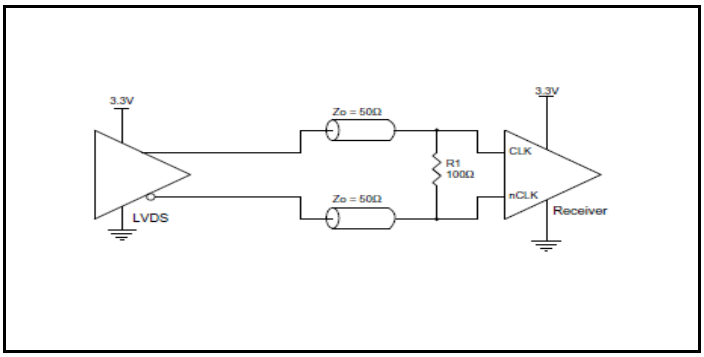



**Figure 2D. CLK/nCLK Input Driven by a 3.3V LVDS Driver**

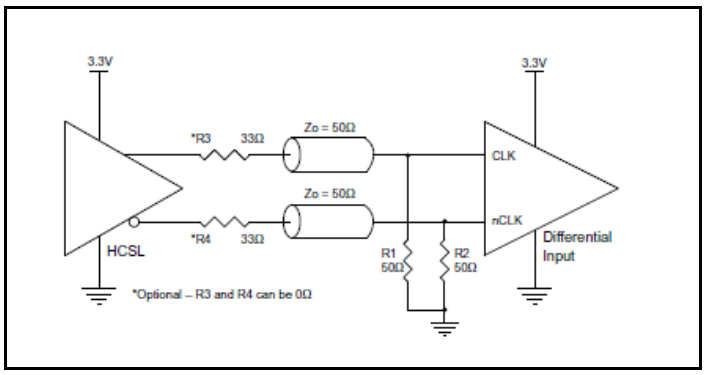



**Figure 2E. CLK/nCLK Input Driven by a 3.3V HCSL Driver**

## Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 3A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 3B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

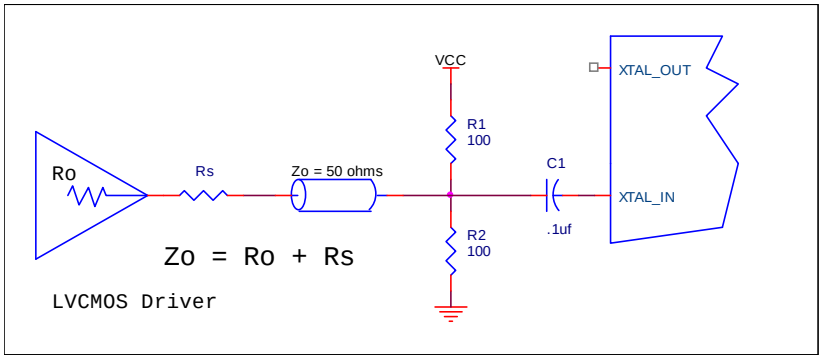



**Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface**

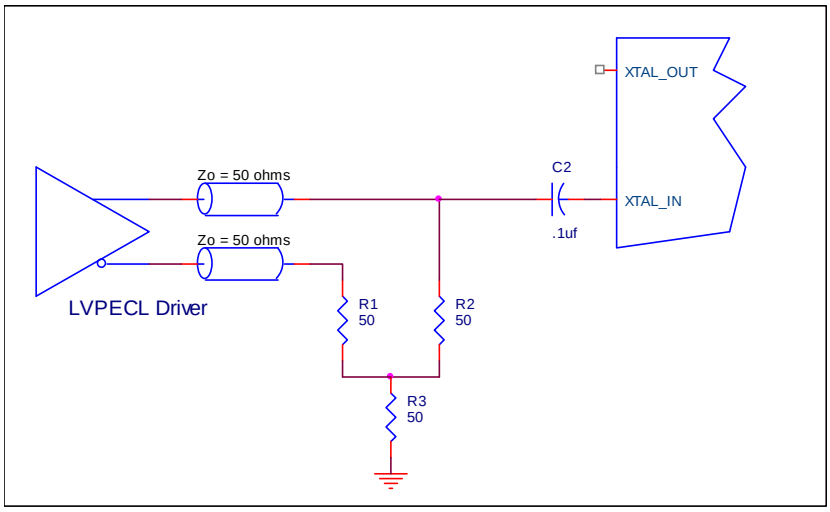



**Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface**

## Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

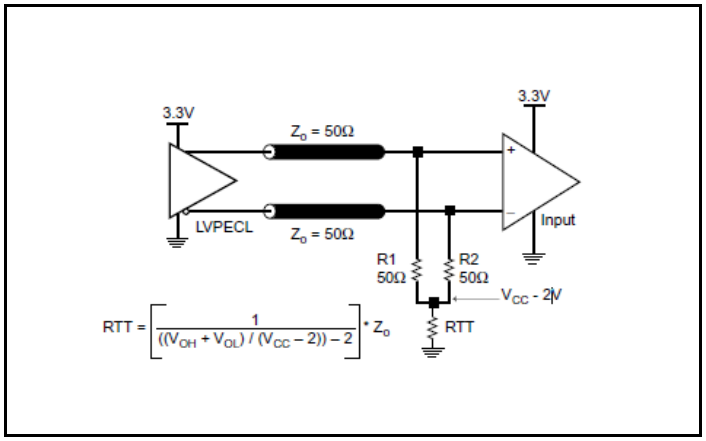



**Figure 4A. 3.3V LVPECL Output Termination**

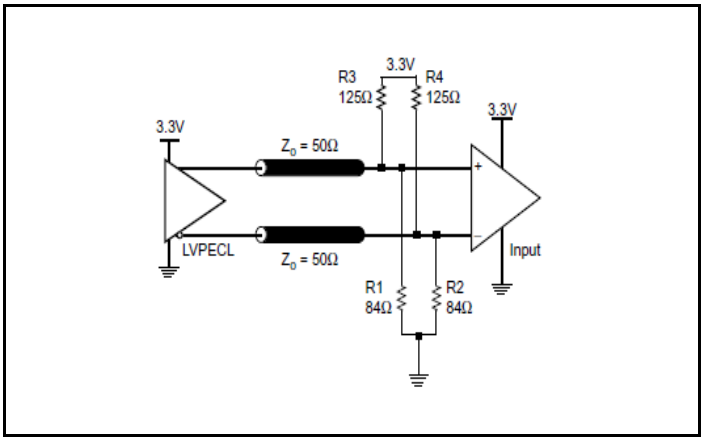



**Figure 4B. 3.3V LVPECL Output Termination**

## Termination for 2.5V LVPECL Outputs

*Figure 5A* and *Figure 5B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to $V_{DD}$ – 2V. For $V_{DDO}$ = 2.5V, the $V_{DDO}$ – 2V is very close to ground level. The R3 in Figure 5B can be eliminated and the termination is shown in *Figure 5C.*

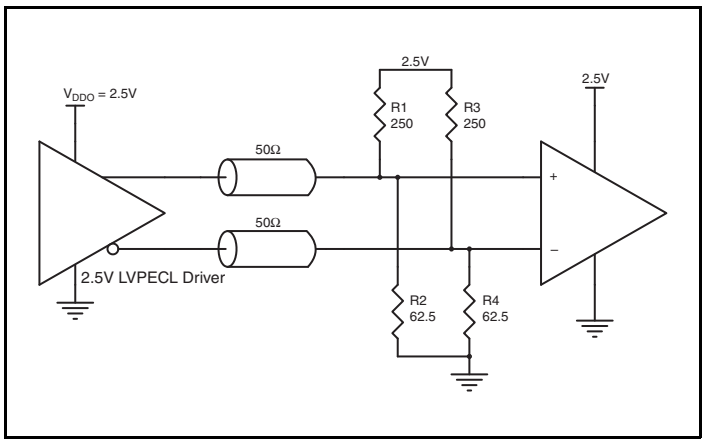



**Figure 5A. 2.5V LVPECL Driver Termination Example**

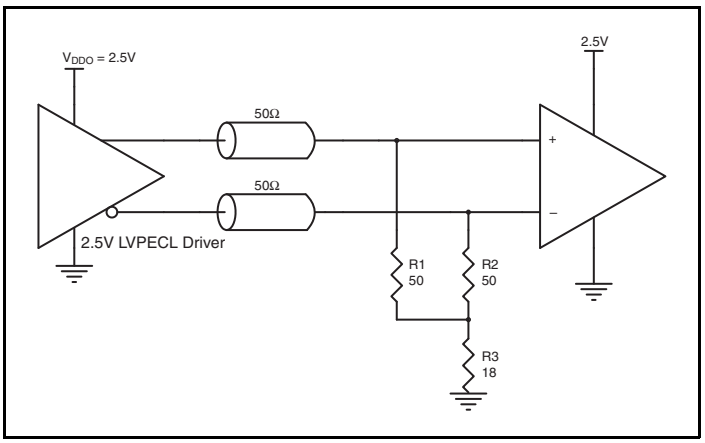



**Figure 5B. 2.5V LVPECL Driver Termination Example**

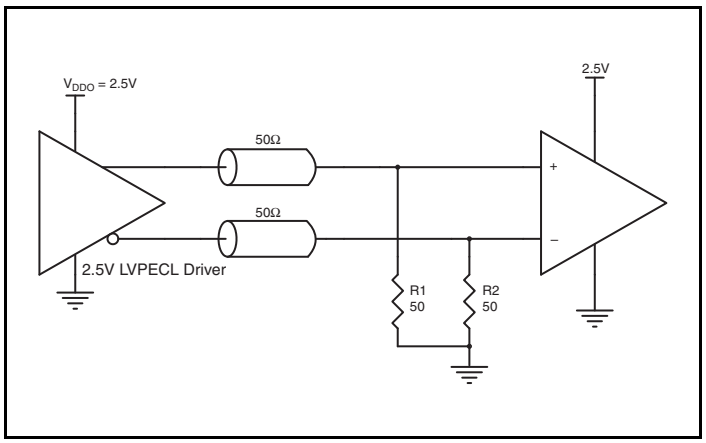



**Figure 5C. 2.5V LVPECL Driver Termination Example**

## Recommended Termination

*Figure 6A* is the recommended source termination for applications where the driver and receiver will be on a separate PCBs. This termination is the standard for PCI Express™ and HCSL output types. All traces should be 50Ω impedance single-ended or 100Ω differential.

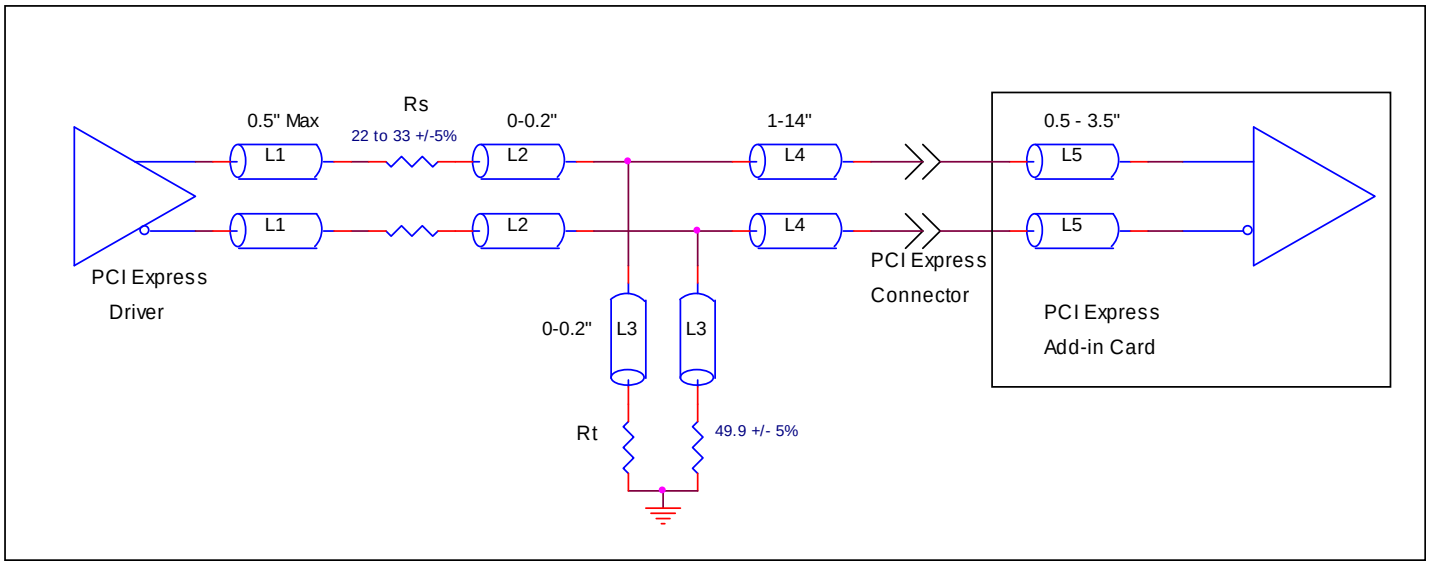



**Figure 6A. Recommended Source Termination (where the driver and receiver will be on separate PCBs)**

*Figure 6B* is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will be minimized. In addition, a series resistor (Rs) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.

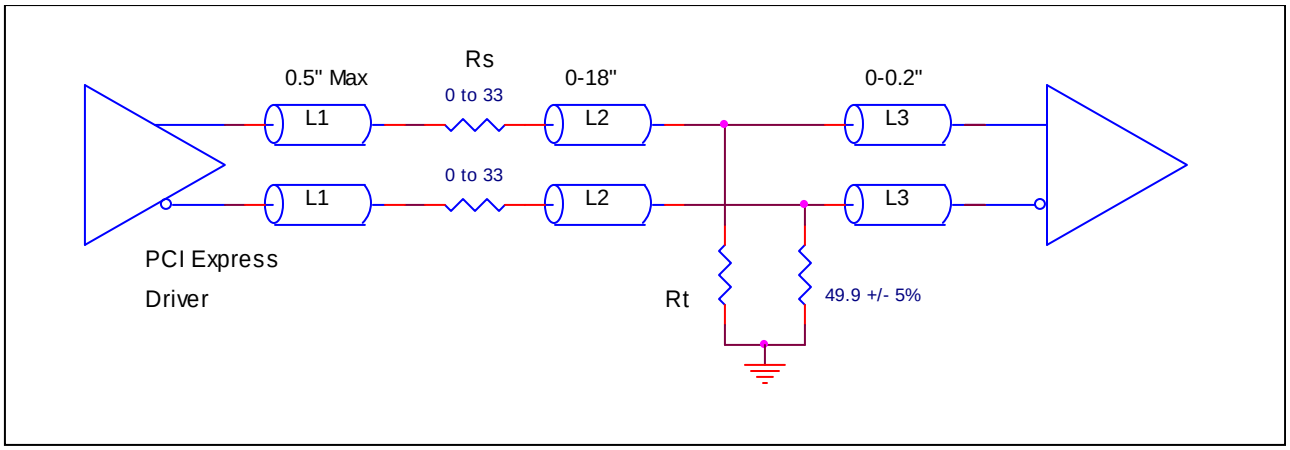



**Figure 6B. Recommended Termination (where a point-to-point connection can be used)**

## Schematic Layout

Figure 7 shows an example of 8413S08 application schematic. In this example, the device is operated $V_{DD}$= $V_{DDO\_A}$= $V_{DDO\_REF}$= $V_{DDO\_B}$= $V_{DDO\_CD}$=$V_{DDO\_REF0}$= 3.3V. The 18pF parallel resonant 25MHz crystal is used. The load capacitance C1 = 18pF and C2 = 18pF are recommended for frequency accuracy. Depending on the parasitic of the printed circuit board layout, these values might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used. For this device, the crystal load capacitors are required for proper operation. As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 8413S08 provides separate power supplies to isolate any high switching noise from coupling into the internal PLL. In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uf capacitor in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for wide range of noise frequency. This low-pass filter starts to attenuate noise at approximately 10 kHz. If a specific frequency noise component with high amplitude interference is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practice for power plane voltage stability suggests adding bulk capacitances in the general area of all devices

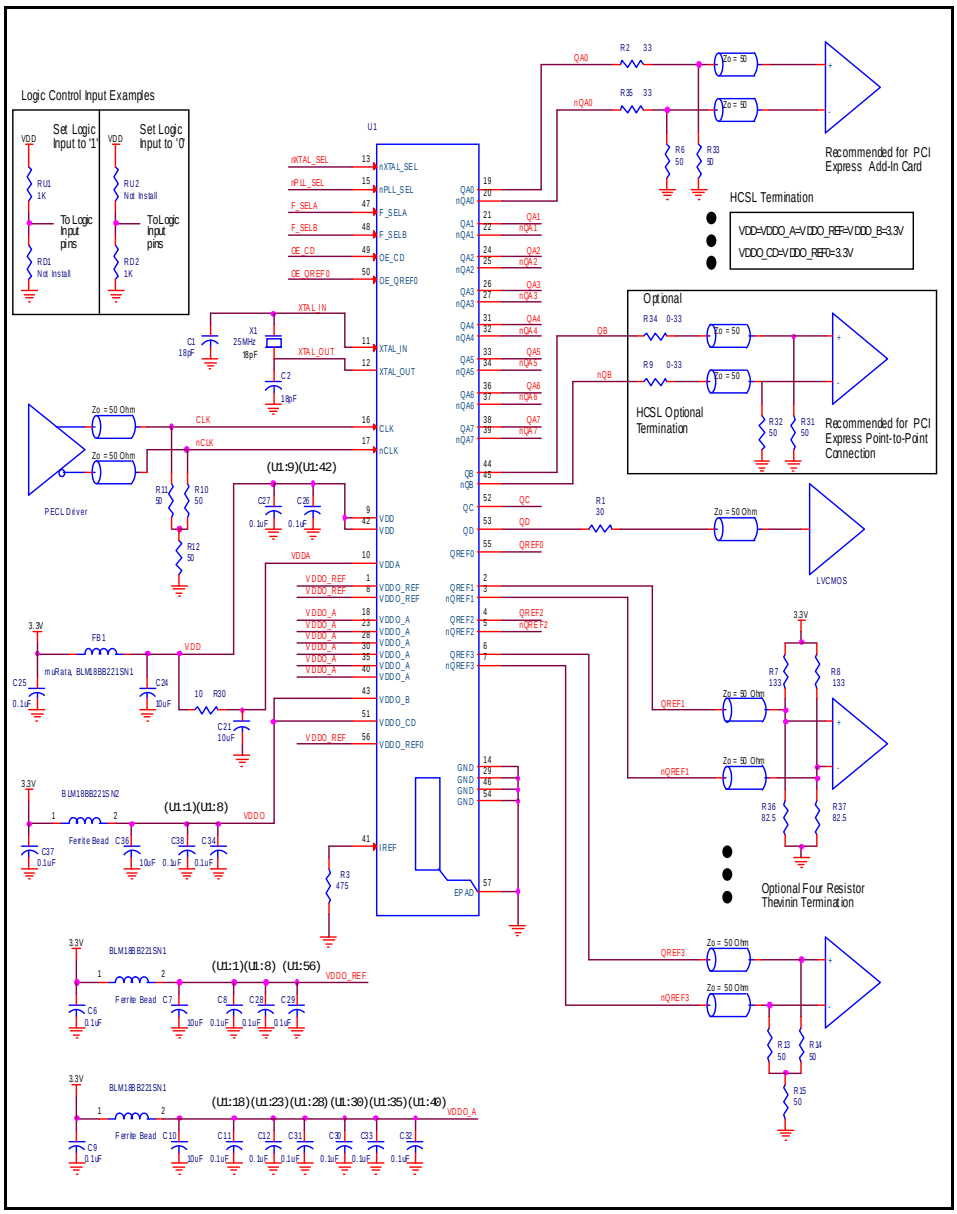



**Figure 7. 8413S08 Application Schematic**

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set.

## VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 8.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

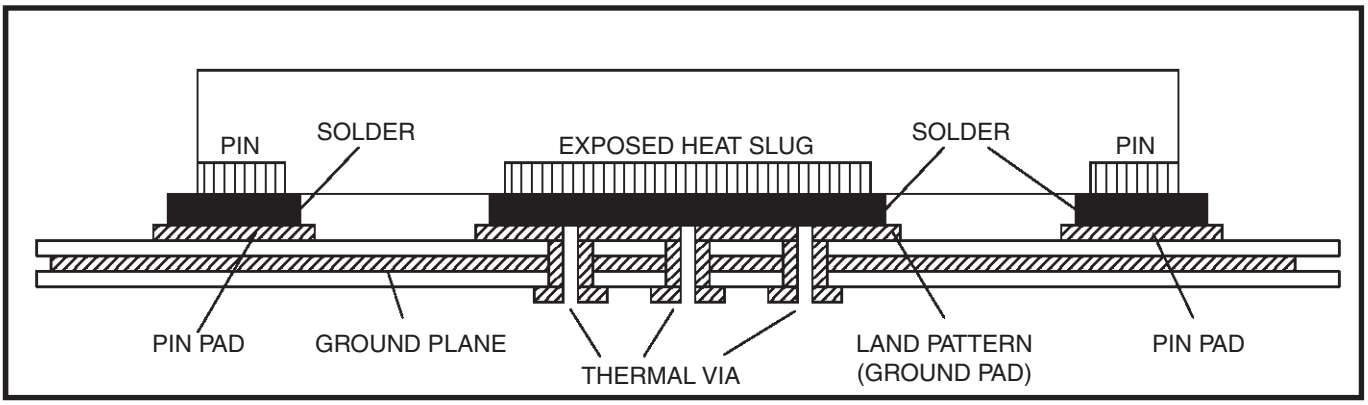



**Figure 8. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)**

# Power Considerations

This section provides information on power dissipation and junction temperature for the 8413S08.
Equations and example calculations are also provided.

### 1. Power Dissipation

The total power dissipation for the 8413S08 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for $V_{DD}$ = 3.3V + 5% = 3.465V, which gives worst case results.

**Core**

- Power(core) = $V_{DD\_MAX}$ * ($I_{DD}$ + $I_{DDA}$ + $I_{DDOx}$) = 3.465V *(84mA + 16mA + 66mA) = **575.19mW**

**LVPECL Output**
LVPECL driver power dissipation is 30mW/Loaded output pair, total LVPECL output dissipation:

- Power(LVPECL) = 30mW * 4 = 120mW

**HSCL Output**
HSCL driver power dissipation is 46.8mW/Loaded output pair, total HSCL output dissipation:

- Power(HSCL) = 46.8mW * 8 = 374.4mW

**LVCMOS Output**

- Output Impedance $R_{OUT}$ Power Dissipation due to Loading 50Ω to $V_{DD}$/2
  Output Current $I_{OUT}$ = $V_{DD\_MAX}$ / [2 * (50Ω + $R_{OUT}$)] = 3.465V / [2 * (50Ω + 20Ω)] = **24.75mA**
- Power Dissipation on the $R_{OUT}$ per LVCMOS output
  Power ($R_{OUT}$) = $R_{OUT}$ * ($I_{OUT}$)$^2$ = 20Ω * (24.75mA)$^2$ = **12.3mW per output**
- Total Power Dissipation on the $R_{OUT}$
  **Total Power ($R_{OUT}$)** = 12.3mW * 3 = **36.9mW**

**Dynamic Power Dissipation at 50MHz**

Power (50MHz) = $C_{PD}$ * Frequency * ($V_{DD}$)$^2$ = 4pF * 50MHz * (3.465V)$^2$ = **2.4mW per output**
**Total Power** (50MHz) = 2.4mW * 3 = **7.2mW**

**Total Power Dissipation**

- **Total Power**
  = Power (core) + Power (LVPECL) + Power(HCSL) + Total Power ($R_{OUT}$) + Total Power (50MHz)
  = 575.19mW + 120mW + 374.4mW + 36.9mW + 7.2mW
  **= 1113.7mW**

**2. Junction Temperature.**

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming no air flow and a multi-layer board, the appropriate value is 31.4°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 1.113W *31.4°C/W = 119.9°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 7. Thermal Resistance $\theta_{JA}$ for 56 Lead VFQFN, Forced Convection**

| $\theta_{JA}$ by Velocity | | | |
|---|---|---|---|
| Meters per Second | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 31.4°C/W | 27.5°C/W | 24.6°C/W |

**3A. Calculations and Equations.**

The purpose of this section is to calculate power dissipation on the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 10.*

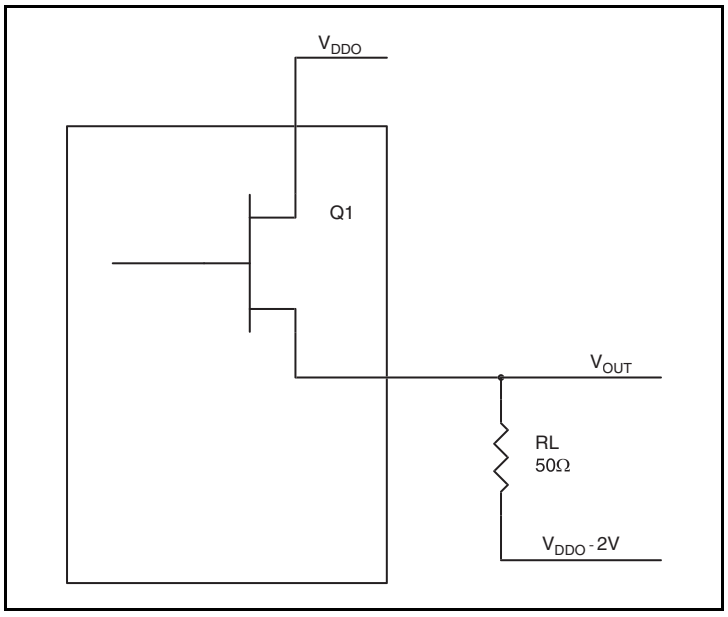



**Figure 9. LVPECL Driver Circuit and Termination**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{DDO}$ – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{DDO\_MAX} - 0.9V}$
  $(V_{DDO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{DDO\_MAX} - 1.7V}$
  $(V_{DDO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{DDO\_MAX} - 2V))/R_L] * (V_{DDO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{DDO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{DDO\_MAX} - V_{OH\_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} - (V_{DDO\_MAX} - 2V))/R_L] * (V_{DDO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{DDO\_MAX} - V_{OL\_MAX}))/R_{L]} * (V_{DDO\_MAX} - V_{OL\_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

**3B. Calculations and Equations.**

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in *Figure 11.*

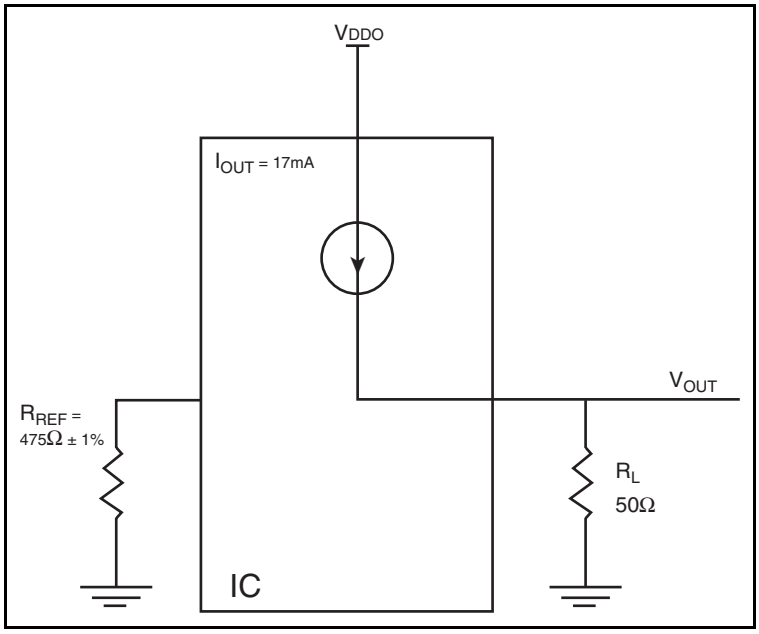



**Figure 10. HCSL Driver Circuit and Termination**

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs when $V_{DDO\_MAX}$.

Power = $(V_{DDO\_MAX} - V_{OUT}) * I_{OUT}$,
since $V_{OUT} - I_{OUT} * R_L$

= $(V_{DDO\_MAX} - I_{OUT} * R_L) * I_{OUT}$

= (3.6V – 17mA * 50Ω) * 17mA

Total Power Dissipation per output pair = **46.8mW**

# Reliability Information

**Table 8. $\theta_{JA}$ vs. Air Flow Table for a 56 Lead VFQFN**

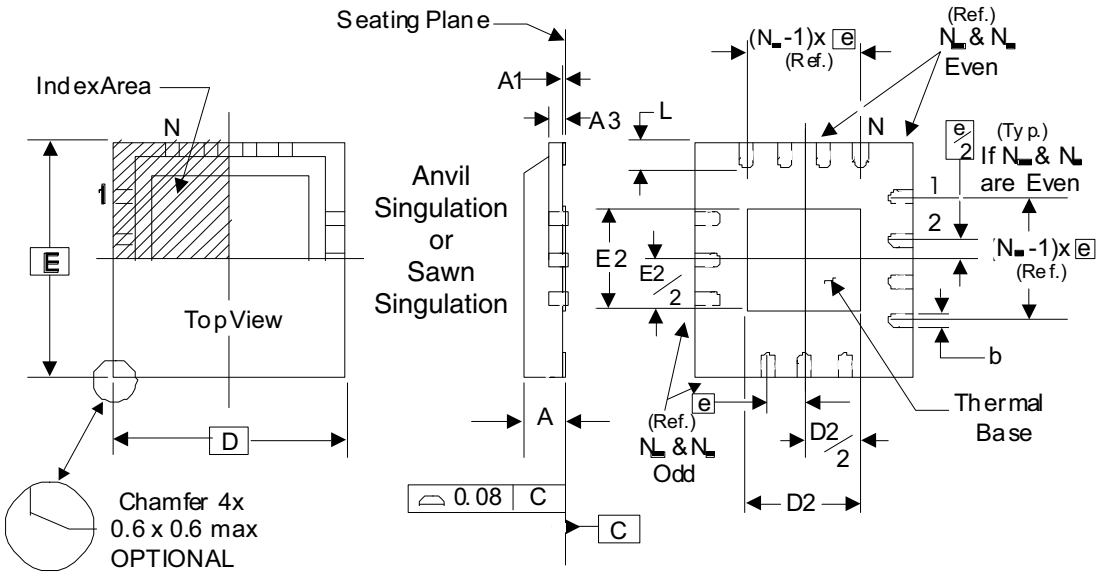
| $\theta_{JA}$ vs. Air Flow | | | |
|---|---|---|---|
| Meters per Second | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 31.4°C/W | 27.5°C/W | 24.6°C/W |

## Transistor Count

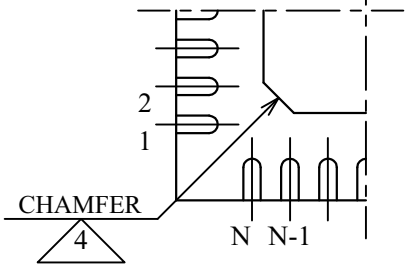
The transistor count for 8413S08 is: 9994

# Package Outline and Package Dimensions

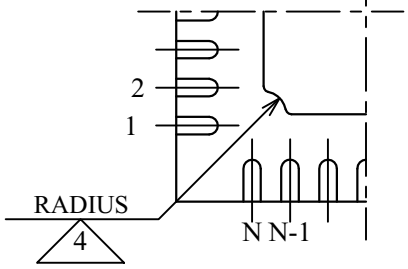
### Package Outline - K Suffix for 56 Lead VFQFN




**Bottom View w/Type A ID**




**Bottom View w/Type C ID**




There are 2 methods of indicating pin 1 corner at the back of the VFQFN package:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type C: Mouse bite on the paddle (near pin 1)

**Table 8. Package Dimensions**

| JEDEC Variation: VLLD-2/-5<br>All Dimensions in Millimeters | | |
|---|---|---|
| **Symbol** | **Minimum** | **Maximum** |
| **N** | 56 | |
| **A** | 0.80 | 1.00 |
| **A1** | 0 | 0.05 |
| **A3** | 0.25 Ref. | |
| **b** | 0.18 | 0.30 |
| **$N_D$ & $N_E$** | 14 | |
| **D & E** | 8.00 Basic | |
| **D2** | 4.35 | 4.65 |
| **E2** | 5.05 | 5.35 |
| **e** | 0.50 Basic | |
| **L** | 0.30 | 0.50 |

Reference Document: JEDEC Publication 95, MO-220

NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 8 below.

# Ordering Information

**Table 9. Ordering Information**

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| 8413S08BKILF | ICS8413S08BIL | “Lead-Free” 56 VFQFN | Tray | -40°C to 85°C |
| 8413S08BKILFT | ICS8413S08BIL | “Lead-Free” 56 VFQFN | Tape & Reel | -40°C to 85°C |

# Revision History

| Revision Date | Description of Change |
|---|---|
| 10/3/16 | Updated header and footer.<br>Removed ICS from part numbers where needed.<br>Ordering Information - Deleted quantity from tape and reel. Removed note from below table. |

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