ICL8048

Log Amplifier

OBSOLETE PRODUCT
NO RECOMMENDED REPLACEMENT
contact our Technical Support Center at
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FN2865
Rev 3.00
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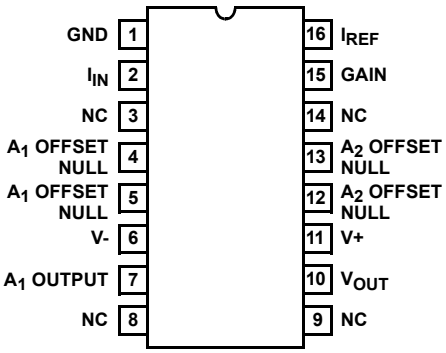
The ICL8048 is a monolithic logarithmic amplifier capable of handling six decades of current input, or three decades of voltage input. It is fully temperature compensated and is nominally designed to provide 1V of output for each decade change of input. For increased flexibility, the scale factor, reference current and offset voltage are externally adjustable.

Part Number Information

PART NUMBER	ERROR (25^oC)	TEMPERATURE RANGE (^oC)	PACKAGE	PKG. NO.
ICL8048BCJE	30mV	0 to 70	16 Ld CERDIP	F16.3

Pinout

ICL8048 (CERDIP)
TOP VIEW

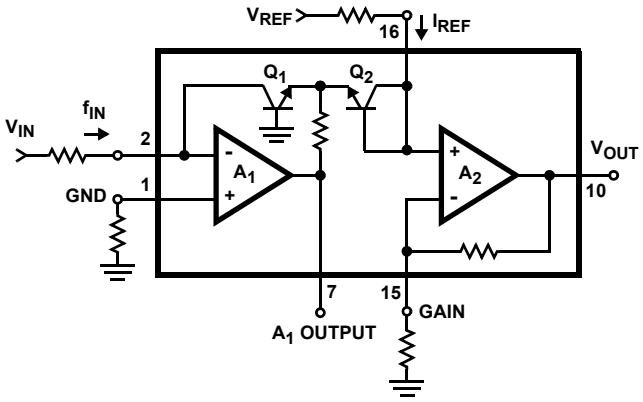


Features

- Full Scale Accuracy 0.5%
- Temperature Compensated Operation . . . . . 0^oC to 70^oC
- Scale Factor, Adjustable 1V/Decade
- Dynamic Current Range. 120dB
- Dynamic Voltage Range 60dB
- Dual JFET Input Op Amps

Functional Diagram

ICL8048



Absolute Maximum Ratings

Supply Voltage . . . . . ±18V
I_{IN} (Input Current) 2mA
I_{REF} (Reference Current) 2mA
Voltage Between Offset Null and V+ . . . . . ±0.5V
Output Short Circuit Duration. . . . . Indefinite

Operating Conditions

Temperature Range. . . . . 0^oC to 70^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package.	75	22

Maximum Junction Temperature (Hermetic Package or Die) . . . 175^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

Die Characteristics

Number of Transistors or Gates 62

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$V_S = \pm15V$, $T_A = 25^oC$, I_{REF} = 1mA, Scale Factor Adjusted for 1V/Decade, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	ICL4048BC			UNITS
		MIN	TYP	MAX	
Dynamic Range					
I_{IN} (1nA - 1mA)	R_{IN} = 10kΩ	120	-	-	dB
V_{IN} (10mV - 10V)		60	-	-	dB
Error, % of Full Scale	I_{IN} = 1nA to 1mA	-	0.20	0.5	%
	$T_A = 0^oC$ to 70^oC, I_{IN} = 1nA to 1mA	-	0.60	1.25	%
Error, Absolute Value	I_{IN} = 1nA to 1mA	-	12	30	mV
	$T_A = 0^oC$ to 70^oC, I_{IN} = 1nA to 1mA	-	36	75	mV
Temperature Coefficient of V_{OUT}	I_{IN} = 1nA to 1mA	-	0.8	-	$mV/^oC$
Power Supply Rejection Ratio	Referred to Output	-	2.5	-	mV/V
Offset Voltage (A_1 and A_2)	Before Nulling	-	15	25	mV
Wideband Noise	At Output, for I_{IN} = 100µA	-	250	-	μV_{RMS}
Output Voltage Swing	R_L = 10kΩ	±12	±14	-	V
	R_L = 2kΩ	±10	±13	-	V
Power Consumption		-	150	200	mW
Supply Current		-	5	6.7	mA

Typical Performance Curves

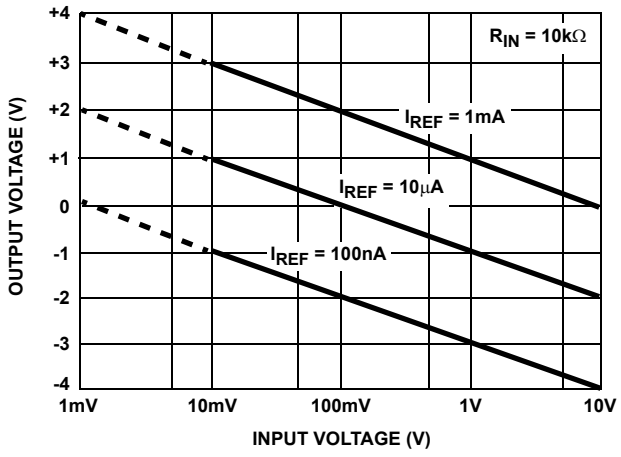


FIGURE 1. TRANSFER FUNCTION FOR VOLTAGE INPUTS

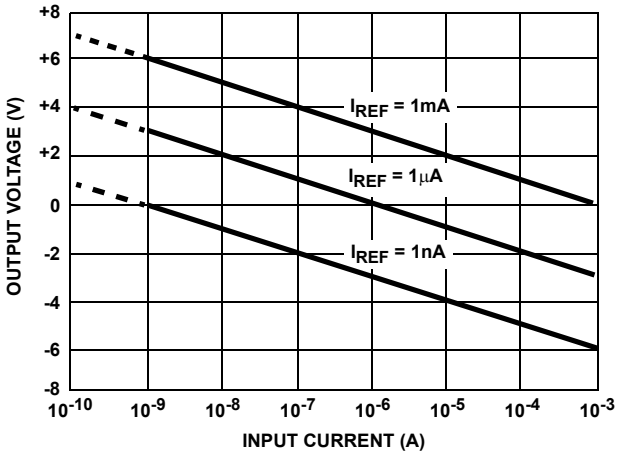


FIGURE 2. TRANSFER FUNCTION FOR CURRENT INPUTS

Typical Performance Curves (Continued)

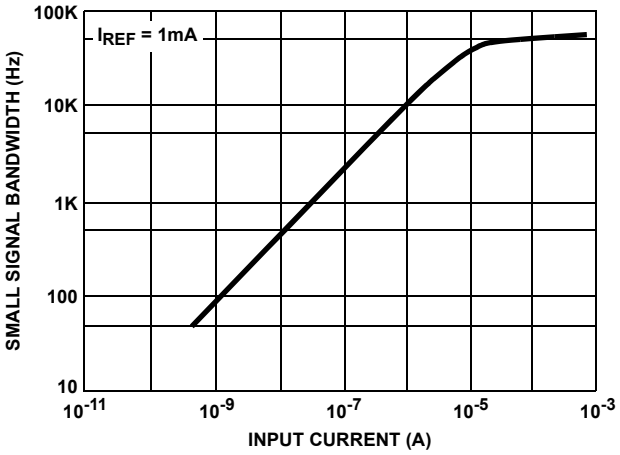


FIGURE 3. SMALL SIGNAL BANDWIDTH vs INPUT CURRENT

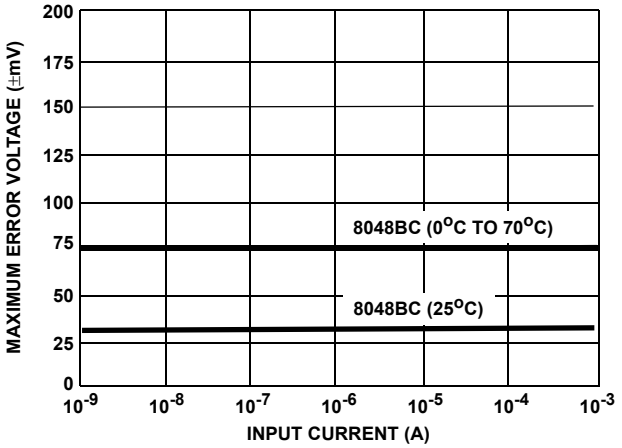


FIGURE 4. MAXIMUM ERROR VOLTAGE AT THE OUTPUT vs INPUT CURRENT

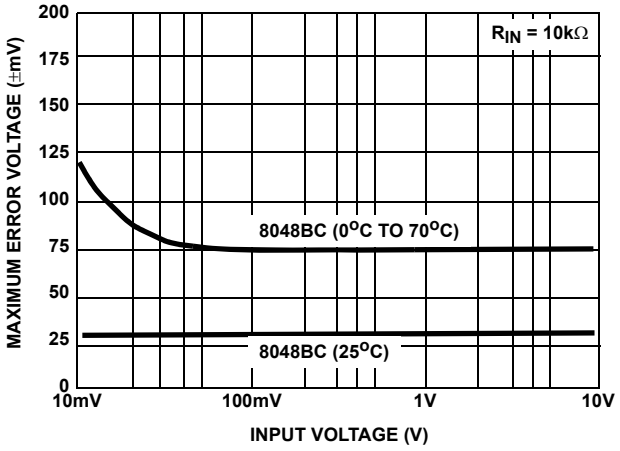


FIGURE 5. MAXIMUM ERROR VOLTAGE AT THE OUTPUT vs INPUT VOLTAGE

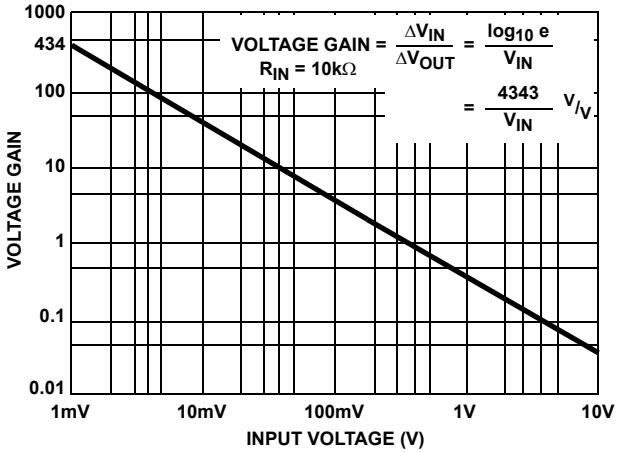


FIGURE 6. SMALL SIGNAL VOLTAGE GAIN vs INPUT VOLTAGE FOR R_S = 10kΩ

ICL8048 Detailed Description

The ICL8048 relies for its operation on the well known exponential relationship between the collector current and the base emitter voltage of a transistor:

$$I_C = I_S\left[\exp\left(\frac{qV_{BE}}{kT}\right) - 1\right] \quad \text{(EQ. 1)}$$

For base emitter voltages greater than 100mV, Equation 1 becomes

$$I_C = I_S \exp\left(\frac{qV_{BE}}{kT}\right) \quad \text{(EQ. 2)}$$

From Equation 2, it can be shown that for two identical transistors operating at different collector currents, the V_{BE} difference (ΔV_{BE}) is given by:

$$\Delta V_{BE} = -2.303 \times \frac{kT}{q} \log_{10}\left[\frac{I_{C1}}{I_{C2}}\right] \quad \text{(EQ. 3)}$$

Referring to Figure 7 it is clear that the potential at the collector of Q_2 is equal to the ΔV_{BE} between Q_1 and Q_2. The output voltage is ΔV_{BE} multiplied by the gain of A_2:

$$V_{OUT} = -2.303\left(\frac{R_1 + R_2}{R_2}\right)\left(\frac{kT}{q}\right)\log_{10}\left[\frac{I_{IN}}{I_{REF}}\right] \quad \text{(EQ. 4)}$$

The expression $2.303 \times \frac{kT}{q}$ has a numerical value of 59mV at 25°C; thus in order to generate 1V/decade at the output, the ratio $(R_1 + R_2)/R_2$ is chosen to be 16.9. For this scale factor to hold constant as a function of temperature, the $(R_1 + R_2)/R_2$ term must have a 1/T characteristic to compensate for kT/q.

In the ICL8048 this is achieved by making R_1 a thin film resistor, deposited on the monolithic chip. It has a nominal value of 15.9kΩ at 25°C, and its temperature coefficient is carefully designed to provide the necessary compensation.

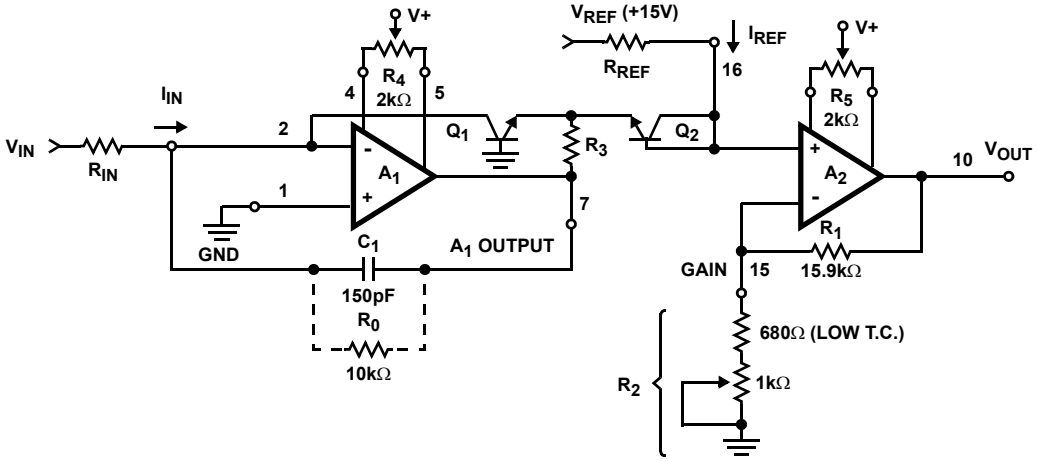


FIGURE 7. ICL8048 OFFSET AND SCALE FACTOR ADJUSTMENT

Resistor R_2 is external and should be a low T.C. type; it should have a nominal value of 1kΩ to provide 1V/decade, and must have an adjustment range of ±20% to allow for production variations in the absolute value of R_1.

ICL8048 Offset and Scale Factor Adjustment

A log amp, unlike an op amp, cannot be offset adjusted by simply grounding the input. This is because the log of zero approaches minus infinity; reducing the input current to zero starves Q_1 of collector current and opens the feedback loop around A_1. Instead, it is necessary to zero the offset voltage of A_1 and A_2 separately, and then to adjust the scale factor. Referring to Figure 7, this is done as follows:

1. Temporarily connect a 10kΩ resistor (R_0) between pins 2 and 7. With no input voltage, adjust R_4 until the output of A_1 (pin 7) is zero. Remove R_0.

   Note that for a current input, this adjustment is not necessary since the offset voltage of A_1 does not cause any error for current source inputs.

2. Set $I_{IN} = I_{REF} = 1mA$. Adjust R_5 such that the output of A_2 (pin 10) is zero.
3. Set $I_{IN} = 1\mu A$, $I_{REF} = 1mA$. Adjust R_2 for $V_{OUT} = 3V$ (for a 1V/decade scale factor) or 6V (for a 2V/decade scale factor).

Step #3 determines the scale factor. Setting $I_{IN} = 1\mu A$ optimizes the scale factor adjustment over a fairly wide dynamic range, from 1mA to 1nA. Clearly, if the ICL8048 is to be used for inputs which only span the range 100µA to 1mA, it would be better to set I_{IN} = 100µA in Step #3. Similarly, adjustment for other scale factors would require different I_{IN} and V_{OUT} values.

Applications Information

ICL8048 Scale Factor Adjustment

The scale factor adjustment procedures outlined previously for the ICL8048, are primarily directed towards setting up 1V (ΔV_{OUT}) per decade (ΔI_{IN} or ΔV_{IN}) for the log amp, or one decade (ΔV_{OUT}) per volt (ΔV_{IN}) for the antilog amp.

This corresponds to K = 1 in the respective transfer functions:

$$V_{OUT} = -K \log_{10}\left[\frac{I_{IN}}{I_{REF}}\right] \quad \text{(EQ. 5)}$$

By adjusting R_2 (Figure 7) the scale factor "K" in Equation 5 can be varied. The effect of changing K is shown graphically in Figure 8 for the log amp. The nominal value of R_2 required to give a specific value of K can be determined from Equation 6. It should be remembered that R_1 has a ±20% tolerance in absolute value, so that allowance shall be made for adjusting the nominal value of R_2 by ±20%.

$$R_2 = \frac{941}{(K - 0.059)}\Omega \quad \text{(EQ. 6)}$$

ICL8048 Automatic Offset Nulling Circuit

The ICL8048 is fundamentally a logarithmic current amplifier. It can be made to act as a voltage amplifier by placing a resistor between the current input and the voltage source but, since $I_{IN} = (V_{IN} - V_{OFFSET})/R_{IN}$, this conversion is accurate only when V_{IN} is much greater than the offset voltage. A substantial reduction of V_{OFFSET} would allow voltage operation over a 120dB range.

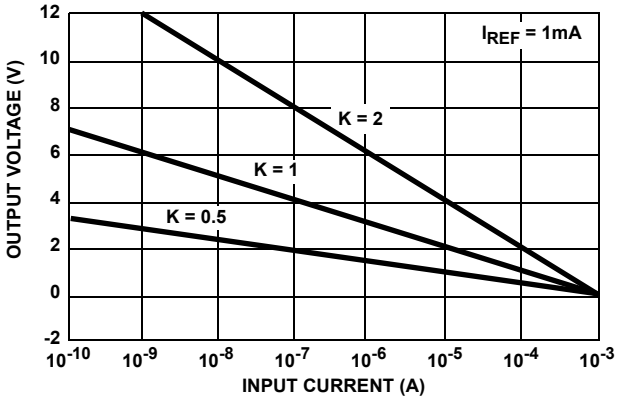


FIGURE 8. EFFECT OF VARYING "K" ON THE LOG AMPLIFIER

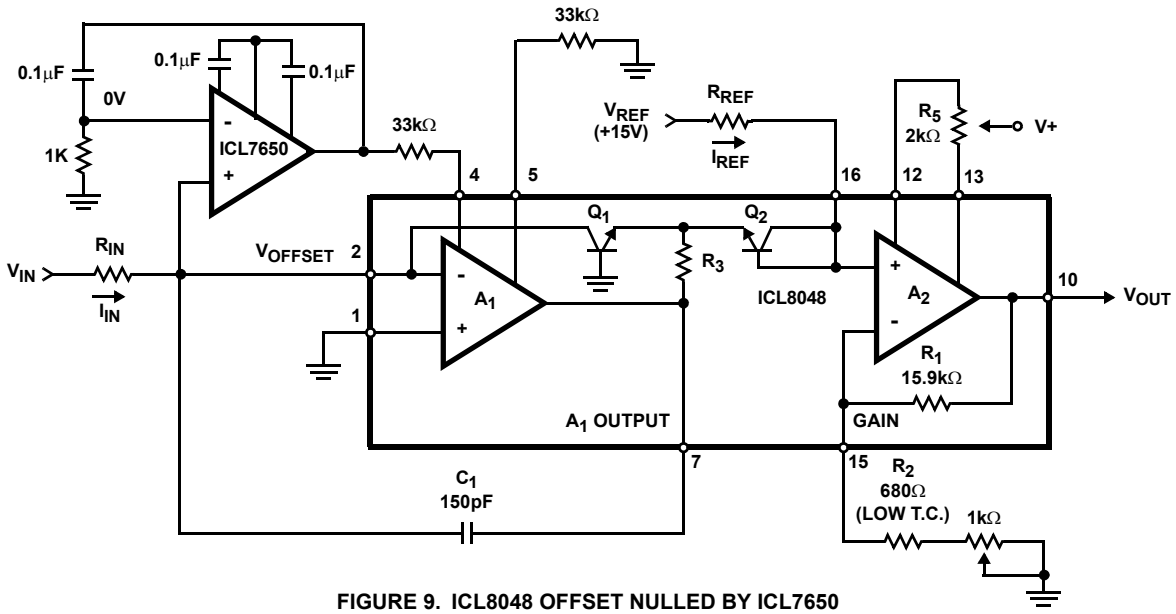


FIGURE 9. ICL8048 OFFSET NULLED BY ICL7650

Figure 9 shows the ICL8048 in an automatic offset nulling configuration using the ICL7650S. The extremely low offset voltage of the ICL7650S forces its non-inverting input (and thus pin 2 of the ICL8048) to the same potential as its inverting input by nulling the first stage of the log amp. Since V_{OFFSET} is now within a few μV of ground potential, R_{IN} can perform its voltage to current conversion much more accurately, and without an offset trimmer pot. Step 1 of the offset and scale factor adjustment is eliminated, simplifying calibration.

NOTE: The ICL7650S op amp has a maximum supply voltage of 18V. The ICL8048 will operate at this voltage, but I_{REF} must be limited to 200μA or less for proper calibration and operation. Best performance will be achieved when the ICL7650S has a ±3V to ±8V supply and the ICL8048 is at its recommended ±15V supply. See A053 for a method of powering the ICL7650S from a ±15V source.

Frequency Compensation

Although the op amps in the ICL8048 are compensated for unity gain, some additional frequency compensation is required. This is because the log transistors in the feedback loop add to the loop gain. In the ICL8048, 150pF should be connected between Pins 2 and 7 (Figure 7).

Error Analysis

Performing a meaningful error analysis of a circuit containing a log and antilog amplifiers is more complex than dealing with a similar circuit involving only op amps. In this data sheet every effort has been made to simplify the analysis task, without in any way compromising the validity of the resultant numbers.

The key difference in making error calculations in log/antilog amps, compared with op amps, is that the gain of the former is a function of the input signal level. Thus, it is necessary, when referring errors from output to input, or vice versa, to check the input voltage level, then determine the gain of the circuit by referring to the graphs given in the Typical Performance Curves section.

The various error terms in the log amplifier, the ICL8048, are Referred To the Output (RTO) of the device. The errors are expressed in this way because in the majority of systems a number of log amps interface with an antilog amp, as shown in Figure 10.

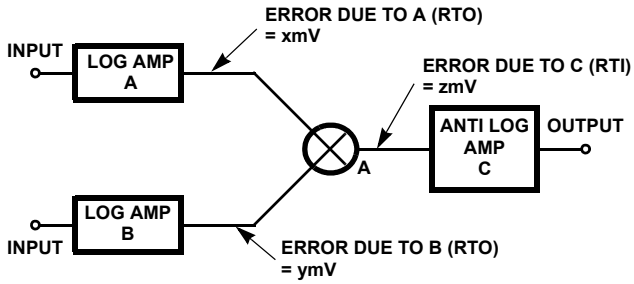


FIGURE 10.

It is very straightforward to estimate the system error at node (A) by taking the square root of the sum-of-the-squares of the errors of each contributing block.

$$\text{Total Error} = \sqrt{x^2 + y^2 + z^2}\ \text{at (A)}$$

If required, this error can be referred to the system output through the voltage gain of the antilog circuit, using the voltage gain versus input voltage plot.

The numerical values of x, y, and z in the above equation are obtained from the maximum error voltage plots. For example, with the ICL8048BC, the maximum error at the output is 30mV at 25°C. This means that the measured output will be within 30mV of the theoretical transfer function, provided the unit has been adjusted per the procedures described previously. Figure 11 illustrates this point.

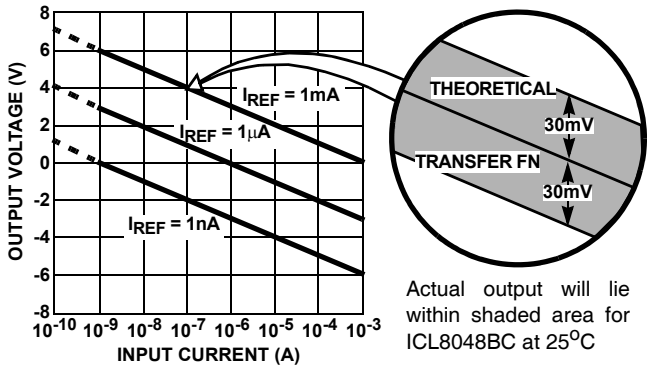


FIGURE 11. TRANSFER FUNCTION FOR CURRENT INPUTS

To determine the maximum error over the operating temperature range, the 0°C to 70°C absolute error values given in the table of electrical specifications should be used. For intermediate temperatures, assume a linear increase in the error between the 25°C value and the 70°C value.

It is important to note that the ICL8048 requires positive values of I_{REF}, and the input current must also be positive. Application of negative I_{IN} to the ICL8048 or negative I_{REF} will cause malfunction, and if maintained for long periods, would lead to device degradation. Some protection can be provided by placing a diode between pin 7 and ground.

Setting Up the Reference Current

The input current reference pin (I_{REF}) is not a true virtual ground. For the ICL8048, a fraction of the output voltage is seen on Pin 16 (Figure 7). This does not constitute an appreciable error provided V_{REF} is much greater than this voltage. A 10V or 15V reference satisfies this condition.

Alternatively, I_{REF} can be provided from a true current source. One method of implementing such a current source is shown in Figure 12.

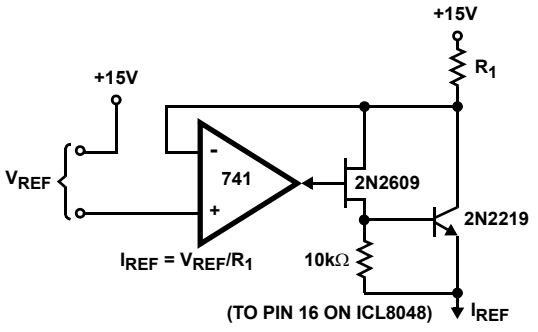


FIGURE 12.

Log of Ratio Circuit, Division

The ICL8048 may be used to generate the log of a ratio by modulating the I_{REF} input. The transfer function remains the same, as defined by Equation 7:

$$V_{OUT} = -K\log_{10}\left[\frac{I_{IN}}{I_{REF}}\right] \quad \text{(EQ. 7)}$$

Clearly it is possible to perform division using just one ICL8048, followed by an antilog amplifier. For multiplication, it is generally necessary to use two log amps, summing their outputs into an antilog amp.

To avoid the problems caused by the I_{REF} input not being a true virtual ground (discussed in the previous section), the circuit of Figure 12 is again recommended if the I_{REF} input is to be modulated.

Definition of Terms

In the definitions which follow, it will be noted that the various error terms are referred to the output of the log amp, and to the input of the antilog amp. The reason for this is explained on the previous page.

Dynamic Range. The dynamic range of the ICL8048 refers to the range of input voltages or currents over which the device is guaranteed to operate.

Error, Absolute Value. The absolute error is a measure of the deviation from the theoretical transfer function, after performing the offset and scale factor adjustments as outlined, (ICL8048). It is expressed in mV and referred to the linear axis of the transfer function plot. Thus, in the case of the ICL8048, it is a measure of the deviation from the theoretical output voltage for a given input current or voltage.

The absolute error specification is guaranteed over the dynamic range.

Error, % of Full Scale. The error as a percentage of full scale can be obtained from the following relationship:

$$\text{Error, \% of Full Scale} = \frac{100 \times \text{Error, absolute value}}{\text{Full Scale Output Voltage}}$$

Temperature Coefficient of V_{OUT}. For the ICL8048 the temperature coefficient refers to the drift with temperature of V_{OUT} for a constant input current.

Power Supply Rejection Ratio. The ratio of the voltage change in the linear axis of the transfer function (V_{OUT} for the ICL8048) to the change in the supply voltage, assuming that the log axis is held constant.

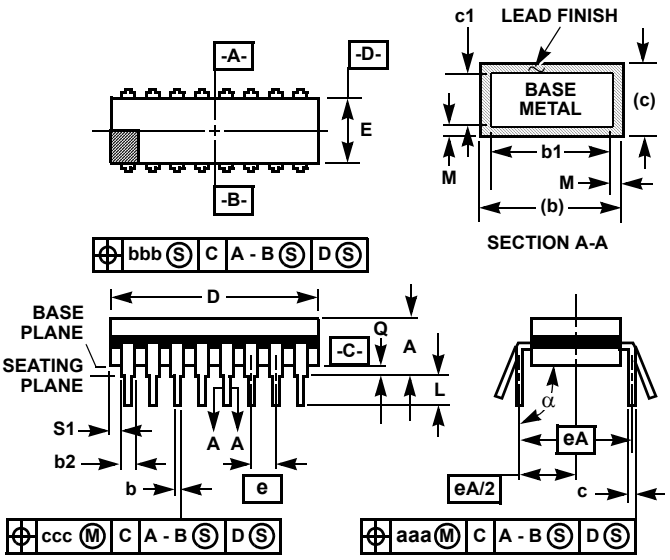
Wideband Noise. For the ICL8048, this is the noise occurring at the output under the specified conditions.

Scale Factor. For the log amp, the scale factor (K) is the voltage change at the output for a decade (i.e., 10:1) change at the input. See Equation 5.

Application Notes

For further applications assistance, see A007 “The ICL8048/8049 Monolithic Log-Antilog Amplifiers”.

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

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