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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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HS54097

Silicon N Channel MOS FET
High Speed Power Switching

REJ03G1669-0100

Rev.1.00

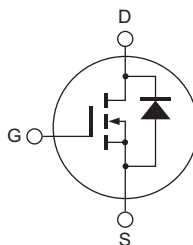
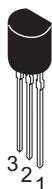
Apr 24, 2008

Features

- Low on-resistance
- Low drive current
- High density mounting

Outline

RENESAS Package code: PRSS0003DA-A
(Package name: TO-92(1))



1. Gate
2. Drain
3. Source

Absolute Maximum Ratings

(Ta = 25°C)

| Item | Symbol | Ratings | Unit |
|---|----------------------------------|-------------|------|
| Drain to source voltage | V_{DSS} | 600 | V |
| Gate to source voltage | V_{GSS} | ±30 | V |
| Drain current | I_D | 0.15 | A |
| Drain peak current | $I_{D(pulse)}$ ^{Note1} | 0.6 | A |
| Body-drain diode reverse drain current | I_{DR} | 0.15 | A |
| Body-drain diode reverse drain peak current | $I_{DR(pulse)}$ ^{Note1} | 0.6 | A |
| Channel dissipation | Pch | 0.75 | W |
| Channel to ambient thermal impedance | θ_{ch-a} | 166.7 | °C/W |
| Channel temperature | Tch | 150 | °C |
| Storage temperature | Tstg | -55 to +150 | °C |

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%

Electrical Characteristics

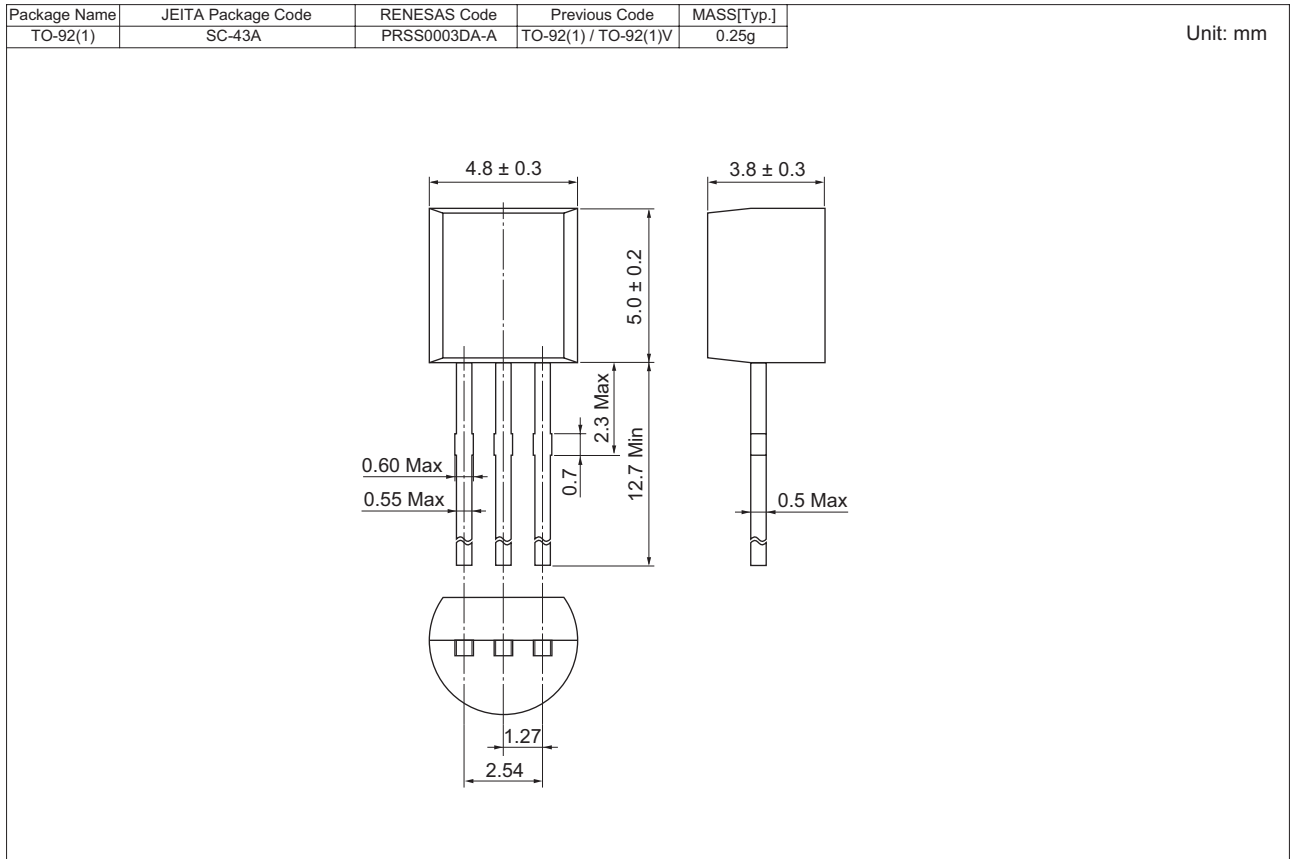
(Ta = 25°C)

| Item | Symbol | Min | Typ | Max | Unit | Test conditions |
|--|---------------|-----|------|-----------|---------------|---|
| Drain to source breakdown voltage | $V_{(BR)DSS}$ | 600 | — | — | V | $I_D = 10 \text{ mA}$, $V_{GS} = 0$ |
| Zero gate voltage drain current | I_{DSS} | — | — | 1 | μA | $V_{DS} = 600 \text{ V}$, $V_{GS} = 0$ |
| Gate to source leak current | I_{GSS} | — | — | ± 0.1 | μA | $V_{GS} = \pm 30 \text{ V}$, $V_{DS} = 0$ |
| Gate to source cutoff voltage | $V_{GS(off)}$ | 3 | — | 5 | V | $V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$ |
| Static drain to source on state resistance | $R_{DS(on)}$ | — | 17 | 25 | Ω | $I_D = 0.075 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note2} |
| Input capacitance | C_{iss} | — | 50 | — | pF | $V_{DS} = 25 \text{ V}$ |
| Output capacitance | C_{oss} | — | 7.2 | — | pF | $V_{GS} = 0$ |
| Reverse transfer capacitance | C_{rss} | — | 1.1 | — | pF | $f = 1 \text{ MHz}$ |
| Turn-on delay time | $t_{d(on)}$ | — | 31 | — | ns | $I_D = 0.075 \text{ A}$ |
| Rise time | t_r | — | 14 | — | ns | $V_{GS} = 10 \text{ V}$ |
| Turn-off delay time | $t_{d(off)}$ | — | 54 | — | ns | $R_L = 4000 \Omega$ |
| Fall time | t_f | — | 218 | — | ns | $R_g = 10 \Omega$ |
| Total gate charge | Q_g | — | 4.5 | — | nC | $V_{DD} = 480 \text{ V}$ |
| Gate to source charge | Q_{gs} | — | 0.5 | — | nC | $V_{GS} = 10 \text{ V}$ |
| Gate to drain charge | Q_{gd} | — | 3.1 | — | nC | $I_D = 0.15 \text{ A}$ |
| Body-drain diode forward voltage | V_{DF} | — | 0.77 | 1.30 | V | $I_F = 0.15 \text{ A}$, $V_{GS} = 0$ ^{Note2} |
| Body-drain diode reverse recovery time | t_{rr} | — | 240 | — | ns | $I_F = 0.15 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 50 \text{ A}/\mu\text{s}$ |

Notes: 2. Pulse test

3. Since this device is equipped with high voltage FET chip ($V_{DSS} \geq 600 \text{ V}$), high voltage may be supplied. Therefore, please be sure to confirm about Electric discharge between Drain terminal and other terminal.

Package Dimensions



Since HS54097 is equipped with high voltage FET chip ($V_{DSS} \geq 600\text{ V}$), high voltage may be supplied. Therefore, please be sure to confirm about Electric discharge between Drain terminal and other terminal.

Ordering Information

| Part No. | Quantity | Shipping Container |
|-------------|----------|-------------------------|
| HS54097TZ-E | 2500 pcs | Hold Box, Radial Taping |

Notes:

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