HS-303ARH, HS-303AEH, HS-303BRH, HS-303BEH

Radiation Hardened CMOS Dual SPDT Analog Switch

Description

The HS-303ARH, HS-303AEH, HS-303BRH, HS-303BEH analog switches are monolithic devices fabricated using the Renesas dielectrically isolated Radiation Hardened Silicon Gate (RSG) process technology to ensure latch-up free operation. They are pinout compatible and functionally equivalent to the HS-303RH, but offer improved 300kRAD(Si) total dose capability. These switches offer low-resistance switching performance for analog voltages up to the supply rails. ON-resistance is low and stays reasonably constant over the full range of operating voltage and current. ON-resistance also stays reasonably constant when exposed to radiation. Break-before-make switching is controlled by 5V digital inputs. The HS-303ARH and HS-303AEH should be operated with nominal ±15V supplies, while the HS-303BRH and HS-303BEH should be operated with nominal ±12V supplies.

Specifications

Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD number listed in the following must be used when ordering.

Detailed Electrical Specifications for the HS-303ARH, HS-303AEH, HS-303BRH, HS-303BEH are contained in SMD 5962-95813.

Functional Diagram

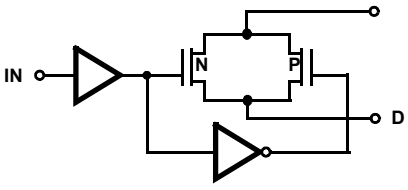


Table 1. Truth Table

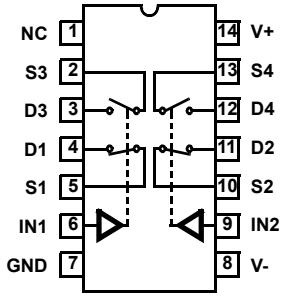
Logic	SW1 and SW2	SW3 and SW4
0	OFF	ON
1	ON	OFF

Features

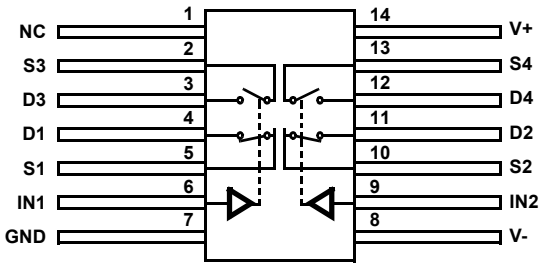
- QML, per MIL-PRF-38535
- Radiation acceptance testing - HS-303xEH
  - HDR (50-300rad(Si)/s): 300krad(Si)
  - LDR (0.01rad(Si)/s): 50krad(Si)
- Radiation acceptance testing - HS-303xRH
  - HDR (50-300rad(Si)/s): 300krad(Si)
- SEE hardness (see SEE report for details)
  - SEE: For LET = 60MeV•cm^2/mg at 60° incident angle, <150pC charge transferred to the output of an off switch (based on SOI design calculations)
- No latch-up, dielectrically isolated device islands
- Pinout and functionally compatible with Renesas HS-303RH and HI-303 series analog switches
- Analog signal range equal to the supply voltage range
- Low leakage: 100nA (max, post-rad)
- Low r_{ON}: 70Ω (max, post-rad)
- Low standby supply current: +150µA/-100µA (max, post-rad)

Pin Configurations

HS1-303ARH, HS-303BRH
(SBDIP), CDIP2-T14
Top View



HS-303ARH, HS-303AEH, HS-303BRH, HS-303BEH
(FLATPACK) CDFP3-F14
Top View



1. Overview

1.1 Ordering Information

Ordering Number[1]	Part Number[2]	Radiation Hardness (Total Ionizing Dose)	Package (RoHS Compliant)	Pkg. Dwg. #	Temp. Range (°C)
5962F9581304QCC	HS1-303ARH-8	HDR to 300krad(Si)	14 LD SBDIP	D14.3	-55 to +125
5962F9581304QXC	HS9-303ARH-8		14 LD Flatpack	K14.A	-55 to +125
5962F9581304V9A	HS0-303ARH-Q[3]		Die	-	-55 to +125
5962F9581304VCC	HS1-303ARH-Q		14 LD SBDIP	D14.3	-55 to +125
5962F9581304VXC	HS9-303ARH-Q		14 LD Flatpack	K14.A	-55 to +125
5962F9581306V9A	HS0-303AEH-Q[3]	HDR to 300krad(Si), LDR to 50krad(Si)	Die	-	-55 to +125
5962F9581306VCC	HS1-303AEH-Q		14 LD SBDIP	D14.3	-55 to +125
5962F9581306VXC	HS9-303AEH-Q		14 LD Flatpack	K14.A	-55 to +125
N/A	HS0-303ARH/SAMPLE[3][4]	N/A	Die	-	-55 to +125
N/A	HS1-303ARH/PROTO[4]		14 LD SBDIP	D14.3	-55 to +125
N/A	HS9-303ARH/PROTO[4]		14 LD Flatpack	K14.A	-55 to +125
5962F9581305QCC	HS1-303BRH-8	HDR to 300krad(Si)	14 LD SBDIP	D14.3	-55 to +125
5962F9581305QXC	HS9-303BRH-8		14 LD Flatpack	K14.A	-55 to +125
5962F9581305V9A	HS0-303BRH-Q[3]		Die	-	-55 to +125
5962F9581305VCC	HS1-303BRH-Q		14 LD SBDIP	D14.3	-55 to +125
5962F9581305VXC	HS9-303BRH-Q		14 LD Flatpack	K14.A	-55 to +125
5962F9581307V9A	HS0-303BEH-Q[3]	HDR to 300krad(Si), LDR to 50krad(Si)	Die	-	-55 to +125
5962F9581307VCC	HS1-303BEH-Q		14 LD SBDIP	D14.3	-55 to +125
5962F9581307VXC	HS9-303BEH-Q		14 LD Flatpack	K14.A	-55 to +125
N/A	HS0-303BRH/SAMPLE[3][4]	N/A	Die	-	-55 to +125
N/A	HS1-303BRH/PROTO[4]		14 LD SBDIP	D14.3	-55 to +125
N/A	HS9-303BRH/PROTO[4]		14 LD Flatpack	K14.A	-55 to +125

1. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
2. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
3. Die product tested at T_A = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in the DLA SMD.
4. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.

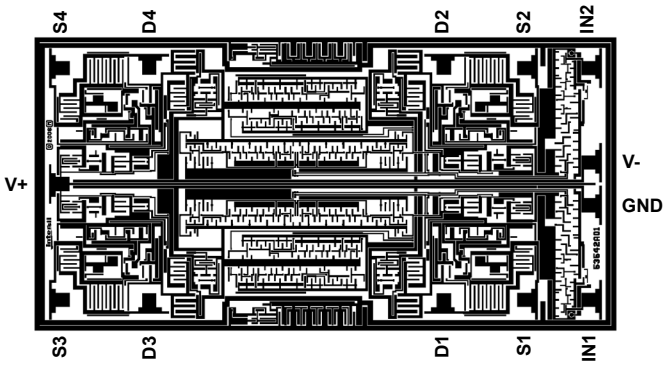
2. Die Characteristics

Table 2. Die and Assembly Related Information

Die Information	
Dimensions	2690µm x 5200µm (106mils x 205mils) Thickness: 483µm ± 25.4µm (19mils ± 1mil)
Interface Materials	
Glassivation	Type: PSG (Phosphorous Silicon Glass) Thickness: 8.0kÅ ± 1.0kÅ
Top Metallization	Type: AlSiCu Thickness: 16.0kÅ ± 2kÅ
Substrate	Radiation Hardened Silicon Gate, Dielectric Isolation
Backside Finish	Silicon
Assembly Information	
Substrate Potential	Unbiased (DI)
Additional Information	
Worst Case Current Density	$<2.0 \times 10^5 A/cm^2$
Transistor Count	332
Weight of Packaged Device	0.31 grams
Lid Characteristics	Finish: Gold Potential: Floating

2.1 Metallization Mask Layout

HS-303ARH, HS-303AEH, HS-303BRH, HS-303BEH



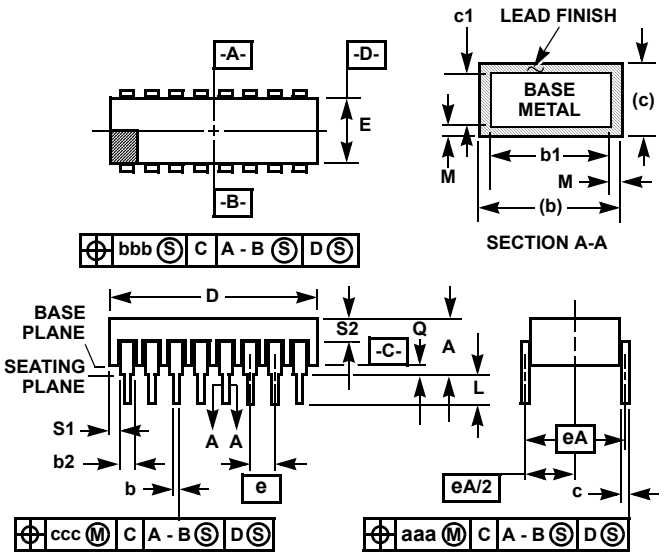
3. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

4. Revision History

Rev.	Date	Description
5.01	May 23, 2025	Applied latest template. Updated POD K14.A to the latest version; changes are as follows: -Applied latest template -Corrected typo in the mm value for dimension E1 from 7.11 to 7.37mm
5.00	Sep 14, 2020	Updated radiation features to new format. Updated ordering information table by adding TID information and notes 3 and 4. On page 3 updated the Lid Characteristics Potential from Grounded, tied to package pin 2, to Floating.
4.00	Jul 18, 2019	Applied new formatting throughout. Updated links throughout. Updated second Features bullet. Updated ordering information table removed package drawing for die related parts and updated notes. Added Revision History section. Updated Disclaimer.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

D14.3 MIL-STD-1835 CDIP2-T14 (D-1, Configuration C)
14 Lead Ceramic Dual In-Line Metal Seal Package

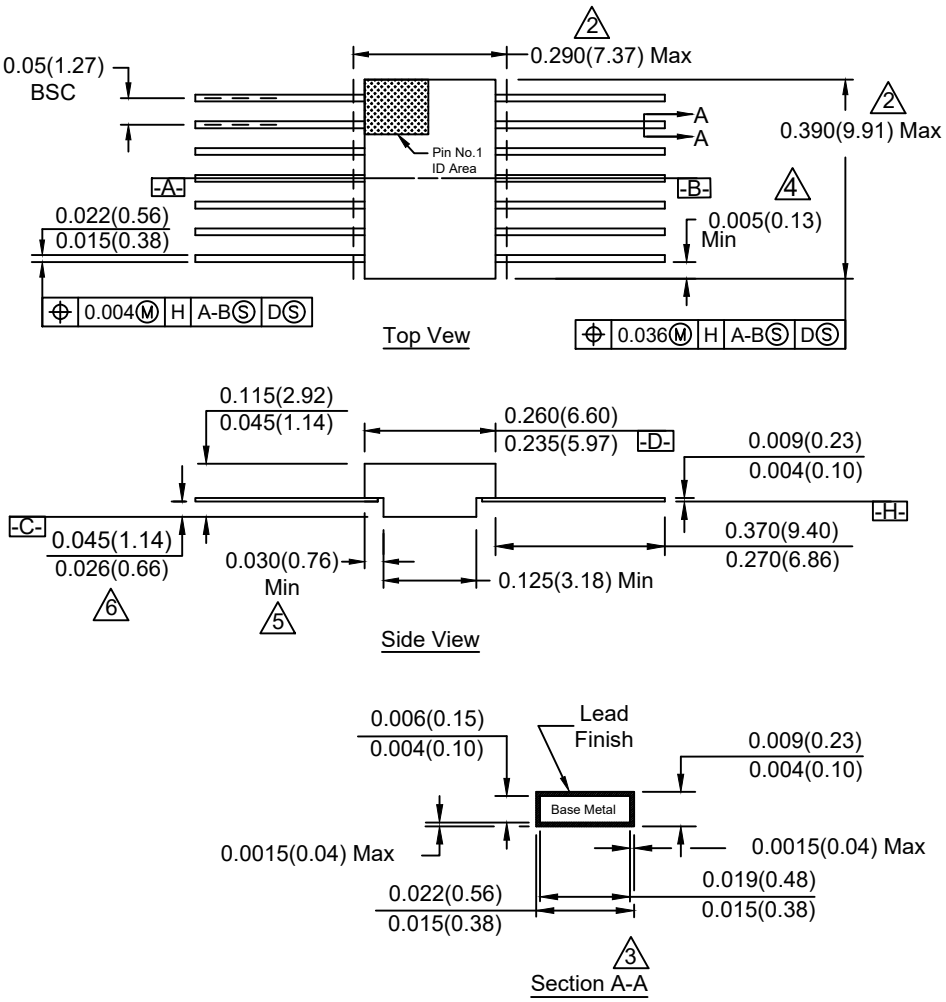
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.785	-	19.94	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	14		14		8

Rev. 0 4/94

Package Outline Drawing

14 Lead Ceramic Metal Seal Flatpack Package

POD Number: K14.A, Revision no: 02, Date Created: Mar 4, 2025



Notes:

1 Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacture's identification shall not be used as a pin one identification mark.

2 This dimension allows for off-center lid, meniscus, and glass overrun.

3 The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate finish is applied.

4 Measure dimension at all four corners.

5 For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.

6 This dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. This dimension's minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.

7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.

8. Dimensions: INCH(mm). Controlling dimension: INCH.

9. Compliant to MIL-STD-1835 CDFP3-F14 (F-2A, CONFIGURATION B).

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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