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DATASHEET

HS-2510RH

Radiation Hardened High Slew Rate Operational Amplifier

The HS-2510RH is a radiation hardened high performance operational amplifier which set the standard for maximum slew rate and wide bandwidth operation in moderately powered, internally compensated, monolithic devices. In addition to excellent dynamic characteristics, this dielectrically isolated amplifier also offers low offset current and high input impedance.

The \pm 50V/ms minimum slew rate and fast settling time of the HS-2510RH are ideally suited for high speed D/A, A/D, and pulse amplification designs. The HS-2510RH superior bandwidth and 750kHz minimum full power bandwidth are extremely useful in RF and video applications. To insure compliance with slew rate and transient response specifications, all devices are 100% tested for AC performance characteristics over full temperature limits. To improve signal conditioning accuracy, the HS-2510RH provides a maximum offset current of 25nA and a minimum input impedance of 50M Ω , both at 25°C, as well as offset voltage trim capability.

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed here must be used when ordering.

Detailed Electrical Specifications for these devices are contained in SMD 5962-95686. A "hot-link" is provided on our homepage for downloading.

Features

- Electrically Screened to SMD # 5962-95686
- QML Qualified per MIL-PRF-38535 Requirements
- High Slew Rate 50V/µs (Min), 65V/µs (Typ)
- Wide Power Bandwidth 750kHz (Min)
- High Input Impedance $\dots \dots 50M\Omega$ (Min), $100M\Omega$ (Typ)
- Wide Small Signal Bandwidth 12MHz (Typ)
- Fast Settling Time (0.1% of 10V Step)..... 250ns (Typ)
- · Internally Compensated For Unity Gain Stability
- Total Gamma Dose 10kRAD(Si)

Applications

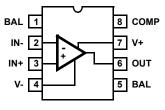
- Data Acquisition Systems
- RF Amplifiers
- Video Amplifiers
- Signal Generators
- Pulse Amplification

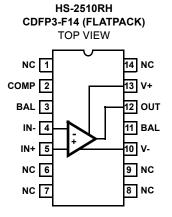
Ordering Information

ORDERING NUMBER	INTERNAL MKT. NUMBER	TEMP. RANGE (^o C)
5962D9568601VPA	HS7-2510RH-Q	-55 to 125
5962D9568601VPC	HS7B-2510RH-Q	-55 to 125
5962D9568601VXC	HS9-2510RH-Q	-55 to 125

Pinouts



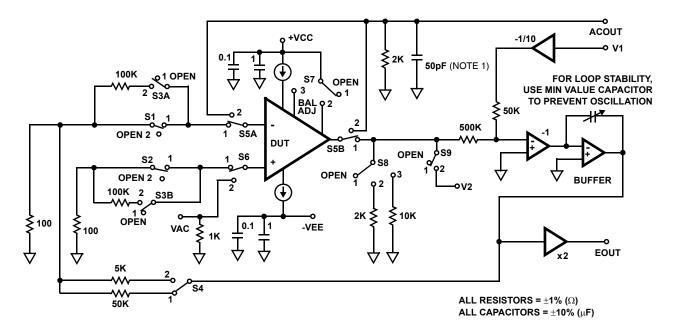




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FN3592 Rev.2.00 August 1999

Test Circuit

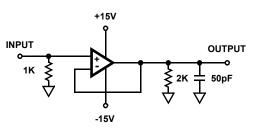


NOTE:

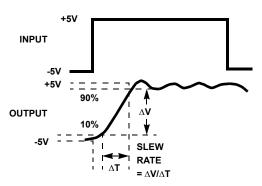
1. Includes stray capacitances.

FIGURE 1. SIMPLIFIED TEST CIRCUIT

Test Circuit and Waveforms

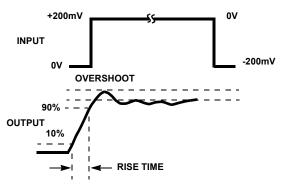






NOTE: Measured on both positive and negative transitions. Capacitance at Compensation pin should be minimized.

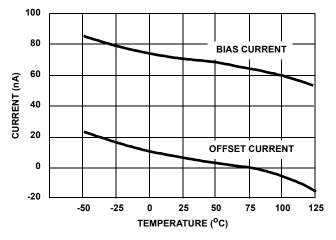
FIGURE 3. SLEW RATE WAVEFORM



NOTE: Measured on both positive and negative transitions. Capacitance at Compensation pin should be minimized.

FIGURE 4. TRANSIENT RESPONSE WAVEFORM

Typical Performance Curves Unless Otherwise Specified: $T_A = 25^{\circ}C$, VSUPPLY = $\pm 15V$





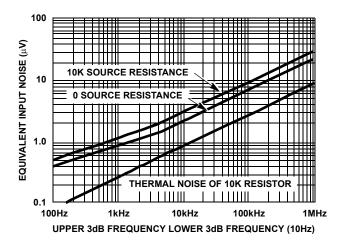
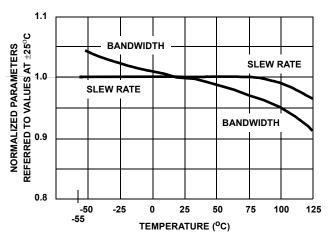


FIGURE 7. EQUIVALENT INPUT NOISE vs BANDWIDTH





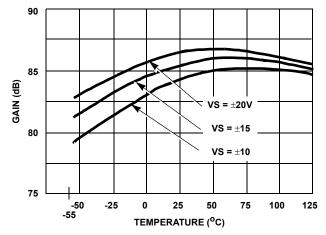


FIGURE 6. OPEN LOOP VOLTAGE GAIN vs TEMPERATURE

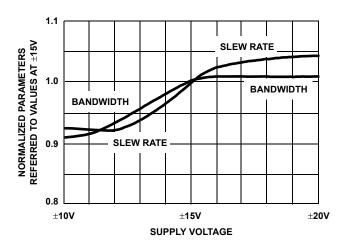
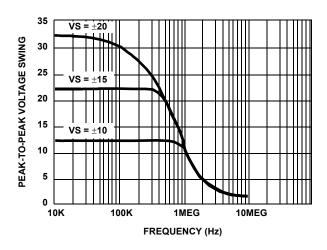
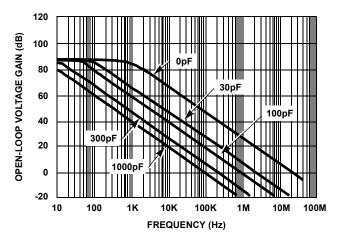


FIGURE 8. NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE AT 25°C

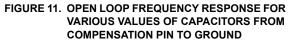


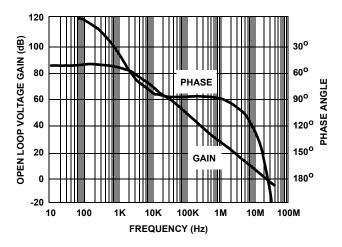


Typical Performance Curves Unless Otherwise Specified: $T_A = 25^{\circ}C$, VSUPPLY = ±15V (Continued)



NOTE: External compensation components are not required for stability, but may be added to reduce bandwidth, if desired.







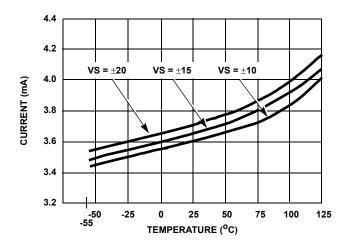
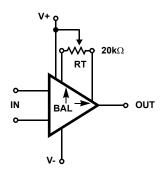


FIGURE 12. POWER SUPPLY CURRENT vs TEMPERATURE



NOTE: Tested offset adjustment is |VOS + 1mV| minimum referred to output typical range is $\pm 8mV$ for RT = $20k\Omega$.

FIGURE 14. SUGGESTED VOS ADJUSTMENT

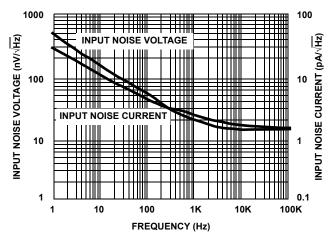
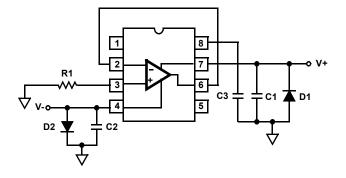


FIGURE 15. INPUT NOISE DENSITY vs FREQUENCY

Burn-In Circuits

HS7-2510RH CERDIP

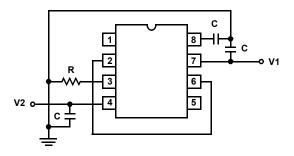


NOTES:

- 2. R1 = 1M Ω , ±5%, 1/4W (Min)
- 3. C1 = C2 = 0.01μ F/Socket (Min) or 0.1μ F/Row (Min)
- 4. C3 = 0.01µF/Socket (10%)
- 5. D1 = D2 = 1N4002 or Equivalent (Per Board)
- 6. |(V+) (V-)| = 30V

Irradiation Circuit

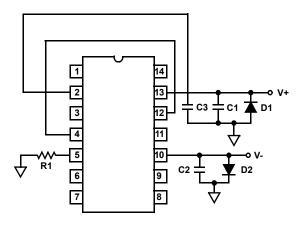
HS7-2510RH



NOTES:

- 12. V1 = +15V $\pm 10\%$
- 13. V2 = -15V $\pm 10\%$
- 14. R = 1M $\Omega \pm 5\%$
- 15. C = $0.1 \mu F \pm 10\%$

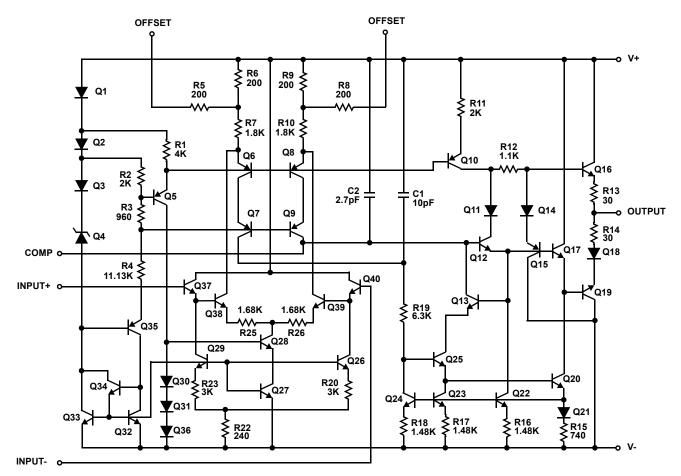
HS9-2510RH CERAMIC FLATPACK



NOTES:

- 7. R1 = 1M Ω , ±5%, 1/4W (Min)
- 8. C1 = C2 = 0.01μ F/Socket (Min) or 0.1μ F/Row (Min)
- 9. C3 = 0.01μ F/Socket (±10%)
- 10. D1 = D2 = 1N4002 or Equivalent (Per Board)
- 11. $|(V+) (V-)| = 31V \pm 1V$

Schematic Diagram



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Die Characteristics

DIE DIMENSIONS:

65 mils x 57 mils x 19 mils (1660μm x 1950μm x 483μm)

INTERFACE MATERIALS:

Glassivation:

Type: Nitride Thickness: 7kÅ ±0.7kÅ

Top Metallization:

Type: Aluminum Thickness: 16kÅ ±2kÅ

Substrate:

Linear Bipolar, DI

Metallization Mask Layout

Silicon ASSEMBLY RELATED INFORMATION: Substrate Potential (Powered Up): Unbiased ADDITIONAL INFORMATION: Worst Case Current Density:

 $<2 \text{ x } 10^5 \text{A/cm}^2$

Backside Finish:

Transistor Count:

40

Die Attach: Temperature: CERDIP 460°C (Max)

HS-2510RH

