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HMP8170

NTSC/PAL Video Encoder

FN4284
Rev 6.00
Sep 2003

The HMP8170 NTSC and PAL encoder is designed for use in systems requiring the generation of high-quality NTSC and PAL video.

YCbCr digital video data drive the P0-P15 inputs. The Y data is optionally lowpass filtered to 6MHz and drives the Y analog output. Cb and Cr are each lowpass filtered to 1.3MHz, quadrature modulated, and added together. The result drives the C analog output. The digital Y and C data are also added together and drive the two composite analog outputs.

The DACs can drive doubly-terminated (37.5Ω) lines, and run at a 2x oversampling rate to simplify the analog output filter requirements.

Applications

- DVD Players
- Video CD Players
- Digital VCRs
- Multimedia PCs

Related Products

- NTSC/PAL Encoders
  - HMP8156
- NTSC/PAL Decoders
  - HMP8117

Features

- (M) NTSC and (B, D, G, H, I, M, N, NC) PAL Operation
- BT.601 and Square Pixel Operation
- Digital Input Formats
  - 8-bit, 16-bit 4:2:2 YCbCr
  - 8-bit BT.656
- Analog Output Formats
  - Y/C + Two Composite
  - RGB + Composite
  - YUV + Composite
- Flexible Video Timing Control
  - Timing Master or Slave
  - Selectable Polarity on Each Control Signal
  - Programmable Blank Output Timing
- “Sliced” VBI Data Support
  - Closed Captioning
  - Widescreen Signalling (WSS)
  - BT.653 System B and C Teletext
    - NABTS (North American Broadcast Teletext)
    - WST (World System Teletext)
- Four 2x Oversampling, 10-Bit DACs
- Fast I^2C Interface

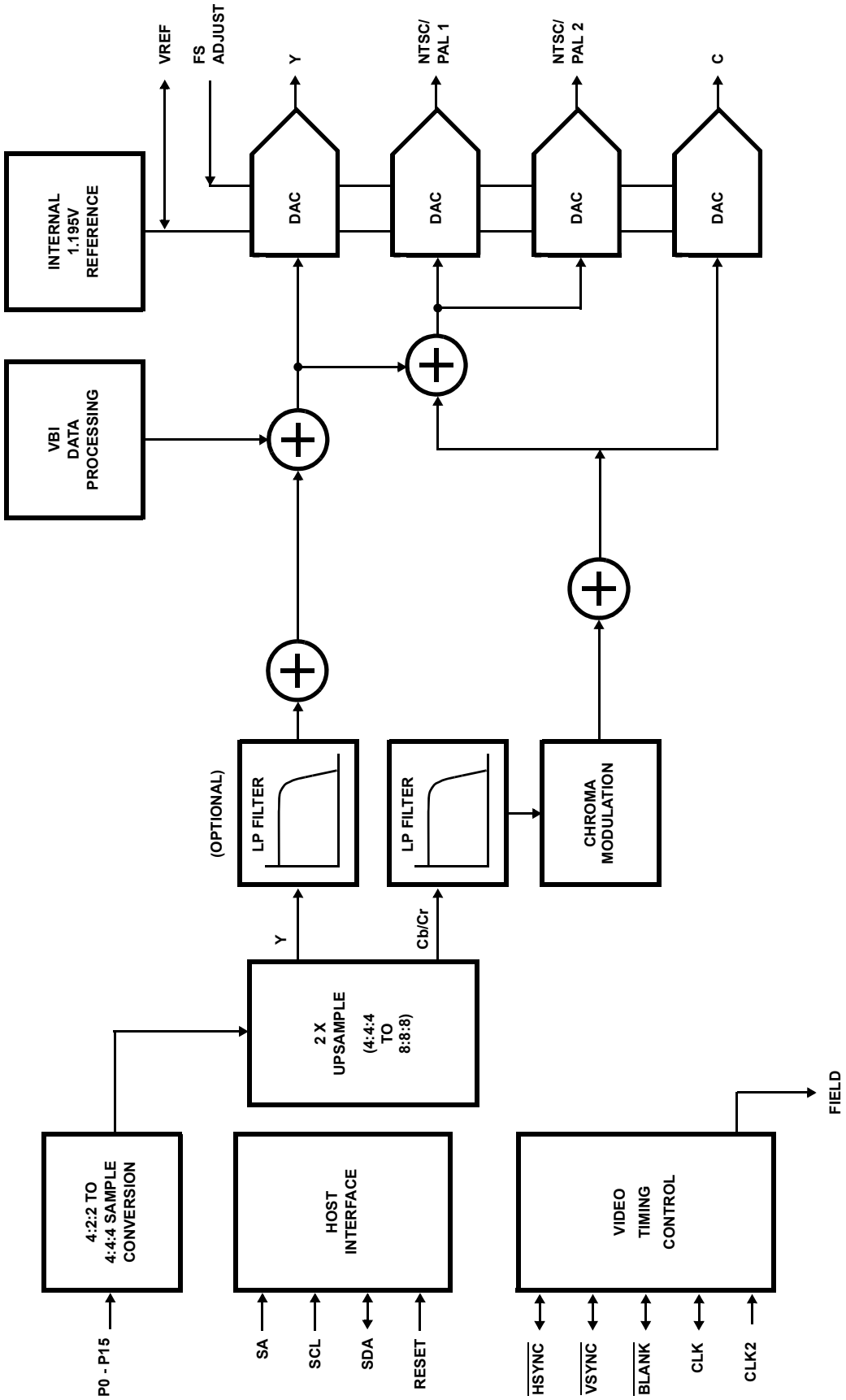
Ordering Information

PART NUMBER	MACROVISION v7.01	RGB / YUV OUTPUTS	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HMP8170CN	no	no	0 to 70	64 Ld PQFP (Note 1)	Q64.14x14
HMP8170EVAL1	Daughter Card Evaluation Platform, (Note 2).				

NOTES:

1. PQFP is also known as QFP and MQFP.
2. Evaluation board descriptions are in the Applications section.

Functional Block Diagram



Functional Operation

The HMP8170 is a fully integrated digital encoder. It accepts YCbCr digital video input data and generate analog video output signals. The four outputs are two composite video signals and Y/C (S-Video).

The HMP8170 accepts pixel data in one of several formats and transforms it into 4:4:4 sampled luminance and chrominance (YCbCr) data. The encoder then interpolates the YCbCr data to twice the pixel rate and low pass filters it to match the bandwidth of the video output format. If enabled, the encoder also adds vertical blanking interval (VBI) information to the Y data. At the same time, the encoder modulates the chrominance data with a digitally synthesized subcarrier. Finally, the encoder outputs luminance, chrominance, and their sum as analog signals using 10-bit D/A converters.

The HMP8170 provides operating modes to support all versions of the NTSC and PAL standards and accepts full size input data with rectangular (BT.601) and square pixel aspect ratios. It operates from a single clock at twice the pixel clock rate determined by the operating mode.

The HMP8170's video timing control is flexible. It may operate as the master, generating the system's video timing control signals, or it may accept external timing controls. The polarity of the timing controls and the number of active pixels and lines are programmable.

Pixel Data Input

The HMP8170 accepts BT.601 YCbCr pixel data via the P0-P15 input pins. The definition of each pixel input pin is determined by the input format selected in the input format register. The definition for each mode is shown in Table 1.

The YCbCr luminance and color difference signals are each 8 bits, scaled 0 to 255. The nominal range for Y is 16 (black) to 235 (white). Y values less than 16 are clamped to 16; values greater than 235 are processed normally. The nominal range for Cb and Cr is 16 to 240 with 128 representing zero. Cb and Cr values outside their nominal range are processed normally. Note that when converted to the analog outputs, some combinations of YCbCr outside their nominal ranges would generate a composite video signal larger than the analog output limit. The composite signal will be clipped, but the S-video outputs (Y and C) will note be.

The color difference signals are time multiplexed into one 8-bit bus beginning with a Cb sample. The Y and CbCr busses may be input in parallel (16-bit mode) or may be time multiplexed and input as a single bus (8-bit mode). The single bus may also contain SAV and EAV video timing reference codes or ancillary data (BT.656 mode).

TABLE 1. PIXEL DATA INPUT FORMATS

PIN NAME	16-BIT 4:2:2 YCBCR	8-BIT 4:2:2 YCBCR	BT.656
P0 P1 P2 P3 P4 P5 P6 P7	Cb0, Cr0 Cb1, Cr1 Cb2, Cr2 Cb3, Cr3 Cb4, Cr4 Cb5, Cr5 Cb6, Cr6 Cb7, Cr7	Ignored	
P8 P9 P10 P11 P12 P13 P14 P15	Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7	Y0, Cb0, Cr0 Y1, Cb1, Cr1 Y2, Cb2, Cr2 Y3, Cb3, Cr3 Y4, Cb4, Cr4 Y5, Cb5, Cr5 Y6, Cb6, Cr6 Y7, Cb7, Cr7	YCbCr Data, SAV and EAV Sequences, and Ancillary Data

Pixel Input and Control Signal Timing

The pixel input timing and the video control signal input/output timing of the HMP8170 depend on the part's operating mode. The periods when the encoder samples its inputs and generates its outputs are summarized in Table 2.

Figures 1, 2, and 3 show the timing of CLK, CLK2, $\overline{\text{BLANK}}$, and the pixel input data with respect to each other. $\overline{\text{BLANK}}$ may be an input or an output; the figures show both. When it is an input, $\overline{\text{BLANK}}$ must arrive coincident with the pixel input data; all are sampled at the same time.

When $\overline{\text{BLANK}}$ is an output, its timing with respect to the pixel inputs depends on the blank timing select bit in the timing_I/O_1 register. If the bit is cleared, the HMP8170 negates $\overline{\text{BLANK}}$ one CLK cycle before it samples the pixel inputs.

If the bit is set, the encoder negates $\overline{\text{BLANK}}$ during the same CLK cycle in which it samples the input data. In effect, the input data must arrive one CLK cycle earlier than when the bit is cleared. This mode is not shown in the figures.

TABLE 2. PIXEL INPUT AND CONTROL SIGNAL I/O TIMING

INPUT FORMAT	INPUT PIXEL DATA SAMPLE	VIDEO TIMING CONTROL (NOTE)		CLK FREQUENCY	
		INPUT SAMPLE	OUTPUT ON	INPUT	OUTPUT
16-Bit YCbCr	Rising edge of CLK2 when CLK is low		Rising edge of CLK2 when CLK is high.	One-half CLK22	
8-Bit YCbCr	Every rising edge of CLK2	Every rising edge of CLK2	Any rising edge of CLK2	Ignored	One-half CLK2
BT.656	Every rising edge of CLK2	Not Allowed	Any rising edge of CLK2	Ignored	One-half CLK2

NOTE: Video timing control signals include $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{BLANK}}$ and FIELD. The sync and blanking I/O directions are independent; FIELD is always an output.

8-Bit YCbCr Format

When 8-bit YCbCr format is selected, the data is latched on each rising edge of CLK2. The pixel data must be [Cb Y Cr Y' Cb Y Cr Y' . . .], with the first active data each scan line being Cb data. The pixel input timing is shown in Figure 1.

As inputs, $\overline{\text{BLANK}}$, $\overline{\text{HSYNC}}$, and $\overline{\text{VSYNC}}$ are latched on each rising edge of CLK2. As outputs, $\overline{\text{BLANK}}$, $\overline{\text{HSYNC}}$, and $\overline{\text{VSYNC}}$ are output following the rising edge of CLK2. If the CLK pin is configured as an input, it is ignored. If configured as an output, it is one-half the CLK2 frequency.

16-Bit YCbCr Format

When 16-bit YCbCr format is selected, the pixel data is latched on the rising edge of CLK2 while CLK is low. The pixel input timing is shown in Figure 2.

As inputs, $\overline{\text{BLANK}}$, $\overline{\text{HSYNC}}$, and $\overline{\text{VSYNC}}$ are latched on the rising edge of CLK2 while CLK is low. As outputs, $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and $\overline{\text{BLANK}}$ are output following the rising edge of CLK2 while CLK is high. In these modes of operation, CLK is one-half the CLK2 frequency.

8-Bit BT.656 Format

When BT.656 format is selected, data is latched on each rising edge of CLK2. The pixel input timing is shown in Figure 3. The figure shows the EAV code at the end of the line. The format of the SAV and EAV codes are shown in Table 3.

The BT.656 input may also include ancillary data to load the VBI or RTCI data registers. The HMP8170 will use the ancillary data when enabled in the VBI data input and Timing I/O registers. The ancillary data formats and the enable registers are described later in this data sheet.

As inputs, the $\overline{\text{BLANK}}$, $\overline{\text{HSYNC}}$, and $\overline{\text{VSYNC}}$ pins are ignored since all timing is derived from the EAV and SAV sequences within the data stream. As outputs, $\overline{\text{BLANK}}$, $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ are output following the rising edge of CLK2. If the CLK pin is configured as an input, it is ignored. If configured as an output, it is one-half the CLK2 frequency.

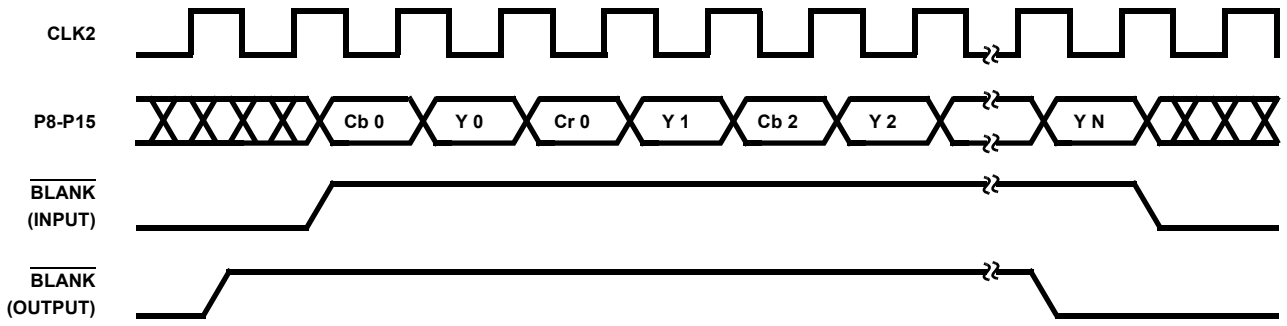


FIGURE 1. PIXEL INPUT TIMING - 8-BIT YCBCR

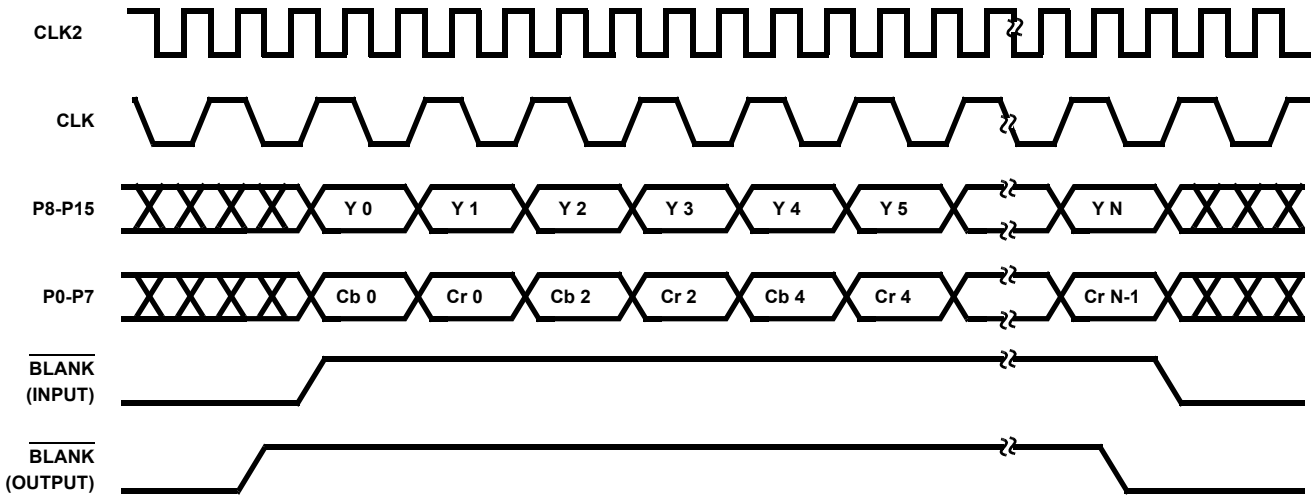


FIGURE 2. PIXEL INPUT TIMING - 16-BIT YCBCR

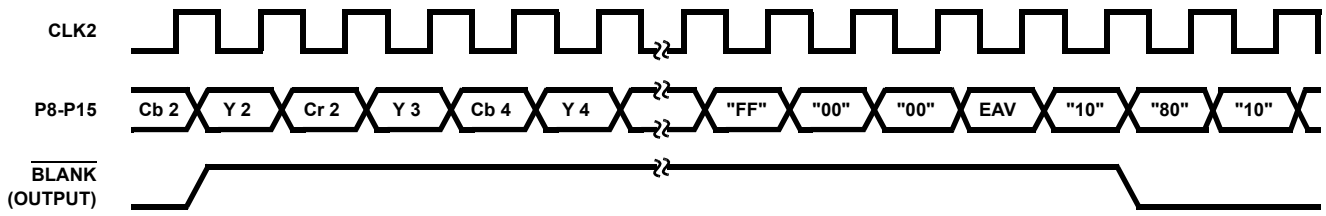


FIGURE 3. PIXEL INPUT TIMING - BT.656

TABLE 3. BT.656 EAV AND SAV SEQUENCES

PIXEL INPUT	P15	P14	P13	P12	P11	P10	P9	P8
Preamble Word 1	1	1	1	1	1	1	1	1
Preamble Word 2	0	0	0	0	0	0	0	0
Preamble Word 3	0	0	0	0	0	0	0	0
Status Word	1	F	V	H	P3	P2	P1	P0

NOTES:
F: 0 = Field 1; 1 = Field 2
V: 0 = Active Line; 1 = Vertical Blanking
H: 0 = Start Active Video; 1 = End Active Video
P3 - P0: Protection bits; Ignored

Video Timing Control

The pixel input data and the output video timing of the HMP8170 are at 50 or 59.94 fields per second interlaced. The timing is controlled by the $\overline{\text{BLANK}}$, $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, FIELD, and CLK2 pins.

$\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and Field Timing

The leading edge of $\overline{\text{HSYNC}}$ indicates the beginning of a horizontal sync interval. If $\overline{\text{HSYNC}}$ is an output, it is asserted for about 4.7µs. If $\overline{\text{HSYNC}}$ is an input, it must be active for at least two CLK2 periods. The width of the analog horizontal sync tip is determined from the video standard and does not depend on the width of $\overline{\text{HSYNC}}$.

The leading edge of $\overline{\text{VSYNC}}$ indicates the beginning of a vertical sync interval. If $\overline{\text{VSYNC}}$ is an output, it is asserted for 3 scan lines in (MM) NTSC and (M, N) PAL modes or 2.5 scan lines in (B, D, G, H, I, NC) PAL modes. If $\overline{\text{VSYNC}}$ is an input, it must be asserted for at least two CLK2 periods.

When $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ are configured as outputs, their leading edges will occur simultaneously at the start of an odd field. At the start of an even field, the leading edge of $\overline{\text{VSYNC}}$ occurs in the middle of the line.

When $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ are configured as inputs, the HMP8170 provides a programmable $\overline{\text{HSYNC}}$ window for determining FIELD. The window is specified with respect to the leading or trailing edge of $\overline{\text{VSYNC}}$. The edge is selected in the field control register. When $\overline{\text{HSYNC}}$ is found inside the window, then the encoder sets FIELD to the value specified in the field control register.

The HMP8170 provides programmable timing for the $\overline{\text{VSYNC}}$ input. At the active edge of $\overline{\text{VSYNC}}$, the encoder resets its vertical half-line counter to the value specified by the field control register. This allows the input and output syncs to be offset, although the data must still be aligned.

The FIELD signal is always an output and changes state near each leading edge of $\overline{\text{VSYNC}}$. The delay between the syncs and FIELD depends on the encoder's operating mode as summarized in Table 4. In modes in which the encoder uses CLK to gate its inputs and outputs, the FIELD signal may be delayed 0-12 additional CLK2 periods.

TABLE 4. FIELD OUTPUT TIMING

OPERATING MODE		CLK2 DELAY	COMMENTS
SYNC I/O DIRECTION	BLANK I/O DIRECTION		
Input	Input	148	FIELD lags $\overline{\text{VSYNC}}$ switching from odd to even. FIELD lags the earlier of $\overline{\text{VSYNC}}$ and $\overline{\text{HSYNC}}$ when syncs are aligned when switching from even to odd.
Input	Output	138	FIELD lags $\overline{\text{VSYNC}}$.
Output	Don't Care	32	FIELD leads $\overline{\text{VSYNC}}$.

Figure 4 illustrates the $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and FIELD general timing for (M) NTSC and (M, N) PAL. Figure 5 illustrates the general timing for (B, D, G, H, I, NC) PAL. In the figures, all the signals are shown active low (their reset state), and FIELD is low during odd fields.

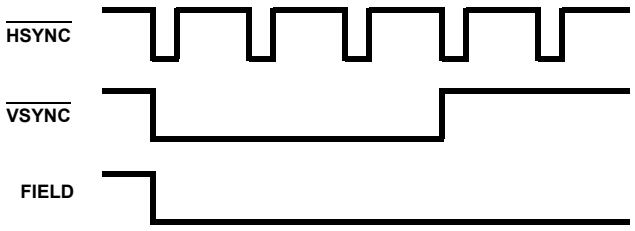


FIGURE 4A. BEGINNING AN ODD FIELD

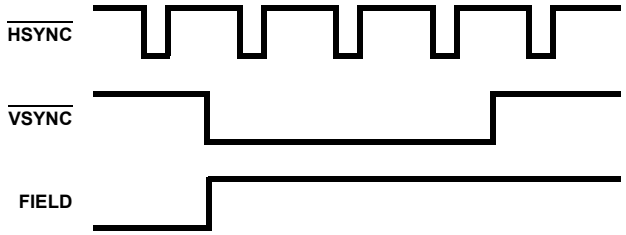


FIGURE 4B. BEGINNING AN EVEN FIELD

FIGURE 4. HSYNC, VSYNC, AND FIELD TIMING FOR (M) NTSC AND (M, N) PAL

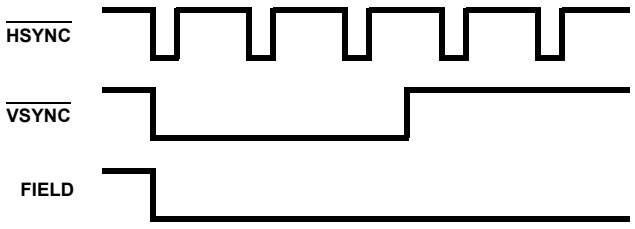


FIGURE 5A. BEGINNING AN ODD FIELD

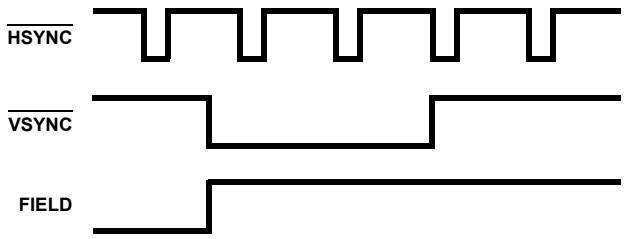


FIGURE 5B. BEGINNING AN EVEN FIELD

FIGURE 5. HSYNC, VSYNC, AND FIELD TIMING FOR (B, D, G, H, I, NC) PAL

BLANK Timing

The encoder uses the HSYNC, VSYNC, FIELD signals to generate a standard composite video waveform with no active video (black burst). The signal includes only sync tips, color burst, and optionally, a 7.5 IRE blanking setup. Based on the BLANK signal, the encoder adds the pixel input data to the video waveform.

The encoder ignores the pixel input data when BLANK is asserted. Instead of the input data, the encoder generates the blanking level. The encoder also ignores the pixel inputs when generating VBI data on a specific line, even if BLANK is negated.

There must be an even number of active and total pixels per line. In the 8-bit YCbCr modes, the number of active and total pixels per line must be a multiple of four. Note that if BLANK is an output, half-line blanking on the output video cannot be done.

The HMP8170 never adds a 7.5 IRE blanking setup during the active line time on scan lines 1-21 and 263-284 for (M) NTSC, scan lines 523-18 and 260-281 for (M) PAL, and scan lines 623-22 and 311-335 for (B, D, G, H, I, N) PAL, allowing the generation of video test signals, timecode, and other information by controlling the pixel inputs appropriately.

The relative timing of BLANK, HSYNC, and the output video depends on the blanking and sync I/O directions. The typical timing relation is shown in Figure 6. The delays which vary with operating mode are indicated. The width of the composite sync tip and the location and duration of the color burst are fixed based on the video format.

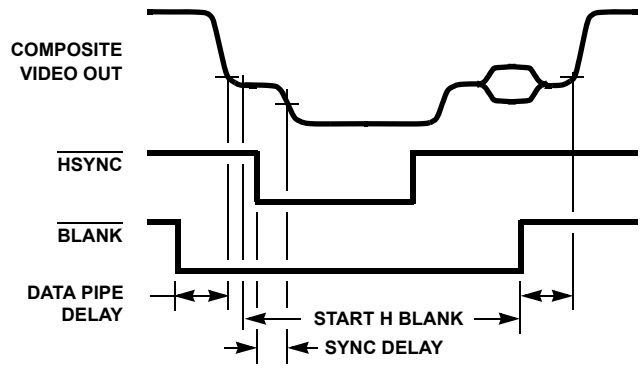


FIGURE 6. HSYNC, BLANK, AND OUTPUT VIDEO TIMING, NORMAL MODE

When BLANK is an output, the encoder asserts it during the inactive portions of active scan lines (horizontal blanking) and for all of each inactive scan line (vertical blanking). The inactive scan lines blanked each field are determined by the start_v_blank and end_v_blank registers. The inactive portion of active scan lines is determined by the start_h_blank and end_h_blank registers.

The zero count for horizontal blanking is 32 CLK2 cycles before the 50% point of the composite sync. From this zero point, the HMP8170 counts every other CLK2 cycle. When the count reaches the value in the start_h_blank register, the encoder negates BLANK. When the count reaches the value in the end_h_blank register, BLANK is asserted. There may be an additional 0-3 CLK2 delays in modes which use CLK.

The data pipeline delay through the HMP8170 is 26 CLK2 cycles. In operating modes which use CLK to gate the inputs into the encoder, the delay may be an additional 0-7 CLK2 cycles. The delay from BLANK to the start or end of active video is an additional one-half CLK cycle when the blank timing select bit is cleared. The active video may also appear to end early or start late since the HMP8170 controls the blanking edge rates.

TABLE 5. TYPICAL VIDEO TIMING PARAMETERS

VIDEO STANDARD	PIXELS PER LINE		HBLANK REGISTER VALUES		VBLANK REGISTER VALUES		CLK2 (MHz)
	TOTAL	ACTIVE	START	END	START	END	
RECTANGULAR PIXELS (BT.601)							
(M) NTSC	858	720	842 (0x34a)	122 (0x7a)	259 (0x103)	19 (0x13)	27.0
(B, D, G, H, I) PAL	864	720	853 (0x355)	133 (0x85)	310 (0x136)	22 (0x16)	27.0
(M) PAL	858	720	842 (0x34a)	122 (0x7a)	259 (0x103)	19 (0x13)	27.0
(N) PAL	864	720	853 (0x355)	133 (0x85)	309 (0x135)	21 (0x15)	27.0
(NC) PAL	864	720	853 (0x355)	133 (0x85)	310 (0x136)	22 (0x16)	27.0
SQUARE PIXELS							
(M) NTSC	780	640	758 (0x2f6)	118 (0x76)	259 (0x103)	19 (0x13)	24.54
(B, D, G, H, I) PAL	944	768	923 (0x39b)	155 (0x9b)	310 (0x136)	22 (0x16)	29.5
(M) PAL	780	640	758 (0x2f6)	118 (0x76)	259 (0x103)	19 (0x13)	24.54
(N) PAL	944	768	923 (0x39b)	155 (0x9b)	309 (0x135)	21 (0x15)	29.5
(NC) PAL	944	768	923 (0x39b)	155 (0x9b)	310 (0x136)	22 (0x16)	29.5

The delay from the active edge of HSYNC to the 50% point of the composite sync is 4-39 CLK2 cycles depending on the HMP8170 operating mode. The delay is shortest when the encoder is the timing master; it is longest when in slave mode.

CLK2 Input Timing

The CLK2 input clocks all of the HMP8170, including its video timing counters. For proper operation, all of the HMP8170 inputs must be synchronous with CLK2. The frequency of CLK2 depends on the device's operating mode and the total number of pixels per line. The standard clock frequencies are shown in Table 5.

Note that the color subcarrier is derived from the CLK2 input. Any jitter on CLK2 will be transferred to the color subcarrier, resulting in color changes. Just 400ps of jitter on CLK2 causes up to a 1 degree color subcarrier phase shift. Thus, CLK2 should be derived from a stable clock source, such as a crystal. The use of a PLL to generate CLK2 is not recommended.

Video Processing

Upsampling

The encoder begins the video processing with the pixel input data. It converts the 4:2:2 YCbCr data to 4:4:4 data. The conversion is done by 2x upsampling the Cb and Cr data. The CbCr upsampling function uses linear interpolation. The HMP8170 then upsamples the 4:4:4 data to generate 8:8:8 data. Again, the encoder uses linear interpolation for the upsampling.

Horizontal Filtering

Unless disabled, the HMP8170 lowpass filters the Y data to 6.0MHz. Lowpass filtering Y removes any aliasing artifacts due to the upsampling process, and simplifies the analog output filters. The Y 6.0MHz lowpass filter response is shown in Figure 7. At this point, the HMP8170 also scales the Y data to generate the proper output levels for the various video standards.

The HMP8170 lowpass filters the Cb and Cr data to 1.3MHz prior to modulation. The lowpass filtering removes any aliasing artifacts due to the upsampling process (simplifying the analog output filters) and also properly bandwidth-limits Cb and Cr prior to modulation. The chrominance filtering is not optional like luminance filtering. The Cb and Cr 1.3MHz lowpass filter response is shown in Figure 8.

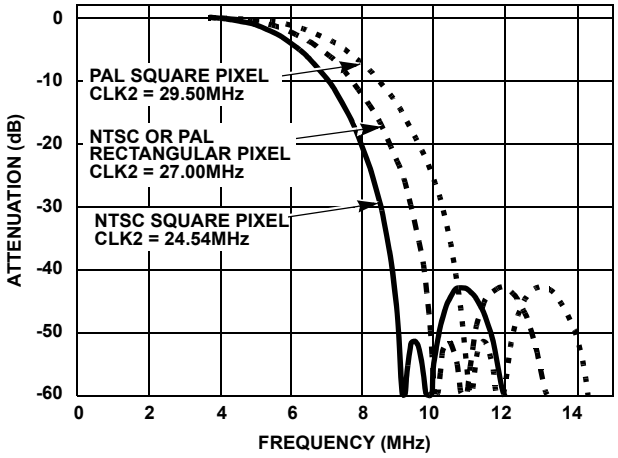


FIGURE 7A. FULL SPECTRUM

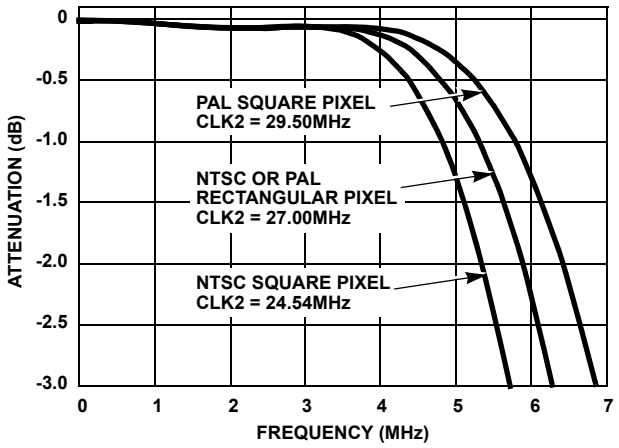


FIGURE 7B. PASS BAND

FIGURE 7. Y LOWPASS FILTER RESPONSE

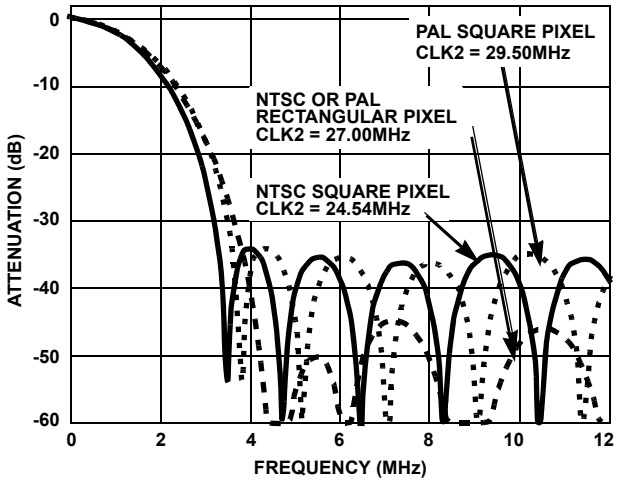


FIGURE 8A. FULL SPECTRUM

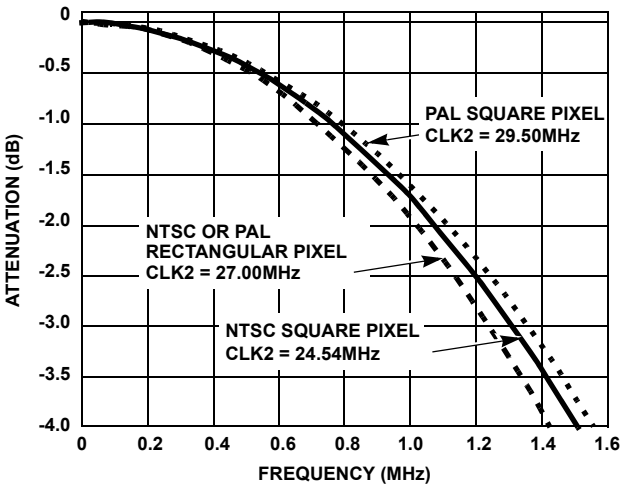


FIGURE 8B. PASS BAND

FIGURE 8. Cb AND Cr LOWPASS FILTER RESPONSE

Color Subcarrier Generation

The HMP8170 uses a numerically controlled oscillator (NCO) clocked by CLK2 and a sine look up ROM to generate the color subcarrier. As shown in Figure 9, the phase increment value (PHINC) of the NCO may come from the encoder's internal look up table, BT.656 ancillary data, or a control register. The PHINC source is selected in timing I/O register 2.

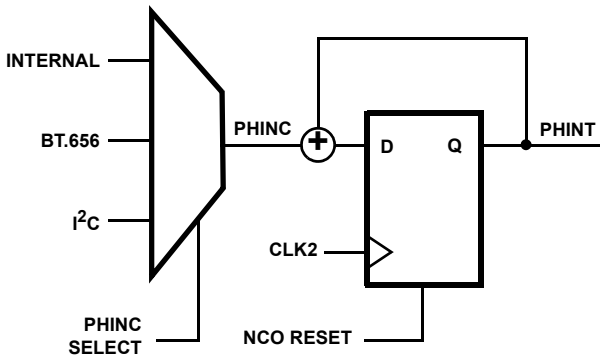


FIGURE 9. COLOR SUBCARRIER GENERATION NCO.

The MSBs of the accumulated phase value (PHINT) are used to address the encoder's sine look up ROM. The sine values from the ROM are pre-scaled to generate the proper levels for the various video standards. Prescaling outside the CbCr data path minimizes color processing artifacts. The HMP8170 modulates the filtered 8:8:8 chrominance data with the synthesized subcarrier.

The SCH phase is 0 degrees after reset but then changes monotonically over time due to residue in the NCO. In an ideal system, zero SCH phase would be maintained forever. In reality, this is impossible to achieve due to pixel clock frequency tolerances and digital rounding errors. When the PHINC source is BT.656 data, the SCH phase reset should be disabled.

If enabled, the HMP8170 resets the NCO periodically to avoid an accumulation of SCH phase error. The reset occurs at the beginning of each field to burst phase sequence. The sequence repeats every 4 fields for NTSC or 8 fields for PAL.

Resetting the SCH phase every four fields (NTSC) or eight fields (PAL) avoids the accumulation of SCH phase error at the expense of requiring any NTSC/PAL decoder after the encoder be able to handle very minor "jumps" (up to 2 degrees) in the SCH phase at the beginning of each four-field or eight-field sequence. Most NTSC/PAL decoders are able to handle this due to video editing requirements.

Composite Video Limiting

The HMP8170 adds the luminance and modulated chrominance together with the sync, color burst, and optional blanking pedestal to form the composite video data. If enabled in the video processing register, the encoder limits the active video so that it is always greater than one-eighth of full scale. This corresponds to approximately one-half the sync height. This allows the generation of "safe" video in the event non-standard YCbCr values are input to the device.

Controlled Edges

The NTSC and PAL video standards specify edge rates and rise and fall times for portions of the video waveform. The HMP8170 automatically implements controlled edge rates and rise and fall times on these edges:

1. Analog Horizontal Sync (Rising and Falling Edges)
2. Analog Vertical Sync Interval (Rising and Falling Edges)
3. Color Burst Envelope
4. Blanking of Analog Active Video
5. Closed Captioning Information
6. WSS Information
7. Teletext Information

"Sliced" VBI Data

The HMP8170 generates three types of vertical blanking interval data: closed captioning, widescreen signalling, and teletext data. The data is generated on the scan lines specified by the selected output video standard which are enabled in the VBI data control register. During scan lines with VBI data, the pixel inputs are ignored.

Closed Captioning (CC)

The HMP8170 captioning data output includes clock run-in and start bits followed by the captioning data. During closed captioning encoding, the pixel inputs are ignored on the scan lines containing captioning information.

The HMP8170 has two 16-bit registers containing the captioning information. Each 16-bit register is organized as two cascaded 8-bit registers. One 16-bit register (caption 21) is read out serially during line 18, 21 or 22; the other 16-bit register (WSS 284) is read out serially during line 281, 284 or 335. The data registers are shifted out LSB first.

The captioning output level is 50 IRE for a logic 1 and 0 IRE for a logic 0. All transitions between levels are controlled to have a raised-cosine shape. The rise or fall time of any transition is 240-288ns.

The caption data registers may be loaded via the I^2C interface or as BT.656 ancillary data. Table 6 illustrates the format of the caption data as BT.656 ancillary data. The transfer should occur only once per field before the start of the SAV sequence of the line containing the captioning output.

When written via the I^2C interface, the bytes may be written in any order but both must be written within one frame time for proper operation. If the registers are not updated, the encoder resends the previously loaded values.

The HMP8170 provides a write status bit for each captioning line. The encoder clears the write status bit to '0' when captioning is enabled and both bytes of the captioning data register have been written. The encoder sets the write status bit to '1' after it outputs the data, indicating the registers are ready to receive new data.

Captioning information may be enabled for either line, both lines, or no lines. The captioning modes are summarized in Table 7.

TABLE 6. BT.656 ANCILLARY DATA FORMAT FOR CLOSED CAPTIONING DATA

PIXEL INPUT	P15	P14	P13	P12	P11	P10	P9	P8
Preamble 1	0	0	0	0	0	0	0	0
Preamble 2	1	1	1	1	1	1	1	1
Preamble 3	1	1	1	1	1	1	1	1
Data ID	ep#	ep	1	1	0	0	0	Line
Data Block Number	ep#	ep	0	0	0	0	0	1
Data Word Count	ep#	ep	0	0	0	0	0	1
Caption Register Byte 3	ep#	ep	0	0	bit 15	bit 14	bit 13	bit 12
Caption Register Byte 1	ep#	ep	0	0	bit 11	bit 10	bit 9	bit 8
Caption Register Byte 1	ep#	ep	0	0	bit 7	bit 6	bit 5	bit 4
Caption Register Byte 0	ep#	ep	0	0	bit 3	bit 2	bit 1	bit 0
CRC	P14#	X	X	X	X	X	X	X

NOTES:
The even parity (EP and EP#) bits are ignored.
Line = Data Register Select: 0 = Line 21; 1 = 284.
X = Don't Care.

TABLE 7. CLOSED CAPTIONING MODES

CLOSED CAPTIONING ENABLE BITS	OUTPUT LINE(S)	CAPTIONING REGISTER		WRITE STATUS BIT	
		284A 284B	21A 21B	284	21
00	None	Ignored	Ignored	Always 1	Always 1
01	21 (NTSC) 18 (M PAL) 22 (Other PAL)	Ignored	Caption Data	Always 1	0 = Loaded 1 = Output
10	284 (NTSC) 281 (M PAL) 335 (Other PAL)	Caption Data	Ignored	0 = Loaded 1 = Output	Always 1
11	21, 284 (NTSC) 18, 281 (M PAL) 22, 335 (Other PAL)	Caption Data	Caption Data	0 = Loaded 1 = Output	0 = Loaded 1 = Output

Widescreen Signalling (WSS)

The HMP8170 WSS data output includes clock run-in and start codes followed by the WSS data. For NTSC operation, the WSS data is followed by six bits of CRC data.

The HMP8170 has two 14-bit registers containing the WSS information and two 6-bit registers containing the WSS CRC data. Each 14-bit register is organized as a 6-bit register cascaded with an 8-bit one. One 14-bit register (WSS 20) is read out serially during line 17, 20 or 23; the other 14-bit register (caption 283) is read out serially during line 280, 283 or 336. The data registers are shifted out LSB first.

The WSS output level depends on the video format. For NTSC operation (EIAJ CPX-1204), the WSS output level is 70 IRE for a logic 1 and 0 IRE for a logic 0. All transitions between levels are controlled to have a raised-cosine shape with a rise or fall time of 240ns. For PAL operation (ITU-R BT.1119), the WSS output level is 71.5 IRE for a logic 1 and 0 IRE for a logic 0. All transitions between levels are controlled to have a raised-cosine shape with a rise or fall time of 118ns.

The WSS data registers may be loaded via the I^2C interface or as BT.656 ancillary data. Table 8 illustrates the format of the WSS data as BT.656 ancillary data. The transfer should occur only once per field before the start of the SAV sequence of the line containing the WSS output.

When written via the I^2C interface, the bytes may be written in any order but all three bytes of each enabled line must be written within one frame time for proper operation. If the registers are not updated, the encoder resends the previously loaded values.

The HMP8170 provides a write status bit for each WSS line. The encoder clears the write status bit to '0' when WSS is enabled and all bytes of the WSS data register have been written. The encoder sets the write status bit to '1' after it outputs the data, indicating the registers are ready to receive new data.

WSS information may be enabled for either line, both lines, or no lines. The WSS modes are summarized in Table 9.

TABLE 8. BT.656 ANCILLARY DATA FORMAT FOR WIDESCREEN SIGNALLING DATA

PIXEL INPUT	P15	P14	P13	P12	P11	P10	P9	P8
Preamble 1	0	0	0	0	0	0	0	0
Preamble 2	1	1	1	1	1	1	1	1
Preamble 3	1	1	1	1	1	1	1	1
Data ID	ep#	ep	1	1	0	0	1	Line
Data Block Number	ep#	ep	0	0	0	0	0	1
Data Word Count	ep#	ep	0	0	0	0	1	0
WSS Data Nibble 3	ep#	ep	0	0	0	0	bit 13	bit 12
WSS Data Nibble 2	ep#	ep	0	0	bit 11	bit 10	bit 9	bit 8
WSS Data Nibble 1	ep#	ep	0	0	bit 7	bit 6	bit 5	bit 4
WSS Data Nibble 0	ep#	ep	0	0	bit 3	bit 2	bit 1	bit 0
WSS CRC Nibble 1	ep#	ep	0	0	0	0	bit 5	bit 4
WSS CRC Nibble 0	ep#	ep	0	0	bit 3	bit 2	bit 1	bit 0
Reserved	ep#	ep	0	0	0	0	0	0
Reserved	ep#	ep	0	0	0	0	0	0
CRC	P14#	X	X	X	X	X	X	X

NOTES:
The even parity (EP and EP#) bits are ignored.
Line = Data Register Select: 0 = Line 20; 1 = 283.
The WSS CRC data bits are ignored during PAL operation but must be included in the transfer.
X = Don't Care.

TABLE 9. WIDESCREEN SIGNALLING MODES

WSS ENABLE BITS	OUTPUT LINE(S)	WSS REGISTERS		WRITE STATUS BIT	
		283A, 283B, CRC283	20A, 20B, CRC20	283	20
00	None	Ignored	Ignored	Always 1	Always 1
01	20 (NTSC) 17 (M PAL) 23 (Other PAL)	Ignored	WSS Data	Always 1	0 = Loaded 1 = Output
10	283 (NTSC) 280 (M PAL) 336 (Other PAL)	WSS Data	Ignored	0 = Loaded 1 = Output	Always 1
11	20, 283 (NTSC) 17, 280 (M PAL) 23, 336 (Other PAL)	WSS Data	WSS Data	0 = Loaded 1 = Output	0 = Loaded 1 = Output

NOTE: The CRC registers are always ignored during PAL operation.

Teletext

The HMP8170 supports ITU-R BT.653 625-line and 525-line teletext system B and C generation. WST (World System Teletext) is the same as BT.653 system B. NABTS (North American Broadcast Teletext Specification) is the same as BT.653 525-line system C. NABTS is also used to transmit Intel Intercast information.

During the teletext encoding, the line's pixel inputs are ignored. The teletext information includes a 16-bit clock synchronization code; the HMP8170 automatically generates it.

The teletext output level depends on the video format. For system B teletext, the output level is 66 IRE for a logic 1 and 0 IRE for a logic 0. All transitions between levels are controlled to have a raised-cosine shape with a rise or fall time of 200ns. For system C teletext, the output level is 70 IRE for a logic 1 and 0 IRE for a logic 0. All transitions between levels are controlled to have a raised-cosine shape with a rise or fall time of 200ns.

The HMP8170 generates teletext output on any scan line that includes teletext data in that line's BT.656 ancillary data. The encoder must receive the ancillary data before the SAV sequence in order to output the teletext data. Table 10 shows the BT.656 ancillary data format for loading the teletext data registers.

TABLE 10. BT.656 ANCILLARY DATA FORMAT FOR TELETEXT DATA

PIXEL INPUT	P15	P14	P13	P12	P11	P10	P9	P8
Preamble 1	0	0	0	0	0	0	0	0
Preamble 2	1	1	1	1	1	1	1	1
Preamble 3	1	1	1	1	1	1	1	1
Data ID	ep#	ep	1	1	0	1	0	0
Data Block Number	ep#	ep	0	0	0	0	0	1
Data Word Count	ep#	ep	0	1	0	1	1	0
Teletext Register Data (86 Nibbles)	ep#	ep	Line	Sys	bit 343	bit 342	bit 341	bit 340
	ep#	ep	0	0	bit 339	bit 338	bit 337	bit 336
	. . .							
	ep#	ep	0	0	bit 7	bit 6	bit 5	bit 4
	ep#	ep	0	0	bit 3	bit 2	bit 1	bit 0
Reserved	ep#	ep	0	0	0	0	0	0
Reserved	ep#	ep	0	0	0	0	0	0
CRC	P14#	X	X	X	X	X	X	X

NOTES:
The even parity (EP and EP#) bits are ignored.
Line = Standard Select: 0 = 525 Lines; 1 = 625 Lines
Sys = System Select: 0 = System B; 1 = System C.
625-line system B uses 43 bytes; all bits are used.
525-line system B uses 35 bytes; bits 343-280 are ignored.
525-line system C uses 34 bytes; bits 343-272 are ignored.
X = Don't Care.

TABLE 11. BT.656 ANCILLARY DATA FORMAT FOR PHINC DATA

PIXEL INPUT	P15	P14	P13	P12	P11	P10	P9	P8
Preamble 1	0	0	0	0	0	0	0	0
Preamble 2	1	1	1	1	1	1	1	1
Preamble 3	1	1	1	1	1	1	1	1
Data ID	ep#	ep	1	1	0	1	0	1
Data Block Number	ep#	ep	0	0	0	0	0	1
Data Word Count	ep#	ep	0	0	0	0	1	1
HPLL Increment (4 Nibbles)	ep#	ep	0	0	bit 15	bit 14	bit 13	bit 12
	ep#	ep	0	0	bit 11	bit 10	bit 9	bit 8
	ep#	ep	0	0	bit 7	bit 6	bit 5	bit 4
	ep#	ep	0	0	bit 3	bit 2	bit 1	bit 0
FSCPLL Increment (8 Nibbles)	ep#	ep	PSW	0	bit 31	bit 30	bit 29	bit 28
	ep#	ep	F2	F1	bit 27	bit 26	bit 25	bit 24
	. . .							
	ep#	ep	0	0	bit 7	bit 6	bit 5	bit 4
	ep#	ep	0	0	bit 3	bit 2	bit 1	bit 0
CRC	P14#	X	X	X	X	X	X	X

NOTES:
The even parity (EP and EP#) bits are ignored.
HPLL, PSW, F2, and F1 are ignored.
X = Don't Care.

Analog Outputs

The HMP8170 converts the video data into analog signals using four 10-bit DACs running at the CLK2 rate. The DACs output a current proportional to the digital data. The full scale output current is determined by the reference voltage VREF and an external resistor RSET. The full scale output current is given by:

$I_{FULLSCALE}$ (mA) = 3.9 * VREF (V)/RSET (kΩ) (EQ 1.)

VREF must be chosen such that it is within the part's operating range; RSET must be chosen such that the maximum output current is not exceeded.

If the VREF pin is not connected, the HMP8170 uses the internal reference voltage. Otherwise, the applied voltage overdrives the internal reference. If an external reference is used, it must decoupled from any power supply noise. An example external reference circuit is shown in the Applications section.

The HMP8170 generates $1V_{P-P}$ nominal video signals across 37.5Ω loads, corresponding to doubly terminated 75Ω lines. The encoder may also drive larger loads. The full scale output current and load must be chosen such that the maximum output voltage is not exceeded.

Output DAC Filtering

Since the DACs run at 2x the pixel sample rate, the sin(x)/x rolloff of the outputs is greatly reduced, and there are fewer high frequency artifacts in the output spectrum. This allows using simple analog output filters. The analog output filter should be flat to $F_S/4$ and have good rejection at $3F_S/4$. Example filters are shown in the Applications section.

Composite + Y/C Output Mode

The HMP8170 provides composite with S-video output mode. When S-video outputs are selected, the encoder outputs the luminance, modulated chrominance, and two copies of the composite video signals. All four outputs are time aligned. The output pin assignments are summarized in Table 12.

Composite + RGB Output Mode

When analog RGB video is selected, the HMP8170 transforms the filtered 8:8:8 YCbCr data into 8:8:8 RGB data. The transform matrix uses different coefficients to generate NTSC or PAL video levels.

The analog RGB outputs have a range of 0.3-1.0V with an optional blanking pedestal. Composite sync information (0.0-0.3V) may be optionally added to the green output. VBI data is not included on the RGB outputs. The HMP8170 also generates composite video when in RGB output mode. All four outputs are time aligned.

The HMP8170 provides selectable pin outs for the RGB outputs. When the SCART compatibility bit is cleared, the analog composite video is output onto the NTSC/PAL 1 pin. Red information is output onto the NTSC/PAL 2 pin, blue information is output onto the C pin, and green information is output onto the Y pin.

When the bit is set, the analog composite video is output onto the Y pin. Red information is output onto the C pin, blue video is output on the NTSC/PAL 2 pin, and the green signal is output on the NTSC/PAL 1 pin. The output pin assignments are summarized in Table 12.

TABLE 12. OUTPUT PIN ASSIGNMENTS

PIN NAME	PIN #	OUTPUT MODE (SCART SELECT BIT)			
		COMP. WITH Y/C (X)	COMP. W/ RGB (0)	COMP. W/ RGB (1)	COMP. W/ YUV (X)
Y	3	Luma	Green	Composite	Composite
C	7	Chroma	Blue	Red	V
NTSC/PAL 1	11	Composite	Composite	Green	Y
NTSC/PAL 2	15	Composite	Red	Blue	U

Composite + YUV Output Mode

When analog YUV video is selected, the HMP8170 scales the filtered YCbCr data to match the levels required by its DACs. During the scaling, values less than 16 are clamped to 16. The scaling factors for Cb and Cr are the same, but the CbCr scaling factor is different from the Y scaling factor. The encoder uses different sets of scale factors for NTSC and PAL to accommodate their different black levels.

The analog YUV outputs have a range of 0.3-1.0V with an optional blanking pedestal. Composite sync information (0.0-0.3V) may be optionally added to the Y output. VBI data is included on the Y output. The HMP8170 also generates composite video when in YUV output mode. All four outputs are time aligned. The output pin assignments are summarized in Table 12.

Power Down Modes

To reduce power dissipation, any of the four output DACs may be turned off. Each DAC has an independent enable bit. Each output may be disabled in the host control register.

When the power down mode is enabled, all of the DACs and internal voltage reference are powered down (forcing their outputs to zero) and the data pipeline registers are disabled. The host processor may still read from and write to the internal control registers.

Host Interfaces

Reset

The HMP8170 resets to its default operating mode on power up, when the reset pin is asserted for at least four CLK cycles, or when the software reset bit of the host control register is set. During the reset cycle, the encoder returns its internal registers to their reset state and deactivates the I^2C interface.

I^2C Interface

The HMP8170 provides a standard I^2C interface and supports fast-mode (up to 400Kbps) transfers. The device acts as a slave for receiving and transmitting data only. It will not respond to general calls or initiate a transfer. The encoder's slave address is either 0100 $000x_B$ when the SA input pin is low or 0100 $001x_B$ when it is high. (The 'x' bit in the address is the I^2C read flag.)

The I^2C interface consists of the SDA and SCL pins. When the interface is not active, SCL and SDA must be pulled high using external 4-6kΩ pull-up resistors. The I^2C clock and data timing is shown in Figures 10 and 11.

During I^2C write cycles, the first data byte after the slave address specifies the sub address, and is written into the address register. Only the seven LSBs of the subaddress are used; the MSB is ignored. Any remaining data bytes in the I^2C write cycle are written to the control registers, beginning with the register specified by the address register. The 7-bit address register is incremented after each data byte in the I^2C write cycle. Data written to reserved bits within registers or reserved registers is ignored.

During I^2C read cycles, data from the control register specified by the address register is output. The address register is incremented after each data byte in the I^2C read cycle. Reserved bits within registers return a value of "0". Reserved registers return a value of 00_H.

The HMP8170's operating modes are determined by the contents of its internal registers which are accessed via the I^2C interface. All internal registers may be written or read by the host processor at any time. However, some of the bits and words are read only or reserved and data written to these bits is ignored.

Table 13 lists the HMP8170's internal registers. Their bit descriptions are listed in Tables 14 through 45.

TABLE 13. CONTROL REGISTER NAMES

SUB ADDRESS (HEX)	CONTROL REGISTER	RESET CONDITION
00	product ID	-
01	output format	00_H
02	input format	06_H
03	video processing	80_H
04	timing I/O 1	00_H
05	timing I/O 2	00_H
06	VBI data enable	00_H
07	VBI data input	00_H
08-0D	reserved	-
0E	host control 1	$1E_H$
0F	host control 2	00_H
10	caption_21A	80_H
11	caption_21B	80_H
12	caption_284A	80_H
13	caption_284B	80_H
14	WSS_20A	00_H
15	WSS_20B	00_H
16	WSS_283A	00_H
17	WSS_283B	00_H
18	CRC_20	$3F_H$
19	CRC_283	$3F_H$
1A-1F	reserved	-
20	start h_blank low	$4A_H$
21	start h_blank high	03_H
22	end h_blank	$7A_H$
23	start v_blank low	03_H
24	start v_blank high	01_H
25	end v_blank	13_H
26	field control 1	00_H
27	field control 2	00_H
28-2F	reserved	-
30-6A	test and unused	-
6B-6F	phase increment	-
70-7F	test and unused	-

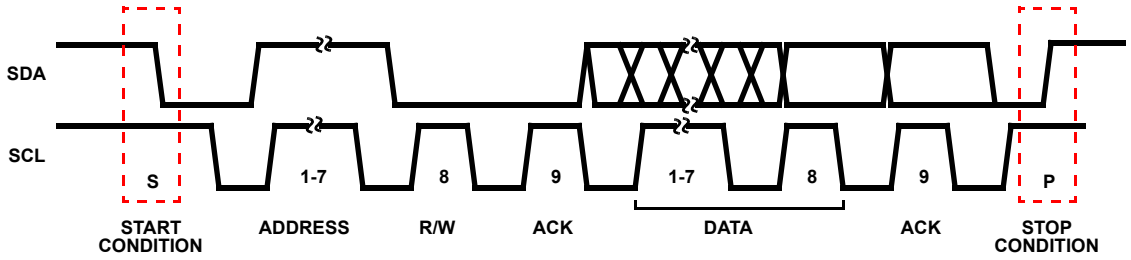


FIGURE 10. I^2C SERIAL TIMING FLOW

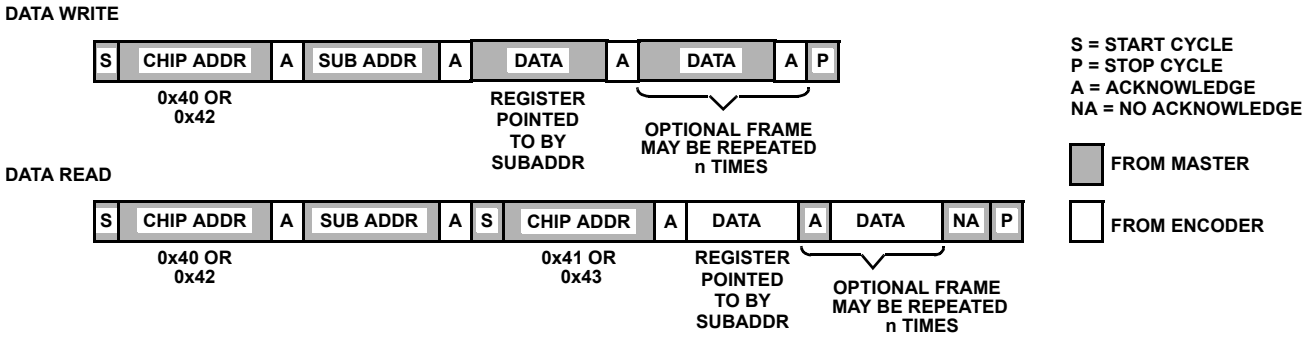


FIGURE 11. REGISTER WRITE PROGRAMMING FLOW

TABLE 14. PRODUCT ID REGISTER

SUB ADDRESS = 00_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Product ID	This 8-bit register specifies the last two digits of the product number. It is a read-only register. Data written to it is ignored.	70H 71H 72H 73H

TABLE 15. OUTPUT FORMAT REGISTER

SUB ADDRESS = 01_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-5	Video Timing Standard	000 = (M) NTSC 001 = reserved 010 = (B, D, G, H, I) PAL 011 = (M) PAL 100 = (N) PAL 101 = (NC) PAL 110 = reserved 111 = reserved	000B
4-3	Output Format	00 = Composite + Y/C	00B
2-0	NTSC / PAL Setup Select	These bits specify the blanking pedestal during active video, from 0 IRE (“000”) to 7.5 IRE (“111”). Typically, these bits should be a “111” during (M) NTSC and (M, N) PAL operation. Otherwise, they should be a “000”. These bits do not affect the analog RGB or YUV outputs.	111B

TABLE 16. INPUT FORMAT REGISTER

SUB ADDRESS = 02_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-5	Input Format	000 = 16-bit 4:2:2 YCbCr 001 = 8-bit 4:2:2 YCbCr 010 = 8-bit BT.656 011 = Reserved 100 = Reserved 101 = Reserved 110 = Reserved 111 = Reserved	000_B
4 - 0	Reserved		00000_B

TABLE 17. VIDEO PROCESSING REGISTER

SUB ADDRESS = 03_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7	Luminance Processing	0 = None 1 = Y Lowpass filtering enabled	1_B
6	Composite Video Limiting	0 = None 1 = Lower limit of composite active video is about half the sync height	0_B
5	SCH Phase Mode	0 = Never reset SCH phase 1 = Reset SCH phase every 4 (NTSC) or 8 (PAL) fields	1_B
4	RGB / YUV Setup Select	This bits specifies the blanking pedestal on the analog RGB and YUV outputs during active video. Typically, this bit should be a “1” during (M) NTSC and (M, N) PAL operation. Otherwise, it should be a “0”. This bit does not affect the analog composite or Y/C outputs. 0 = 0 IRE 1 = 7.5 IRE	0_B
3	RGB Output Pins Select	This bit configures on what pins the analog RGB video is output. 0 = HMP8156 compatible 1 = SCART compatible	0_B
2-0	Reserved		000_B

TABLE 18. TIMING I/O REGISTER #1

SUB ADDRESS = 04_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7	$\overline{\text{BLANK}}$ Timing Select	This bit is ignored unless $\overline{\text{BLANK}}$ is configured to be an output. 0 = Data for the first active pixel of the scan line must arrive the CLK cycle after the encoder negates $\overline{\text{BLANK}}$. 1 = Data for the first active pixel of the scan line must arrive immediately after the encoder negates $\overline{\text{BLANK}}$.	0_B
6	Reserved		0_B
5	$\overline{\text{BLANK}}$ Output Control	0 = $\overline{\text{BLANK}}$ is an input 1 = $\overline{\text{BLANK}}$ is an output	0_B
4	$\overline{\text{BLANK}}$ Polarity	0 = Active low (low during blanking) 1 = Active high (high during blanking)	0_B
3	$\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ Output Control	0 = $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ are inputs 1 = $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ are outputs	0_B
2	$\overline{\text{HSYNC}}$ Polarity	0 = Active low (low during horizontal sync) 1 = Active high (high during horizontal sync)	0_B
1	$\overline{\text{VSYNC}}$ Polarity	0 = Active low (low during vertical sync) 1 = Active high (high during vertical sync)	0_B
0	FIELD Polarity	0 = Active low (low during odd fields) 1 = Active high (high during odd fields)	0_B

TABLE 19. TIMING I/O REGISTER #2

SUB ADDRESS = 05_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-6	Reserved		00_B
5	CLK Polarity Control	0 = Inputs are sampled when CLK is low (see Table 2). 1 = Inputs are sampled when CLK is high.	0_B
4	CLK Output Control	0 = CLK is an input 1 = CLK is an output	0_B
3	Aspect Ratio Mode	This bit must be set to “0” during BT.656 input mode. 0 = Rectangular (BT.601) pixels 1 = Square pixels	0_B
2	Reserved		0_B
1-0	Subcarrier PHINC Select	Selects the source of the color subcarrier NCO phase increment value. 00 = Internal (fixed) data. 01 = Reserved 10 = BT.656 RTCI ancillary data 11 = I^2C interface PHINC register	00_B

TABLE 20. AUXILIARY DATA ENABLE REGISTER

SUB ADDRESS = 06_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-6	Closed Captioning Enable	00 = Closed caption disabled 01 = Closed caption enabled for odd fields: line 21 for NTSC, line 18 for (M) PAL, or line 22 for (B, D, G, H, I, N, NC) PAL 10 = Closed caption enabled for even fields: line 284 for NTSC, line 281 for (M) PAL, or line 335 for (B, D, G, H, I, N, NC) PAL 11 = Closed caption enabled for both odd and even fields	00_B
5-4	WSS Enable	00 = WSS disabled 01 = WSS enabled for odd fields: line 20 for NTSC; line 17 for (M) PAL, or line 23 for (B, D, G, H, I, N, NC) PAL 10 = WSS enabled for even fields: line 283 for NTSC, line 280 for (M) PAL, or line 336 for (B, D, G, H, I, N, NC) PAL 11 = WSS enabled for both odd and even fields	00_B
3	Teletext Enable	00 = Teletext disabled 01 = System B teletext enabled 10 = System C teletext enabled 11 = reserved	00_B
1-0	Reserved		00_B

TABLE 21. VBI DATA INPUT REGISTER

SUB ADDRESS = 07_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7	Closed Caption Line 21 BT.656 Enable	Setting this bit enables BT.656 ancillary data to be written into the closed caption line 21 data registers. It is ignored unless in the BT.656 input mode. 0 = Ignore BT.656 ancillary data 1 = Use BT.656 ancillary data	0_B
6	Closed Caption Line 284 BT.656 Enable	Setting this bit enables BT.656 ancillary data to be written into the closed caption line 284 data registers. It is ignored unless in the BT.656 input mode. 0 = Ignore BT.656 ancillary data 1 = Use BT.656 ancillary data	0_B
5	WSS Line 20 BT.656 Enable	Setting this bit enables BT.656 ancillary data to be written into the WSS line 20 data registers. It is ignored unless in the BT.656 input mode. 0 = Ignore BT.656 ancillary data 1 = Use BT.656 ancillary data	0_B
4	WSS Line 283 BT.656 Enable	Setting this bit enables BT.656 ancillary data to be written into the WSS line 283 data registers. It is ignored unless in the BT.656 input mode. 0 = Ignore BT.656 ancillary data 1 = Use BT.656 ancillary data	0_B
3-0	Reserved		0000_B

TABLE 22. HOST CONTROL REGISTER 1

SUB ADDRESS = $0E_H$			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-5	Reserved		000_B
4	Closed Caption Line 21 Write Status	0 = Caption_21A and Caption_21B data registers contain unused data 1 = Data has been output, host processor may now write to the registers	1_B
3	Closed Caption Line 284 Write Status	0 = Caption_284A and Caption_284B data registers contain unused data 1 = Data has been output, host processor may now write to the registers	1_B
2	WSS Line 20 Write Status	0 = WSS_20A, WSS_20B, CRC_20A, and CRC_20B data registers contain unused data 1 = Data has been output, host processor may now write to the registers	1_B
1	WSS Line 283 Write Status	0 = WSS_283A and WSS_283B data registers contain unused data 1 = Data has been output, host processor may now write to the registers	1_B
0	Reserved		0_B

TABLE 23. HOST CONTROL REGISTER 2

SUB ADDRESS = $0F_H$			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7	Software Reset	Setting this bit to “1” initiates a software reset. It is automatically reset to a “0” after the reset sequence is complete.	0_B
6	General Power Down	This bit powers down all DAC outputs and most of the digital circuitry. 0 = Normal operation 1 = Power down mode	0_B
5	Power Down NTSC/PAL 1 Output DAC	This bit powers down only the NTSC/PAL 1 DAC output. 0 = Normal operation 1 = Power down mode	0_B
4	Power Down NTSC/PAL 2 Output DAC	This bit powers down only the NTSC/PAL 2 DAC output. 0 = Normal operation 1 = Power down mode	0_B
3	Power Down Y Output DAC	This bit powers down only the Y DAC output. 0 = Normal operation 1 = Power down mode	0_B
2	Power Down C Output DAC	This bit powers down only the C DAC output. 0 = Normal operation 1 = Power down mode	0_B
1-0	Reserved		00_B

TABLE 24. CLOSED CAPTION_21A DATA REGISTER

SUB ADDRESS = 10_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Line 21 Caption LSB Data	This register is cascaded with the closed caption_21B data register and they are read out serially as 16 bits during line 18, 21, or 22 if line 21 captioning is enabled. Bit D0 of the 21A data register is shifted out first.	80_H

TABLE 25. CLOSED CAPTION_21B DATA REGISTER

SUB ADDRESS = 11_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Line 21 Caption MSB Data	This register is cascaded with the closed caption_21A data register and they are read out serially as 16 bits during line 18, 21, or 22 if line 21 captioning is enabled. Bit D0 of the 21A data register is shifted out first.	80_H

TABLE 26. CLOSED CAPTION_284A DATA REGISTER

SUB ADDRESS = 12_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Line 284 Caption LSB Data	This register is cascaded with the closed caption_284B data register and they are read out serially as 16 bits during line 281, 284, or 335 if line 284 captioning is enabled. Bit D0 of the 284A data register is shifted out first.	80_H

TABLE 27. CLOSED CAPTION_284B DATA REGISTER

SUB ADDRESS = 13_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Line 284 Caption MSB Data	This register is cascaded with the closed caption_284A data register and they are read out serially as 16 bits during line 281, 284, or 335 if line 284 captioning is enabled. Bit D0 of the 284A data register is shifted out first.	80_H

TABLE 28. WSS_20A DATA REGISTER

SUB ADDRESS = 14_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Line 20 WSS LSB Data	This register is cascaded with the WSS_20B data register and they are read out serially as 14 bits during line 17, 20, or 23 if WSS is enabled. Bit D0 of the WSS_20A data register is shifted out first.	00_H

TABLE 29. WSS_20B DATA REGISTER

SUB ADDRESS = 15_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7 - 6	Reserved		00_B
5 - 0	Line 20 WSS MSB Data	This register is cascaded with the WSS_20A data register and they are read out serially as 14 bits during line 17, 20, or 23 if WSS is enabled. Bit D0 of the WSS_20A data register is shifted out first.	000000_B

TABLE 30. WSS_283A DATA REGISTER

SUB ADDRESS = 16_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Line 283 WSS LSB Data	This register is cascaded with the WSS_283B data register and they are read out serially as 14 bits during line 280, 283, or 336 if WSS is enabled. Bit D0 of the WSS_283A data register is shifted out first.	00_H

TABLE 31. WSS_283B DATA REGISTER

SUB ADDRESS = 17_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7 - 6	Reserved		00_B
5 - 0	Line 283 WSS MSB Data	This register is cascaded with the WSS_283A data register and they are read out serially as 14 bits during line 280, 283, or 336 if WSS is enabled. Bit D0 of the WSS_283A data register is shifted out first.	000000_B

TABLE 32. CRC_20 REGISTER

SUB ADDRESS = 18_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-6	Reserved		00_B
5-0	Line 20 WSS CRC Data	This register is read out serially after the 14 bits of NTSC WSS data, if WSS is enabled. It is ignored during PAL WSS operation. Bit D0 is shifted out first.	111111_B

TABLE 33. CRC_283 REGISTER

SUB ADDRESS = 19_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-6	Reserved		00_B
5-0	Line 283 WSS CRC Data	This register is read out serially after the 14 bits of NTSC WSS data, if WSS is enabled. It is ignored during PAL WSS operation. Bit D0 is shifted out first.	111111_B

TABLE 34. START H_BLANK LOW REGISTER

SUB ADDRESS = 20_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	LSB Assert $\overline{BLANK}$ Output Signal (Horizontal)	This 8-bit register is cascaded with Start H_Blank High Register to form a 10-bit start_horizontal_blank register. It specifies the horizontal count (in 1x clock cycles) at which to start ignoring pixel data each scan line. The leading edge of $\overline{HSYNC}$ is count 020_H. This register is ignored unless $\overline{BLANK}$ is configured as an output.	$4A_H$

TABLE 35. START H_BLANK HIGH REGISTER

SUB ADDRESS = 21_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-2	Reserved		000000_B
1-0	MSB Assert $\overline{BLANK}$ Output Signal (Horizontal)	This 2-bit register is cascaded with Start H_Blank Low Register to form a 10-bit start_horizontal_blank register. It specifies the horizontal count (in 1x clock cycles) at which to start ignoring pixel data each scan line. The leading edge of $\overline{HSYNC}$ is count 020_H. This register is ignored unless $\overline{BLANK}$ is configured as an output.	11_B

TABLE 36. END H_BLANK REGISTER

SUB ADDRESS = 22_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Negate $\overline{BLANK}$ Output Signal (Horizontal)	This 8-bit register specifies the horizontal count (in 1x clock cycles) at which to start inputting pixel data each scan line. The leading edge of $\overline{HSYNC}$ is count 000_H. This register is ignored unless $\overline{BLANK}$ is configured as an output.	$7A_H$

TABLE 37. START V_BLANK LOW REGISTER

SUB ADDRESS = 23_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	LSB Assert $\overline{BLANK}$ Output Signal (Vertical)	This 8-bit register is cascaded with Start V_Blank High Register to form a 9-bit start_vertical_blank register. During normal operation, it specifies the line number (n) to start ignoring pixel input data (and what line number to start blanking the output video) each odd field; for even fields, it occurs on line (n + 262) or (n + 313). The leading edge of $\overline{VSYNC}$ at the start of an odd field is count 000_H (note that this does not follow standard NTSC or PAL line numbering). This register is ignored unless $\overline{BLANK}$ is configured as an output.	03_H

TABLE 38. START V_BLANK HIGH REGISTER

SUB ADDRESS = 24_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-1	Reserved		0000000_B
0	MSB Assert $\overline{BLANK}$ Output Signal (Vertical)	This 1-bit register is cascaded with Start V_Blank Low Register to form a 9-bit start_vertical_blank register. This register is ignored unless $\overline{BLANK}$ is configured as an output.	1_B

TABLE 39. END V_BLANK REGISTER

SUB ADDRESS = 25_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Negate $\overline{BLANK}$ Output Signal (Vertical)	During normal operation, this 8-bit register specifies the line number (n) to start inputting pixel input data (and what line number to start generating active output video) each odd field; for even fields, it occurs on line (n + 262) or (n + 313). The leading edge of $\overline{VSYNC}$ at the start of an odd field is count 000_H (note that this does not follow standard NTSC or PAL line numbering). This register is ignored unless $\overline{BLANK}$ is configured as an output.	13_H

TABLE 40. FIELD CONTROL REGISTER 1

SUB ADDRESS = 26_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Field Detect Window Size Low	This 8-bit register is cascaded with Field Detect Window Size High to form a 9-bit Field Detect Window Size value. The value specifies the number of 1x clock cycles in the detection window before and after the selected edge of $\overline{VSYNC}$. It may range from 0 to 511. If the leading edge of $\overline{HSYNC}$ occurs within the window, it is the start of an odd or even field, as specified by the FIELD Detect Select bit. This register is ignored unless $\overline{HSYNC}$ and $\overline{VSYNC}$ are configured as inputs.	80_H

TABLE 41. FIELD CONTROL REGISTER 2

SUB ADDRESS = 27_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-4	Half Line Count Reset Value	These bits specify the value to load to the vertical half line counter when the selected edge of $\overline{VSYNC}$. The value is ignored when $\overline{HSYNC}$ and $\overline{VSYNC}$ are configured as outputs.	00000_B
2	$\overline{VSYNC}$ Edge Select	This bit specifies whether the encoder uses the leading or trailing edge of $\overline{VSYNC}$ to determine the field and to reset the half line counter. It is ignored unless $\overline{HSYNC}$ and $\overline{VSYNC}$ are configured as inputs. 0 = leading edge 1 = trailing edge	0_B
1	FIELD Detect Select	This bit specifies whether an odd or even field is starting when the leading edge of $\overline{HSYNC}$ occurs within the FIELD Detect Window. It is ignored unless $\overline{HSYNC}$ and $\overline{VSYNC}$ are configured as inputs. 0 = odd field 1 = even field	0_B
0	Field Detect Window Size High	This bit is cascaded with Field Detect Window Size Low to form a 9-bit Field Detect Window Size value. This bit is ignored unless $\overline{HSYNC}$ and $\overline{VSYNC}$ are configured as inputs.	0_B

TABLE 42. PHASE INCREMENT REGISTER 0

SUB ADDRESS = $6B_H$			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	PHINC 0 (LSB)	The 8-bit registers PHINC 0–3 are cascaded together to form a 32-bit PHINC value. The PHINC value is the phase increment value of the color subcarrier generation NCO. When the BT.656 ancillary data is selected as the PHINC source, the PHINC registers may be read to determine the last PHINC value loaded via the selected interface.	00_H

TABLE 43. PHASE INCREMENT REGISTER 1

SUB ADDRESS = $6C_H$			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	PHINC 1	The 8-bit registers PHINC 0–3 are cascaded together to form a 32-bit PHINC value. The PHINC value is the phase increment value of the color subcarrier generation NCO. When the BT.656 ancillary data is selected as the PHINC source, the PHINC registers may be read to determine the last PHINC value loaded via the selected interface.	00_H

TABLE 44. PHASE INCREMENT REGISTER 2

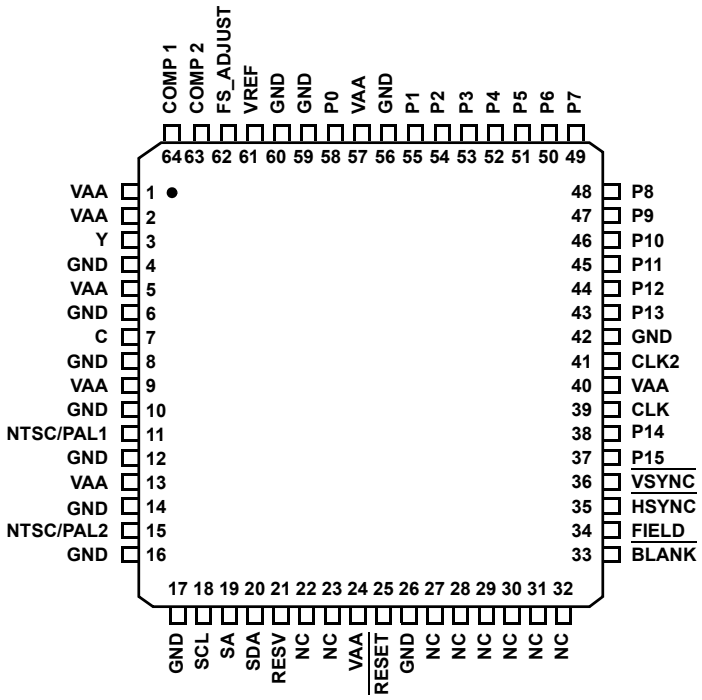
SUB ADDRESS = $6D_H$			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	PHINC 2	The 8-bit registers PHINC 0–3 are cascaded together to form a 32-bit PHINC value. The PHINC value is the phase increment value of the color subcarrier generation NCO. When the BT.656 ancillary data is selected as the PHINC source, the PHINC registers may be read to determine the last PHINC value loaded via the selected interface.	00_H

TABLE 45. PHASE INCREMENT REGISTER 1

SUB ADDRESS = $6E_H$			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	PHINC 3 (MSB)	The 8-bit registers PHINC 0–3 are cascaded together to form a 32-bit PHINC value. The PHINC value is the phase increment value of the color subcarrier generation NCO. When the BT.656 ancillary data is selected as the PHINC source, the PHINC registers may be read to determine the last PHINC value loaded via the selected interface.	00_H

Pinout

HMP8170
(PQFP)
TOP VIEW



Pin Descriptions

PIN NAME	PIN NUMBER	INPUT/ OUTPUT	DESCRIPTION
P0-P15	58, 55-43, 38, 37	I	Pixel input pins. See Table 1. Any pixel inputs not used should be connected to GND.
NC	32-27, 23, 22	I	No connect pins. These pins are not used. They may be left floating or may be connected to GND.
RESV	21	I	This pin is reserved and should be connected to GND.
FIELD	34	O	FIELD output. The field output indicates that the encoder is outputting the odd or even video field. The polarity of FIELD is programmable.
$\overline{\text{HSYNC}}$	35	I/O	Horizontal sync input/output. As an input, this pin must be asserted during the horizontal sync intervals. If it occurs early, the line time will be shortened. If it occurs late, the line time will be lengthened by holding the outputs at the front porch level. As an output, it is asserted during the horizontal sync intervals. The polarity of $\overline{\text{HSYNC}}$ is programmable. If not driven, the circuit for this pin should include a 4-12kΩ pull up resistor connected to VAA.
$\overline{\text{VSYNC}}$	36	I/O	Vertical sync input/output. As an input, this pin must be asserted during the vertical sync intervals. If it occurs early, the field time will be shortened. If it occurs late, the field time will be lengthened by holding the outputs at the blanking level. As an output, it is asserted during the vertical sync intervals. The polarity of $\overline{\text{VSYNC}}$ is programmable. If not driven, the circuit for this pin should include a 4-12kΩ pull up resistor connected to VAA.
$\overline{\text{BLANK}}$	33	I/O	Composite blanking input/output. As an input, this pin must be asserted during the horizontal and vertical blanking intervals. As an output, it is asserted during the horizontal and vertical blanking intervals. The polarity of $\overline{\text{BLANK}}$ is programmable. If not driven, the circuit for this pin should include a 4-12kΩ pull up resistor connected to VAA.

Pin Descriptions (Continued)

PIN NAME	PIN NUMBER	INPUT/ OUTPUT	DESCRIPTION
CLK	39	I/O	1x pixel clock input/output. As an input, this clock must be free-running and synchronous to the clock signal on the CLK2 pin. As an output, this pin may drive a maximum of one LS TTL load. CLK is generated by dividing CLK2 by two or four, depending on the mode. If not driven, the circuit for this pin should include a 4-12kΩ pull up resistor connected to VAA.
CLK2	41	I	2x pixel clock input. This clock must be a continuous, free-running clock.
SCL	18	I	I^2C interface clock input. The circuit for this pin should include a 4-6kΩ pull-up resistor connected to VAA.
SA	19	I	I^2C interface address select input.
SDA	20	I/O	I^2C interface data input/output. The circuit for this pin should include a 4-6kΩ pull-up resistor connected to VAA.
$\overline{\text{RESET}}$	25	I	Reset control input. A logical zero for a minimum of four CLK cycles resets the device. $\overline{\text{RESET}}$ must be a logical one for normal operation.
Y	3	O	Luminance analog current output. This output contains luminance video, sync, blanking, and information. In analog YUV or RGB output mode, an alternate signal is generated (see Table 12). It is capable of driving a 37.5Ω load. If not used, it should be connected to GND.
C	7	O	Chrominance analog current output. This output contains chrominance video, and blanking information. In analog YUV or RGB output mode, an alternate signal is generated (see Table 12). It is capable of driving a 37.5Ω load. If not used, it should be connected to GND.
NTSC/PAL 1	11	O	Composite video analog current output. This output contains composite video, sync, blanking, and information. In analog YUV or RGB output mode, an alternate signal is generated (see Table 12). It is capable of driving a 37.5Ω load. If not used, it should be connected to GND.
NTSC/PAL 2	15	O	Composite video analog current output. This output contains composite video, sync, blanking, and information. In analog YUV or RGB output mode, an alternate signal is generated (see Table 12). It is capable of driving a 37.5Ω load. If not used, it should be connected to GND.
VREF	61	I/O	Voltage reference. An optional external 1.235V reference may be used to drive this pin. If left floating, the internal voltage reference is used.
FS_ADJUST	62		Full scale adjust control. A resistor (RSET) connected between this pin and GND sets the full-scale output current of each of the DACs.
COMP 1	64		Compensation pin. A 0.1µF ceramic chip capacitor should be connected between this pin and VAA, as close to the device as possible.
COMP 2	63		Compensation pin. A 0.1µF ceramic chip capacitor should be connected between this pin and VAA as close to the device as possible.
VAA			+5V power. A 0.1µF ceramic capacitor, in parallel with a 0.01µF chip capacitor, should be used between each group of VAA pins and GND. These should be as close to the device as possible.
GND			Ground

Absolute Maximum Ratings

Supply Voltage (V_{AA} to GND) 6.0V
All Signal Pins . . . . . (GND – 0.5V) to (V_{AA} + 0.5V)
ESD Classification . . . . . Class 2

Operating Conditions

Temperature Range . . . . . 0^oC to 70^oC

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} $^oC/W$
PQFP Package	56

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Vapor Phase Soldering, 1 Minute (PQFP - Lead Tips Only) . . . . . 220^oC

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation printed circuit board in free air. Dissipation rating assumes that the device is mounted with all its leads soldered to the PCB.

Electrical Specifications

V_{AA} = +5V ±5%, RSET = 133Ω, VREF Unconnected, T_A = 25^oC, Unless Otherwise Specified

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
DC PARAMETERS, DIGITAL INPUTS EXCEPT CLK2, SDA, SCL					
Input Logic Low Voltage, V_{IL}		-	-	0.8	V
Input Logic High Voltage, V_{IH}		2.0	-	-	V
Input Logic Low Current, I_{IL}	V_{IN} = 0.0V	-	-	-10	µA
Input Logic High Current, I_{IH}	V_{IN} = V_{AA}	-	-	10	µA
Input Capacitance, C_{IN}		-	8	-	pF
DC PARAMETERS, CLK2 INPUT					
Input Logic Low Voltage, V_{IL}		-	-	0.3 x V_{AA}	V
Input Logic High Voltage, V_{IH}		0.7 x V_{AA}	-	-	V
Input Logic Low Current, I_{IL}	V_{IN} = 0.0V	-	-	-10	µA
Input Logic High Current, I_{IH}	V_{IN} = V_{AA}	-	-	10	µA
Input Capacitance, C_{IN}		-	8	-	pF
DC PARAMETERS, SDA AND SCL INPUTS					
Input Logic Low Voltage, V_{IL}		-	-	0.3 x V_{AA}	V
Input Logic High Voltage, V_{IH}		0.7 x V_{AA}	-	-	V
Input Current, I_I	V_{IN} = 0.0V – V_{AA}	-	-	±10	µA
Input Capacitance, C_{IN}		-	8	-	pF
DC PARAMETERS, DIGITAL OUTPUTS, EXCEPT SDA					
Output Logic Low Voltage, V_{OL}	I_{OL} = 2mA	-	-	0.4	V
Output Logic High Voltage, V_{OH}	I_{OH} = -2mA	2.4	-	-	V
Output Capacitance, C_{OUT}		-	8	-	pF
DC PARAMETERS, SDA OUTPUT					
Output Logic Low Voltage, V_{OL}	I_{OL} = 3mA	-	-	0.4	V
Output Capacitance, C_{OUT}		-	8	-	pF
DC PARAMETERS, ANALOG OUTPUTS					
DAC Resolution		-	10	-	Bits
Integral Nonlinearity, INL		-	0.5	±2	LSB
Differential Nonlinearity, DNL		-	0.5	±1	LSB
Output Current		-	-	34.8	mA
Output Impedance	I_{OUT} = 0mA	-	2M	-	Ω
	I_{OUT} = 34mA	-	300K	-	Ω
Output Capacitance	I_{OUT} = 0mA, CLK = 13.5MHz	-	15	-	pF
Output Compliance Range		0	-	1.4	V

Electrical Specifications V_{AA} = +5V ±5%, RSET = 133Ω, VREF Unconnected, T_A = 25°C, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Video Level Error Internal Voltage Reference	(Note 4) VREF Unconnected, RSET = 133Ω	-	-	±10	%
External Voltage Reference	VREF = 1.230V (Figure 27), RSET = 140Ω	-	-	±10	%
DAC to DAC Matching		-	-	5	%
VREF Output Voltage	Pin not connected, using internal reference	1.13	1.19	1.32	V
VREF Output Current		-50	-	50	µA
VREF Input Voltage	Pin connected to external reference shown in Figure 27.	1.11	1.23	1.36	V
VREF Input Current		-500	-	500	µA
AC PARAMETERS, ANALOG OUTPUTS					
Differential Gain Error	Using analog output filter shown in Figure 28A.	-	1	-	%
Differential Phase Error		-	1	-	Degree
SNR (Weighted)		-	70	-	dB
Hue Accuracy		-	2	-	Degree
Color Saturation Accuracy		-	2	-	%
Luminance Nonlinearity		-	1	-	%
Residual Subcarrier		-	-60	-	dB
SCH Phase	SCH Phase Reset enabled	-	±1.5	-	Degree
Analog Output Skew, t_{ASK}		-	-	3	ns
Analog Output Delay, t_{AD}		-	-	12	ns
DAC-DAC Crosstalk		-	-60	-	dB
Glitch Energy	Using analog output filter shown in Figure 28A. Includes clock and data feedthrough	-	35	-	pV-s
AC PARAMETERS, DIGITAL INPUTS AND OUTPUTS EXCEPT SCL AND SDA					
Setup Time, t_S	Note 5.	8	-	-	ns
Hold Time, t_H		0	-	-	ns
CLK2 to Output Delay, t_D		3	-	15	ns
CLK2 Frequency		-	-	30.0	MHz
CLK2 High Time, $CLK2_H$		13.6	-	20.3	ns
CLK2 Low Time, $CLK2_L$		13.6	-	20.3	ns
RESET* Pulse Width Low, t_{RES}		4	-	-	CLK Cycles
AC PARAMETERS, SCL AND SDA (I^2C INTERFACE)					
All AC parameters meet the fast-mode I^2C Bus Interface specification.					
POWER SUPPLY CHARACTERISTICS					
DAC PSRR at DC	Note 6	-	64	-	dB
Power Supply Range, V_{AA}		4.75	5.0	5.25	V
Normal Supply Current, I_{AA}		-	-	260	mA
Power-Down Supply Current, I_{AA}	Note 7	-	-	750	µA
Power Dissipation		-	1100	1300	mW

NOTES:

4. Output level is dependent on the voltage on VREF, the value of RSET, and the load.
5. Test performed with C_L = 40pF, I_O = ±2mA, V_{IH} = 3.0V, V_{IL} = 0.0V. Input reference level is 2.0V for all inputs.
6. The supply voltage rejection is the relative variation of the full-scale output driving a 37.5Ω load for a ±5% supply variation: PSRR = 20 x log ($\Delta V_{AA}/\Delta V_{OUT}$).
7. If using an external voltage reference, it is not powered down. The internal voltage reference is powered down.

Typical Performance Curves

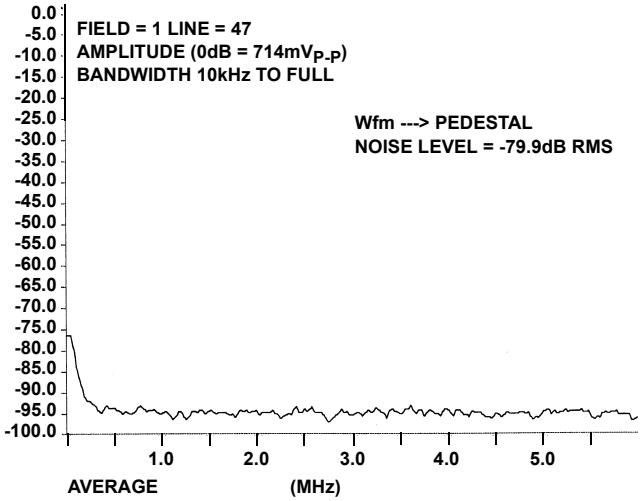


FIGURE 12. NOISE SPECTRUM (NTSC)

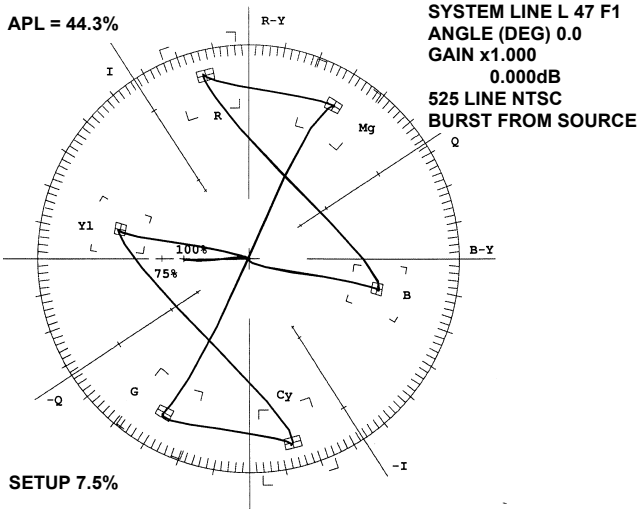


FIGURE 13. NTSC COLOR BAR VECTOR SCOPE PLOT

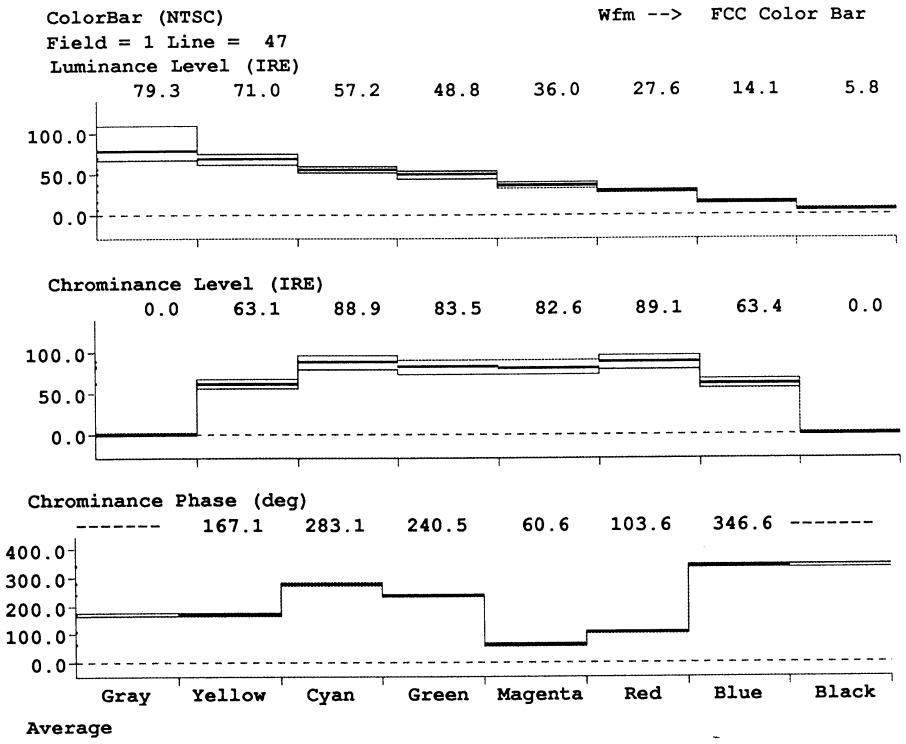


FIGURE 14. NTSC FCC COLOR BAR

Typical Performance Curves (Continued)

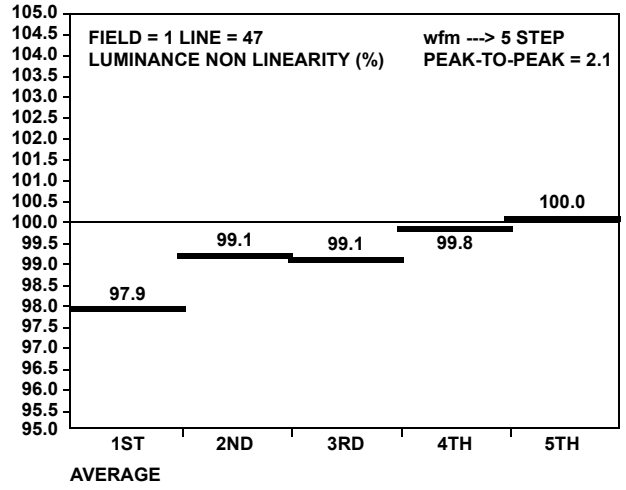


FIGURE 15. LUMINANCE NON LINEARITY (NTSC)

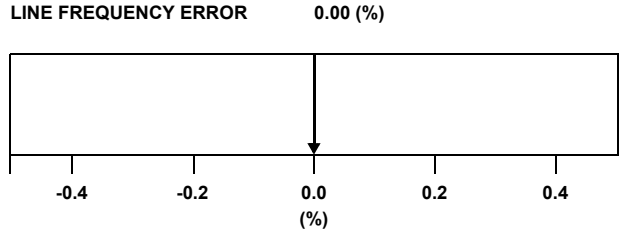


FIGURE 16. LINE FREQUENCY (NTSC)

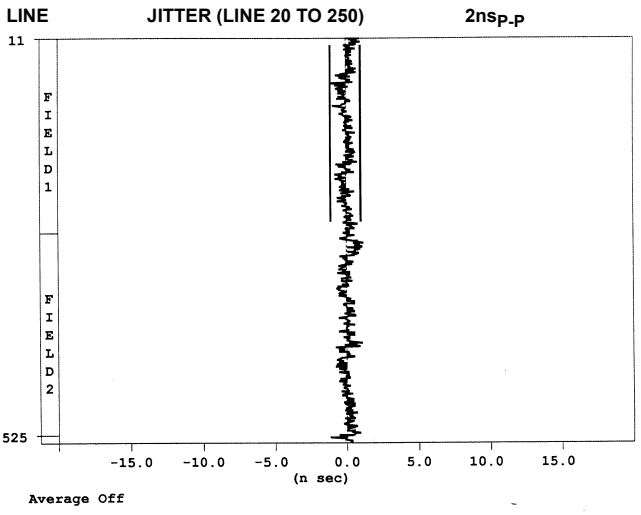


FIGURE 17. H SYNC JITTER IN A FRAME (NTSC)

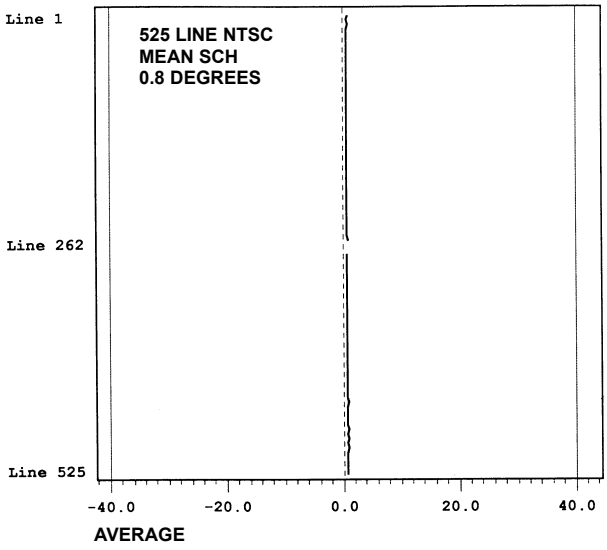


FIGURE 18. SCH PHASE MEASUREMENT

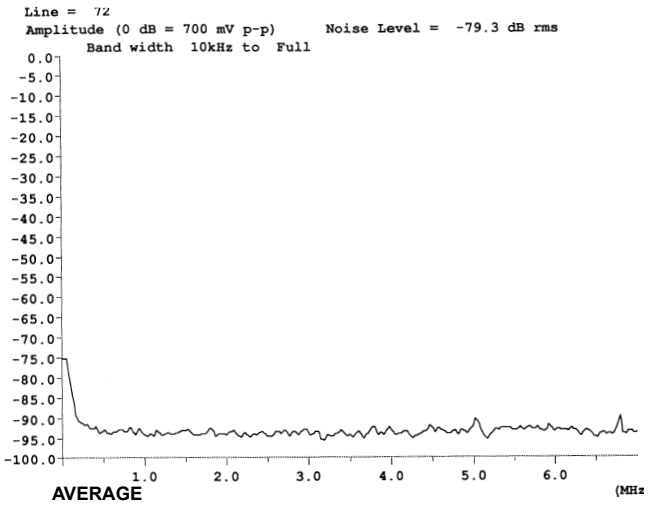


FIGURE 19. NOISE SPECTRUM (PAL)

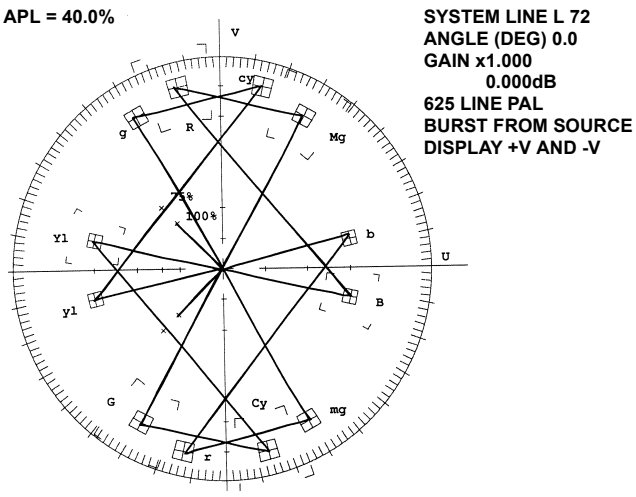


FIGURE 20. PAL COLOR BAR VECTOR SCAPE PLOT

Typical Performance Curves (Continued)

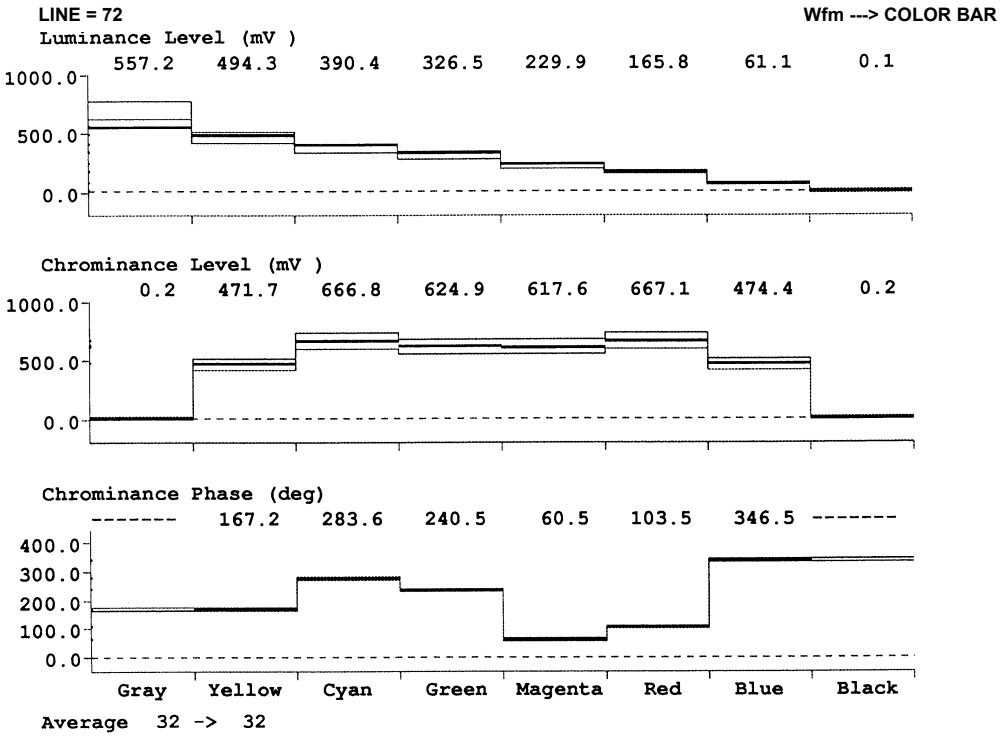


FIGURE 21. COLORBAR (PAL)

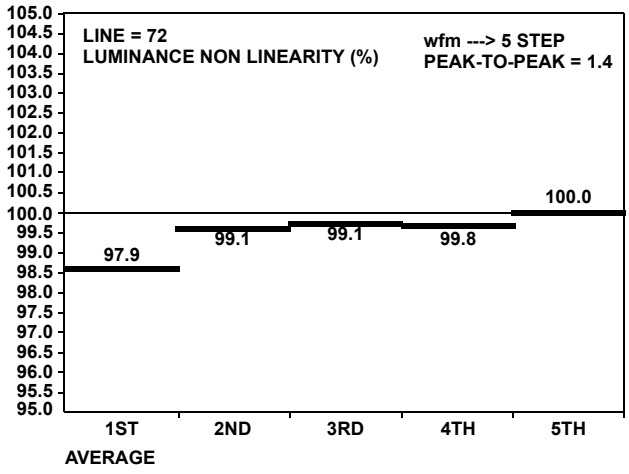


FIGURE 22. LUMINANCE NON LINEARITY (PAL)

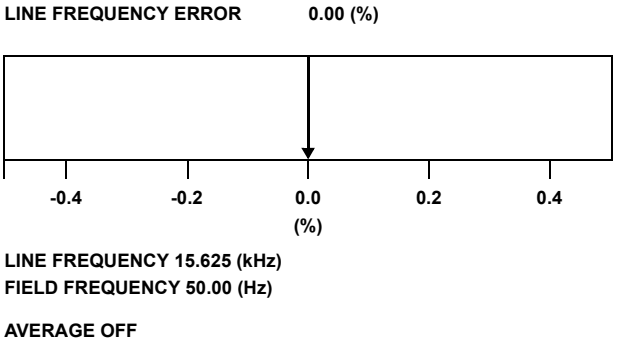


FIGURE 23. LINE FREQUENCY (PAL)

Typical Performance Curves (Continued)

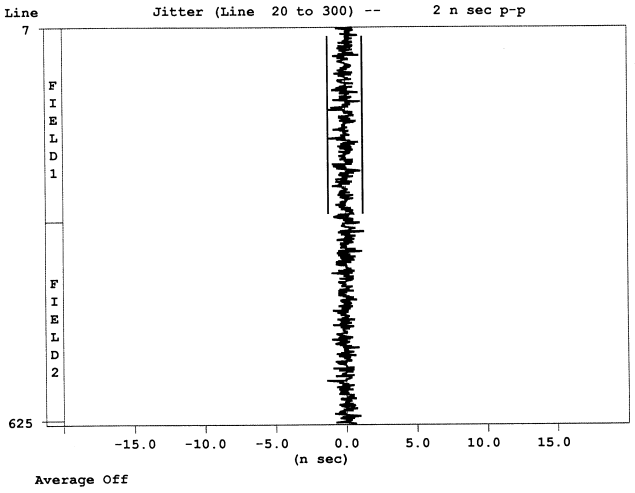


FIGURE 24. H SYNC JITTER IN A FRAME (PAL)

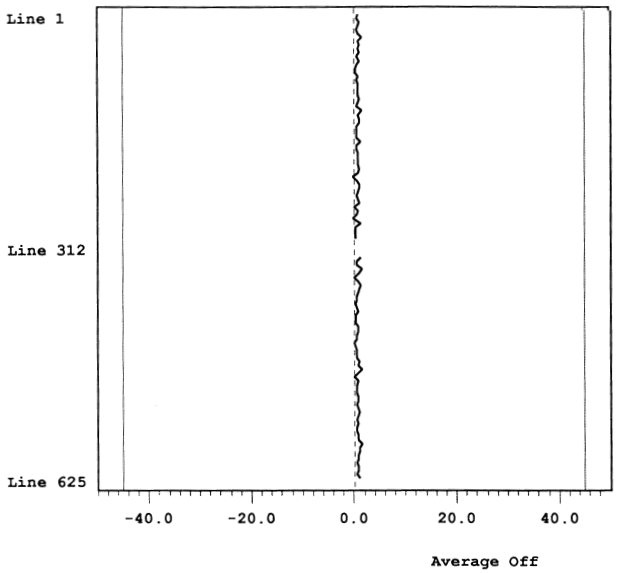


FIGURE 25. SCH PHASE MEASUREMENT

Application Information

PCB Considerations

A PCB board with a minimum of 4 layers is recommended, with layers 1 and 4 (top and bottom) for signals and layers 2 and 3 for power and ground. The PCB layout should implement the lowest possible noise on the power and ground planes by providing excellent decoupling. PCB trace lengths between groups of V_{AA} and GND pins should be as short as possible.

Component Placement

The optimum layout places the HMP8170 at the edge of the PCB and as close as possible to the video output connector. External components should be positioned as close as possible to the appropriate pin, ideally such that traces can be connected point to point. Chip capacitors are recommended where possible, with radial lead ceramic capacitors the second-best choice.

Traces containing digital signals should not be routed over, under, or adjacent to the analog output traces to minimize crosstalk. If this is not possible, coupling can be minimized by routing the digital signals at a 90 degree angle to the analog signals. The analog output traces should also not cross over or under the V_{CC} power plane to maximize high-frequency power supply rejection.

Power and Ground Planes

A common ground plane for all devices, including the HMP8170, is recommended. However, placing the encoder on an electrically connected GND peninsula reduces noise levels. All GND pins on the HMP8170 must be connected to the ground plane. Typical power and ground planes are shown in Figure 26.

The small connection between the ground areas should be made wide enough so that most of the encoders digital inputs can be routed over or under it. It is especially important that the CLK and CLK2 signals cross through the connection.

The HMP8170 should have its own power plane that is isolated from the common power plane of the board, with a gap between the two power planes of at least 1/8 inch. All V_{AA} pins of the HMP8170 must be connected to this isolated power plane.

The HMP8170 power plane should be connected to the board's normal V_{CC} power plane at a single point though a low-resistance ferrite bead, such as a Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001. The ferrite bead provides resistance to switching currents, improving the performance of HMP8170. A single, large capacitor should also be used between the HMP8170 power plane and the ground plane to control low-frequency power supply ripple.

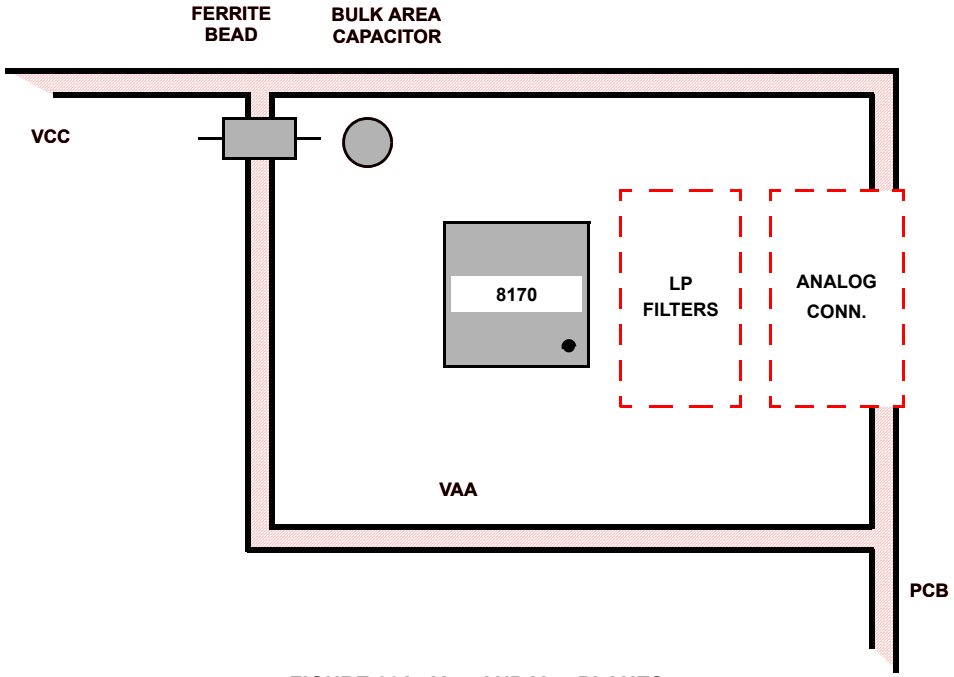


FIGURE 26A. V_{CC} AND V_{AA} PLANES

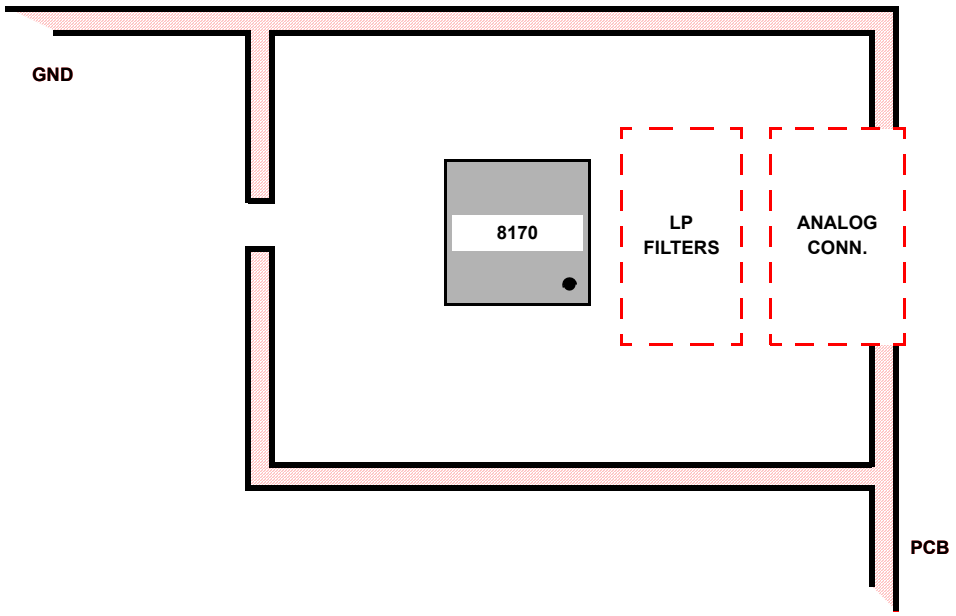


FIGURE 26B. COMMON GROUND PLANE

FIGURE 26. EXAMPLE POWER AND GROUND PLANES

For proper operation, power supply decoupling is required. It should be done using a 0.1µF ceramic capacitor in parallel with a 0.01µF chip capacitor for each group of V_{AA} pins to ground. These capacitors should be located as close to the V_{AA} and GND pins as possible, using short, wide traces.

If a separate linear regulator is used to provide power to the HMP8170 power plane, the power-up sequence should be designed to ensure latchup will not occur. A separate linear regulator is recommended if the power supply noise on the VAA pins exceeds 200mV. About 10% of the noise (that is less than 1MHz) on the VAA pins will couple onto the analog outputs.

External Reference Voltage

If an external reference voltage is used, its circuitry should receive power from the same plane as the HMP8170. The external VREF must also be stable and well decoupled from the power plane. An example VREF circuit using a band gap reference diode is shown in Figure 27.

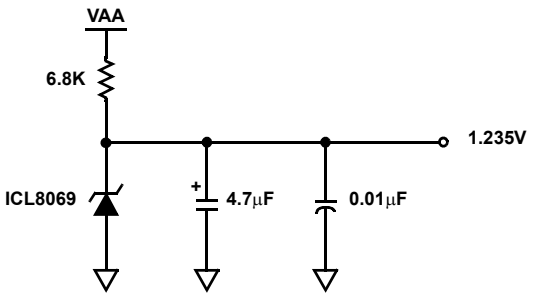


FIGURE 27. EXTERNAL REFERENCE VOLTAGE CIRCUIT

Analog Output Filters

The various video standards specify the frequency response of the video signal. The HMP8170 uses 2X oversampling DACs to simplify the reconstruction filter required. Example post filters are shown in Figure 28. The analog output filters should be as close as possible to the HMP8170.

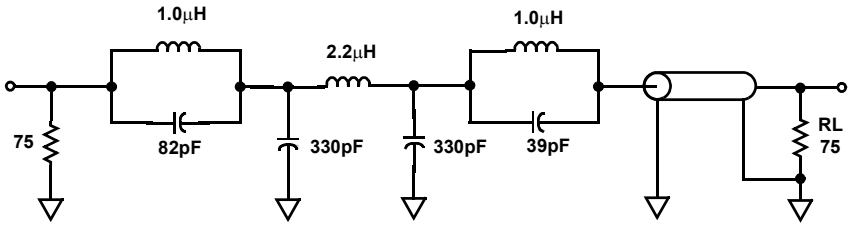


FIGURE 28A. HIGH QUALITY FILTER

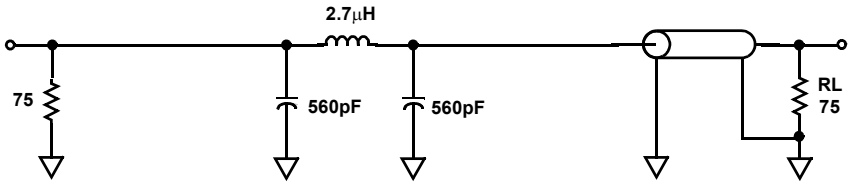


FIGURE 28B. LOW COST FILTER

FIGURE 28. EXAMPLE POST-FILTER CIRCUITS

Evaluation Kits

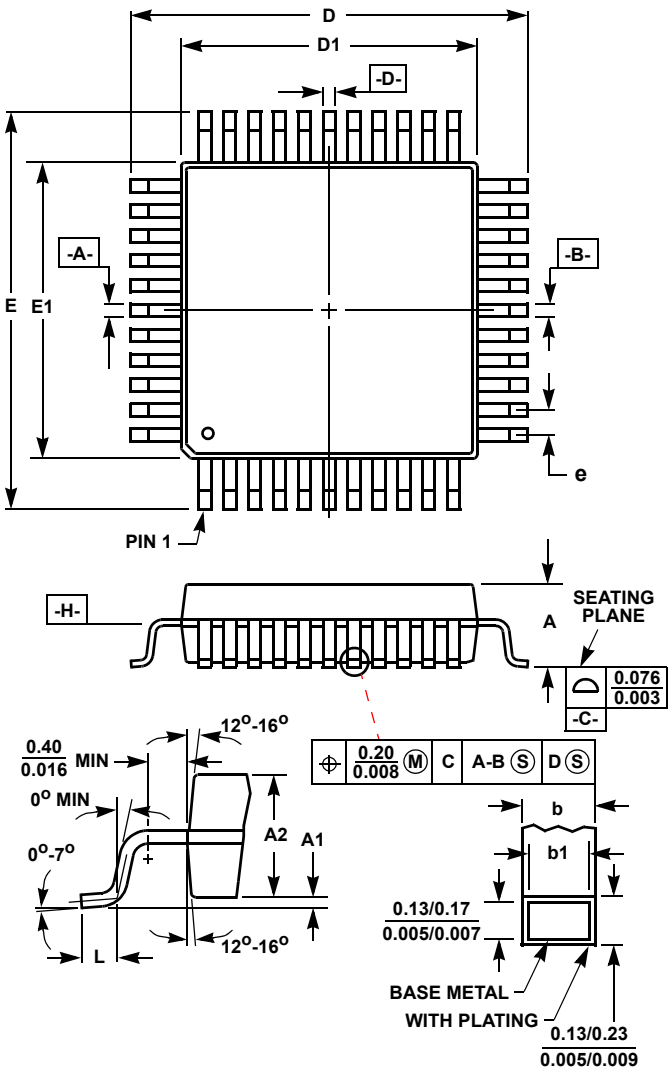
The HMP8170EVAL1 is a small (index card size) printed circuit board containing the encoder, voltage references and bypassing, analog output filters, and input/output connectors. The board allows the encoder's operation and performance to be observed and measured.

The HMP8170EVAL1 board has a 50 pin, two row receptacle which allows connection into an existing system. The connector provides access to all of the encoder's digital inputs and outputs.

The HMP8156EVAL2 is the Intersil designed mother board for the HMP8170EVAL1. The mother board is a standard size PC add in card with an ISA bus interface and application software. The HMP8156EVAL2 kit is a complete system which allows demonstrating all of both encoders' operating modes. It has analog video inputs for composite, S-video, and component RGB signals. The analog signals are converted/decoded to the digital domain and input to the encoder. The board also provides a 3 megabyte video RAM for image capture and display and a BT.656 connector and interface.

For simpler operation, the HMP8170EVAL1 may also be driven by external power supplies, a BT.656 signal generator, and a PC parallel port. The evaluation kit includes application software to program the part using its I^2C bus connected to the printer port. The board includes the standard 25 pin BT.656 connector and interface.

Metric Plastic Quad Flatpack Packages (MQFP)



Q64.14x14 (JEDEC MS-022BE ISSUE B)
64 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.124	-	3.15	-
A1	0.004	0.010	0.10	0.25	-
A2	0.100	0.108	2.55	2.75	-
b	0.012	0.018	0.30	0.45	6
b1	0.012	0.016	0.30	0.40	-
D	0.672	0.682	17.08	17.32	3
D1	0.546	0.556	13.88	14.12	4, 5
E	0.673	0.681	17.10	17.30	3
E1	0.547	0.555	13.90	14.10	4, 5
L	0.029	0.040	0.73	1.03	-
N	64		64		7
e	0.032 BSC		0.80 BSC		-

Rev. 1 4/99

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total.
7. “N” is the number of terminal positions.