

HITJ0302MP

-30V, -2.2A, 173mΩmax.
Silicon P Channel MOS FET
Power Switching

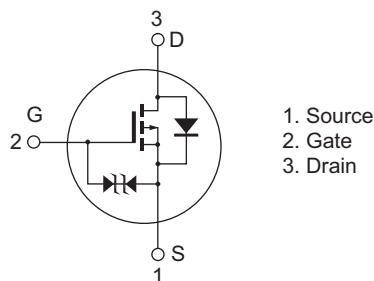
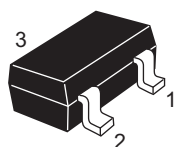
R07DS0477EJ0200
Rev.2.00
May 09, 2013

Features

- Low on-resistance
 $R_{DS(on)} = 138 \text{ m}\Omega$ typ ($V_{GS} = -10 \text{ V}$, $I_D = -1.1 \text{ A}$)
- Low drive current
- High speed switching
- 4.5 V gate drive

Outline

RENESAS Package code: PLSP0003ZB-A
(Package name: MPAK)



1. Source
2. Gate
3. Drain

Note: Marking is "NV".

Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	-30	V
Gate to source voltage	V_{GSS}	+10 / -20	V
Drain current	I_D	-2.2	A
Drain peak current	$I_{D(Pulse)}$ ^{Note1}	-5	A
Body - drain diode reverse drain current	I_{DR}	-2.2	A
Channel dissipation	P_{ch} ^{Note2}	0.8	W
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

- Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$
2. When using the glass epoxy board (FR-4: $40 \times 40 \times 1 \text{ mm}$)

Electrical Characteristics

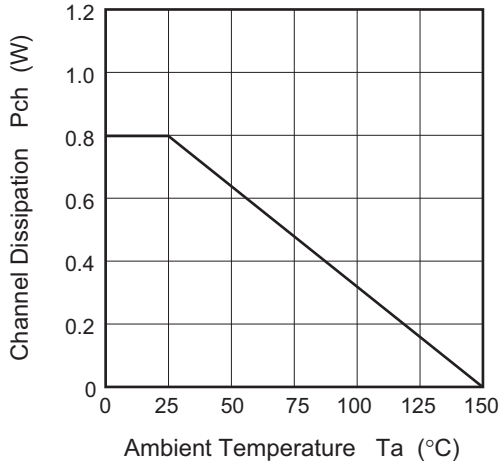
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-30	—	—	V	$I_D = -10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	+10	—	—	V	$I_G = +100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	-20	—	—	V	$I_G = -100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	+10	μA	$V_{GS} = +8 \text{ V}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	-10	μA	$V_{GS} = -16 \text{ V}$, $V_{DS} = 0$
Drain to source leak current	I_{DSS}	—	—	-1	μA	$V_{DS} = -30 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.0	V	$V_{DS} = -10 \text{ V}$, $I_D = -1 \text{ mA}$
Drain to source on state resistance	$R_{DS(on)}$	—	138	173	$\text{m}\Omega$	$I_D = -1.1 \text{ A}$, $V_{GS} = -10 \text{ V}$ ^{Note3}
	$R_{DS(on)}$	—	216	303	$\text{m}\Omega$	$I_D = -1.1 \text{ A}$, $V_{GS} = -4.5 \text{ V}$ ^{Note3}
Forward transfer admittance	$ y_{fs} $	1.2	2.1	—	S	$I_D = -1.1 \text{ A}$, $V_{DS} = -10 \text{ V}$ ^{Note3}
Input capacitance	C_{iss}	—	195	—	pF	$V_{DS} = -10 \text{ V}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	42	—	pF	
Reverse transfer capacitance	C_{rss}	—	29	—	pF	
Turn - on delay time	$t_{d(on)}$	—	19	—	ns	
Rise time	t_r	—	25	—	ns	$I_D = -0.5 \text{ A}$, $V_{GS} = -10 \text{ V}$, $R_L = 20 \text{ }\Omega$, $R_g = 4.7 \text{ }\Omega$
Turn - off delay time	$t_{d(off)}$	—	30	—	ns	
Fall time	t_f	—	4.6	—	ns	
Total gate charge	Q_g	—	4.2	—	nC	
Gate to source charge	Q_{gs}	—	0.7	—	nC	$V_{DD} = -10 \text{ V}$, $V_{GS} = -10 \text{ V}$, $I_D = -2.2 \text{ A}$
Gate to drain charge	Q_{gd}	—	1.0	—	nC	
Body - drain diode forward voltage	V_{DF}	—	-0.9	—	V	
						$I_F = -1.5 \text{ A}$, $V_{GS} = 0$ ^{Note3}

Notes: 3. Pulse test

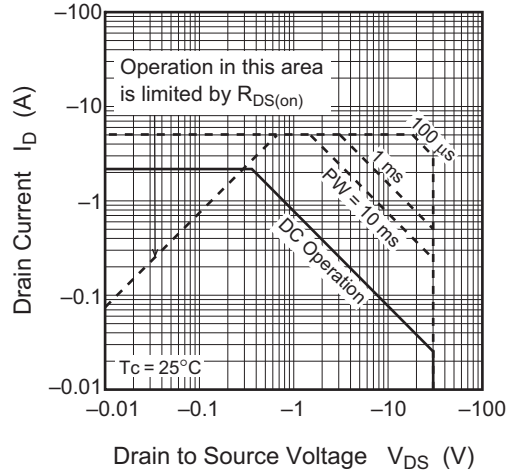
Main Characteristics

Maximum Channel Power Dissipation Curve

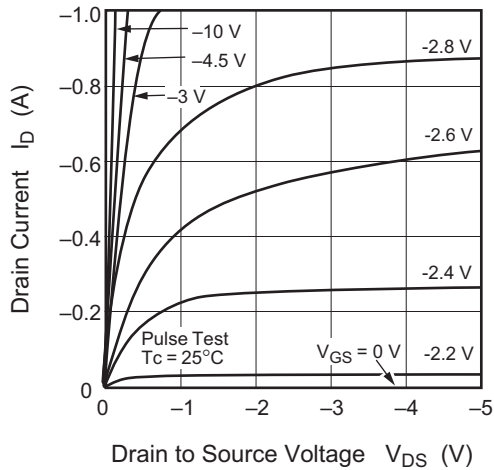


*When using the glass epoxy board (FR-4: 40 × 40 × 1 mm)

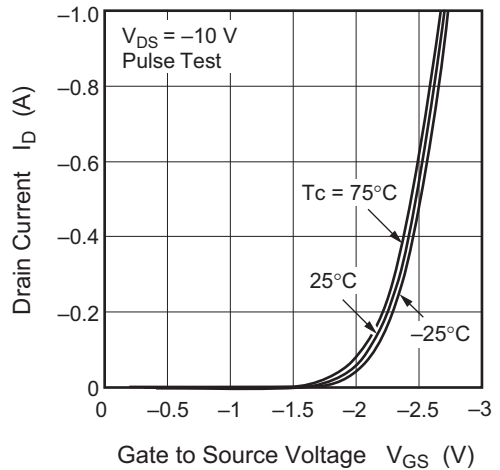
Maximum Safe Operation Area



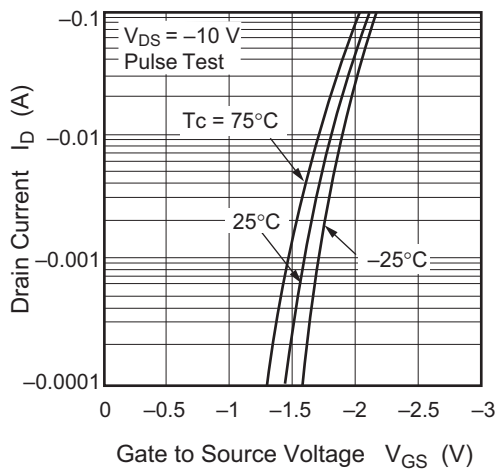
Typical Output Characteristics



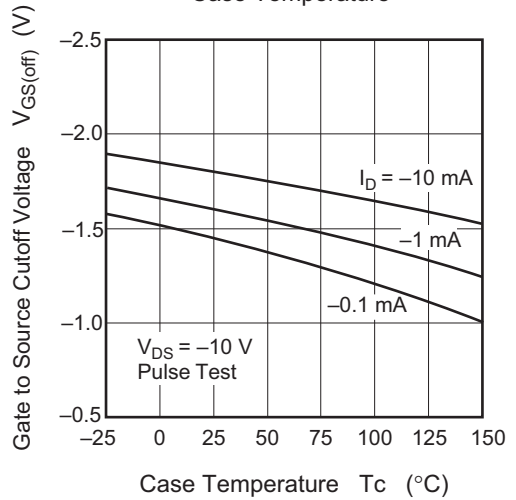
Typical Transfer Characteristics (1)

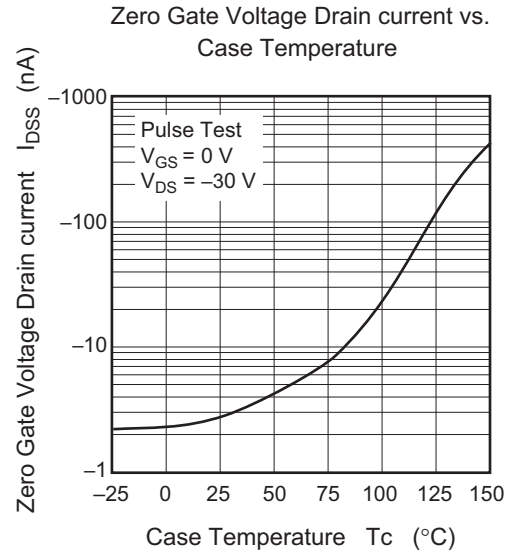
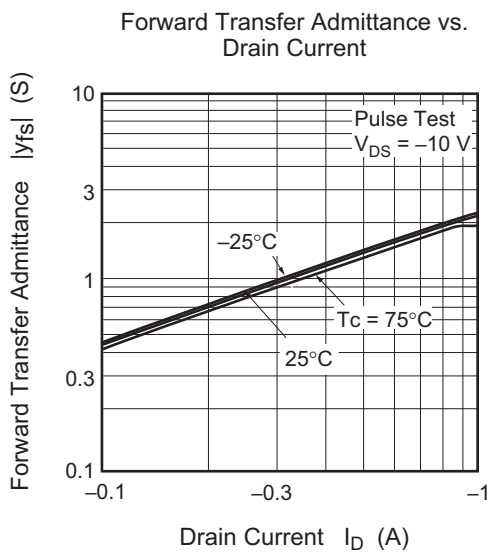
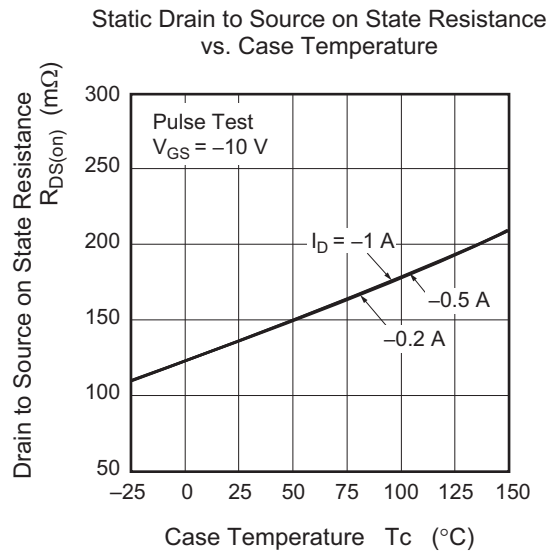
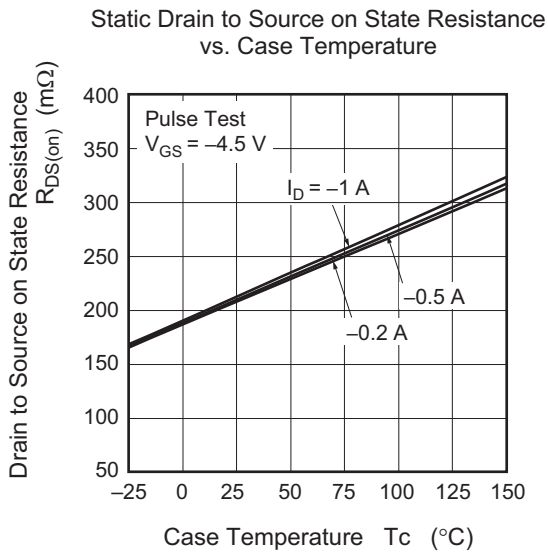
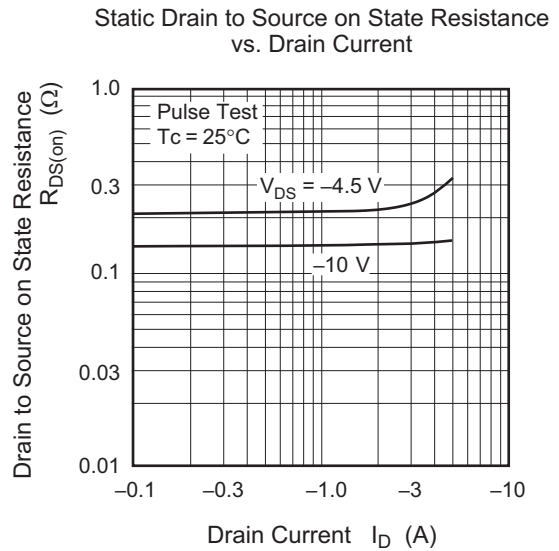
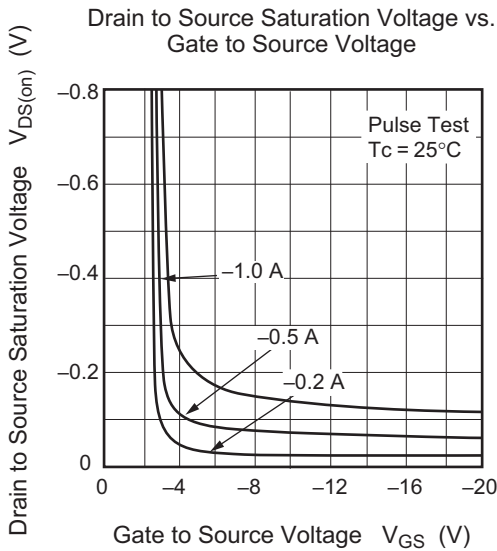


Typical Transfer Characteristics (2)

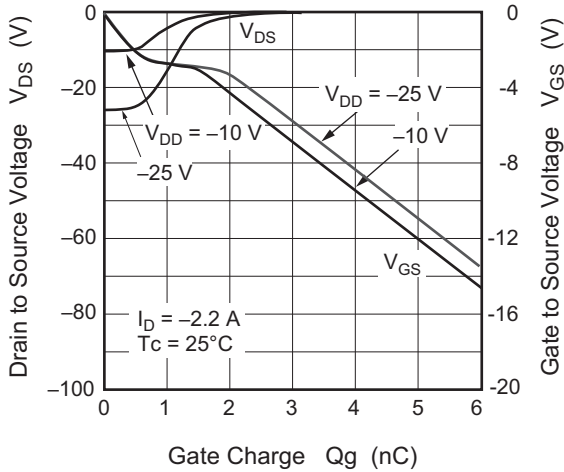


Gate to Source Cutoff Voltage vs. Case Temperature

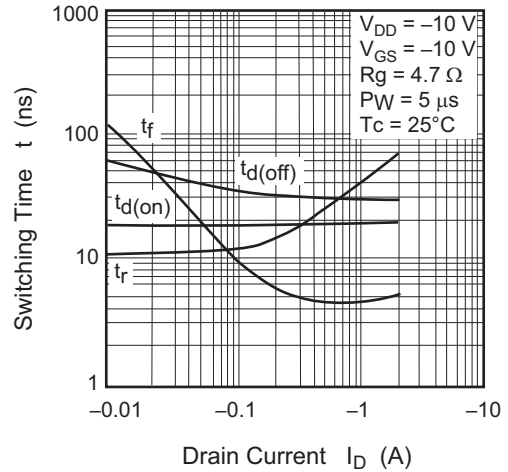




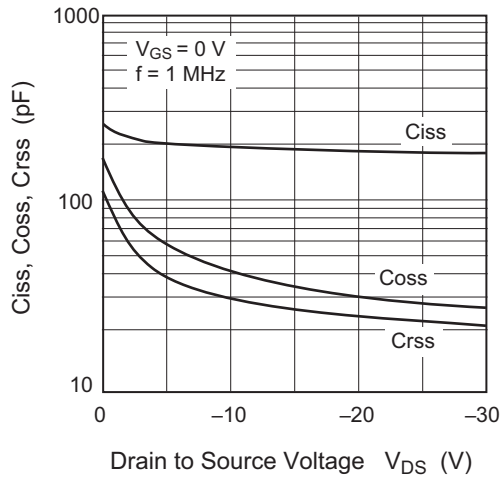
Dynamic Input Characteristics



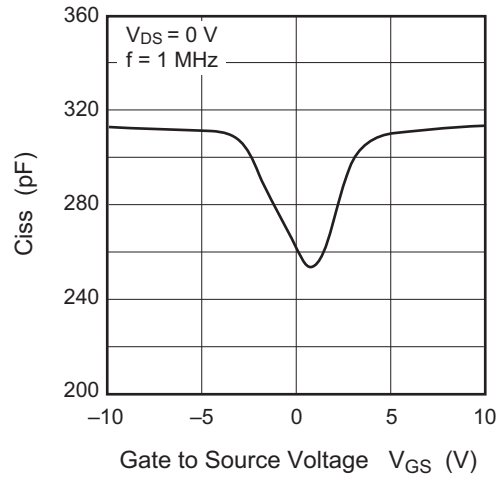
Switching Characteristics



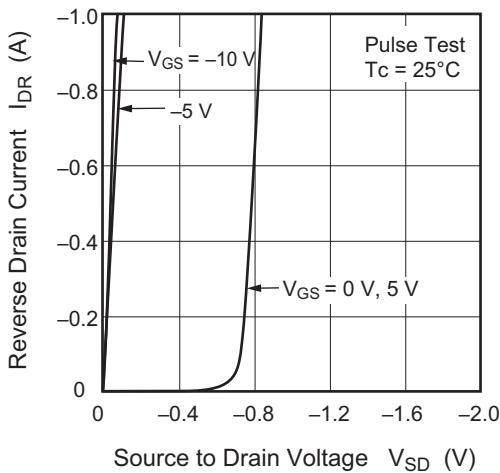
Typical Capacitance vs. Drain to Source Voltage



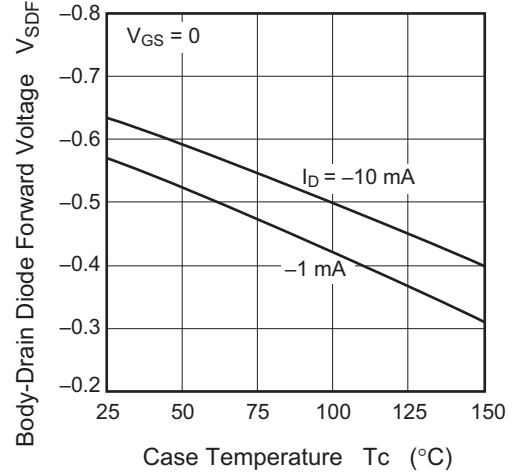
Input Capacitance vs. Gate to Source Voltage



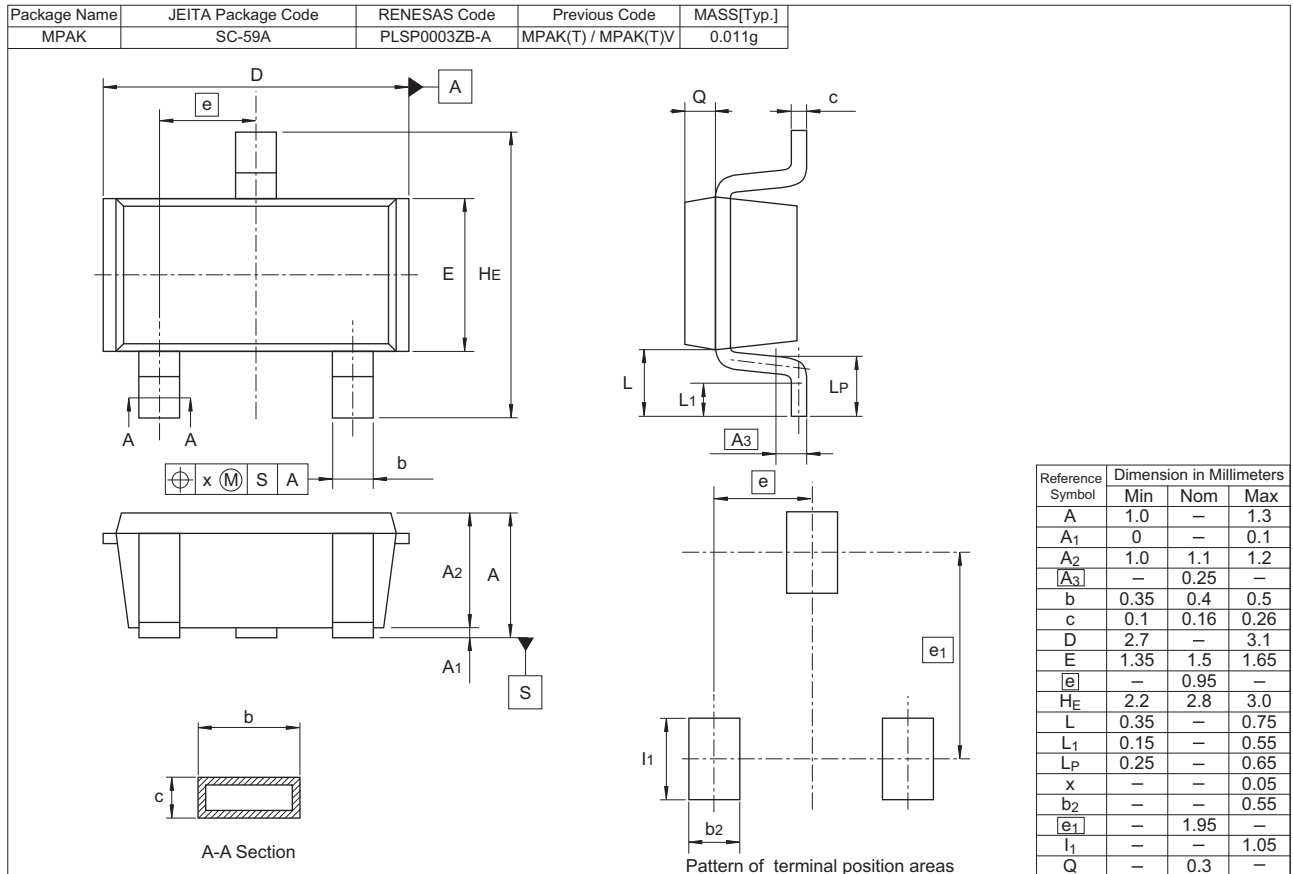
Reverse Drain Current vs. Source to Drain Voltage



Body-Drain Diode Forward Voltage vs. Case Temperature



Package Dimensions



Ordering Information

Orderable Part Number	Quantity	Shipping Container
HITJ0302MPTL-HQ	3000 pcs.	φ178 mm reel, 8 mm Emboss taping

Note: This product is designed for consumer use and not for automotive.

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