HI1175

8-Bit, 20MSPS, Flash A/D Converter

Pb-Free and RoHS Compliant

FN3577
Rev 8.00
October 25, 2005

The HI1175 is an 8-bit, analog-to-digital converter built in a 1.4µm CMOS process. The low power, low differential gain and phase, high sampling rate, and single 5V supply make the HI1175 ideal for video and imaging applications.

The adoption of a 2-step flash architecture achieves low power consumption (60mW) at a maximum conversion speed of 20MSPS (Min), 35MSPS typical with only a 2.5 clock cycle data latency. The HI1175 also features digital output enable/disable and a built in voltage reference. The HI1175 can be configured to use the internal reference or an external reference if higher precision is required.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI1175JCB	-40 to 85	24 Ld SOIC	M24.2-S
HI1175-EV	25	Evaluation Board	

Features

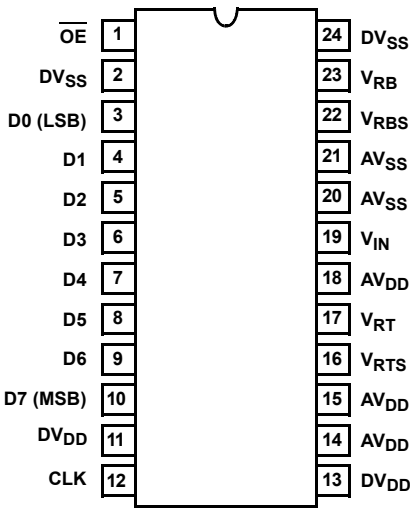
- Resolution . . . . . 8-Bit ±0.3 LSB (DNL)
- Maximum Sampling Frequency 20MSPS
- Low Power Consumption . . . . . 60mW (at 20MSPS Typ) (Reference Current Excluded)
- Built-In Sample and Hold Circuit
- Built-In Reference Voltage Self Bias Circuit
- Three-State TTL Compatible Output
- Single +5V Power Supply
- Low Input Capacitance. . . . . 11pF (Typ)
- Reference Impedance . . . . . 300Ω (Typ)
- Evaluation Board Available (HI1175-EV)
- Low Cost
- Direct Replacement for the Sony CXD1175

Applications

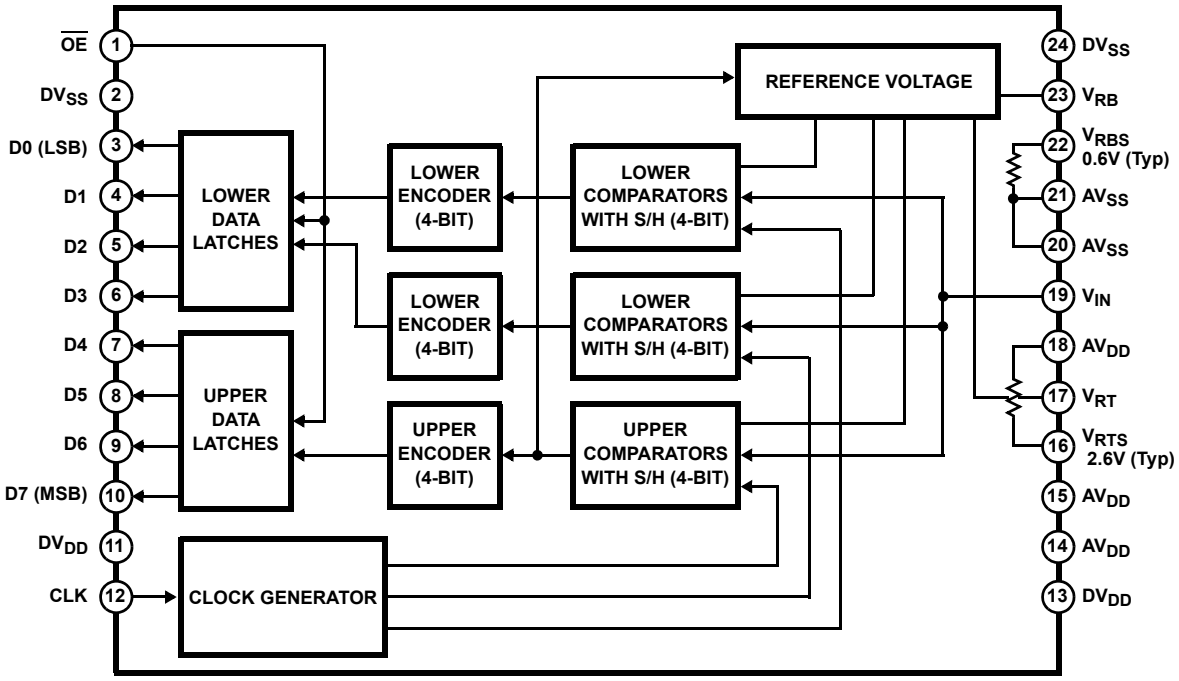
- Video Digitizing
- PC Video Capture
- Image Scanners
- TV Set Top Boxes
- Multimedia
- Personal Communication Systems (PCS)

Pinout

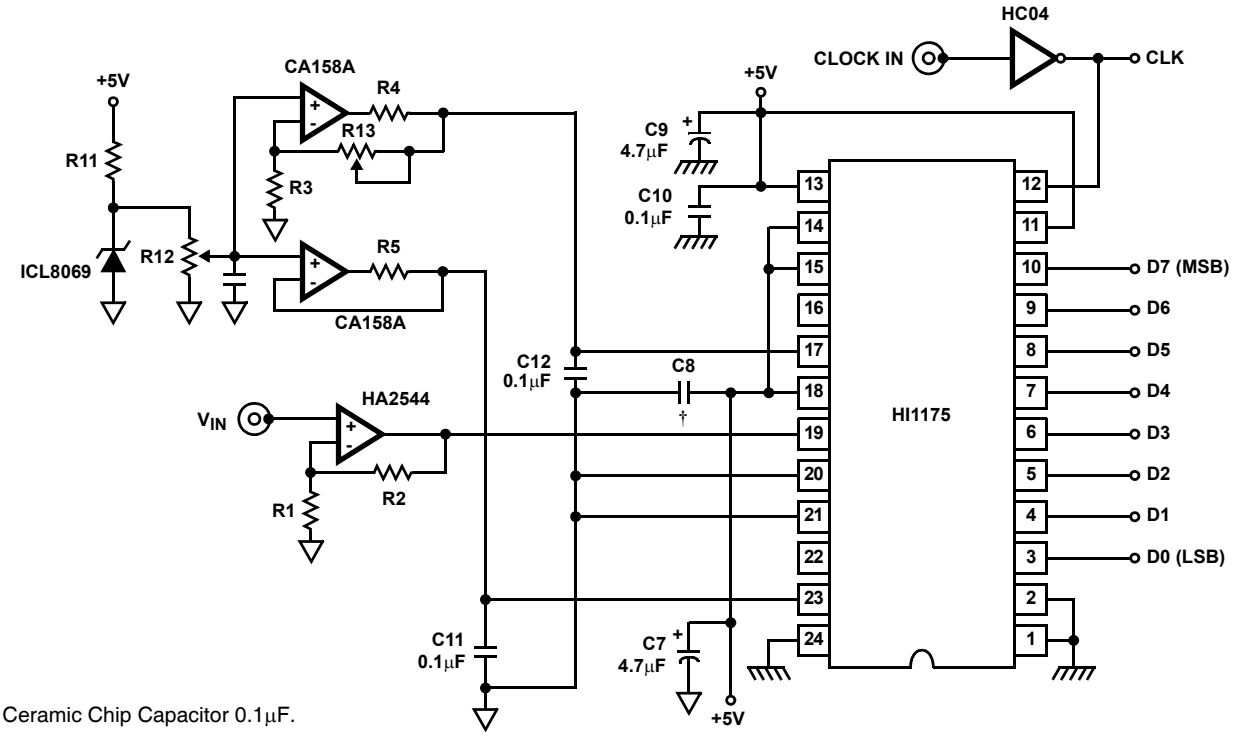
HI1175 (SOIC)
TOP VIEW



Functional Block Diagram



Typical Application Schematic



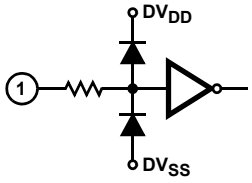
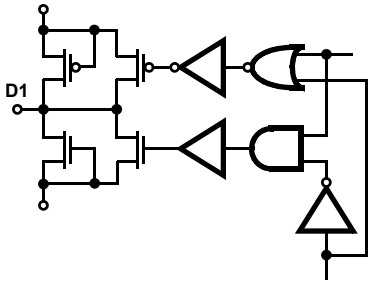
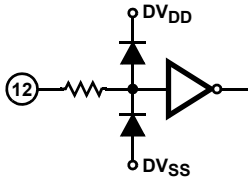
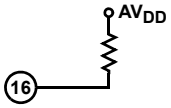
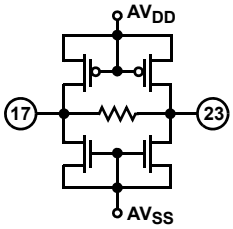
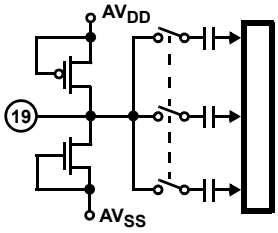
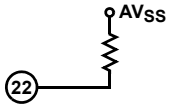
† : Ceramic Chip Capacitor 0.1µF.

: Analog GND.

: Digital GND.

NOTE: It is necessary that AV_{DD} and DV_{DD} pins be driven from the same supply. The gain of analog input signal can be changed by adjusting the ratio of R2 to R1.

Pin Descriptions and Equivalent Circuits

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1	$\overline{OE}$		When $\overline{OE}$ = Low, Data is valid. When $\overline{OE}$ = High, D0 to D7 pins high impedance.
2, 24	DV_{SS}		Digital GND.
3-10	D0 to D7		D0 (LSB) to D7 (MSB) Output.
11, 13	DV_{DD}		Digital +5V.
12	CLK		Clock Input.
16	V_{RTS}		Shorted with V_{RT} generates, +2.6V.
17	V_{RT}		Reference Voltage (Top).
23	V_{RB}		Reference Voltage (Bottom).
14, 15, 18	AV_{DD}		Analog +5V.
19	V_{IN}		Analog Input.
20, 21	AV_{SS}		Analog GND.
22	V_{RBS}		Shorted with V_{RB} generates +0.6V.

Absolute Maximum Ratings

Supply Voltage, V_{DD} 7V
Reference Voltage, V_{RT}, V_{RB} . . . . . V_{DD} to V_{SS}
Analog Input Voltage, V_{IN} . . . . . V_{DD} to V_{SS}
Digital Input Voltage, CLK . . . . . V_{DD} to V_{SS}
Digital Output Voltage, V_{OH}, V_{OL} . . . . . V_{DD} to V_{SS}

Operating Conditions (Note 1)

Temperature Range, T_A . . . . . -40°C to 85°C
Supply Voltage
AV_{DD}, AV_{SS}, DV_{DD}, DV_{SS} . . . . . +4.75V to +5.25V
|DGND-AGND| . . . . . 0mV to 100mV
Reference Input Voltage
V_{RB} . . . . . 0V and Above
V_{RT} . . . . . 2.8V and Below
Analog Input Range, V_{IN} . . . . . V_{RB} to V_{RT} ($1.8V_{P-P}$ to $2.8V_{P-P}$)
Clock Pulse Width
t_{PW1} . . . . . 25ns (Min)
t_{PW0} . . . . . 25ns (Min)

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
SOIC Package 98
Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range, T_{STG} . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

f_C = 20 MSPS, V_{DD} = +5V, V_{RB} = 0.5V, V_{RT} = 2.5V, T_A = 25°C (Note 1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PERFORMANCE					
Offset Voltage		-	-	-	-
E_{OT}		-60	-35	-10	mV
E_{OB}		0	+15	+45	mV
Integral Non-Linearity, INL	f_C = 20 MSPS, V_{IN} = 0.6V to 2.6V	-	±0.5	±1.3	LSB
Differential Non-Linearity, DNL	f_C = 20 MSPS, V_{IN} = 0.6V to 2.6V	-	±0.3	±0.5	LSB
DYNAMIC CHARACTERISTICS					
Effective Number of Bits, ENOB	f_{IN} = 1MHz	-	7.6	-	Bits
Spurious Free Dynamic Range	f_{IN} = 1MHz	-	51	-	dB
Signal to Noise Ratio, SINAD $= \frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	f_C = 20MHz, f_{IN} = 1MHz	-	46	-	dB
	f_C = 20MHz, f_{IN} = 3.58MHz	-	46	-	dB
Maximum Conversion Speed, f_C	V_{IN} = 0.6V to 2.6V, f_{IN} = 1kHz Ramp	20	35	-	MSPS
Minimum Conversion Speed		-	-	0.5	MSPS
Differential Gain Error, DG	NTSC 40 IRE Mod Ramp, f_C = 14.3 MSPS	-	1.0	-	%
Differential Phase Error, DP		-	0.5	-	Degree
Aperture Jitter, t_{AJ}		-	30	-	ps
Sampling Delay, t_{DS}		-	4	-	ns
Data Latency, t_{LAT}		-	-	2.5	Cycles
ANALOG INPUTS					
Analog Input Bandwidth (-1dB), BW		-	18	-	MHz
Analog Input Capacitance, C_{IN}	V_{IN} = 1.5V + $0.07V_{RMS}$	-	11	-	pF

Electrical Specifications f_C = 20 MSPS, V_{DD} = +5V, V_{RB} = 0.5V, V_{RT} = 2.5V, T_A = 25°C (Note 1) **(Continued)**

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
REFERENCE INPUT						
Reference Pin Current, I_{REF}			4.5	6.6	8.7	mA
Reference Resistance (V_{RT} to V_{RB}), R_{REF}			230	300	450	Ω
INTERNAL VOLTAGE REFERENCE						
Self Bias Mode 1			-	-	-	-
V_{RB}	Short V_{RB} and V_{RBS}, Short V_{RT} and V_{RTS}		0.60	0.64	0.68	V
V_{RT} - V_{RB}			1.96	2.09	2.21	V
Self Bias Mode 2, V_{RT}	V_{RB} = AGND, Short V_{RT} and V_{RTS}		2.25	2.39	2.53	V
DIGITAL INPUTS						
Digital Input Voltage			-	-	-	-
V_{IH}			4.0	-	-	V
V_{IL}			-	-	1.0	V
Digital Input Current			-	-	-	-
I_{IH}	V_{DD} = Max	V_{IH} = V_{DD}	-	-	5	µA
I_{IL}		V_{IL} = 0V	-	-	5	µA
DIGITAL OUTPUTS						
Digital Output Current			-	-	-	-
I_{OH}	$\overline{OE}$ = V_{SS}, V_{DD} = Min	V_{OH} = V_{DD} -0.5V	-1.1	-	-	mA
I_{OL}		V_{OL} = 0.4V	3.7	-	-	mA
Digital Output Current			-	-	-	-
I_{OZH}	$\overline{OE}$ = V_{DD}, V_{DD} = Max	V_{OH} = V_{DD}	-	0.01	16	µA
I_{OZL}		V_{OL} = 0V	-	0.01	16	µA
TIMING CHARACTERISTICS						
Output Data Delay, t_{DL}			-	18	30	ns
POWER SUPPLY CHARACTERISTIC						
Supply Current, I_{DD}	f_C = 20 MSPS, NTSC Ramp Wave Input		-	12	17	mA

NOTE:

2. Electrical specifications guaranteed only under the stated operating conditions.

Timing Diagrams

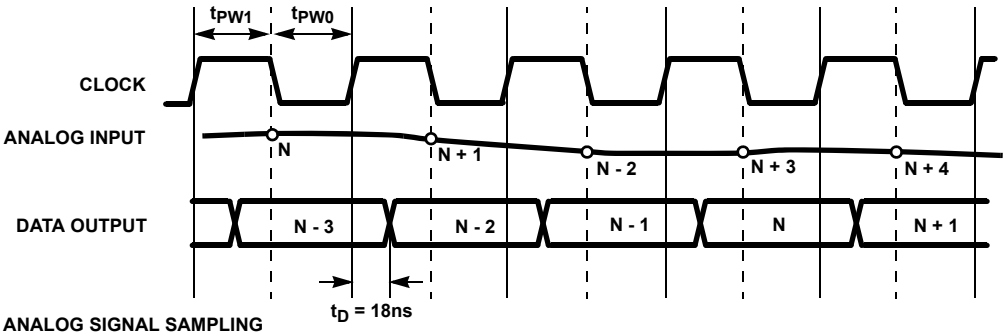


FIGURE 1.

Timing Diagrams (Continued)

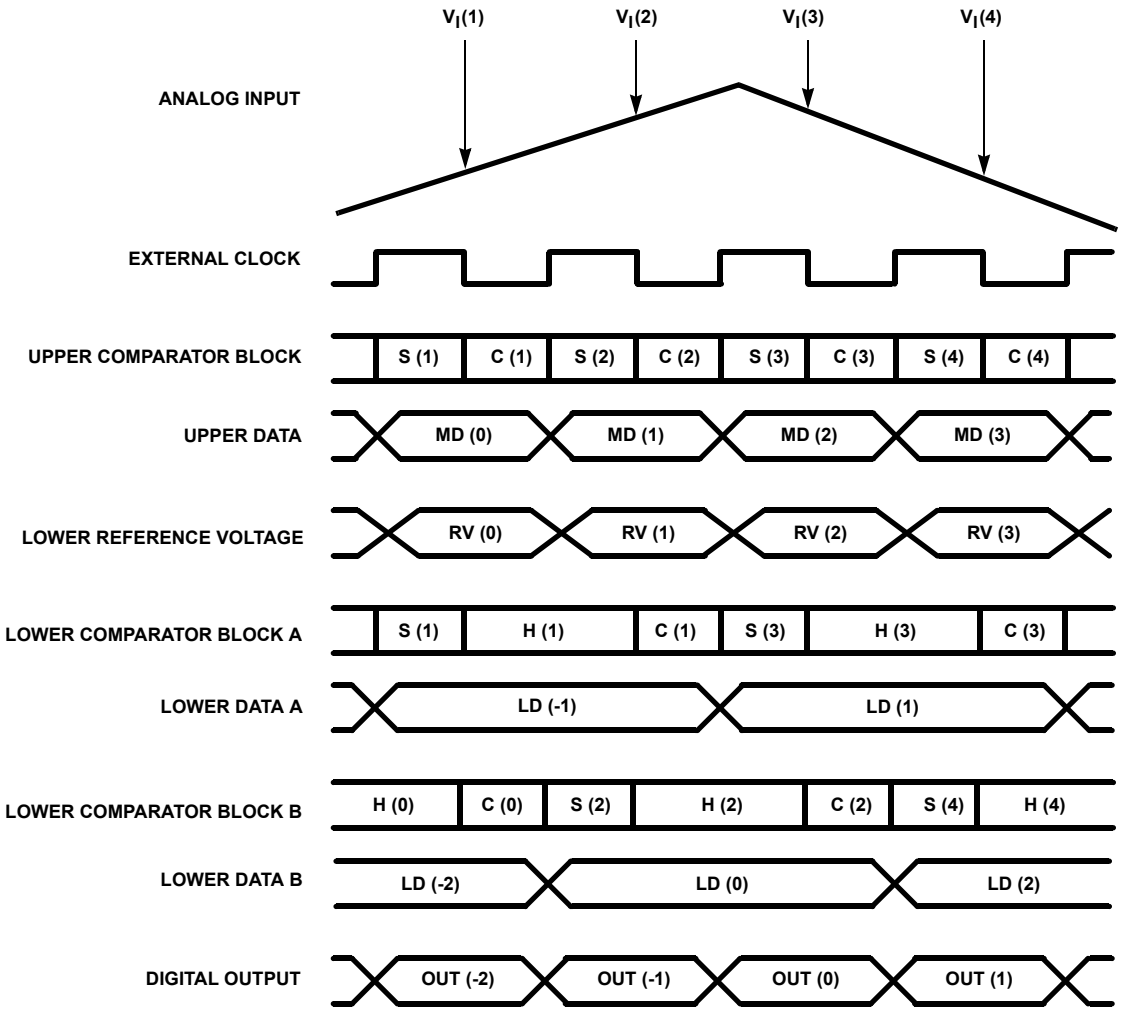


FIGURE 2.

Typical Performance Curves

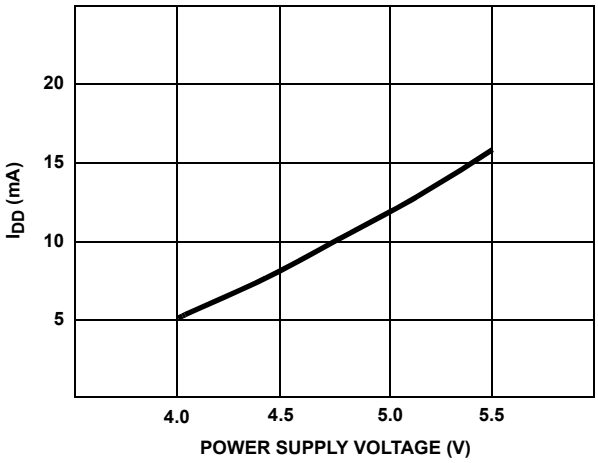


FIGURE 3. SUPPLY CURRENT vs SUPPLY VOLTAGE

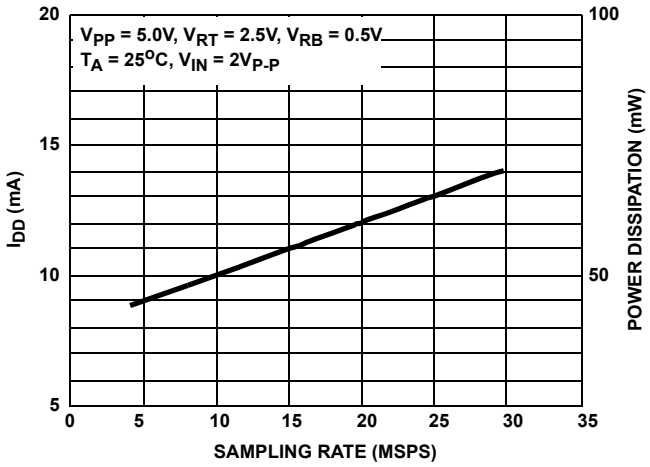


FIGURE 4. SUPPLY CURRENT AND POWER vs SAMPLING RATE

Typical Performance Curves (Continued)

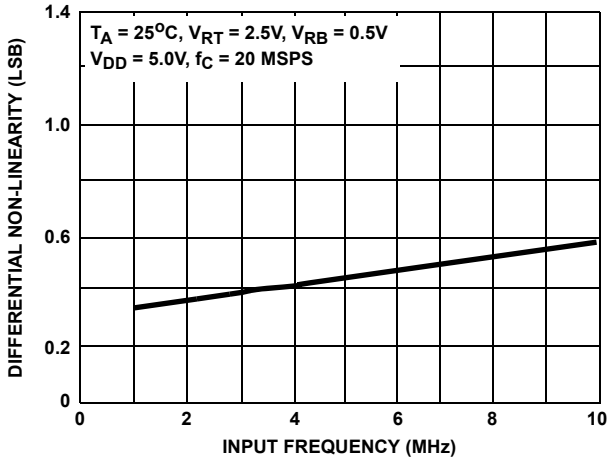


FIGURE 5. DIFFERENTIAL NON-LINEARITY vs INPUT FREQUENCY

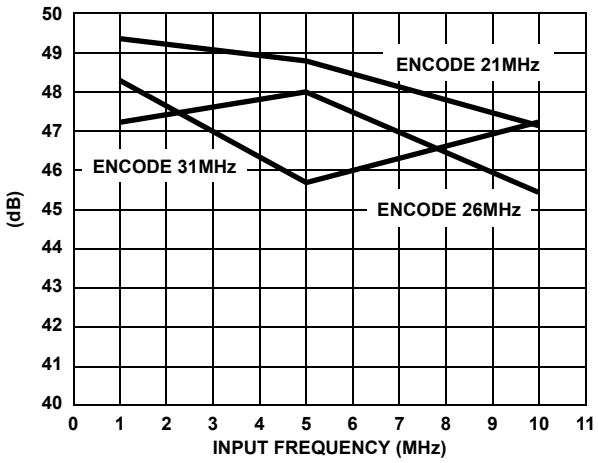


FIGURE 6. HI1175JCP SNR vs INPUT FREQUENCY

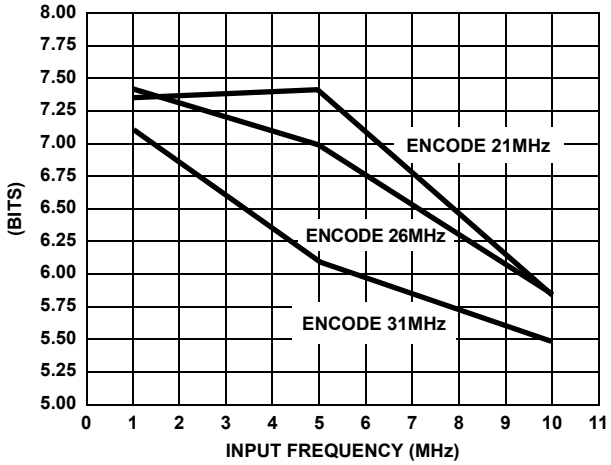


FIGURE 7. HI1175JCP ENOB vs INPUT FREQUENCY

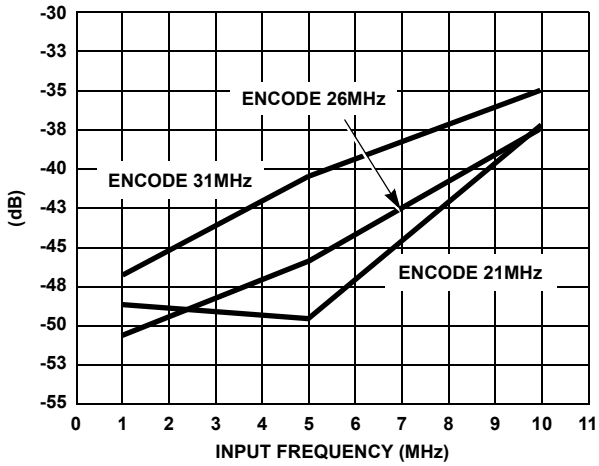


FIGURE 8. HI1175JCP THD vs INPUT FREQUENCY

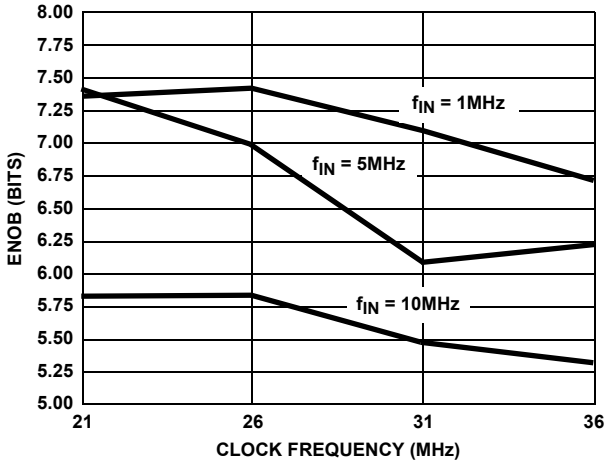


FIGURE 9. ENOB vs CLOCK FREQUENCY

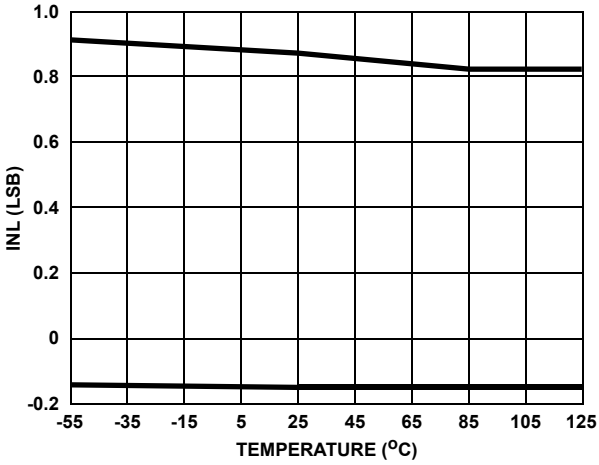


FIGURE 10. INL vs TEMPERATURE

Typical Performance Curves (Continued)

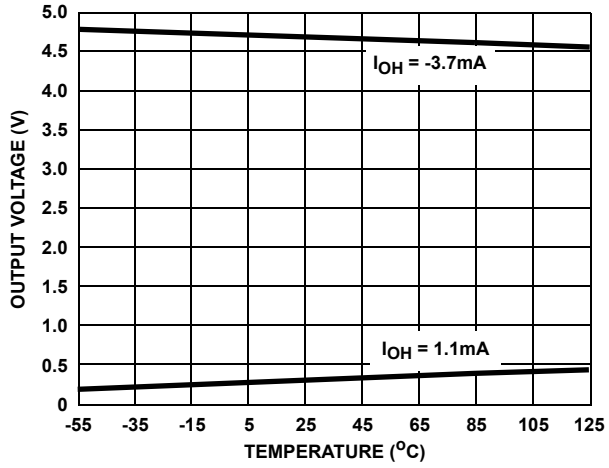


FIGURE 11. DIGITAL OUTPUT VOLTAGE vs TEMPERATURE

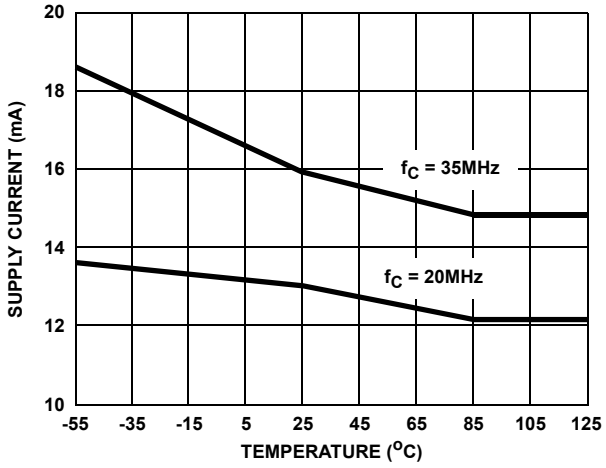


FIGURE 12. SUPPLY CURRENT vs TEMPERATURE

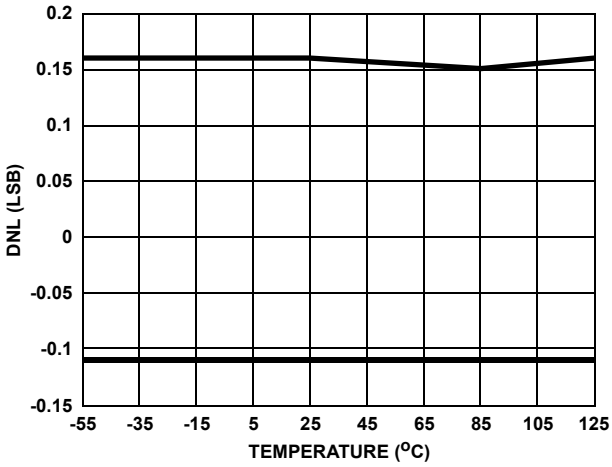


FIGURE 13. DNL vs TEMPERATURE

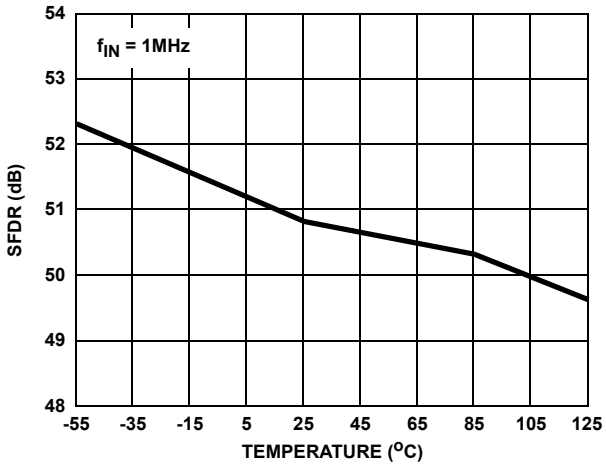


FIGURE 14. SFDR vs TEMPERATURE

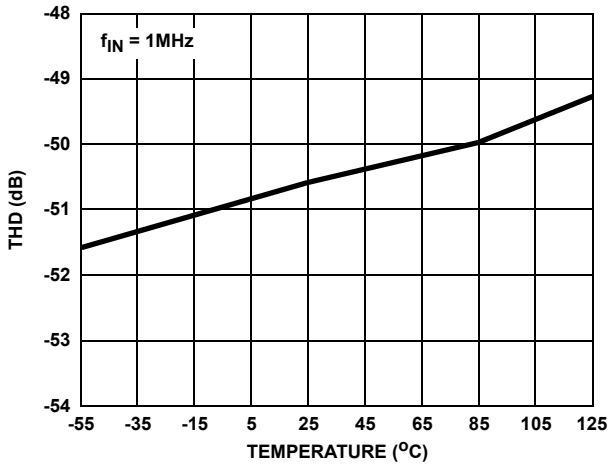


FIGURE 15. THD vs TEMPERATURE

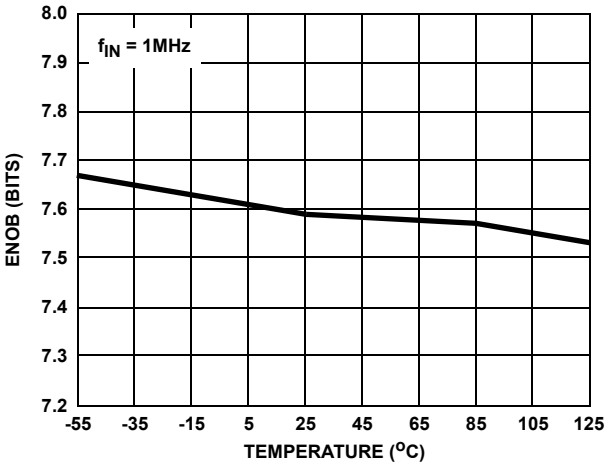


FIGURE 16. ENOB vs TEMPERATURE

Typical Performance Curves (Continued)

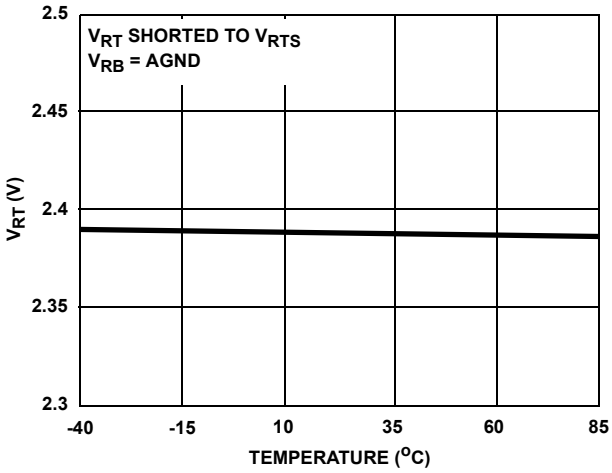


FIGURE 17. V_{RT} vs TEMPERATURE

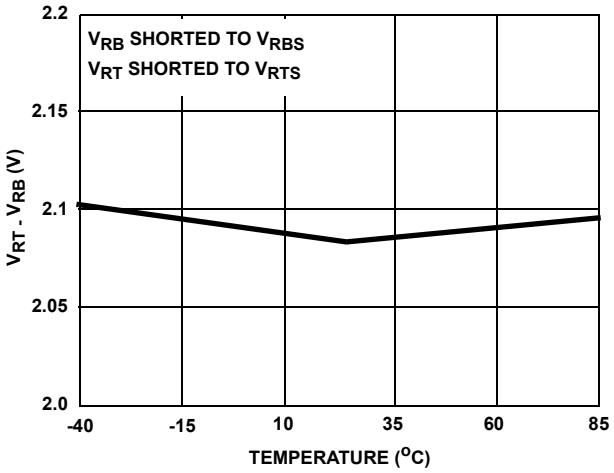


FIGURE 18. V_{RT} - V_{RB} vs TEMPERATURE

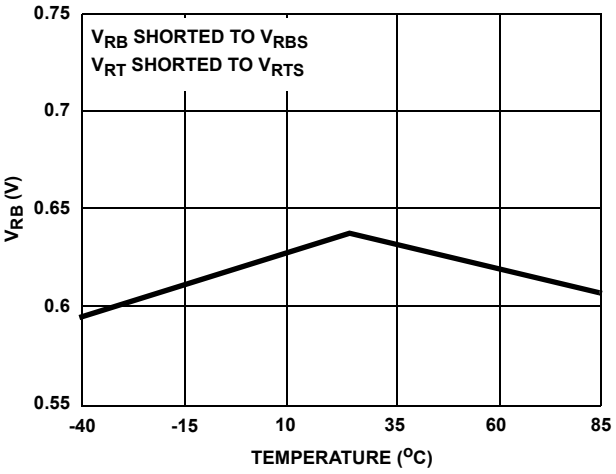


FIGURE 19. V_{RB} vs TEMPERATURE

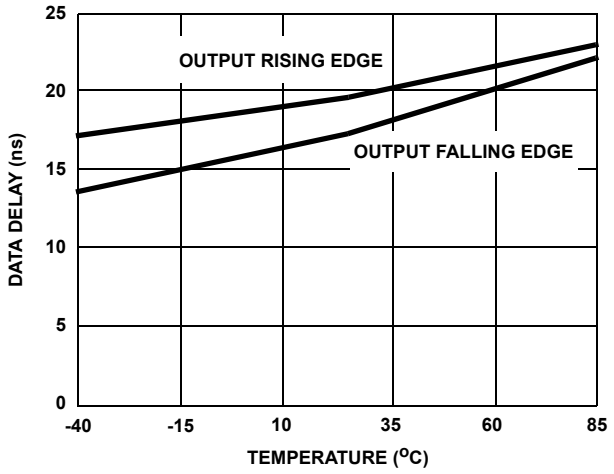


FIGURE 20. OUTPUT DATA DELAY vs TEMPERATURE

A/D OUTPUT CODE TABLE

INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE							
		MSB	D6	D5	D4	D3	D2	D1	LSB
V_{RT}	255	1	1	1	1	1	1	1	1
•	•					•			
•	•					•			
•	•					•			
•									
•	128	1	0	0	0	0	0	0	0
•	127	0	1	1	1	1	1	1	1
•									
•	•					•			
	•					•			
	•					•			
V_{RB}	0	0	0	0	0	0	0	0	0

Detailed Description

The HI1175 is a 2-step A/D converter featuring a 4-bit upper comparator group and two lower comparator groups of 4 bits each. The reference voltage can be obtained from the onboard bias generator or be supplied externally. This IC uses an offset canceling type comparator that operates synchronously with an external clock. The operating modes of the part are input sampling (S), hold (H), and compare (C).

The operation of the part is illustrated in Figure 2. A reference voltage that is between V_{RT}-V_{RB} is constantly applied to the upper 4-bit comparator group. $V_I(1)$ is sampled with the falling edge of the first clock by the upper comparator block. The lower block A also samples $V_I(1)$ on the same edge. The upper comparator block finalizes comparison data MD(1) with the rising edge of the first clock. Simultaneously the reference supply generates a reference voltage RV(1) that corresponds to the upper results and applies it to the lower comparator block A. The lower comparator block finalizes comparison data LD(1) with the rising edge of the second clock. MD(1) and LD(1) are combined and output as OUT(1) with the rising edge of the third clock. There is a 2.5 cycle clock delay from the analog input sampling point to the corresponding digital output data. Notice how the lower comparator blocks A and B alternate generating the lower data in order to increase the overall A/D sampling rate.

Power, Grounding, and Decoupling

To reduce noise effects, separate the analog and digital grounds.

In order to avoid latchup at power up, it is necessary that AV_{DD} and DV_{DD} be driven from the same supply.

Bypass both the digital and analog V_{DD} pins to their respective grounds with a ceramic 0.1µF capacitor close to the pin.

Analog Input

The input capacitance is small when compared with other flash type A/D converters. However, it is necessary to drive the input with an amplifier with sufficient bandwidth and drive capability. In order to prevent parasitic oscillation, it may be necessary to insert a low value (i.e., 0.24Ω) resistor between the output of the amplifier and the A/D input.

Reference Input

The range of the A/D is set by the voltage between V_{RT} and V_{RB}. The internal bias generator will set V_{RTS} to 2.6V and V_{RBS} to 0.6V. These can be used as the part reference by shorting V_{RT} and V_{RTS} and V_{RB} to V_{RBS}. The analog input range of the A/D will now be from 0.6V to 2.6V and is referred to as Self Bias Mode 1. Self Bias Mode 2 is where V_{RB} is connected to AGND and V_{RT} is shorted to V_{RTS}. The analog input range will now be from 0V to 2.4V.

Test Circuits

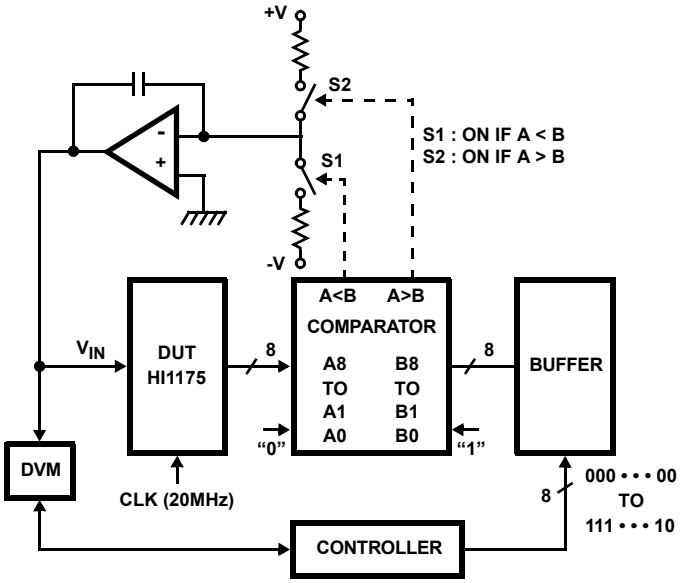


FIGURE 21. INTEGRAL AND DIFFERENTIAL NON-LINEARITY ERROR AND OFFSET VOLTAGE TEST CIRCUIT

Test Circuits (Continued)

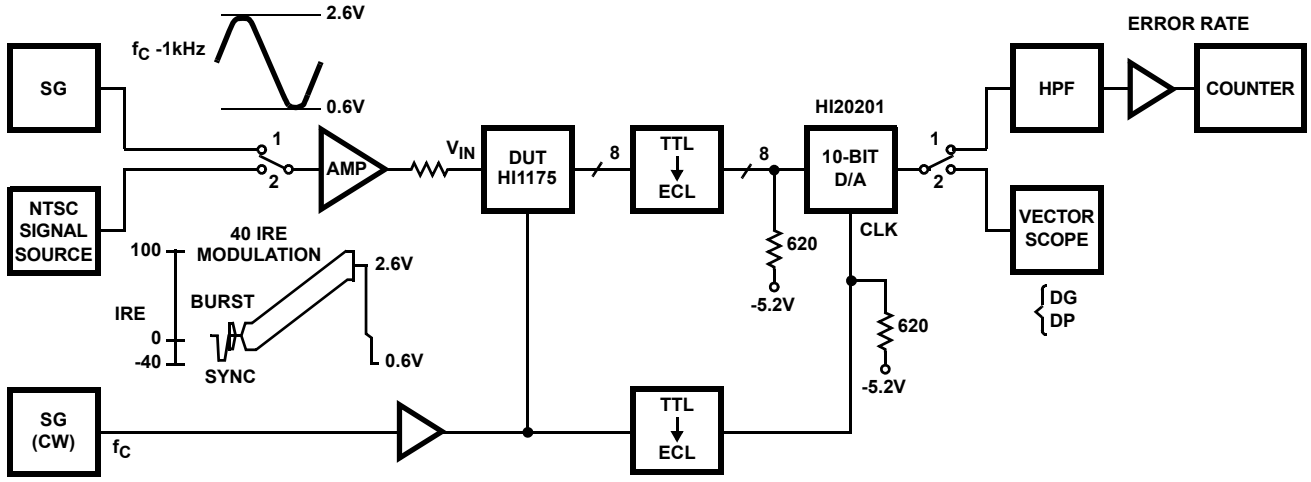


FIGURE 22. MAXIMUM OPERATIONAL SPEED AND DIFFERENTIAL GAIN AND PHASE ERROR TEST CIRCUIT

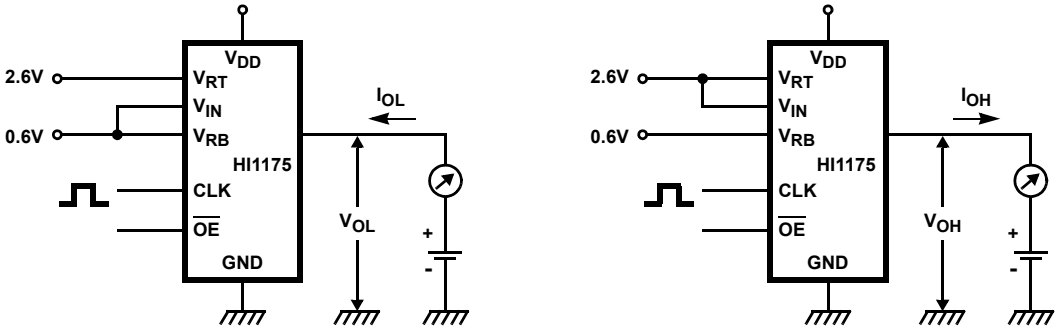
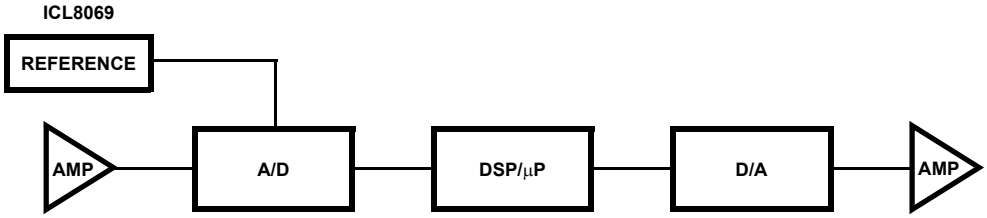


FIGURE 23. DIGITAL OUTPUT CURRENT TEST CIRCUIT



HA5020 (Single) HA5022(Dual) HA5024 (Quad) HA5013 (Triple)	HI1175 (8-Bit)	HSP9501 HSP48901 HSP43881 HSP43168	HI3338 (8-Bit) HI1171 (8-Bit)	HA5020 (Single)

HSP9501: Programmable Data Buffer
HSP48901: 3 x 3 Image Filter, 30MHz, 8-Bit
HSP43881: Digital Filter, 30MHz, 1-D and 2-D FIR Filters
HSP43168: Dual FIR Filter, 10-Bit, 33MHz/45MHz

CMOS Logic Available in HC, HCT, AC, ACT and FCT.

HA5013: Triple, 125MHz, I_{OUT} = 20mA
HA5020: Single, 100MHz, I_{OUT} = 30mA, Output Enable/Disable
HA5022: Dual, 125MHz, I_{OUT} = 20mA, Output Enable/Disable
HA5024: Quad, 125MHz, I_{OUT} = 20mA, Output Enable/Disable

FIGURE 24. 8-BIT SYSTEM COMPONENTS

Static Performance Definitions

Offset, full scale, and gain all use a measured value of the internal voltage reference to determine the ideal plus and minus full scale values. The results are all displayed in LSBs.

Offset Error (E_{OB})

The first code transition should occur at a level $^1/_2$ LSB above the bottom reference voltage. Offset is defined as the deviation of the actual code transition from this point. Note that this is adjustable to zero.

Full Scale Error (E_{OT})

The last code transition should occur for a analog input that is $1^1/_2$ LSBs below full scale. Full scale error is defined as the deviation of the actual code transition from this point.

Differential Linearity Error (DNL)

DNL is the worst case deviation of a code width from the ideal value of 1 LSB. The converter is guaranteed to have no missing codes.

Integral Linearity Error (INL)

INL is the worst case deviation of a code center from a best fit straight line calculated from the measured data.

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the HI1175. A low distortion sine wave is applied to the input, it is sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with a 1024 point FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is -0.5dB down from fullscale for all these tests. The distortion numbers are quoted in dBc (decibels with respect to carrier) and **DO NOT** include any correction factors for normalizing to fullscale.

Signal-to-Noise Ratio (SNR)

SNR is the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components except the fundamental and the first five harmonics.

Signal-to-Noise + Distortion Ratio (SINAD)

SINAD is the measured RMS signal to RMS sum of all other spectral components below the Nyquist frequency excluding DC.

Effective Number Of Bits (ENOB)

The effective number of bits (ENOB) is derived from the SINAD data. ENOB is calculated from:

$$ENOB = (SINAD - 1.76 + V_{CORR}) / 6.02,$$

where: $V_{CORR} = 0.5dB$.

Total Harmonic Distortion

This is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the measured input signal.

2nd and 3rd Harmonic Distortion

This is the ratio of the RMS value of the 2nd and 3rd harmonic component respectively to the RMS value of the measured input signal.

Spurious Free Dynamic Range (SFDR)

SFDR is the ratio of the fundamental RMS amplitude to the RMS amplitude of the next largest spur or spectral component. If the harmonics are buried in the noise floor it is the largest peak.

Full Power Input Bandwidth

Full power bandwidth is the frequency at which the amplitude of the digitally reconstructed output has decreased 3dB below the amplitude of the input sine wave. The input sine wave has a peak-to-peak amplitude equal to the reference voltage. The bandwidth given is measured at the specified sampling frequency.

Timing Definitions

Sampling Delay (t_{SD})

Sampling delay is the time delay between the external sample command (the falling edge of the clock) and the time at which the signal is actually sampled. This delay is due to internal clock path propagation delays.

Aperture Jitter (t_{AJ})

This is the RMS variation in the sampling delay due to variation of internal clock path delays.

Data Latency (t_{LAT})

After the analog sample is taken, the data on the bus is available after 2.5 cycles of the clock. This is due to the architecture of the converter where the data has to ripple through the stages. This delay is specified as the data latency. After the data latency time, the data representing each succeeding sample is output at the following clock pulse. The digital data lags the analog input by 2.5 cycles.

Output Data Delay (t_D)

Output Data Delay is the delay time from when the data is valid (rising clock edge) to when it shows up at the output bus. This is due to internal delays at the digital output.