July 2004 FN3607.6

Dual 350MHz, Low Power Closed Loop Buffer Amplifier

The HFA1212 is a dual closed loop Buffer featuring user programmable gain and high speed performance. Manufactured on Intersil's proprietary complementary bipolar UHF-1 process, these devices offer wide -3dB bandwidth of 350MHz, very fast slew rate, excellent gain flatness and high output current.

A unique feature of the pinout allows the user to select a voltage gain of +1, -1, or +2, without the use of any external components. Gain selection is accomplished via connections to the inputs, as described in the "Application Information" section. The result is a more flexible product, fewer part types in inventory, and more efficient use of board space.

Compatibility with existing op amp pinouts provides flexibility to upgrade low gain amplifiers, while decreasing component count. Unlike most buffers, the standard pinout provides an upgrade path should a higher closed loop gain be needed at a future date.

Part # Information

PART NUMBER (BRAND)	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
HFA1212IB (H1212I)	-40 to 85	8 Ld SOIC	M8.15

Features

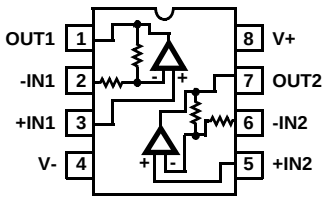
- Differential Gain 0.025%
- Differential Phase . . . . . 0.03 Degrees
- Wide -3dB Bandwidth (A_V = +2) 350MHz
- Very Fast Slew Rate (A_V = -1) 1100V/µs
- Low Supply Current 6mA/Buffer
- High Output Current 60mA
- Excellent Gain Accuracy 0.99V/V
- User Programmable For Closed-Loop Gains of +1, -1 or +2 Without Use of External Resistors
- Overdrive Recovery 8ns
- Standard Operational Amplifier Pinout

Applications

- High Resolution Monitors
- Professional Video Processing
- Medical Imaging
- Video Digitizing Boards/Systems
- RF/IF Processors
- Battery Powered Communications
- Flash Converter Drivers
- High Speed Pulse Amplifiers

Pinout

HFA1212 (SOIC)
TOP VIEW



Absolute Maximum Rating

Supply Voltage (V+ to V-) 11V
DC Input Voltage . . . . . V_{SUPPLY}
Output Current (Note 1) . . . . . .Short Circuit Protected
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) 600V

Operating Conditions

Temperature Range . . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)
SOIC Package	160

Maximum Junction Temperature (Die) . . . . . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Output is protected for short circuits to ground. Brief short circuits to ground will not degrade reliability, however, continuous (100% duty cycle) output current should not exceed 30mA for maximum reliability.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_L = 100\Omega$, Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP (^oC)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Output Offset Voltage		A	25	-	2	10	mV
		A	Full	-	3	15	mV
Average Output Offset Voltage Drift		B	Full	-	22	70	$\mu V/^oC$
Channel-to-Channel Output Offset Voltage Mismatch		A	25	-	-	15	mV
		A	Full	-	-	30	mV
Common-Mode Rejection Ratio	$\Delta V_{CM} = \pm1.8V$	A	25	42	45	-	dB
	$\Delta V_{CM} = \pm1.8V$	A	85	40	44	-	dB
	$\Delta V_{CM} = \pm1.2V$	A	-40	40	45	-	dB
Power Supply Rejection Ratio	$\Delta V_{PS} = \pm1.8V$	A	25	45	49	-	dB
	$\Delta V_{PS} = \pm1.8V$	A	85	43	48	-	dB
	$\Delta V_{PS} = \pm1.2V$	A	-40	43	48	-	dB
Input Bias Current		A	25	-	1	15	μA
		A	Full	-	3	25	μA
Input Bias Current Drift		B	Full	-	30	80	$nA/^oC$
Channel-to-Channel Input Bias Current Mismatch		A	25	-	-	15	μA
		A	Full	-	-	25	μA
Input Bias Current Power Supply Sensitivity	$\Delta V_{PS} = \pm1.25V$	A	25	-	0.5	1	$\mu A/V$
		A	Full	-	-	3	$\mu A/V$
Input Resistance	$\Delta V_{CM} = \pm1.8V$	A	25	0.8	1.1	-	$M\Omega$
	$\Delta V_{CM} = \pm1.8V$	A	85	0.5	1.4	-	$M\Omega$
	$\Delta V_{CM} = \pm1.2V$	A	-40	0.5	1.3	-	$M\Omega$
Inverting Input Resistance		C	25	-	350	-	Ω
Input Capacitance		C	25	-	2	-	pF
Input Voltage Common Mode Range (Implied by V_{IO} CMRR and $+R_{IN}$ tests)		A	25, 85	±1.8	±2.4	-	V
		A	-40	±1.2	±1.7	-	V
Input Noise Voltage Density (Note 4)	f = 100kHz	B	25	-	7	-	$nV/\sqrt{Hz}$
Input Noise Current Density (Note 4)	f = 100kHz	B	25	-	3.6	-	$pA/\sqrt{Hz}$

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_L = 100Ω, Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP (°C)	MIN	TYP	MAX	UNITS
TRANSFER CHARACTERISTICS							
Gain (V_{IN} = -1V to +1V)	A_V = -1	A	25	-0.98	0.996	-1.02	V/V
		A	Full	0.975	1.000	-1.025	V/V
	A_V = +1	A	25	0.98	0.992	1.02	V/V
		A	Full	0.975	0.993	1.025	V/V
	A_V = +2	A	25	1.96	1.988	2.04	V/V
		A	Full	1.95	1.990	2.05	V/V
Channel-to-Channel Gain Mismatch	A_V = -1	A	25	-	-	±0.02	V/V
		A	Full	-	-	±0.025	V/V
	A_V = +1	A	25	-	-	±0.025	V/V
		A	Full	-	-	±0.025	V/V
	A_V = +2	A	25	-	-	±0.04	V/V
		A	Full	-	-	±0.05	V/V
AC CHARACTERISTICS							
-3dB Bandwidth (V_{OUT} = 0.2V_{P-P}, Note 4)	A_V = -1	B	25	-	300	-	MHz
	A_V = +1, +R_S = 620Ω	B	25	-	240	-	MHz
	A_V = +2	B	25	-	350	-	MHz
Full Power Bandwidth (V_{OUT} = 5V_{P-P} at A_V = +2 or -1, V_{OUT} = 4V_{P-P} at A_V = +1, Note 4)	A_V = -1	B	25	-	165	-	MHz
	A_V = +1, +R_S = 620Ω	B	25	-	150	-	MHz
	A_V = +2	B	25	-	125	-	MHz
Gain Flatness (V_{OUT} = 0.2V_{P-P}, Note 4)	A_V = +2, To 25MHz	B	25	-	±0.03	-	dB
	A_V = +2, To 50MHz	B	25	-	±0.04	-	dB
Crosstalk (All Channels Hostile, Note 4)	5MHz	B	25	-	-65	-	dB
	10MHz	B	25	-	-60	-	dB
OUTPUT CHARACTERISTICS							
Output Voltage Swing (Note 4)	A_V = -1	A	25	±3.0	±3.2	-	V
		A	Full	±2.8	±3.0	-	V
Output Current (Note 4)	A_V = -1, R_L = 50Ω	A	25, 85	50	55	-	mA
		A	-40	28	42	-	mA
Output Short Circuit Current		B	25	-	100	-	mA
DC Closed Loop Output Impedance	A_V = +2	B	25	-	0.2	-	Ω
Second Harmonic Distortion (A_V = +2, V_{OUT} = 2V_{P-P}, Note 4)	10MHz	B	25	-	-60	-	dBc
	20MHz	B	25	-	-50	-	dBc
Third Harmonic Distortion (A_V = +2, V_{OUT} = 2V_{P-P}, Note 4)	10MHz	B	25	-	-60	-	dBc
	20MHz	B	25	-	-50	-	dBc
Reverse Isolation (S_{12}, Note 4)	30MHz, A_V = +2	B	25	-	-65	-	dB
TRANSIENT RESPONSE A_V = +2, Unless Otherwise Specified							
Rise and Fall Times (V_{OUT} = 0.5V_{P-P})	Rise Time	B	25	-	1.0	-	ns
	Fall Time	B	25	-	1.1	-	ns

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_L = 100Ω, Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS		(NOTE 3) TEST LEVEL	TEMP (^oC)	MIN	TYP	MAX	UNITS
Overshoot (V_{OUT} = 0.5V_{P-P}, V_{IN} t_{RISE} = 1ns, Note 5)	+OS		B	25	-	4	-	%
	-OS		B	25	-	13	-	%
Slew Rate (V_{OUT} = 5V_{P-P} at A_V = +2 or -1, V_{OUT} = 4V_{P-P} at A_V = +1)	A_V = -1	+SR	B	25	-	2000	-	V/µs
		-SR	B	25	-	1150	-	V/µs
	A_V = +1, +R_S = 620Ω	+SR	B	25	-	1100	-	V/µs
		-SR	B	25	-	850	-	V/µs
	A_V = +2	+SR	B	25	-	1300	-	V/µs
		-SR	B	25	-	900	-	V/µs
Settling Time (V_{OUT} = +2V to 0V Step, Note 4)	To 0.1%		B	25	-	24	-	ns
	To 0.05%		B	25	-	37	-	ns
	To 0.02%		B	25	-	60	-	ns
Overdrive Recovery Time	V_{IN} = ±2V		B	25	-	8.5	-	ns
VIDEO CHARACTERISTICS								
Differential Gain (f = 3.58MHz, A_V = +2)	R_L = 150Ω		B	25	-	0.025	-	%
Differential Phase (f = 3.58MHz, A_V = +2)	R_L = 150Ω		B	25	-	0.03	-	Degrees
POWER SUPPLY CHARACTERISTICS								
Power Supply Range			C	25	±4.5	-	±5.5	V
Power Supply Current			A	25	-	5.9	6.1	mA/Op Amp
			A	Full	-	6.1	6.3	mA/Op Amp

NOTE:

3. Test Level: A. Production Tested; B. Typical or Guaranteed Limit Based on Characterization; C. Design Typical for Information Only.
4. See Typical Performance Curves for more information.
5. Negative overshoot dominates for output signal swings below GND (e.g. 0.5V_{P-P}), yielding a higher overshoot limit compared to the V_{OUT} = 0V to 0.5V condition. See the “Application Information” section for details.

Application Information

HFA1212 Advantages

The HFA1212 features a novel design which allows the user to select from three closed loop gains, without any external components. The result is a more flexible product, fewer part types in inventory, and more efficient use of board space. Implementing a dual, gain of 2, cable driver with this IC eliminates the four gain setting resistors, which frees up board space for termination resistors.

Like most newer high performance amplifiers, the HFA1212 is a current feedback amplifier (CFA). CFAs offer high bandwidth and slew rate at low supply currents, but can be difficult to use because of their sensitivity to feedback capacitance and parasitics on the inverting input (summing node). The HFA1212 eliminates these concerns by bringing the gain setting resistors on-chip. This yields the optimum placement and value of the feedback resistor, while minimizing feedback and summing node parasitics. Because there is no access to the summing node, the PCB parasitics do not impact performance at gains of +2 or -1 (see “Unity Gain Considerations” for discussion of parasitic impact on unity gain performance).

The HFA1212’s closed loop gain implementation provides better gain accuracy, lower offset and output impedance, and better distortion compared with open loop buffers.

Closed Loop Gain Selection

This “buffer” operates in closed loop gains of -1, +1, or +2, with gain selection accomplished via connections to the ±inputs. Applying the input signal to +IN and floating -IN selects a gain of +1 (see next section for layout caveats), while grounding -IN selects a gain of +2. A gain of -1 is obtained by applying the input signal to -IN with +IN grounded through a 50Ω resistor.

The table below summarizes these connections:

GAIN (A_{CL})	CONNECTIONS	
	+INPUT	-INPUT
-1	50Ω to GND	Input
+1	Input	NC (Floating)
+2	Input	GND

Unity Gain Considerations

Unity gain selection is accomplished by floating the -Input of the HFA1212. Anything that tends to short the -Input to GND, such as stray capacitance at high frequencies, will cause the amplifier gain to increase toward a gain of +2. The result is excessive high frequency peaking, and possible instability. Even the minimal amount of capacitance associated with attaching the -Input lead to the PCB results in approximately 6dB of gain peaking. At a minimum this requires due care to ensure the minimum capacitance at the -Input connection.

Table 1 lists five alternate methods for configuring the HFA1212 as a unity gain buffer, and the corresponding performance. The implementations vary in complexity and involve performance trade-offs. The easiest approach to implement is simply shorting the two input pins together, and applying the input signal to this common node. The amplifier bandwidth decreases from 430MHz to 280MHz, but excellent gain flatness is the benefit. A drawback to this approach is that the amplifier input noise voltage and input offset voltage terms see a gain of +2, resulting in higher noise and output offset voltages. Alternately, a 100pF capacitor between the inputs shorts them only at high frequencies, which prevents the increased output offset voltage but delivers less gain flatness.

Another straightforward approach is to add a 620W resistor in series with the amplifier's positive input. This resistor and the HFA1212 input capacitance form a low pass filter which rolls off the signal bandwidth before gain peaking occurs. This configuration was employed to obtain the data sheet AC and transient parameters for a gain of +1.

Pulse Overshoot

The HFA1212 utilizes a quasi-complementary output stage to achieve high output current while minimizing quiescent supply current. In this approach, a composite device replaces the traditional PNP pulldown transistor. The composite device switches modes after crossing 0V, resulting in added distortion for signals swinging below ground, and an increased overshoot on the negative portion of the output waveform (see Figure 6, Figure 9, and Figure 12). This overshoot isn't present for small bipolar signals (see Figure 4, Figure 7, and Figure 10) or large positive signals (see Figure 5, Figure 8 and Figure 11).

PC Board Layout

This amplifier's frequency response depends greatly on the care taken in designing the PC board (PCB). **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10μF) tantalum in parallel with a small value (0.1μF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance directly on the output must be minimized, or isolated as discussed in the next section.

An example of a good high frequency layout is the Evaluation Board shown in Figure 3.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the R_S and C_L combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 350MHz. By decreasing R_S as C_L increases (as illustrated in the curves), the maximum bandwidth is obtained without sacrificing stability. In spite of this, bandwidth decreases as the load capacitance increases.

TABLE 1. UNITY GAIN PERFORMANCE FOR VARIOUS IMPLEMENTATIONS

APPROACH	PEAKING (dB)	BW (MHz)	±0.1dB GAIN FLATNESS (MHz)
Remove -IN Pin	4.5	430	21
$+R_S = 620\Omega$	0	220	27
$+R_S = 620\Omega$ and Remove -IN Pin	0.5	215	15
Short +IN to -IN (e.g., Pins 2 and 3)	0.6	280	70
100pF Capacitor Between +IN and -IN	0.7	290	40

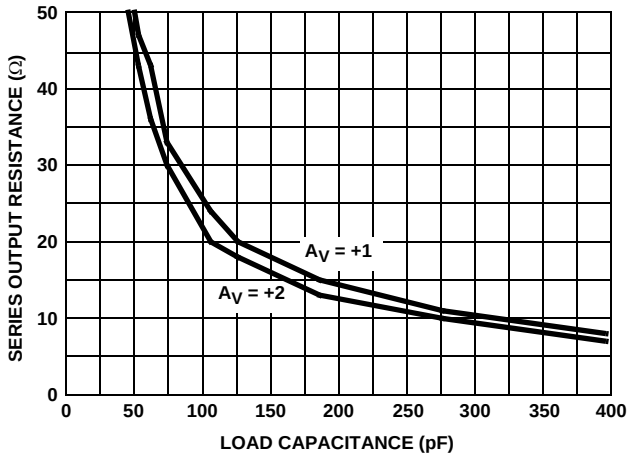


FIGURE 1. RECOMMENDED SERIES RESISTOR vs LOAD CAPACITANCE

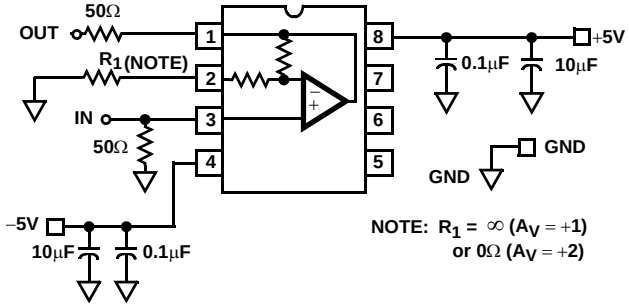


FIGURE 2. MODIFIED EVALUATION BOARD SCHEMATIC

Evaluation Board

The performance of the HFA1212 may be evaluated using the HA5023 Evaluation Board, slightly modified as follows:

1. Remove the two feedback resistors, and leave the connections open.
2. a. For A_V = +1 evaluation, remove the gain setting resistors (R_1), and leave pins 2 and 6 floating.
   b. For A_V = +2, replace the gain setting resistors (R_1) with 0Ω resistors to GND.
3. Replace the 0Ω series output resistors with 50Ω.

The modified schematic for amplifier 1, and the board layout are shown in Figures 2 and 3.

NOTE: Note: The SOIC version may be evaluated in the DIP board by using a SOIC-to-DIP adapter such as Aries Electronics Part Number 08-350000-10.

To order evaluation boards (part number HA5023EVAL), please contact your local sales office.

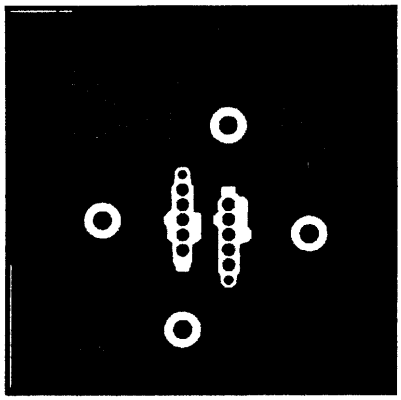


FIGURE 3B. BOTTOM LAYOUT

FIGURE 3. EVALUATION BOARD LAYOUT

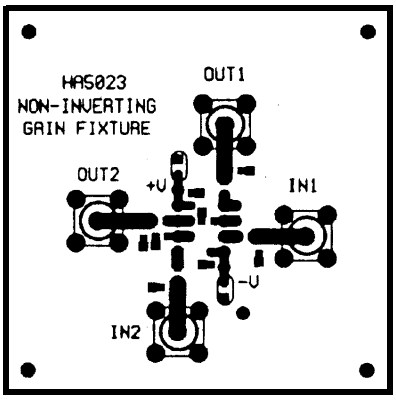


FIGURE 3A. TOP LAYOUT

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified

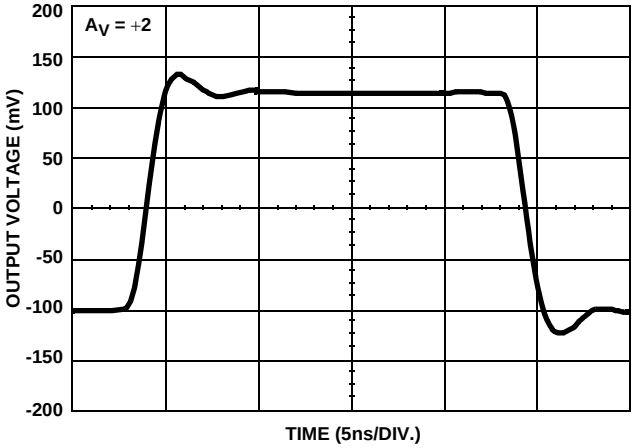


FIGURE 4. SMALL SIGNAL PULSE RESPONSE

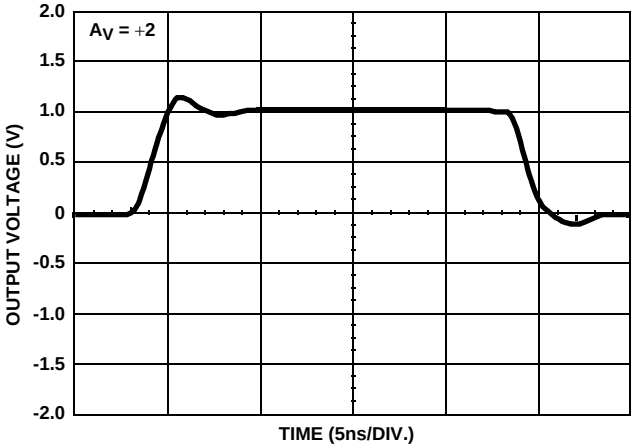


FIGURE 5. LARGE SIGNAL POSITIVE PULSE RESPONSE

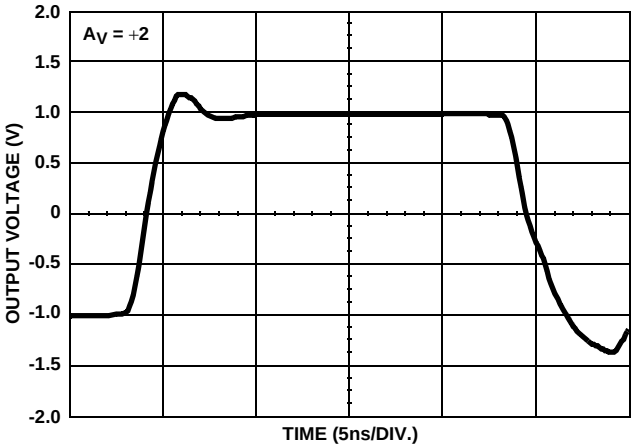


FIGURE 6. LARGE SIGNAL BIPOLAR PULSE RESPONSE

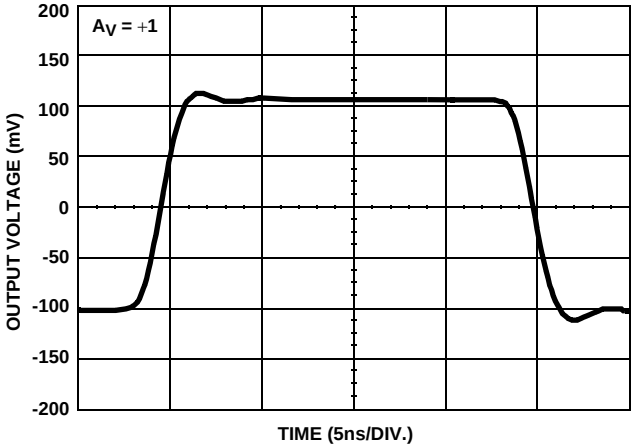


FIGURE 7. SMALL SIGNAL PULSE RESPONSE

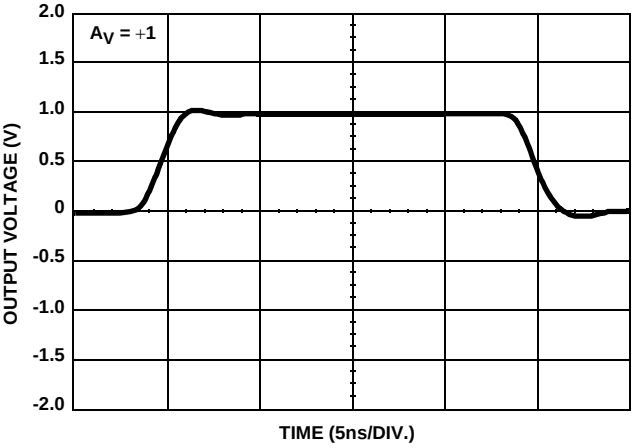


FIGURE 8. LARGE SIGNAL POSITIVE PULSE RESPONSE

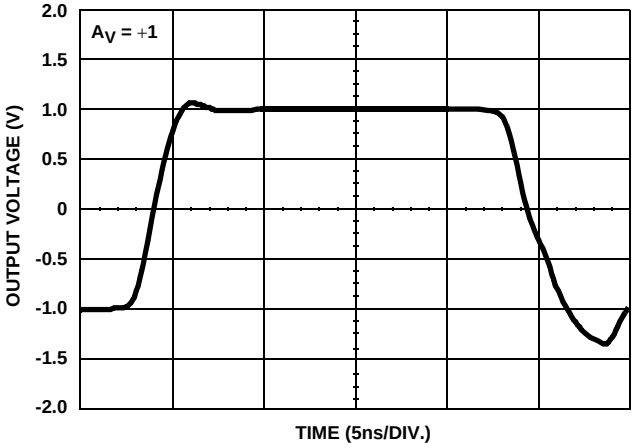


FIGURE 9. LARGE SIGNAL BIPOLAR PULSE RESPONSE

Typical Performance Curves (Continued) $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified

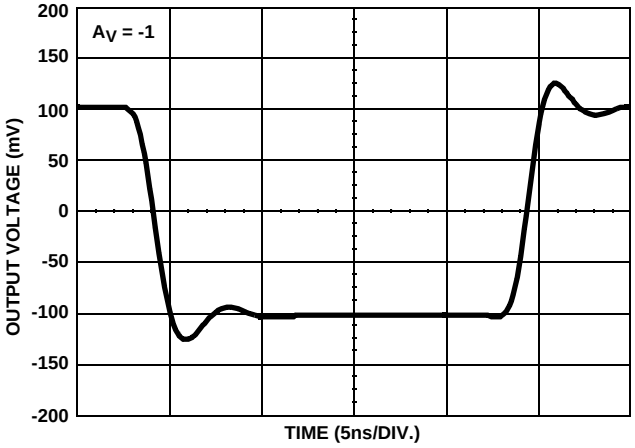


FIGURE 10. SMALL SIGNAL PULSE RESPONSE

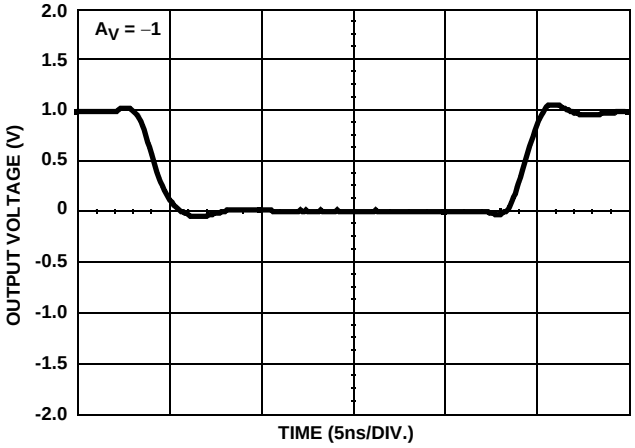


FIGURE 11. LARGE SIGNAL POSITIVE PULSE RESPONSE

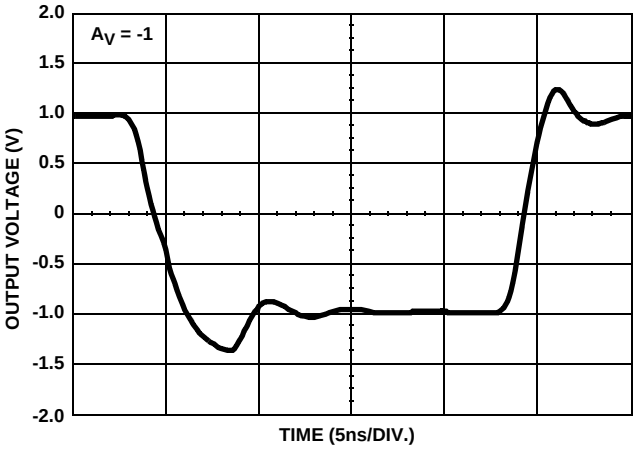


FIGURE 12. LARGE SIGNAL BIPOLAR PULSE RESPONSE

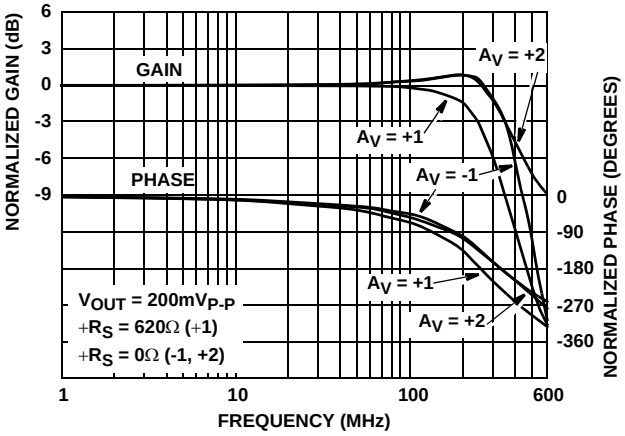


FIGURE 13. FREQUENCY RESPONSE

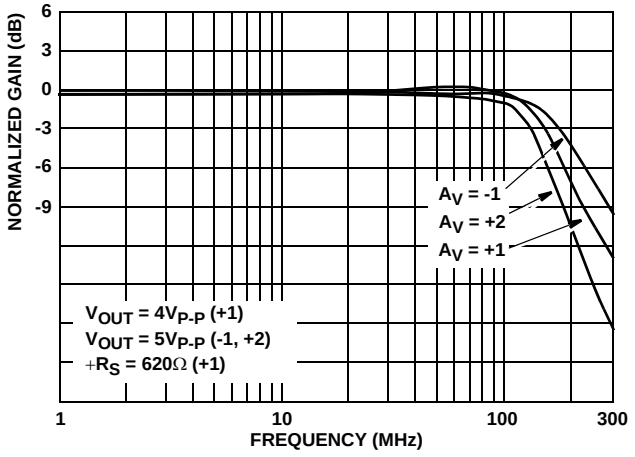


FIGURE 14. FULL POWER BANDWIDTH

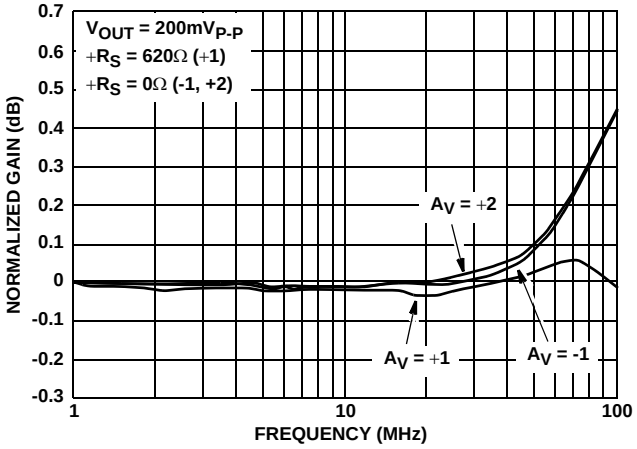


FIGURE 15. GAIN FLATNESS

Typical Performance Curves (Continued) $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified

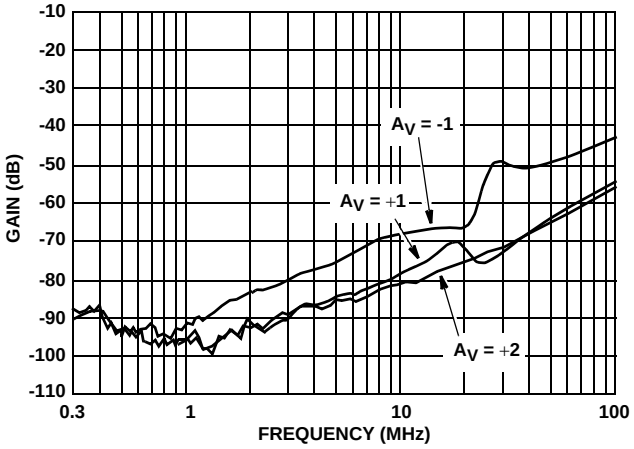


FIGURE 16. REVERSE ISOLATION

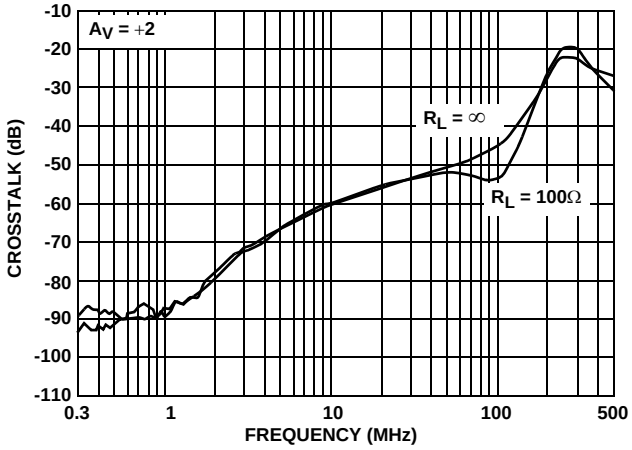


FIGURE 17. ALL HOSTILE CROSSTALK

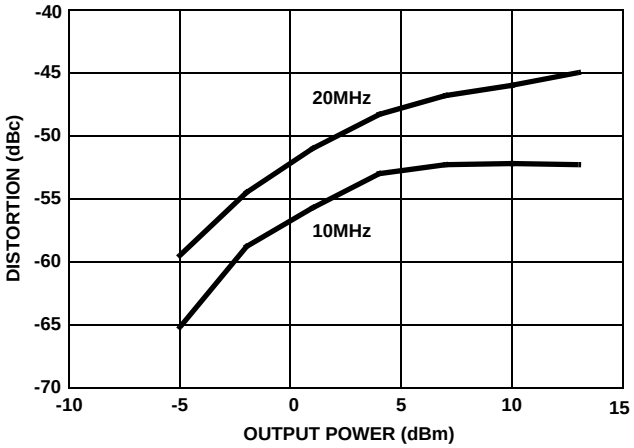


FIGURE 18. 2nd HARMONIC DISTORTION vs P_{OUT}

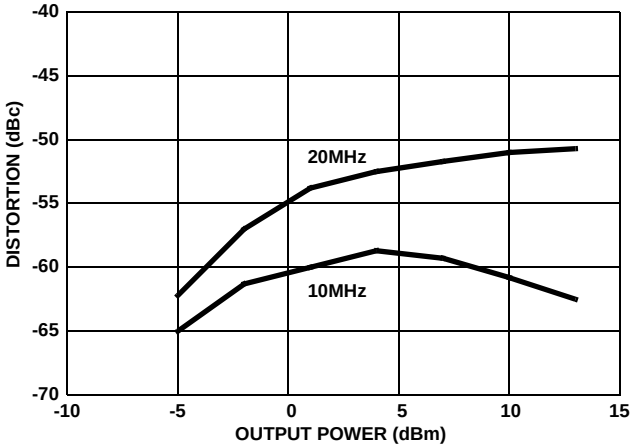


FIGURE 19. 3rd HARMONIC DISTORTION vs P_{OUT}

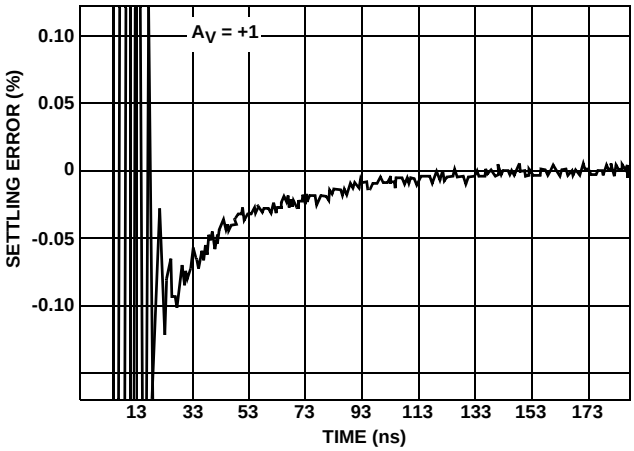


FIGURE 20. SETTLING RESPONSE

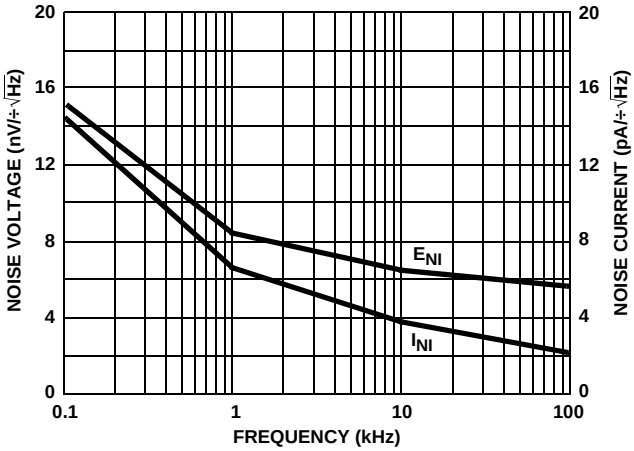


FIGURE 21. INPUT NOISE CHARACTERISTICS

Typical Performance Curves (Continued) $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified

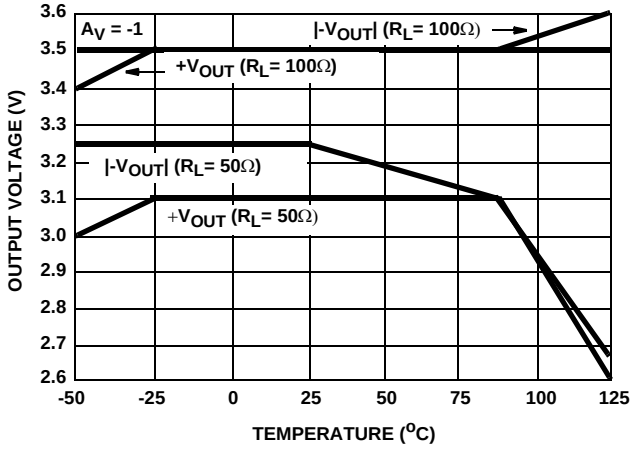


FIGURE 22. OUTPUT VOLTAGE vs TEMPERATURE

Die Characteristics

DIE DIMENSIONS:

69 mils x 92 mils x 19 mils
1750µm x 2330µm x 483µm

METALLIZATION:

Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ

Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

PASSIVATION:

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT:

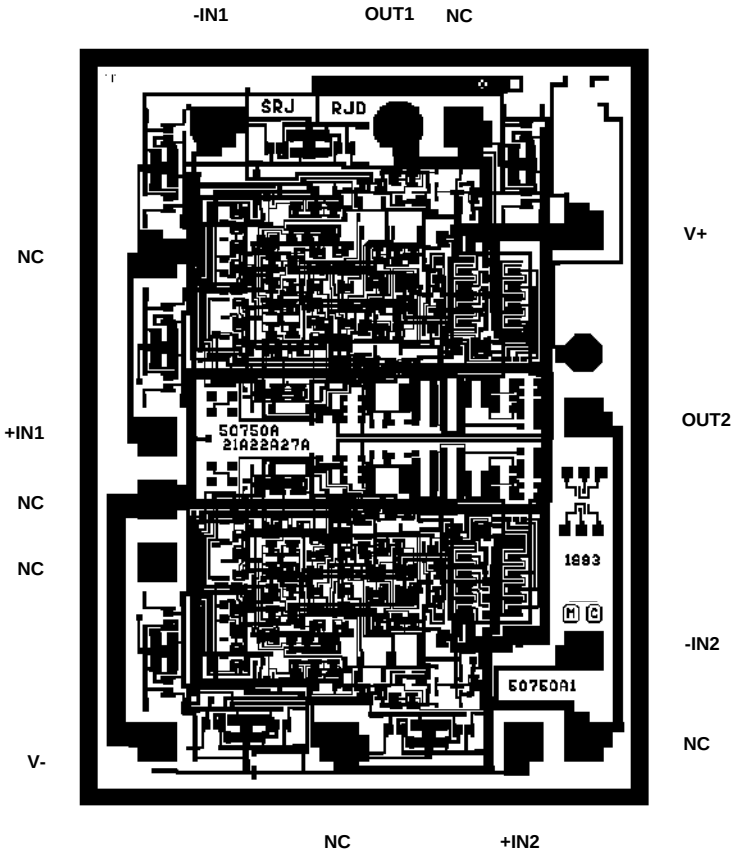
180

SUBSTRATE POTENTIAL (Powered Up):

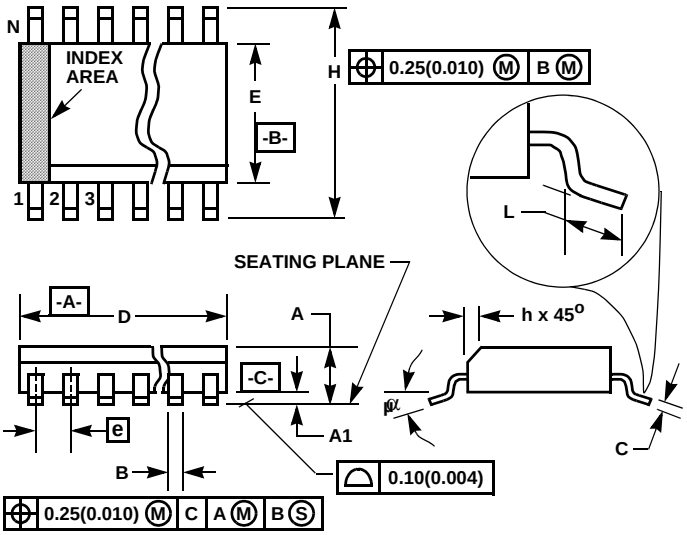
Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1212



Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0^o	8^o	0^o	8^o	-

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