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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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HD74LV2GT245A

Dual Bus Transceivers with 3-state Outputs / CMOS Logic Level Shifter

REJ03D0153-0200Z
(Previous ADE-205-694A (Z))
Rev.2.00
Oct.23.2003

Description

The HD74LV2GT245A has two buffers with three state output in a 8 pin package. When DIR is high, data is transferred from the A inputs to the B outputs, and when DIR is low, data is transferred from the B inputs to the A outputs. The A and B buses are separated by making the enable input (\overline{OE}) high level. The input protection circuitry on this device allows over voltage tolerance on the input, allowing the device to be used as a logic-level translator from 3.0 V CMOS Logic to 5.0 V CMOS Logic or from 1.8 V CMOS logic to 3.0 V CMOS Logic while operating at the high-voltage power supply. Low voltage and high-speed operation is suitable for the battery powered products (e.g., notebook computers), and the low power consumption extends the battery life.

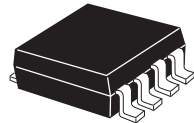
Features

- The basic gate function is lined up as Renesas uni logic series.
- Supplied on emboss taping for high-speed automatic mounting.
- TTL compatible input level.
Supply voltage range : 3.0 to 5.5 V
Operating temperature range : -40 to +85°C
- Logic-level translate function
3.0 V CMOS logic → 5.0 V CMOS logic (@V_{CC} = 5.0 V)
1.8 V or 2.5 V CMOS logic → 3.3 V CMOS logic (@V_{CC} = 3.3 V)
- All inputs V_{IH} (Max.) = 5.5 V (@V_{CC} = 0 V to 5.5 V)
All outputs V_O (Max.) = 5.5 V (@V_{CC} = 0 V, Output : Z)
- Output current ±6 mA (@V_{CC} = 3.0 V to 3.6 V), ±12 mA (@V_{CC} = 4.5 V to 5.5 V)
- All the logical input has hysteresis voltage for the slow transition.
- Ordering Information

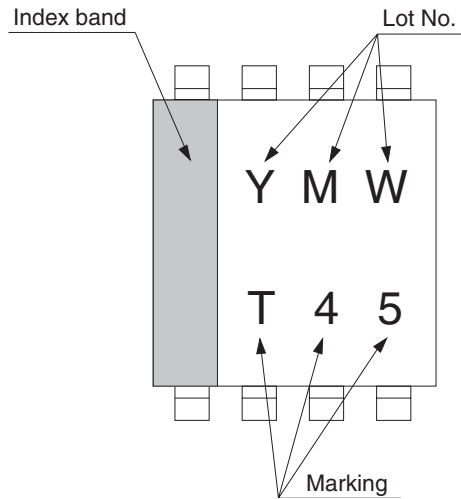
Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LV2GT245AUSE	SSOP-8 pin	TTP-8DBV	US	E (3,000 pcs/reel)

Outline and Article Indication

- HD74LV2GT245A



SSOP-8



Y : Year code
(the last digit of year)
M : Month code
W : Week code

Function Table

Inputs

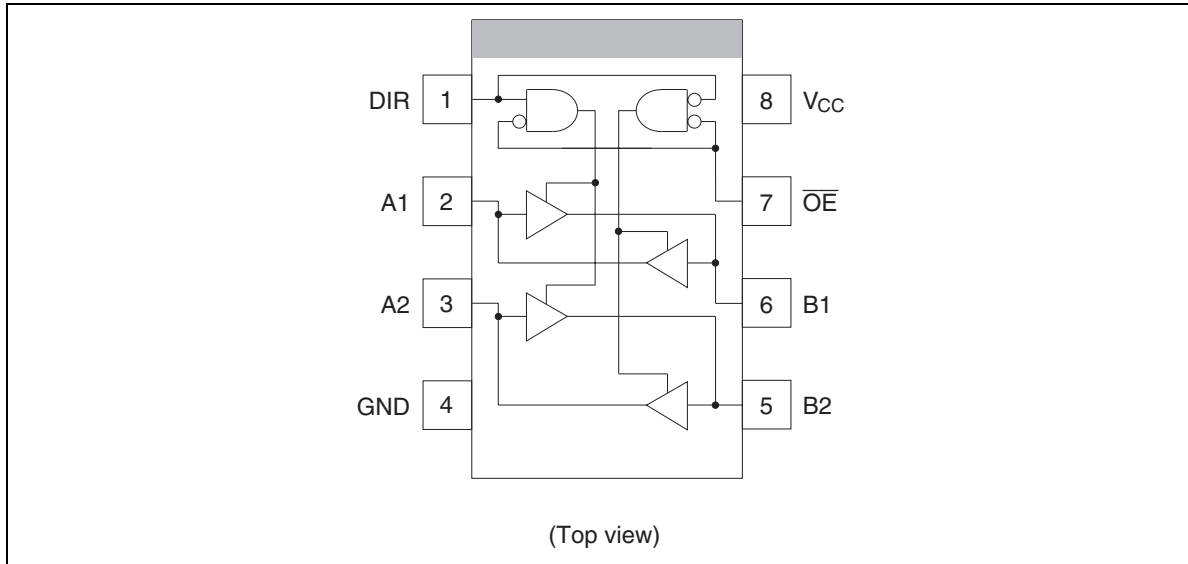
\overline{OE}	DIR	Operation
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H : High level

L : Low level

X : Immaterial

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Test Conditions
Supply voltage range	V_{CC}	-0.5 to 7.0	V	
Input voltage range ^{*1}	V_I	-0.5 to 7.0	V	
Output voltage range ^{*1, 2}	V_O	-0.5 to $V_{CC} + 0.5$	V	Output : H or L
		-0.5 to 7.0		V_{CC} : OFF or output : Z
Input clamp current	I_{IK}	-20	mA	$V_I < 0$
Output clamp current	I_{OK}	± 50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	± 25	mA	$V_O = 0$ to V_{CC}
Continuous current through V_{CC} or GND	I_{CC} or I_{GND}	± 50	mA	
Maximum power dissipation at $T_a = 25^\circ\text{C}$ (in still air) ^{*3}	P_T	200	mW	
Storage temperature	T_{stg}	-65 to 150	$^\circ\text{C}$	

- Notes:
- The absolute maximum ratings are values, which must not individually be exceeded, and furthermore no two of which may be realized at the same time.
 - 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 5.5 V maximum.
 - 3. The maximum package power dissipation was calculated using a junction temperature of 150°C .

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Test Conditions
Supply voltage	V_{CC}	3.0 to 5.5	V	
Input voltage	V_{IN}	0 to 5.5	V	
Output voltage	V_{OUT}	0 to V_{CC}	V	
		0 to 5.5		Output : Z
Operating temperature	T_{opr}	-40 to +85	°C	
Input rise / fall time	t_r, t_f	0 to 100 ($V_{CC} = 3.0$ to 3.6 V)	ns	
		0 to 20 ($V_{CC} = 4.5$ to 5.5 V)		

HD74LV2GT245A

Electrical Characteristics

- $T_a = -40$ to 85°C

Item	Symbol	V_{CC} (V) *	Min	Typ	Max	Unit	Test condition
Input voltage	V_{IH}	3.0 to 3.6	1.5	—	—	V	
		4.5 to 5.5	2.0	—	—		
	V_{IL}	3.0 to 3.6	—	—	0.6		
		4.5 to 5.5	—	—	0.8		
Hysteresis voltage	V_H	3.3	—	0.10	—	V	$V_T^+ - V_T^-$
		5.0	—	0.15	—		
Output voltage	V_{OH}	Min to Max	$V_{CC}-0.1$	—	—	V	$I_{OH} = -50\ \mu\text{A}$
		3.0	2.48	—	—		$I_{OH} = -6\ \text{mA}$
		4.5	3.8	—	—		$I_{OH} = -12\ \text{mA}$
	V_{OL}	Min to Max	—	—	0.1		$I_{OL} = 50\ \mu\text{A}$
		3.0	—	—	0.44		$I_{OL} = 6\ \text{mA}$
		4.5	—	—	0.55		$I_{OL} = 12\ \text{mA}$
Input current	I_{IN}	0 to 5.5	—	—	± 1	μA	$V_{IN} = 5.5\ \text{V}$ or GND
Off state output current	I_{OZ}	Min to Max	—	—	± 5	μA	$V_O = 5.5\ \text{V}$ or GND
Quiescent supply current	I_{CC}	5.5	—	—	10	μA	$V_{IN} = V_{CC}$ or GND, $I_O = 0$
	ΔI_{CC}	5.5	—	—	1.5	mA	One input $V_{IN} = 3.4\ \text{V}$, other input V_{CC} or GND
Output leakage current	I_{OFF}	0	—	—	5	μA	$V_O = 5.5\ \text{V}$
Input capacitance	C_{IN}	5.0	—	3.0	—	pF	$V_{IN} = V_{CC}$ or GND
Output capacitance	C_O	5.0	—	5.5	—	pF	$V_O = V_{CC}$ or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

- $V_{CC} = 3.3 \pm 0.3 \text{ V}$

Item	Symbol	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } 85^\circ\text{C}$		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t_{PLH}	—	6.0	8.5	1.0	10.0	ns	$C_L = 15 \text{ pF}$	A or B	B or A
	t_{PHL}	—	8.0	12.0	1.0	13.5		$C_L = 50 \text{ pF}$		
Enable time	t_{ZH}	—	8.0	13.5	1.0	15.5	ns	$C_L = 15 \text{ pF}$	\overline{OE}	A or B
	t_{ZL}	—	10.0	17.0	1.0	19.0		$C_L = 50 \text{ pF}$		
Disable time	t_{HZ}	—	9.5	16.5	1.0	19.5	ns	$C_L = 15 \text{ pF}$	\overline{OE}	A or B
	t_{LZ}	—	14.0	20.0	1.0	22.0		$C_L = 50 \text{ pF}$		

- $V_{CC} = 5.0 \pm 0.5 \text{ V}$

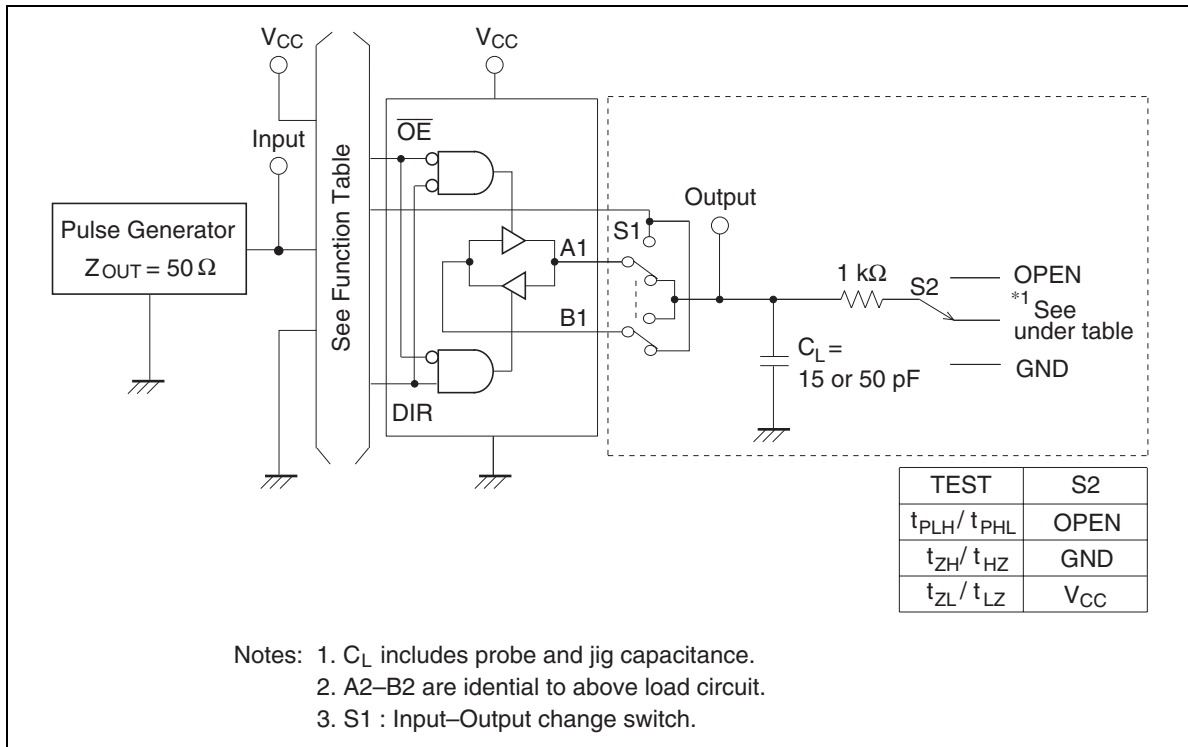
Item	Symbol	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } 85^\circ\text{C}$		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t_{PLH}	—	4.3	5.5	1.0	6.5	ns	$C_L = 15 \text{ pF}$	A or B	B or A
	t_{PHL}	—	5.6	7.5	1.0	8.5		$C_L = 50 \text{ pF}$		
Enable time	t_{ZH}	—	5.7	8.5	1.0	10.0	ns	$C_L = 15 \text{ pF}$	\overline{OE}	A or B
	t_{ZL}	—	7.0	10.6	1.0	12.0		$C_L = 50 \text{ pF}$		
Disable time	t_{HZ}	—	7.8	12.8	1.0	14.2	ns	$C_L = 15 \text{ pF}$	\overline{OE}	A or B
	t_{LZ}	—	10.9	14.7	1.0	16.0		$C_L = 50 \text{ pF}$		

Operating Characteristics

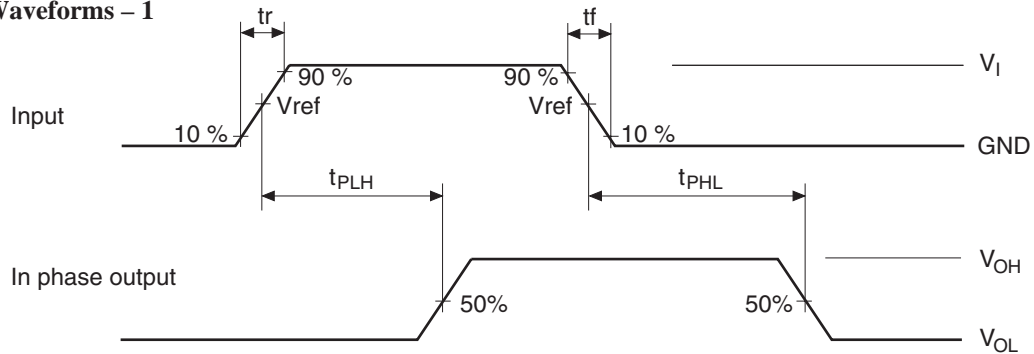
- $C_L = 50 \text{ pF}$

Item	Symbol	$V_{CC} \text{ (V)}$	$T_a = 25^\circ\text{C}$			Unit	Test Conditions
			Min	Typ	Max		
Power dissipation capacitance	C_{PD}	5.0	—	25.0	—	pF	$f = 10 \text{ MHz}$

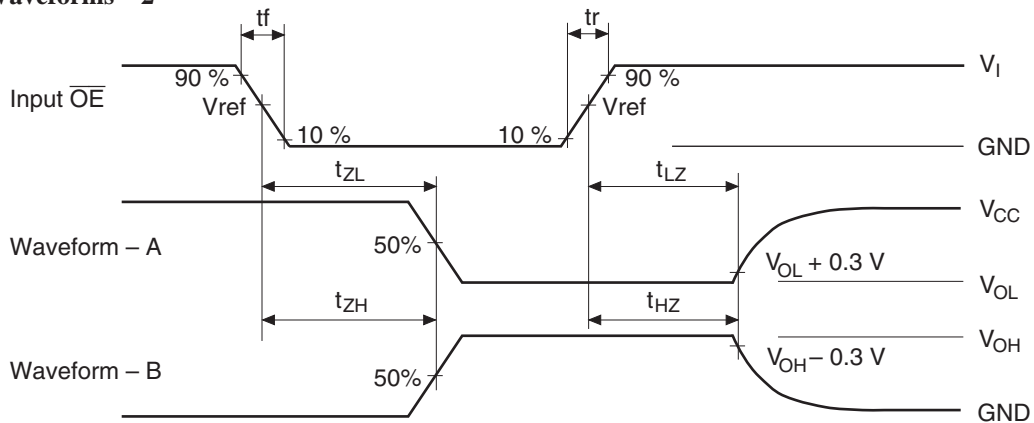
Test Circuit



• Waveforms – 1



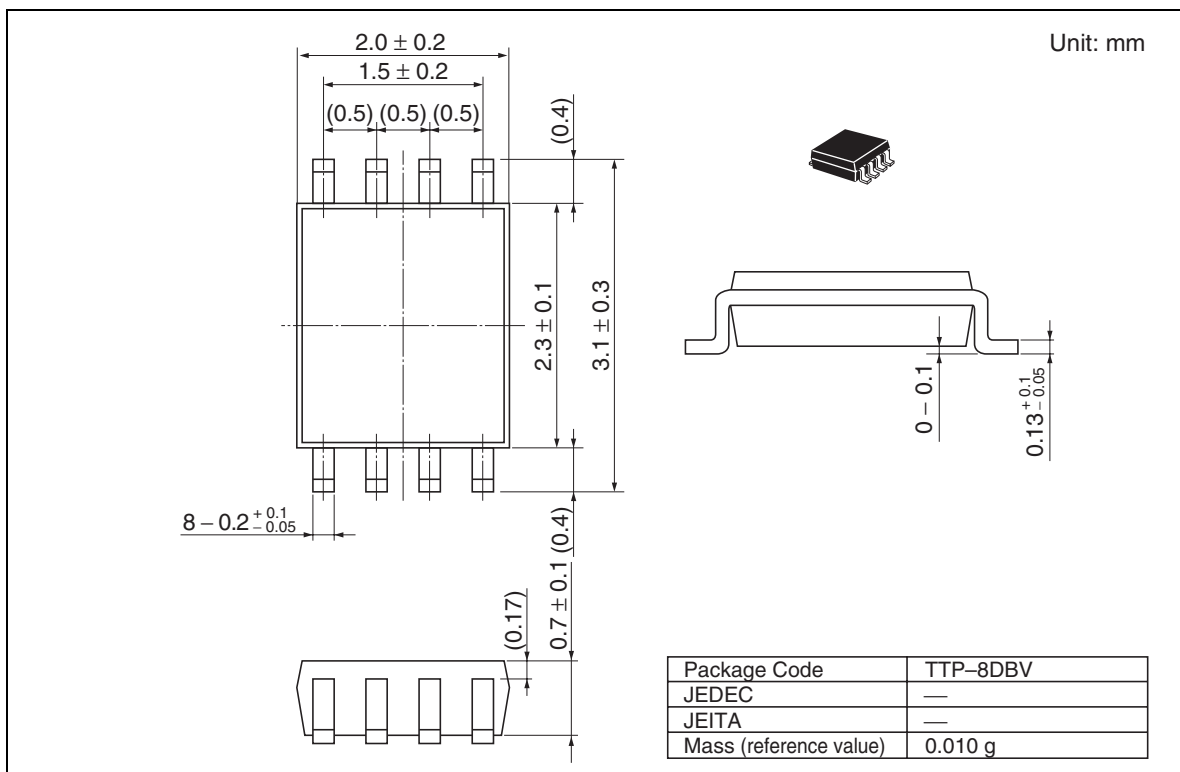
• Waveforms – 2



V_{CC} (V)	INPUTS		V_{ref}
	V_I	t_r / t_f	
3.3 ± 0.3	2.5 V	≤ 3.0 ns	50%
5.0 ± 0.5	3 V	≤ 3.0 ns	1.5 V

- Notes:
1. Input waveform : $PRR \leq 1$ MHz, $Z_o = 50 \Omega$.
 2. Waveform – A is for an output with internal conditions such that the output is low except when disabled by the output control.
 3. Waveform – B is for an output with internal conditions such that the output is high except when disabled by the output control.
 4. The output are measured one at a time with one transition per measurement.

Package Dimensions



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