

To our customers,

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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# HD74HC390

## Dual Decade Counters

REJ03D0624-0200  
 (Previous ADE-205-503)  
 Rev.2.00  
 Mar 30, 2006

### Description

The HD74HC390 incorporate dual decade counters, each composed of a divide-by-two and a divide-by-five counter. The divide-by-two and divide-by-five counters can be cascaded to form dual decade, dual bi-quinary, or various combinations up to a single divide-by-100 counter.

The HD74HC390 is incremented on the high to low transition (negative edge) of the clock input, and each has an independent clear input. When clear is set high all four bits of each counter are set to a low level. This enables count truncation and allows the implementation of divide-by-N counter configurations.

### Features

- High Speed Operation:  $t_{pd}$  (Clock A to  $Q_A$ ) = 11 ns typ ( $C_L = 50$  pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage:  $V_{CC} = 2$  to 6 V
- Low Input Current: 1  $\mu$ A max
- Low Quiescent Supply Current:  $I_{CC}$  (static) = 4  $\mu$ A max ( $T_a = 25^\circ\text{C}$ )
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HC390P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—
HD74HC390FPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)

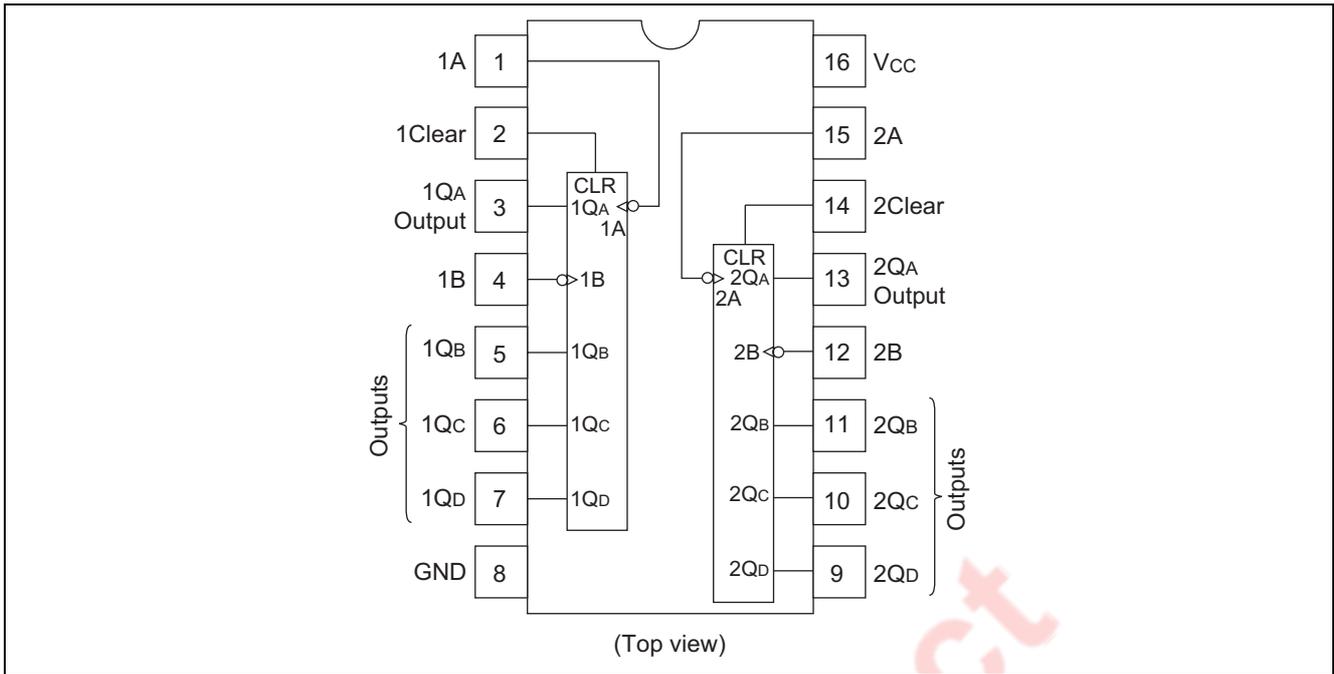
Note: Please consult the sales office for the above package availability.

### Function Table

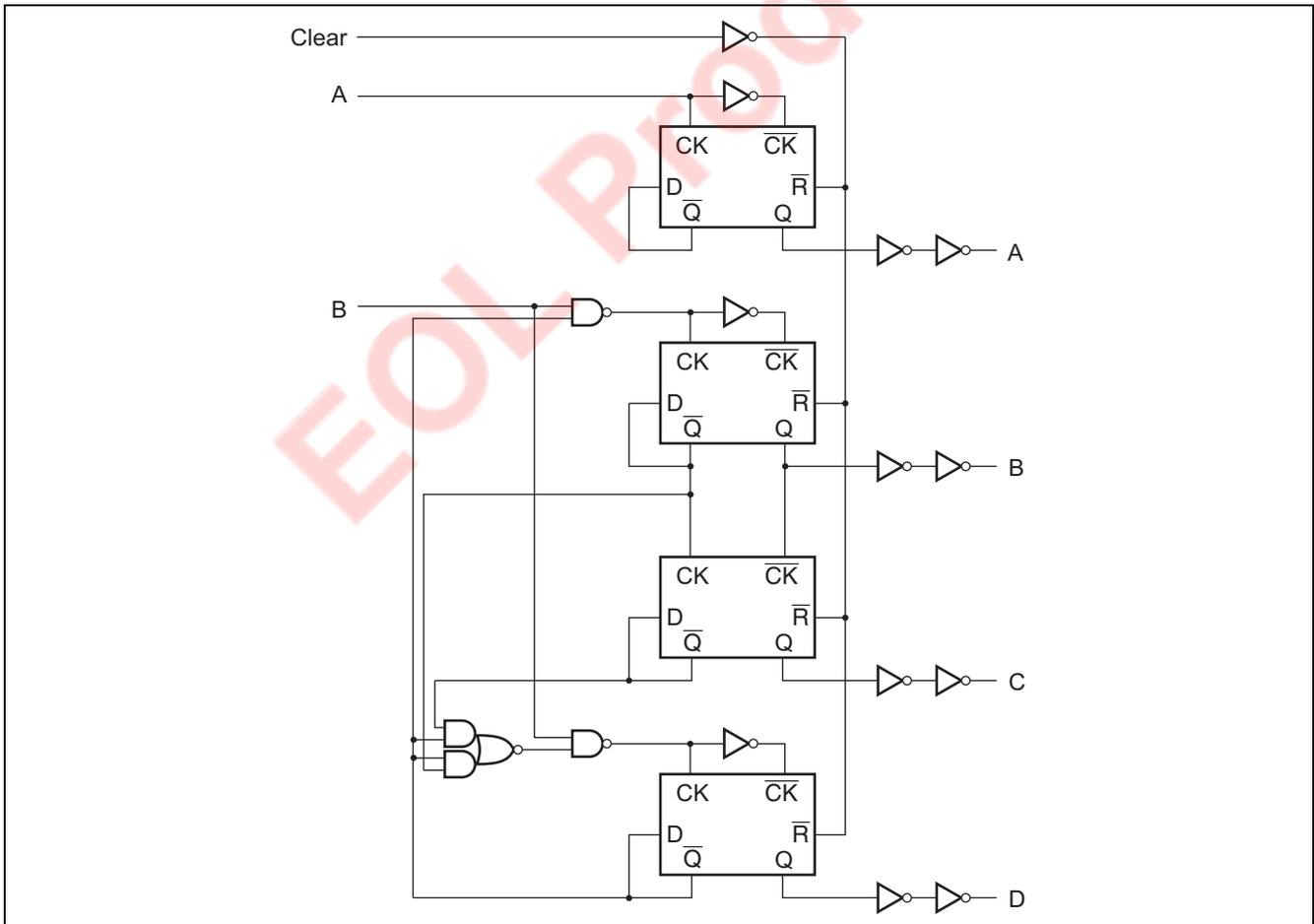
Clock		Clear	Operation
A	B		
X	X	H	Clear $\div 2$ and $\div 5$
$\overline{\text{X}}$	X	L	Increment $\div 2$
X	$\overline{\text{X}}$	L	Increment $\div 5$

Note: 1. H; High level, L; Low level, X; Irrelevant, Z; High impedance

Pin Arrangement



Logic Diagram



### Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V
Input / Output voltage	$V_{IN}, V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input / Output diode current	$I_{IK}, I_{OK}$	$\pm 20$	mA
Output current	$I_{OUT}$	$\pm 25$	mA
$V_{CC}$ , GND current	$I_{CC}$ or $I_{GND}$	$\pm 50$	mA
Power dissipation	$P_T$	500	mW
Storage temperature	$T_{stg}$	-65 to +150	°C

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

### Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{CC}$	2 to 6	V	
Input / Output voltage	$V_{IN}, V_{OUT}$	0 to $V_{CC}$	V	
Operating temperature	$T_a$	-40 to 85	°C	
Input rise / fall time <sup>*1</sup>	$t_r, t_f$	0 to 1000	ns	$V_{CC} = 2.0$ V
		0 to 500		$V_{CC} = 4.5$ V
		0 to 400		$V_{CC} = 6.0$ V

Note: 1. This item guarantees maximum limit when one input switches.

Waveform: Refer to test circuit of switching characteristics.

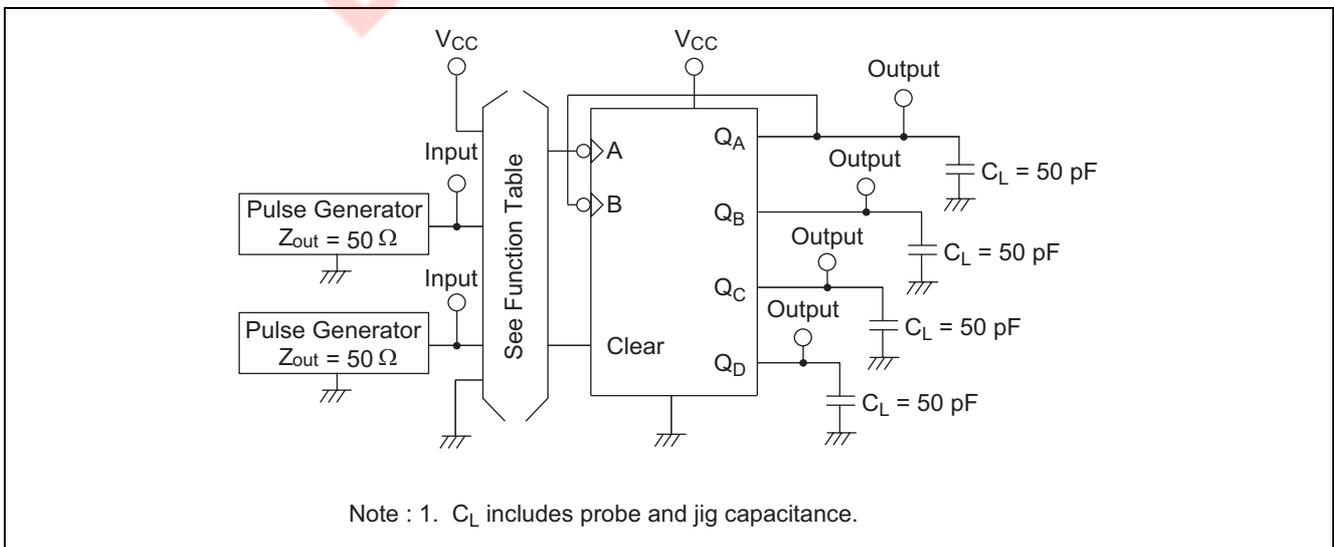
### Electrical Characteristics

Item	Symbol	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } +85^\circ\text{C}$		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	$V_{IH}$	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	$V_{IL}$	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	$V_{OH}$	2.0	1.9	2.0	—	1.9	—	V	$V_{in} = V_{IH}$ or $V_{IL}$	$I_{OH} = -20 \mu\text{A}$
		4.5	4.4	4.5	—	4.4	—			$I_{OH} = -4 \text{ mA}$
		6.0	5.9	6.0	—	5.9	—			$I_{OH} = -5.2 \text{ mA}$
		4.5	4.18	—	—	4.13	—			
		6.0	5.68	—	—	5.63	—			
	$V_{OL}$	2.0	—	0.0	0.1	—	0.1	V	$V_{in} = V_{IH}$ or $V_{IL}$	$I_{OL} = 20 \mu\text{A}$
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			$I_{OH} = 4 \text{ mA}$
		6.0	—	—	0.26	—	0.33			$I_{OH} = 5.2 \text{ mA}$
Input current	$I_{in}$	6.0	—	—	$\pm 0.1$	—	$\pm 1.0$	$\mu\text{A}$	$V_{in} = V_{CC}$ or GND	
Quiescent supply current	$I_{CC}$	6.0	—	—	4.0	—	40	$\mu\text{A}$	$V_{in} = V_{CC}$ or GND, $I_{out} = 0 \mu\text{A}$	

Switching Characteristics ( $C_L = 50 \text{ pF}$ , Input  $t_r = t_f = 6 \text{ ns}$ )

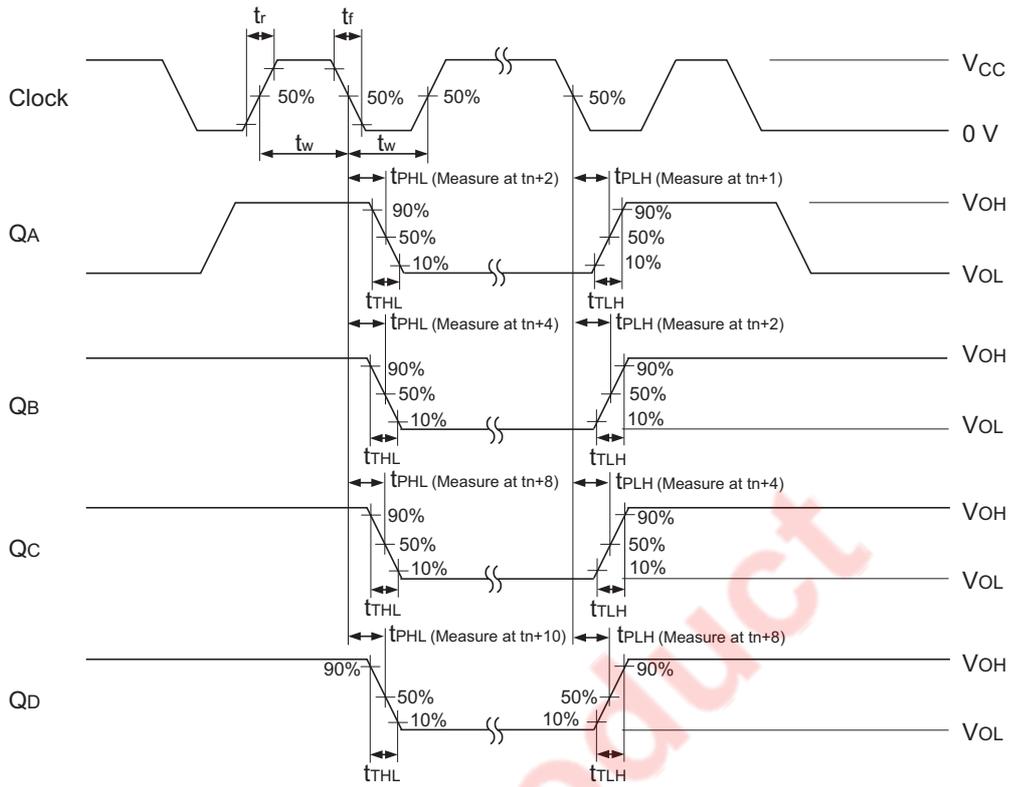
Item	Symbol	$V_{CC} \text{ (V)}$	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } +85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	$f_{max}$	2.0	—	—	5	—	4	MHz	
		4.5	—	—	27	—	21		
		6.0	—	—	32	—	25		
Propagation delay time	$t_{PLH}$	2.0	—	—	120	—	150	ns	Clock A to $Q_A$
		4.5	—	11	24	—	30		
		6.0	—	—	20	—	26		
	$t_{PHL}$	2.0	—	—	290	—	365	ns	Clock A to $Q_C$ ( $Q_A$ connected to Clock B)
		4.5	—	32	58	—	73		
		6.0	—	—	49	—	62		
	$t_{PLH}$	2.0	—	—	130	—	165	ns	Clock B to $Q_B$
		4.5	—	16	26	—	33		
		6.0	—	—	22	—	28		
	$t_{PHL}$	2.0	—	—	185	—	230	ns	Clock B to $Q_C$
		4.5	—	20	37	—	46		
		6.0	—	—	31	—	39		
	$t_{PLH}$	2.0	—	—	130	—	165	ns	Clock B to $Q_D$
		4.5	—	15	26	—	33		
		6.0	—	—	22	—	28		
$t_{PHL}$	2.0	—	—	165	—	205	ns	Clear to $Q_A, Q_B, Q_C, Q_D$	
	4.5	—	14	33	—	41			
	6.0	—	—	28	—	35			
Pulse width	$t_w$	2.0	80	—	—	100	—	ns	
		4.5	16	8	—	20	—		
		6.0	14	—	—	17	—		
Removal time	$t_h$	2.0	25	—	—	31	—	ns	
		4.5	5	1	—	6	—		
		6.0	4	—	—	5	—		
Output rise/fall time	$t_{TLH}$ $t_{THL}$	2.0	—	—	75	—	95	ns	
		4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	$C_{in}$	—	—	5	10	—	10	pF	

Test Circuit



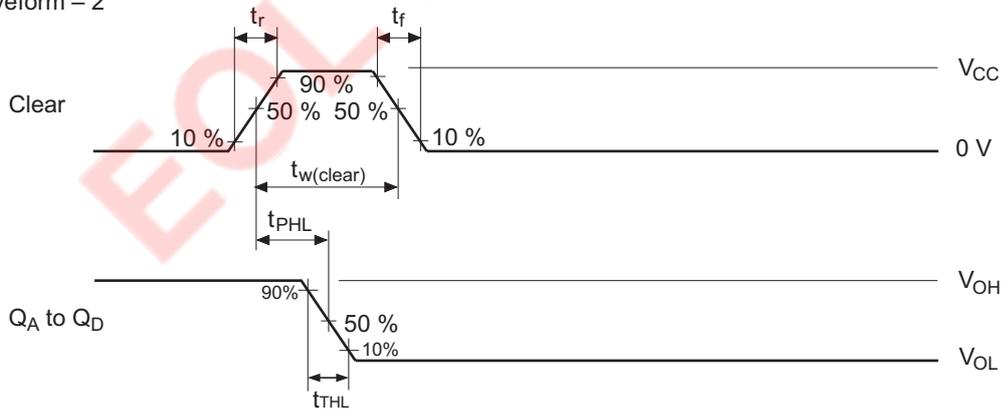
Waveforms

• Waveform – 1



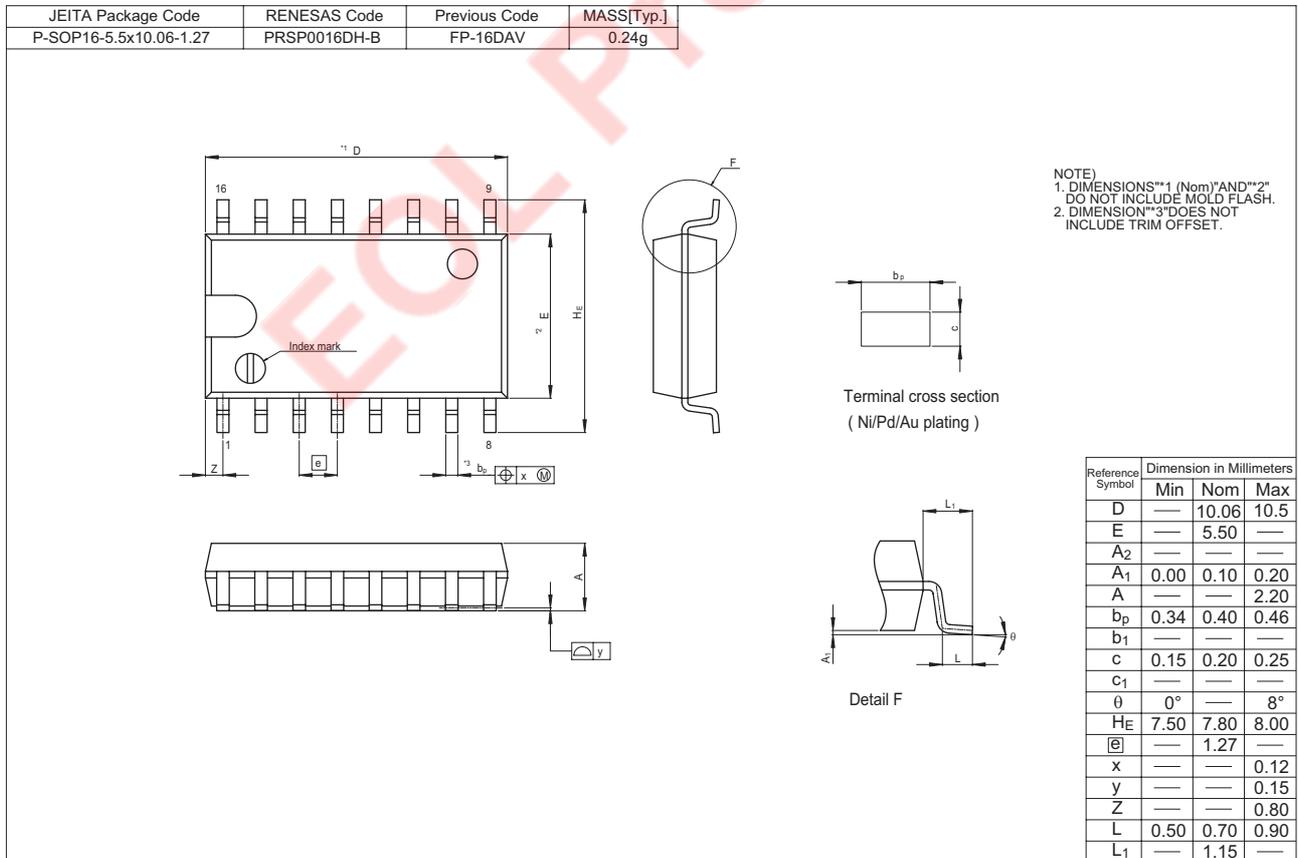
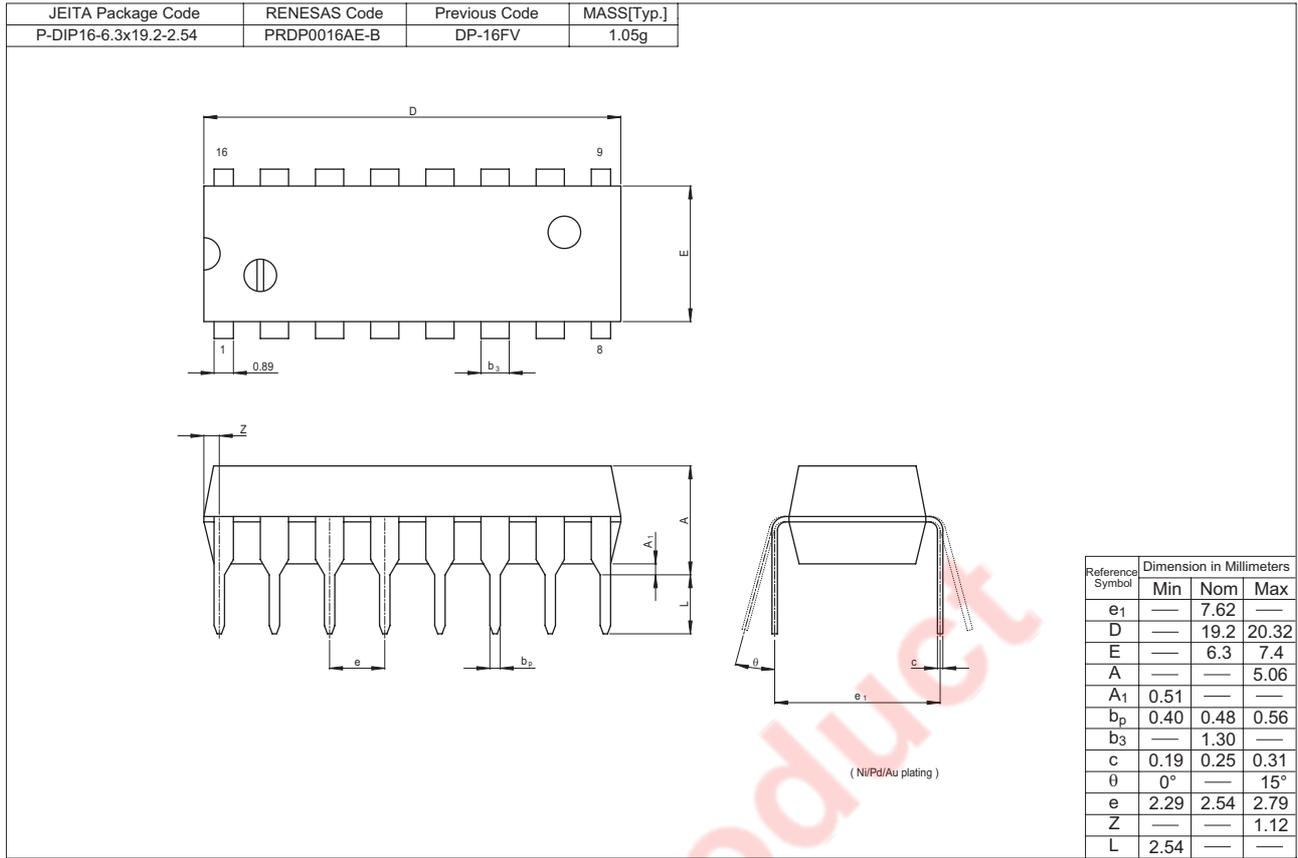
Notes: 1. Input waveform:  $PRR \leq 1 \text{ MHz}$ ,  $Z_o = 50 \Omega$ ,  $t_r \leq 6 \text{ ns}$ ,  $t_f \leq 6 \text{ ns}$   
 2.  $t_n$  is bit time with all outputs at low.

• Waveform – 2



Notes: 1. Input waveform:  $PRR \leq 1 \text{ MHz}$ ,  $Z_o = 50 \Omega$ ,  $t_r \leq 6 \text{ ns}$ ,  $t_f \leq 6 \text{ ns}$   
 2. The output are measured one at a time with one transition per measurement.

Package Dimensions



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Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

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Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7898

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Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea  
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

### **Renesas Technology Malaysia Sdn. Bhd**

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia  
Tel: <603> 7955-9390, Fax: <603> 7955-9510