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April 1st, 2010
Renesas Electronics Corporation

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for new design

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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HD74CBT16210

20-bit FET Bus Switch

RENESAS

ADE-205-646A (Z)

Preliminary
Rev. 1
Feb. 2002

Description

The HD74CBT16210 provides 20-bits of high speed TTL-compatible bus switching. The low on state resistance of the switch allows connections to be made with minimal propagation delay. The device is organized as a dual 10-bit bus switch with separate output enable (\overline{OE}) inputs. It can be used as two 10-bit bus switches or as one 20-bit bus switch. When \overline{OE} is low, the associated 10-bit bus switch is on, and port A is connected to port B. When \overline{OE} is high, the switch is open, and the high impedance state exists between the ports.

Features

- Minimal propagation delay through the switch.
- 5 Ω switch connection between two ports.
- TTL-compatible input levels.
- Ultra low quiescent power.
-Ideally suited for notebook applications.
- Package type
Product code example: HD74CBT16210TEL

Package type	Package code	Package suffix	Taping code
TSSOP-48pin	TTP-48DBV	T	EL(1,000pcs / Reel)

Function Table

Input \overline{OE}	Function
L	A port = B port
H	Disconnect

H: High level

L: Low level

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CC}	-0.5 to 7.0	V	
Input voltage range ¹	V_I	-0.5 to 7.0	V	
Input clamp current	I_{IK}	-50	mA	$V_I < 0$
Continuous output current	I_o	128	mA	$V_o = 0$ to V_{CC}
Continuous current through V_{CC} or GND	I_{CC} or I_{GND}	± 100	mA	
Maximum power dissipation at $T_a = 25^\circ\text{C}$ (in still air) ²	P_T	1.08	W	
Storage temperature	T_{stg}	-65 to 150	$^\circ\text{C}$	

Notes: The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

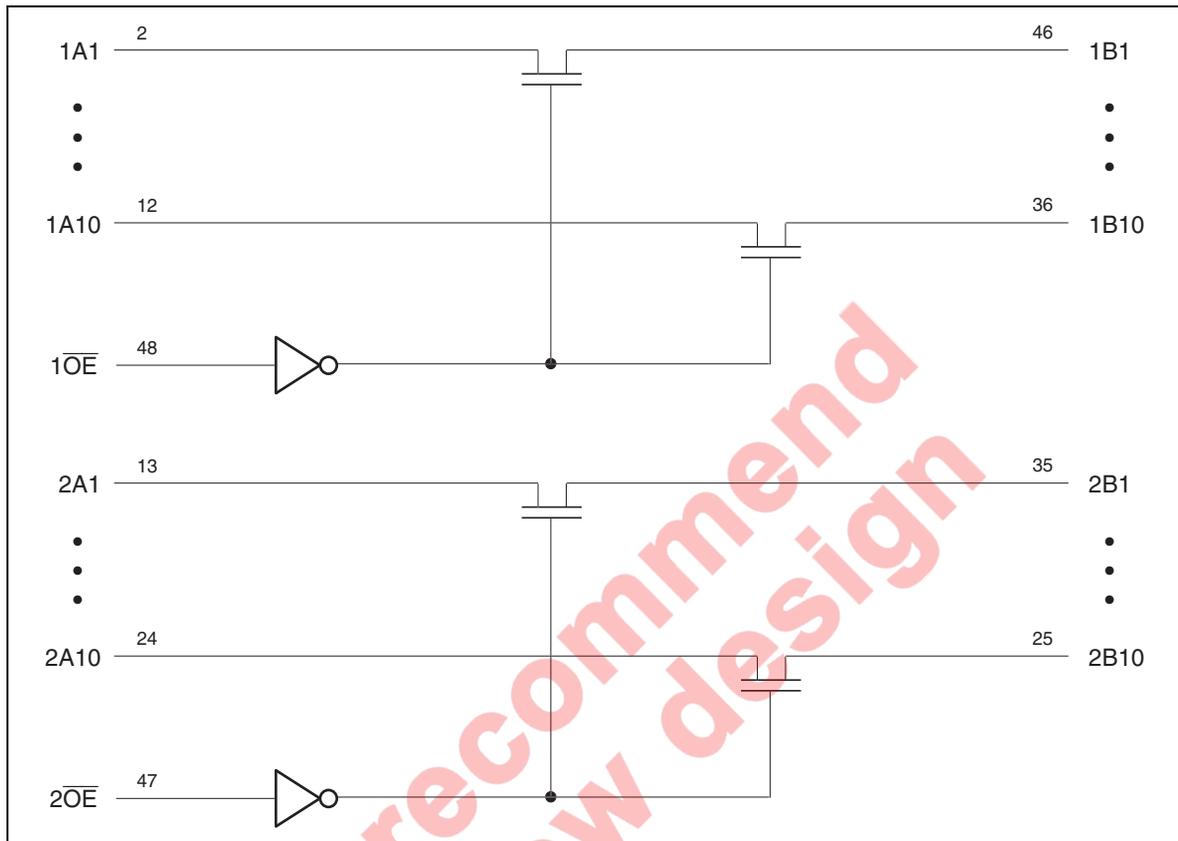
1. The input and output voltage ratings may be exceeded even if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation was calculated using a junction temperature of 150°C .

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	V_{CC}	4.0	5.5	V	
Input voltage range	V_I	0	5.5	V	
Output voltage range	V_{IO}	0	5.5	V	
Input transition rise or fall rate	$\Delta t / \Delta v$	0	5	ns / V	$V_{CC} = 4.5$ to 5.5 V
Operating free-air temperature	T_a	-40	85	$^\circ\text{C}$	

Note: Unused or floating inputs must be held high or low.

Block Diagram



DC Electrical Characteristics

(Ta = -40 to 85°C)

Item	Symbol	V _{CC} (V)	Min	Typ ¹	Max	Unit	Test conditions
Clamp diode voltage	V _{IK}	4.5	—	—	-1.2	V	I _{IN} = -18 mA
Input voltage	V _{IH}	4.0 to 5.5	2.0	—	—	V	
	V _{IL}	4.0 to 5.5	—	—	0.8		
On-state switch resistance ²	R _{ON}	4.0	—	14	20	Ω	V _{IN} = 2.4 V, I _{IN} = 15 mA Typ at V _{CC} = 4.0 V
		4.5	—	5	7		V _{IN} = 0 V, I _{IN} = 64 mA
		4.5	—	5	7		V _{IN} = 0 V, I _{IN} = 30 mA
		4.5	—	8	12		V _{IN} = 2.4 V, I _{IN} = 15 mA
Input current	I _{IN}	0 to 5.5	—	—	±1.0	μA	V _{IN} = 5.5 V or GND
Off-state leakage current	I _{OZ}	5.5	—	—	±1.0	μA	0 ≤ A, B ≤ V _{CC}
Quiescent supply current	I _{CC}	5.5	—	—	3	μA	V _{IN} = V _{CC} or GND, I _O = 0 mA
Increase in I _{CC} per input ³	ΔI _{CC}	5.5	—	—	2.5	mA	One input at 3.4 V, other inputs at V _{CC} or GND

Notes: For condition shown as Min or Max use the appropriate values under recommended operating conditions.

1. All typical values are at V_{CC} = 5 V (unless otherwise noted), Ta = 25°C.
2. Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower voltage of the two (A or B) terminals.
3. This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

Capacitance

(Ta = 25°C)

Item	Symbol	V _{CC} (V)	Min	Typ	Max	Unit	Test conditions
Control input capacitance	C _{IN}	5.0	—	5	—	pF	V _{IN} = 0 or 3 V
Input / output capacitance	C _{I/O(OFF)}	5.0	—	7	—	pF	V _O = 0 or 3 V OE = V _{CC}

Note: This parameter is determined by device characterization is not production tested.

Switching Characteristics

(Ta = -40 to 85°C)

- V_{CC} = 4.0 V

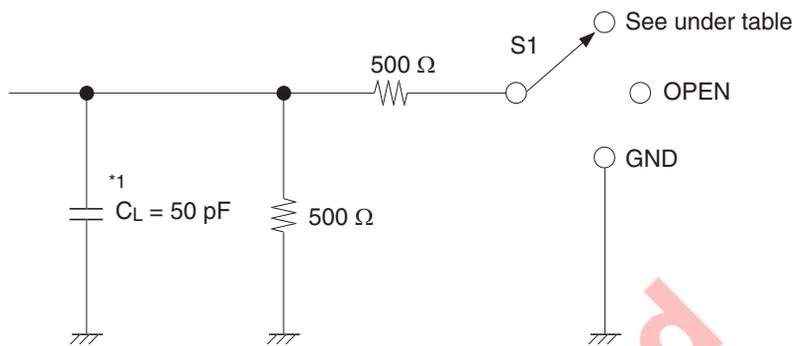
Item	Symbol	Min	Max	Unit	Test conditions	FROM (Input)	TO (Output)
Propagation delay time ¹⁾	t _{PLH} t _{PHL}	—	0.35	ns	C _L = 50 pF R _L = 500 Ω	A or B	B or A
Enable time	t _{ZH} t _{ZL}	—	9.3	ns	C _L = 50 pF R _L = 500 Ω	\overline{OE}	A or B
Disable time	t _{HZ} t _{LZ}	—	7.1	ns	C _L = 50 pF R _L = 500 Ω	\overline{OE}	A or B

- V_{CC} = 5.0±0.5 V

Item	Symbol	Min	Max	Unit	Test conditions	FROM (Input)	TO (Output)
Propagation delay time ¹⁾	t _{PLH} t _{PHL}	—	0.25	ns	C _L = 50 pF R _L = 500 Ω	A or B	B or A
Enable time	t _{ZH} t _{ZL}	3.3	8.6	ns	C _L = 50 pF R _L = 500 Ω	\overline{OE}	A or B
Disable time	t _{HZ} t _{LZ}	2.8	7.9	ns	C _L = 50 pF R _L = 500 Ω	\overline{OE}	A or B

Note: 1. The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

Test Circuit



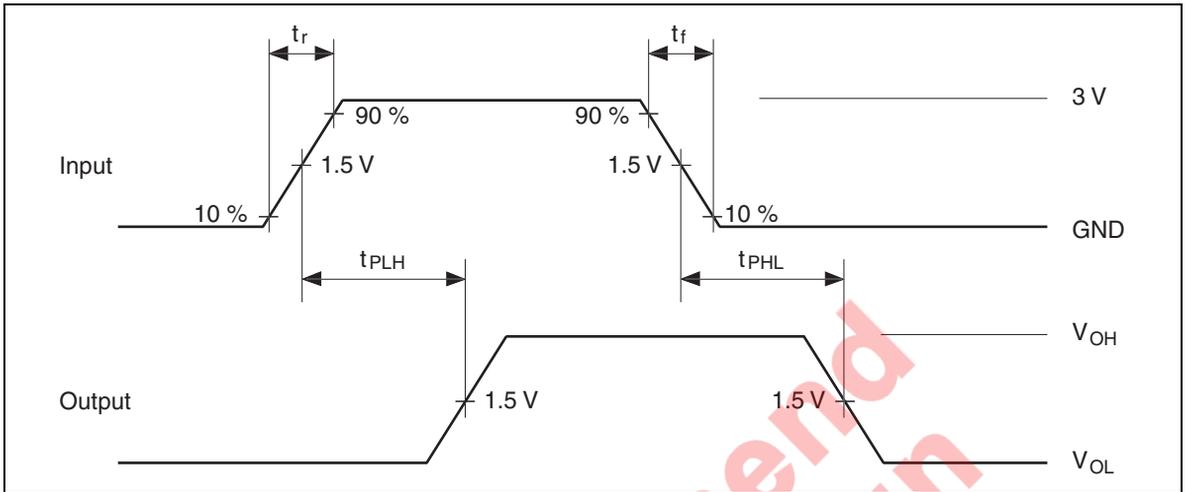
Load circuit for outputs

Symbol	S1
t_{PLH} / t_{PHL}	OPEN
t_{ZH} / t_{HZ}	OPEN
t_{ZL} / t_{LZ}	7 V

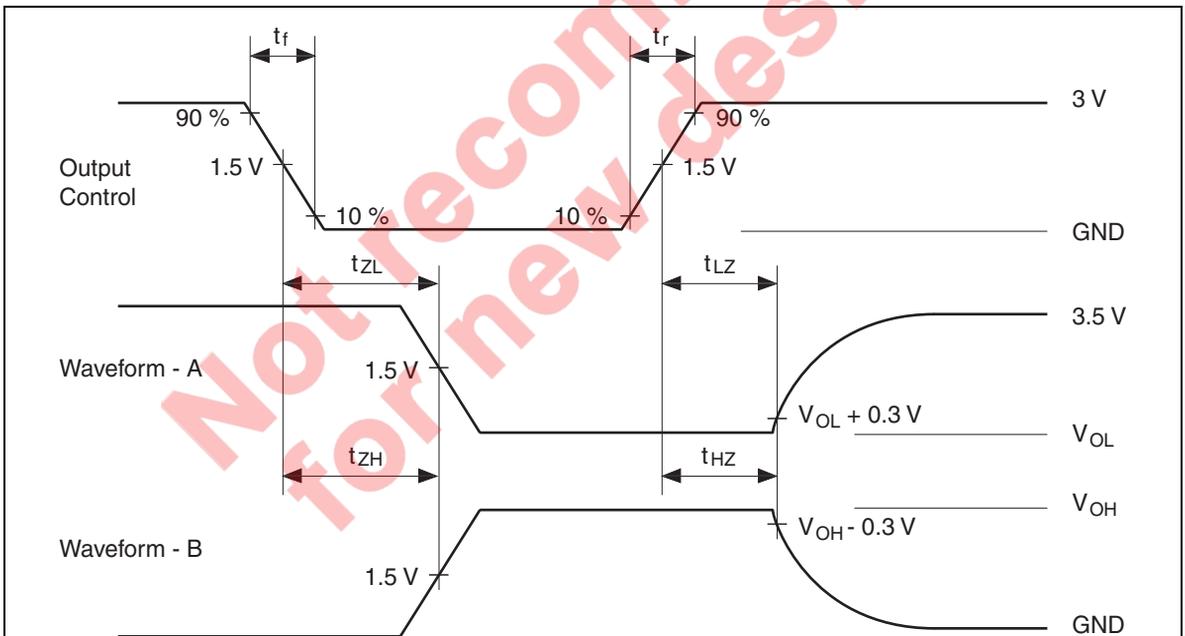
Note: 1. C_L includes probe and jig capacitance.

Not recommended for new design

Waveforms – 1



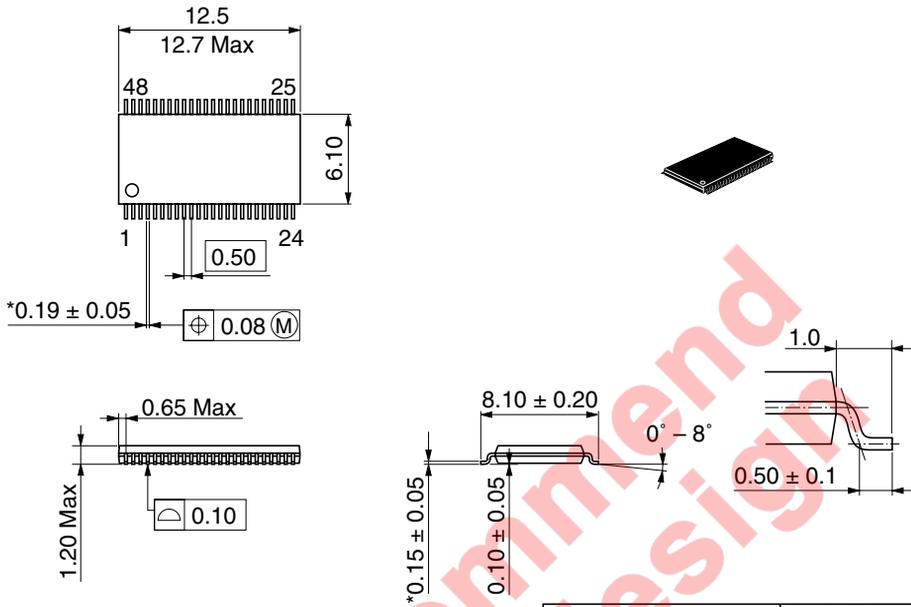
Waveforms – 2



- Notes:
1. All input pulses are supplied by generators having the following characteristics :
 $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 2. Waveform - A is for an output with internal conditions such that the output is low except when disabled by the output control.
 3. Waveform - B is for an output with internal conditions such that the output is high except when disabled by the output control.
 4. The output are measured one at a time with one transition per measurement.

Package Dimensions

As of July, 2001
Unit: mm



*Pd plating

Hitachi Code	TTP-48DBV
JEDEC	—
JEITA	—
Mass (reference value)	0.20 g

Not recommended for new design

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