

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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# HD74ALVCH162501

## 18-bit Universal Bus Transceivers with 3-state Outputs

REJ03D0047-0200Z  
(Previous ADE-205-182 (Z) )  
Rev 2.00  
Oct.02.2003

### Description

Data flow in each direction is controlled by output enable (OEAB and  $\overline{\text{OEBA}}$ ), latch enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A to B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch flip flop on the low to high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high impedance state. Data flow for B to A is similar to that of A to B but uses  $\overline{\text{OEBA}}$ , LEBA, and CLKBA. The output enables are complementary (OEAB is active high, and  $\overline{\text{OEBA}}$  is active low). Active bus hold circuitry is provided to hold unused or floating data inputs at a valid logic level. All outputs, which are designed to sink up to 12 mA, include 26  $\Omega$  resistors to reduce overshoot and undershoot.

### Features

- $V_{CC} = 2.3 \text{ V}$  to  $3.6 \text{ V}$
- Typical  $V_{OL}$  ground bounce  $< 0.8 \text{ V}$  ( $@V_{CC} = 3.3 \text{ V}$ ,  $T_a = 25^\circ\text{C}$ )
- Typical  $V_{OH}$  undershoot  $> 2.0 \text{ V}$  ( $@V_{CC} = 3.3 \text{ V}$ ,  $T_a = 25^\circ\text{C}$ )
- High output current  $\pm 12 \text{ mA}$  ( $@V_{CC} = 3.0 \text{ V}$ )
- Bus hold on data inputs eliminates the need for external pullup / pulldown resistors
- All outputs have equivalent 26  $\Omega$  series resistors, so no external resistors are required.

**Function Table** <sup>\*3</sup>

Inputs				Output B
OEAB	LEAB	CLKAB	A	
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	H	X	B <sub>0</sub> <sup>*1</sup>
H	L	L	X	B <sub>0</sub> <sup>*2</sup>

H : High level

L : Low level

X : Immaterial

Z : High impedance

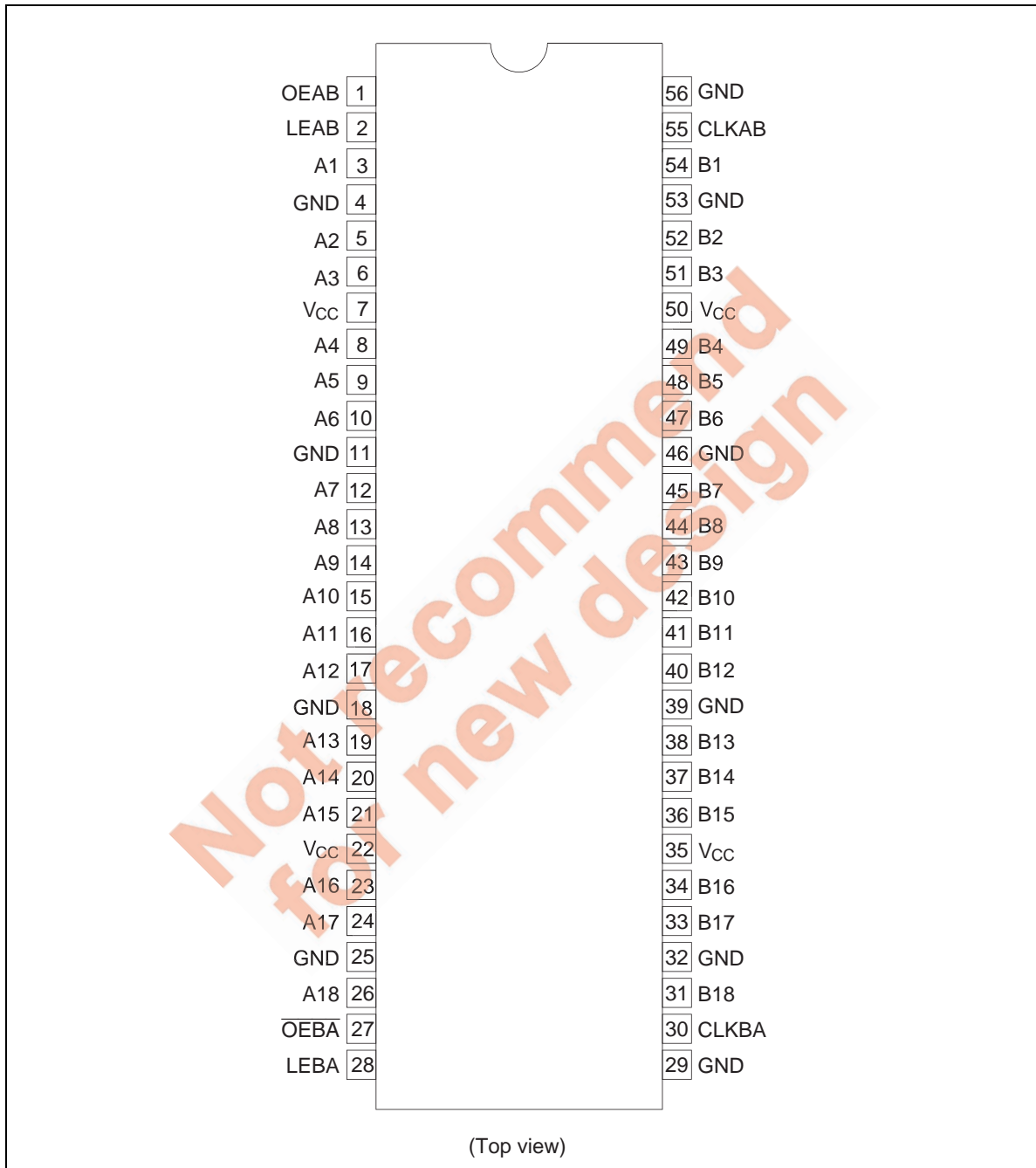
↑ : Low to high transition

Notes: 1. Output level before the indicated steady state input conditions were established, provided that CLKAB was high before LEAB went low.

2. Output level before the indicated steady state input conditions were established.

3. A to B data flow is show; B to A flow is similar but uses OEBA, LEBA, and CLKBA.

## Pin Arrangement



**Absolute Maximum Ratings**

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{CC}$	-0.5 to 4.6	V	
Input voltage <sup>*1, 2</sup>	$V_I$	-0.5 to 4.6 -0.5 to $V_{CC} + 0.5$	V	Except I/O ports I/O ports
Output voltage <sup>*1, 2</sup>	$V_O$	-0.5 to $V_{CC} + 0.5$	V	
Input clamp current	$I_{IK}$	-50	mA	
Output clamp current	$I_{OK}$	±50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	$I_O$	±50 ±100	mA	$V_O = 0$ to $V_{CC}$
Maximum power dissipation at $T_a = 55^\circ\text{C}$ (in still air) <sup>*3</sup>	$P_T$	1	W	TSSOP
Storage temperature	$T_{stg}$	-65 to 150	$^\circ\text{C}$	

Notes: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

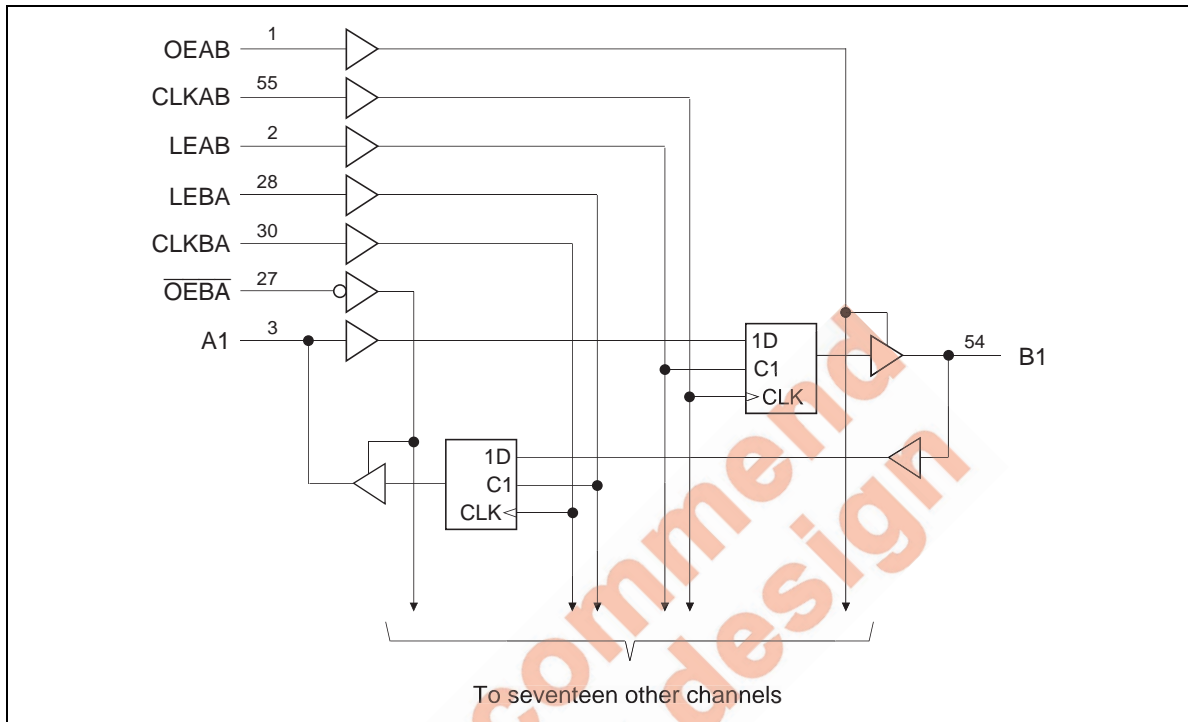
1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of  $150^\circ\text{C}$  and a board trace length of 750 mils.

**Recommended Operating Conditions**

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage	$V_{CC}$	2.3	3.6	V	
Input voltage	$V_I$	0	$V_{CC}$	V	
Output voltage	$V_O$	0	$V_{CC}$	V	
High level output current	$I_{OH}$	—	-6 -8 -12	mA	$V_{CC} = 2.3\text{ V}$ $V_{CC} = 2.7\text{ V}$ $V_{CC} = 3.0\text{ V}$
Low level output current	$I_{OL}$	—	6 8 12	mA	$V_{CC} = 2.3\text{ V}$ $V_{CC} = 2.7\text{ V}$ $V_{CC} = 3.0\text{ V}$
Input transition rise or fall rate	$\Delta t / \Delta v$	0	10	ns / V	
Operating temperature	$T_a$	-40	85	$^\circ\text{C}$	

Note: Unused control inputs must be held high or low to prevent them from floating.

## Logic diagram



## Electrical Characteristics

(Ta = -40 to 85°C)

Item	Symbol	V <sub>CC</sub> (V) *1	Min	Max	Unit	Test Conditions
Input voltage	V <sub>IH</sub>	2.3 to 2.7	1.7	—	V	
		2.7 to 3.6	2.0	—		
	V <sub>IL</sub>	2.3 to 2.7	—	0.7		
		2.7 to 3.6	—	0.8		
Output voltage	V <sub>OH</sub>	Min to Max	V <sub>CC</sub> -0.2	—	V	I <sub>OH</sub> = -100 μA
		2.3	1.9	—		I <sub>OH</sub> = -4 mA, V <sub>IH</sub> = 1.7 V
		2.3	1.7	—		I <sub>OH</sub> = -6 mA, V <sub>IH</sub> = 1.7 V
		3.0	2.4	—		I <sub>OH</sub> = -6 mA, V <sub>IH</sub> = 2.0 V
		2.7	2.0	—		I <sub>OH</sub> = -8 mA, V <sub>IH</sub> = 2.0 V
		3.0	2.0	—		I <sub>OH</sub> = -12 mA, V <sub>IH</sub> = 2.0 V
	V <sub>OL</sub>	Min to Max	—	0.2		I <sub>OL</sub> = 100 μA
		2.3	—	0.4		I <sub>OL</sub> = 4 mA, V <sub>IL</sub> = 0.7 V
		2.3	—	0.55		I <sub>OL</sub> = 6 mA, V <sub>IL</sub> = 0.7 V
		3.0	—	0.55		I <sub>OL</sub> = 6 mA, V <sub>IL</sub> = 0.8 V
		2.7	—	0.6		I <sub>OL</sub> = 8 mA, V <sub>IL</sub> = 0.8 V
		3.0	—	0.8		I <sub>OL</sub> = 12 mA, V <sub>IL</sub> = 0.8 V
Input current	I <sub>IN</sub>	3.6	—	±5	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
	I <sub>IN (hold)</sub>	2.3	45	—		V <sub>IN</sub> = 0.7 V
		2.3	-45	—		V <sub>IN</sub> = 1.7 V
		3.0	75	—		V <sub>IN</sub> = 0.8 V
		3.0	-75	—		V <sub>IN</sub> = 2.0 V
		3.6	—	±500		V <sub>IN</sub> = 0 to 3.6 V
Off state output current *2	I <sub>OZ</sub>	3.6	—	±10	μA	V <sub>OUT</sub> = V <sub>CC</sub> or GND
Quiescent supply current	I <sub>CC</sub>	3.6	—	40	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
	ΔI <sub>CC</sub>	3.0 to 3.6	—	750	μA	V <sub>IN</sub> = one input at (V <sub>CC</sub> -0.6) V, other inputs at V <sub>CC</sub> or GND

Notes: 1. For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

2. For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.



**Switching Characteristic**

(Ta = -40 to 85°C)

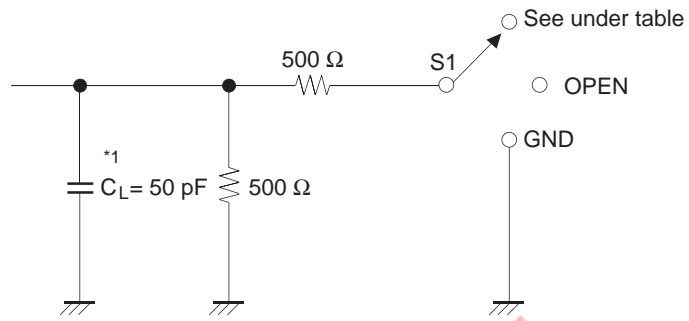
Item	Symbol	V <sub>CC</sub> (V)	Min	Typ	Max	Unit	FROM (Input)	TO (Output)
Maximum clock frequency	f <sub>max</sub>	2.5±0.2	150	—	—	MHz		
		2.7	150	—	—			
		3.3±0.3	150	—	—			
Propagation delay time	t <sub>PLH</sub>	2.5±0.2	1.2	—	5.9	ns	A or B	B or A
	t <sub>PHL</sub>	2.7	—	—	5.2			
		3.3±0.3	1.0	—	4.5			
		2.5±0.2	1.6	—	6.8	LE	A or B	
		2.7	—	—	6.0			
		3.3±0.3	1.3	—	5.2			
		2.5±0.2	1.7	—	7.2	CLK	A or B	
		2.7	—	—	6.3			
		3.3±0.3	1.4	—	5.5			
Output enable time	t <sub>ZH</sub>	2.5±0.2	1.1	—	6.8	ns	OEAB	B
	t <sub>ZL</sub>	2.7	—	—	6.0			
		3.3±0.3	1.0	—	5.2			
		2.5±0.2	1.4	—	7.3	$\overline{\text{OEBA}}$	A	
		2.7	—	—	6.7			
		3.3±0.3	1.1	—	5.6			
Output disable time	t <sub>HZ</sub>	2.5±0.2	2.2	—	6.9	ns	OEAB	B
	t <sub>LZ</sub>	2.7	—	—	6.2			
		3.3±0.3	1.4	—	5.5			
		2.5±0.2	2.0	—	6.0	$\overline{\text{OEBA}}$	A	
		2.7	—	—	5.1			
		3.3±0.3	1.3	—	4.7			
Input capacitance	C <sub>IN</sub>	3.3	—	4.0	—	pF	Control inputs	
Output capacitance	C <sub>IN / O</sub>	3.3	—	8.0	—	pF	A or B ports	

## Switching Characteristics (cont.)

(Ta = -40 to 85°C)

Item	Symbol	V <sub>CC</sub> (V)	Min	Typ	Max	Unit	FROM (Input)
Setup time	t <sub>su</sub>	2.5±0.2	2.2	—	—	ns	Data before CLK↑
		2.7	2.1	—	—		
		3.3±0.3	1.7	—	—		
		2.5±0.2	1.9	—	—		Data before LE↓
		2.7	1.6	—	—		CLK "H"
		3.3±0.3	1.5	—	—		
		2.5±0.2	1.3	—	—		Data before LE↓
		2.7	1.1	—	—		CLK "L"
		3.3±0.3	1.0	—	—		
Hold time	t <sub>h</sub>	2.5±0.2	0.6	—	—	ns	Data after CLK↑
		2.7	0.6	—	—		
		3.3±0.3	0.7	—	—		
		2.5±0.2	1.4	—	—		Data after LE↓
		2.7	1.7	—	—		CLK "H" or "L"
		3.3±0.3	1.4	—	—		
Pulse width	t <sub>w</sub>	2.5±0.2	3.3	—	—	ns	LE "H"
		2.7	3.3	—	—		
		3.3±0.3	3.3	—	—		
		2.5±0.2	3.3	—	—		CLK "H" or "L"
		2.7	3.3	—	—		
		3.3±0.3	3.3	—	—		

• Test Circuit

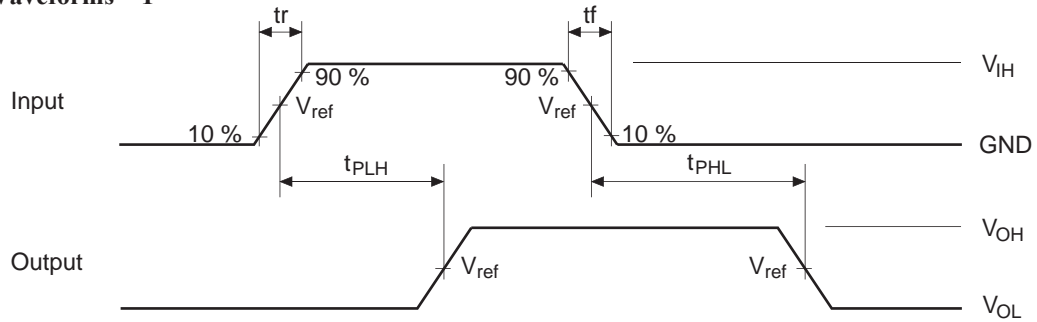


Load Circuit for Outputs

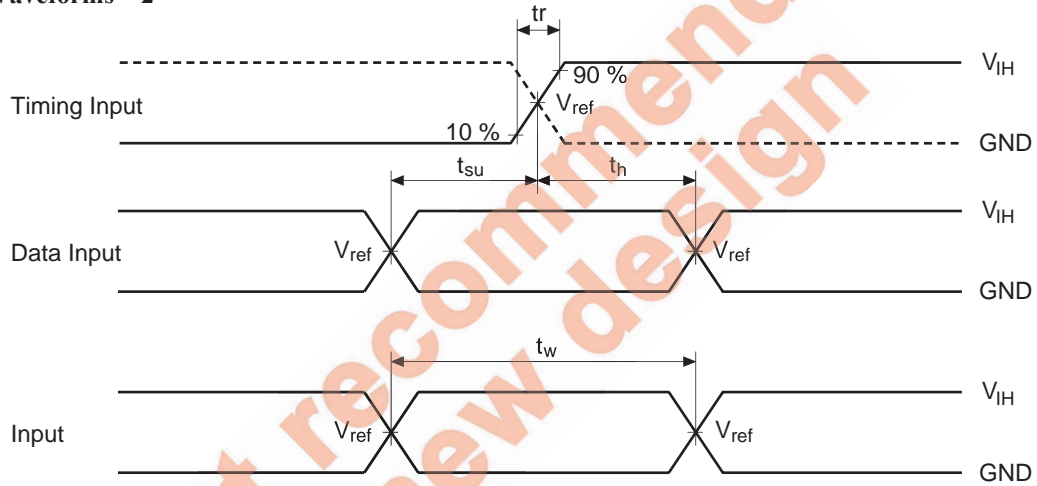
Symbol	V <sub>CC</sub> =2.5±0.2 V	V <sub>CC</sub> =2.7 V, 3.3±0.3 V
t <sub>PLH</sub> /t <sub>PHL</sub>	OPEN	OPEN
t <sub>su</sub> /t <sub>h</sub> /t <sub>w</sub>	OPEN	OPEN
t <sub>ZH</sub> /t <sub>HZ</sub>	GND	GND
t <sub>ZL</sub> /t <sub>LZ</sub>	4.6 V	6.0 V

Note: 1. C<sub>L</sub> includes probe and jig capacitance.

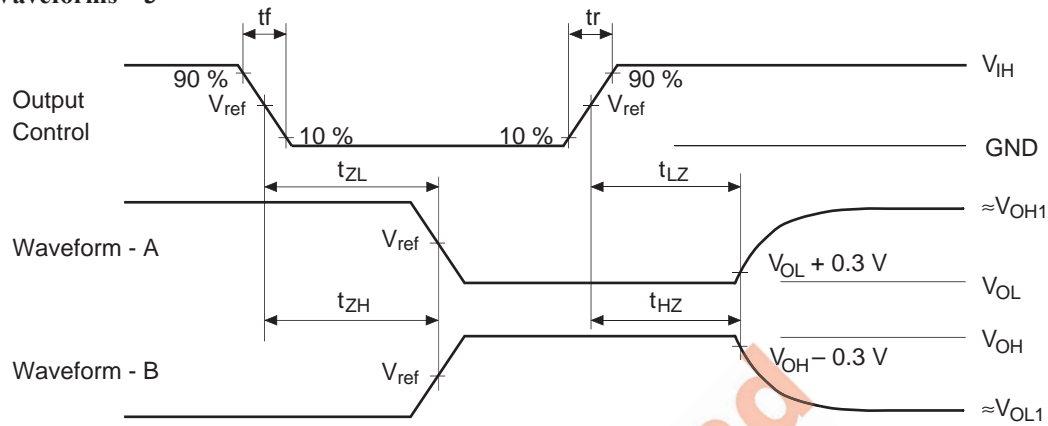
• Waveforms – 1



• Waveforms – 2



- **Waveforms – 3**

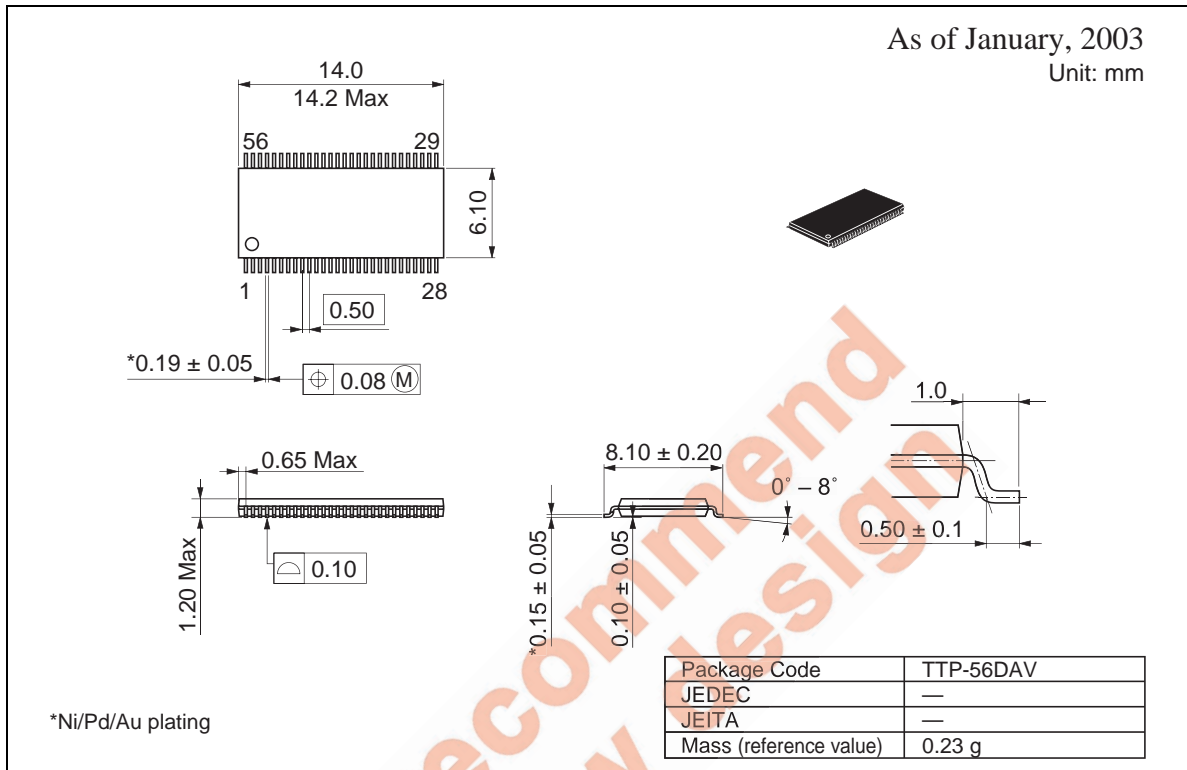


TEST	V <sub>CC</sub> =2.5±0.2V	V <sub>CC</sub> =2.7V, 3.3±0.3V
V <sub>IH</sub>	2.3 V	2.7 V
V <sub>ref</sub>	1.2 V	1.5 V
V <sub>OH1</sub>	2.3 V	3.0 V
V <sub>OL1</sub>	GND	GND

Notes: 1. All input pulses are supplied by generators having the following characteristics:  
 $PRR \leq 10 \text{ MHz}$ ,  $Z_o = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .

2. Waveform – A is for an output with internal conditions such that the output is low except when disabled by the output control.
3. Waveform – B is for an output with internal conditions such that the output is high except when disabled by the output control.
4. The output are measured one at a time with one transition per measurement.

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