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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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Not recommended
for new design

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HD74AC153

Dual 4-Input Multiplexer

REJ03D0251-0200Z
 (Previous ADE-205-370 (Z))
 Rev.2.00
 Jul.16.2004

Description

The HD74AC153 is a high-speed dual 4-input multiplexer with common select inputs and individual enable inputs for each section. It can select two lines of data from four sources. The two buffered outputs present data in the true (noninverted) form. In addition to multiplexer operation, the HD74AC153 can act as a function generator and generate any two functions of three variables.

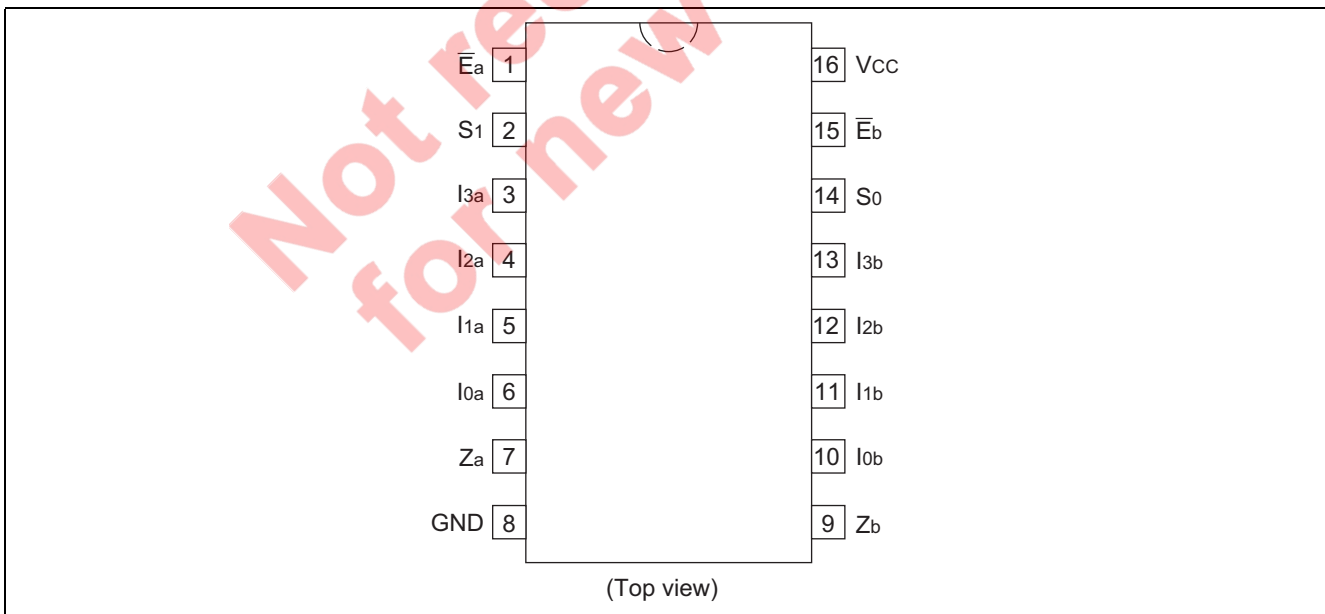
Features

- Outputs Source/Sink 24 mA
- Ordering Information

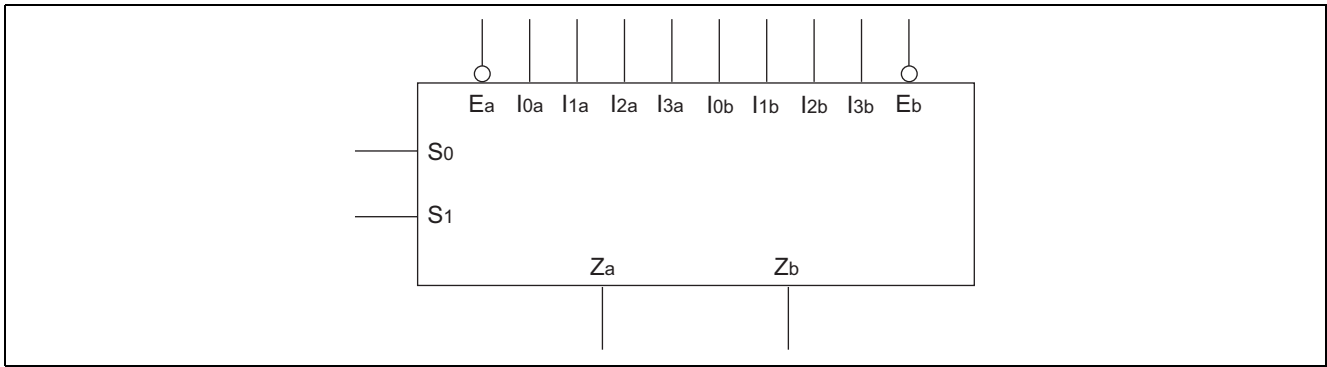
Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74AC153FPEL	SOP-16 pin (JEITA)	FP-16DAV	FP	EL (2,000 pcs/reel)
HD74AC153RPEL	SOP-16 pin (JEDEC)	FP-16DNV	RP	EL (2,500 pcs/reel)

- Notes: 1. Please consult the sales office for the above package availability.
 2. The packages with lead-free pins are distinguished from the conventional products by adding V at the end of the package code.

Pin Arrangement



Logic Symbol



Pin Names

- I_{0a} to I_{3a} Side A Data Inputs
- I_{0b} to I_{3b} Side B Data Inputs
- S₀, S₁ Common Select Inputs
- \bar{E}_a Side A Enable Input
- \bar{E}_b Side B Enable Input
- Z_a Side A Output
- Z_b Side B Output

Functional Description

The HD74AC153 is a dual 4-input multiplexer. It can select two bits of data from up to four sources under the control of the common Select inputs (S₀, S₁). The two 4-input multiplexer circuits have individual active-Low Enables (\bar{E}_a , \bar{E}_b) which can be used to strobe the outputs independently. When the Enables (\bar{E}_a , \bar{E}_b) are High, the corresponding outputs (Z_a, Z_b) are forced Low. The HD74AC153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select inputs. The logic equations for the outputs are shown below.

$$Z_a = \bar{E}_a \cdot (I_{0a} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1a} \cdot \bar{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \bar{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

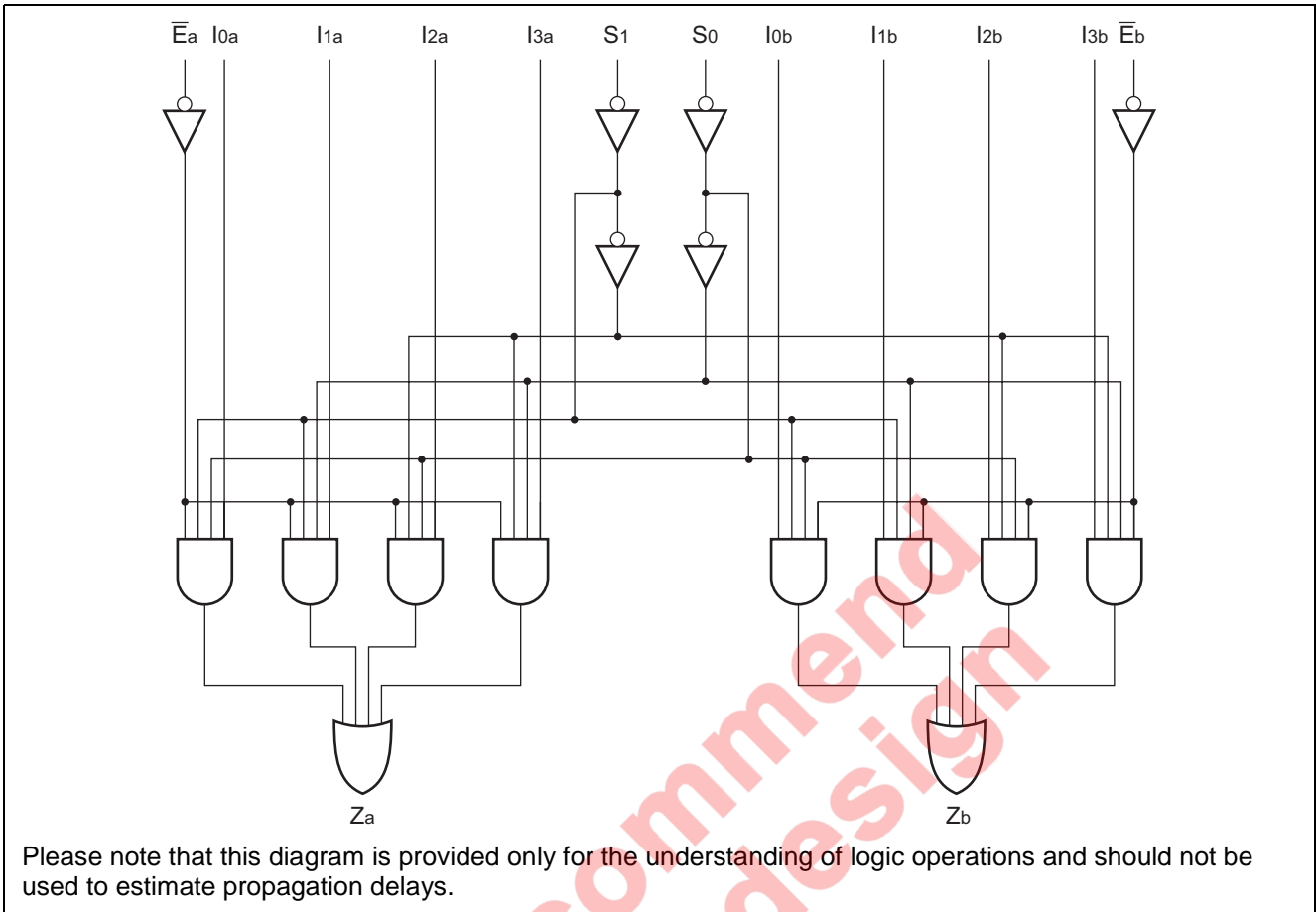
$$Z_b = \bar{E}_b \cdot (I_{0b} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1b} \cdot \bar{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \bar{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

Truth Table

Select Inputs		Input (a or b)					Output
S ₀	S ₁	\bar{E}	I ₀	I ₁	I ₂	I ₃	Z
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

- H : High Voltage Level
- L : Low Voltage Level
- X : Immaterial

Logic Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	-0.5 to 7	V	
DC input diode current	I_{IK}	-20	mA	$V_I = -0.5V$
		20	mA	$V_I = V_{CC}+0.5V$
DC input voltage	V_I	-0.5 to $V_{CC}+0.5$	V	
DC output diode current	I_{OK}	-50	mA	$V_O = -0.5V$
		50	mA	$V_O = V_{CC}+0.5V$
DC output voltage	V_O	-0.5 to $V_{CC}+0.5$	V	
DC output source or sink current	I_O	± 50	mA	
DC V_{CC} or ground current per output pin	I_{CC}, I_{GND}	± 50	mA	
Storage temperature	T_{stg}	-65 to +150	$^{\circ}C$	

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	2 to 6	V	
Input and output voltage	V_I, V_O	0 to V_{CC}	V	
Operating temperature	T_a	-40 to +85	$^{\circ}C$	
Input rise and fall time (except Schmitt inputs) V_{IN} 30% to 70% V_{CC}	t_r, t_f	8	ns/V	$V_{CC} = 3.0V$
				$V_{CC} = 4.5 V$
				$V_{CC} = 5.5 V$

DC Characteristics

Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Condition		
			min.	typ.	max.	min.	max.				
Input Voltage	V _{IH}	3.0	2.1	1.5	—	2.1	—	V	V _{OUT} = 0.1 V or V _{CC} -0.1 V		
		4.5	3.15	2.25	—	3.15	—				
		5.5	3.85	2.75	—	3.85	—				
	V _{IL}	3.0	—	1.50	0.9	—	0.9		V _{OUT} = 0.1 V or V _{CC} -0.1 V		
		4.5	—	2.25	1.35	—	1.35				
		5.5	—	2.75	1.65	—	1.65				
Output voltage	V _{OH}	3.0	2.9	2.99	—	2.9	—	V	V _{IN} = V _{IL} or V _{IH} I _{OUT} = -50 μA		
		4.5	4.4	4.49	—	4.4	—				
		5.5	5.4	5.49	—	5.4	—				
		3.0	2.58	—	—	2.48	—			V _{IN} = V _{IL} or V _{IH} I _{OH} = -12 mA	
		4.5	3.94	—	—	3.80	—				I _{OH} = -24 mA
		5.5	4.94	—	—	4.80	—				I _{OH} = -24 mA
	V _{OL}	3.0	—	0.002	0.1	—	0.1	V	V _{IN} = V _{IL} or V _{IH} I _{OUT} = 50 μA		
		4.5	—	0.001	0.1	—	0.1				
		5.5	—	0.001	0.1	—	0.1				
		3.0	—	—	0.32	—	0.37			V _{IN} = V _{IL} or V _{IH} I _{OL} = 12 mA	
		4.5	—	—	0.32	—	0.37				I _{OL} = 24 mA
		5.5	—	—	0.32	—	0.37				I _{OL} = 24 mA
Input leakage current	I _{IN}	5.5	—	—	±0.1	—	±1.0	μA	V _{IN} = V _{CC} or GND		
Dynamic output current*	I _{OLD}	5.5	—	—	—	86	—	mA	V _{OLD} = 1.1 V		
	I _{OHD}	5.5	—	—	—	-75	—	mA	V _{OHD} = 3.85 V		
Quiescent supply current	I _{CC}	5.5	—	—	8.0	—	80	μA	V _{IN} = V _{CC} or ground		

*Maximum test duration 2.0 ms, one output loaded at a time.

AC Characteristics: HD74AC153

Item	Symbol	V _{CC} (V)*1	Ta = +25°C C _L = 50 pF			Ta = -40°C to +85°C C _L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Propagation delay S _n to Z _n	t _{PLH}	3.3	1.0	9.5	15.0	1.0	17.5	ns
		5.0	1.0	6.5	11.0	1.0	12.5	
Propagation delay S _n to Z _n	t _{PHL}	3.3	1.0	8.5	14.5	1.0	16.5	ns
		5.0	1.0	6.5	11.0	1.0	12.0	
Propagation delay E _n to Z _n	t _{PLH}	3.3	1.0	8.0	13.5	1.0	16.0	ns
		5.0	1.0	5.5	9.5	1.0	11.0	
Propagation delay E _n to Z _n	t _{PHL}	3.3	1.0	7.0	11.0	1.0	12.5	ns
		5.0	1.0	5.0	8.0	1.0	9.0	
Propagation delay I _n to Z _n	t _{PLH}	3.3	1.0	7.5	12.5	1.0	14.5	ns
		5.0	1.0	5.5	9.0	1.0	10.5	
Propagation delay I _n to Z _n	t _{PHL}	3.3	1.0	7.0	11.5	1.0	13.0	ns
		5.0	1.0	5.0	8.5	1.0	10.0	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

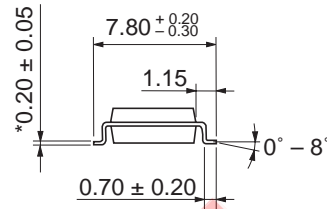
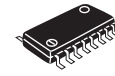
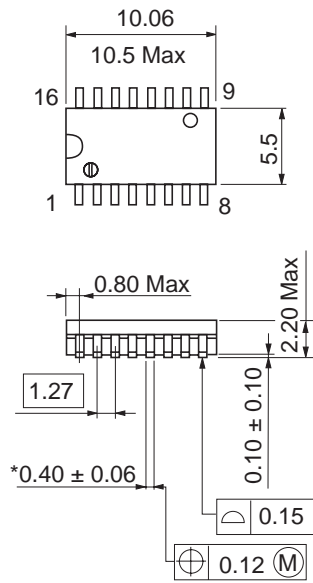
Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C_{IN}	4.5	pF	$V_{CC} = 5.5 \text{ V}$
Power dissipation capacitance	C_{PD}	65.0	pF	$V_{CC} = 5.0 \text{ V}$

Not recommend
for new design

Package Dimensions

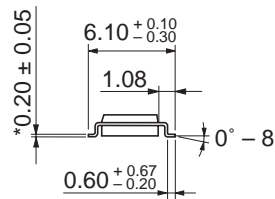
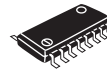
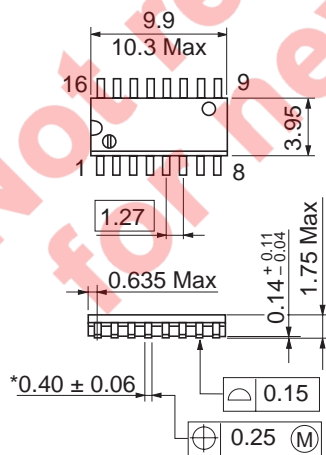
As of January, 2003
Unit: mm



*Ni/Pd/Au plating

Package Code	FP-16DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.24 g

As of January, 2003
Unit: mm



*Ni/Pd/Au plating

Package Code	FP-16DNV
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	0.15 g

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